Digital Design: Propagation delay calculation

Weijie Jiang, Ce Ma, Wim Dehaene

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1 TSCP register

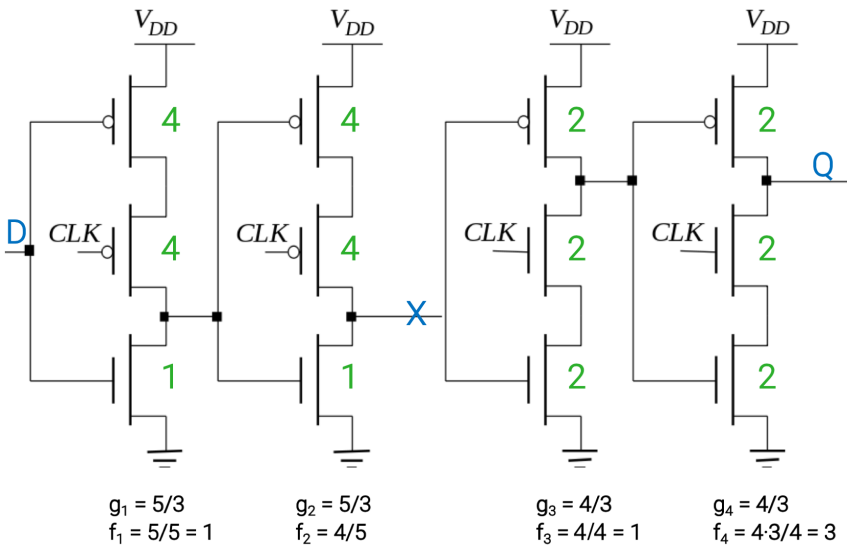


Figure 1: Transistor sizing *r=2*

As we are working with a complex gate, we opt for the approximation:

$$t_{pd} = t_{pd_0} \cdot (p + \frac{g \cdot f}{\gamma}) = t_{pd_0} \cdot d \tag{1}$$

- Relative setup time (ts): Delay from D to node X when CLK=0 (negative latch).

$$ts = t_{pd_1} + t_{pd_2} = t_{pd_0} \cdot (2 + \frac{5}{3} \cdot 1) + t_{pd_0} \cdot (2 + \frac{5}{3} \cdot \frac{4}{5}) = 7 \cdot t_{pd_0} \tag{2}$$

- Relative propagation delay (tcq): Delay from X to node Q when CLK=1 (positive latch).

$$ts = t_{pd_3} + t_{pd_4} = t_{pd_0} \cdot (2 + \frac{4}{3} \cdot 1) + t_{pd_0} \cdot (2 + \frac{4}{3} \cdot 3) = 9.3 \cdot t_{pd_0} \tag{3}$$

Note that in this gate, p acquires a value between 1 and 2. In this solution, we choose $p = 2$.

2 SRAM design

In SRAMs normally the cells will be inactive, so the main problem will be leakage. Therefore, we will choose a high VT, designing for lower power. Now, based on the requirements, conditions for all transistors can be derived using the transistor parameters in table 1 and 2.

2.1 Writable (Critical Write logical '0')

In this case, node q is logical '1' (and consequently node *qbar* is logical '0'. Additionally, word line (WL) is logical '1', and bit line (BL) is logical '0'.

In the absolute worst-case condition, the node *qbar* is still logical '0' and the node of interest, q, is already pulled down to VDD/8. Now, to sustain critical reading, the PMOS pull-up current needs to be smaller (or equal) than the NMOS access sinking current. For each transistor:

- PMOS:
  - VGS = VDD = 1V > 0.515 = VT -> transistor is on
  - VDS = 7/8V > 0.358 = VDsat -> saturation
  - VGS = 1.3V > 0.561 = VT -> transistor is on
  - VDS = 1/8VDD = 0.125V < 0.290 = VDsat -> linear

```
> ## solve write equations
  # pull up current equation(sat)
  I2 := Kp·WLp·((VDD − abs(Vtp))·Vdsatp − Vdsatp²/2)·(1 + lambdap·VDD/4);
  # access current equation(lin)
  I1 := Kn·WLn2·((VWL − Vtn)·Vq − Vq²/2);
                        I2 := 51.48756000 WLp
                        I1 := 78.64312500
> solve(I1 = I2, WLp)
                              1.527419924
```

2.2 Readable (Critical Read logical '0')

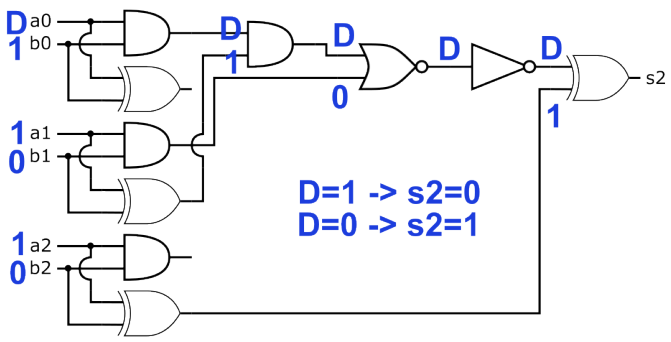
In this case, node q is logical '0', the BL is precharged with logical '1' and the WL is logical '1'. At the beginning of the read cycle, a large current rushes into the NMOS access transistor and cannot immedately be sinked by the NMOS pull-down transistor. This increases the voltage on node q. The voltage on node q is required to be less than VDD/8.

In the most critical part, at a voltage rise of VDD/8 on node q, the current flowing into node q via the NMOS access transistor needs to be smaller (or equal) to de current being sinked by the NMOS pull-down transistor

- NMOS access transistor: sat
- NMOs pull-down transistor: lin

```
> ## solve read equations
  # access current equation(sat)
  I1 := Kn·WLn2·( ((VWL − Vq) - Vtn)·Vdsatn − Vdsatn^2/2 )·(1 + lambdan·(VDD
      − Vq));
  # pull down current equation(lin)
  I2 := Kn·WLn1·( (VDD − Vtn)·Vq − Vq^2/2 );
                          I1 := 187.3622756
                          I2 := 43.76812500 WLn1
> solve(I1 = I2, WLn1)
                              4.280792828
```

3 Testing



Note that there can be multiple solutions.