EXERCISE 1: SYNTHESIS

CELLS	leakage	switching	internal	Total power	slack(ps)
HVT+SVT					
SVT+LVT					

Questions:

See how the tool reports the timing. What does the negative slack mean? .....
.....
.....

Which cells are used in the ciritcal path (LVT, SVT, HVT) and why?..... .....
.....
.....

Assuming that both designs have zero slack, mention an application where you would use each design? .....
.....
.....

EXERCISE 2: CHILL CONSTRAINTS AND 4 METALS FOR ROUTING

Internal Power	Switching Power	Leakage Power	Total Power	Cells in clock tree	Levels in clock tree
				--	--
CLOCK POWER					

Insert clock tree architecture:

Questions:

Check setup violations: *report_timing*
Check hold violations: *report_timing -early*
Copy the timing information here:

How would you fix this hold violation? .....
.....
.....

Fix hold violations:
deleteFiller
optDesign -postRoute -hold -outDir timingReports/optRoute
addFiller
Check the new timing information of the previous path:
report_timing -early -to data_memory/process_for_mem[0].spad_inst/din1[18]
Copy the new timing information here:

How has the tool fixed the hold violation on the previous path?.....
.....
.....

How many hold buffers were inserted in total?.....
deselectAll
*selectInst [get_cells -hier -filter "ref_name=~*BUF*"]*
llength [dbGet selected]
Report power. Which changes do you observe?.....
.....
.....

Report timing and fill in the fanout, load, slew and arrival time numbers that appear in the first line, wich are associated to the clock pin (CK) of instruction_fw_ID_EX/r_reg[3] register.
report_timing -from instruction_fw_ID_EX/r_reg[3]

Instance	Pin	Fanout	Load	Slew	Arrival Time
instruction_fw_ID_EX/r_reg[3]	CK				

EXERCISE 3: TIGHT CONSTRAINTS AND 4 METALS FOR ROUTING

Internal Power	Switching Power	Leakage Power	Total Power	Cells in clock tree	Levels in clock tree
				--	--
CLOCK POWER					

Insert clock tree architecture

Questions

How much has power consumption increased? .....
.....

Report timing and fill in the fanout, load, slew and arrival time numbers that appear in the first line, wich are associated to the clock pin (CK) of instruction_fw_ID_EX/r_reg[3] register.
report_timing -from instruction_fw_ID_EX/r_reg[3]

Instance	Pin	Fanout	Load	Slew	Arrival Time
instruction_fw_ID_EX/r_reg[3]	CK				

Compare the clock tree architecture and the timing information of the register instruction_fw_ID_EX/r_reg[3] when using chill and tight constraints. Which main differences do you observe? How do they improve the transition delay and clock skew constraints?.....
.....
.....
.....

Report area: *report_area -detail*
How many cells/instances compound the design? .....
What is the total area? .....
How much area do buffers occupy in the design? .....

Report number of buffers: .....
deselectAll
*selectInst [get_cells -hier -filter "ref_name=~*BUF*"]*
llength [dbGet selected]
Report number of hold buffers: .....
#FE_PHC instance added my hold time repair
deselectAll
*selectInst [get_cells -hier *FE_PHC*]*
llength [dbGet selected]
What is its percentage with respect to the total number of buffers?.....
Estimate the area that those hold buffers require in the chip?.....

EXERCISE 4: TIGHT CONSTRAINTS AND DERATES AND 4 METALS FOR ROUTING

Internal Power	Switching Power	Leakage Power	Total Power	Cells in clock tree	Levels in clock tree
				--	--
CLOCK POWER					

Insert clock tree architecture:

Questions

How much has power consumption increased? .....
.....

Report area: *report_area -detail*

How many cells/instances compound the design? .....
What is the total area? .....
How much area do inverters and buffers occupy in the design? .....

Report number of buffers: .....
deselectAll
*selectInst [get_cells -hier -filter "ref_name=~*BUF*"]*
llength [dbGet selected]
Report number of hold buffers: .....
#FE_PHC instance added my hold time repair
deselectAll
*selectInst [get_cells -hier *FE_PHC*]*
llength [dbGet selected]
Which is the percentage compared to the total number of buffers? .....
Estimate the area that those hold buffers require in the chip .....

Let's imagine that this chip is part of your phd and you want to tape it out through Europratice TSMC mini@sic. Let's imagine that the increment of hold buffers forces increasing physically the area of the chip. How much money would the increment on area cost MICAS department?
TSMC 65LPMSRF :.....
TSMC 28HPC+RF :.....
TSMC 16FFCRF :.....

MPW | $ MPW | mini@sic | € mini@sic

TSMC mini@sic Pricelist	Standard prices		Discounted prices	
	EUR / min area	EUR / extra area	EUR / min area	EUR / extra area
TSMC 130 BCD+ (min area = 6 mm^2)	13,982	231 / 0.1 mm^2	12,482	190 / 0.1 mm^2
TSMC 65 LP MS RF (min area = 1 mm^2)	4,462	418 / 0.1 mm^2	3,662	358 / 0.1 mm^2
TSMC 40 LP MS RF (min area = 3 mm^2) [1]	21,249	662 / 0.1 mm^2	18,249	599 / 0.1 mm^2
TSMC 28 HPC+ RF (min area = 1 mm^2) [1]	10,541	915 / 0.1 mm^2	8,441	830 / 0.1 mm^2
TSMC 16 FFC RF (min area = 1mm^2) [2, 3]	30,364	2,814 / 0.1 mm^2	26,364	2,557 / 0.1 mm^2

EXERCISE 5: TIGHT CONSTRAINTS AND DERATES AND 10 METALS FOR ROUTING

Internal Power	Switching Power	Leakage Power	Total Power	Cells in clock tree	Levels in clock tree
				--	--
	CLOCK POWER				

How much has power consumption increased? .....
.....

Insert clock tree architecture:

EXERCISE 6: TIGHT CONSTRAINTS AND DERATES AND 10 METALS FOR ROUTING INCLUDYING ACTIVITY

Internal Power	Switching Power	Leakage Power	Total Power
CLOCK POWER			

Questions:

Why does leakage remain utterly invariant? .....
.....

From the total power, what percentage corresponds to leakage? How much did we estimate? .....

Did we estimate properly the activity of the clock? .....
.....

What percentage of power does the clock consume in the cpu? Hoe much did we estimate?
.....

Did we estimate properly the activity of the cpu inputs and thus the combinational logic? Is the real activity higher or lower than the estimated?.....
.....