Digital Design: Propagation delay calculation

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This document can be used as background material for Exercise session 4 (question 2 and 3) and explains how to calculate propagation delay through a logic circuit. First, it explains how to calculate the sizes of the transistors for an arbitrary CMOS gate. Then, the propagation delay of an inverter chain is explained. Finally, the propagation delay of an arbitrary circuit is covered.

1 Gate sizing

The first step consists on sizing the transistors of the gate. p-channel devices have a higher channel resistance, therefore we compensate for this by making the p-channel device (r) times wider than the n-channel device. Typically we use a pmos/nmos ratio of 2, so that they have approximately the same equivalent resistance, meaning the same driving capability, obtaining symmetrical output rise and fall edges.

The second step consists on sizing the whole gate. Following the same premise, we will size the pull-up and pull-down tree to have the same equivalent resistance and obtain a symmetrical output. Table.1 shows the sizing computation of an inverter, a 2-input NAND and NOR gates in terms of r. The result applying $r = 2$ is depicted in Fig.1.

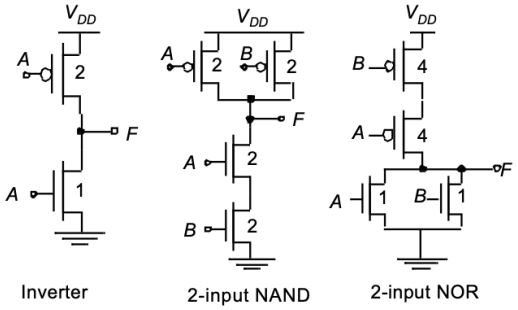

Figure 1: Example of gates sizing with *r=2*

	inverter	2-input NAND	2-input NOR
pmos	r	r	r · 2 (serie)
nmos	1	1 · 2(serie)	1

Table 1: Sizing of gates from Fig.1.

2 Propagation delay of an inverter

In any electronic implementation of a CMOS gate, there is a delay between the switching of an input and the switching of the output. Since n-channel devices and p-channel devices have different on-resitance the output rise delay, $t_{pd,r}$ and the output fall delay $t_{pd,f}$ are inherently different. The delay of a gate is the average of rising and falling delay.

The delay model is the same as the delay model for a capacitor being (dis)charged through a resistor with resistance R_{eff} as shown below.

$$t_{pd,inv} = \frac{t_{pd,r} + t_{pd,f}}{2} = \frac{ln(2)}{2} \cdot (R_{eff,p} + R_{eff,n}) \cdot (C_{int} + C_{ext}) \tag{1}$$

where C_{int} is the intrinsic capacitance of the inverter, which is *estimated* as the sum of all the gate capacitances, multiplied with a technology factor γ. C_{ext} is the external capacitance (wire and actual gate capacitances of all connected gates). Using the input gate capacitance as reference, the RC delay of Eq.1 can be written as:

$$t_{pd,inv} = \frac{0.69}{2} \cdot C_{int} \cdot (R_{eff,p} + R_{eff,n}) \cdot (1 + \frac{C_{ext}}{C_{int}}) = t_{pd_0} \cdot (1 + \frac{C_{ext}}{\gamma \cdot C_g}) = t_{pd_0} \cdot (1 + \frac{f}{\gamma}) \tag{2}$$

where:

- t_{pd_0}: the **intrinsic delay** of the cell.
- $\boldsymbol{f}$: the **electrical effort** or effective fan-out, is the ratio between the external load C_{ext} and input capacitance C_g.
- γ : this term is function of technology, close to 1 for submicron processes.

3 Propagation delay of complex gates

Redefining the previous Eq.2 to characterize more complex gates we obtain the following propagation delay:

$$t_{pd} = t_{pd_0} \cdot (p + \frac{g \cdot f}{\gamma}) = t_{pd_0} \cdot d \tag{3}$$

where:

- $\boldsymbol{g}$: represents the **logical effort**, meaning the ratio of the input gate capacitance C_g to the input capacitance of an inverter that delivers the same output current. This factor is included because for a given load, complex gates have to work harder than an inverter to produce a similar response. Table 2 summarizes the logical effort for some gates assuming all transistors scaled so that each gate has the same drive strength as a minimal inverter (as covered in Section 1).
- $\boldsymbol{p}$: states for the ratio of the intrinsic delay of the cell to the intrinsic delay of an inverter. The more involved structure of the multiple-input gate causes its intrinsic delay to be higher than that of an inverter. Table 3 depicts p ratio for some gates.

Gate type	Number of inputs		
	2	3	n
NAND	4/3	5/3	(n+2)/3
NOR	5/3	7/3	(2n+1)/3
Multiplexer	2	2	2
XOR,XNOR	4	12	

Table 2: Logical effort g in different gates.

Gate type	p
inverter	1
n-input NAND	n
n-input NOR	n
n-way multiplexer	2n
XOR, XNOR	n2^(n-1)

Table 3: p ratio in different gates.

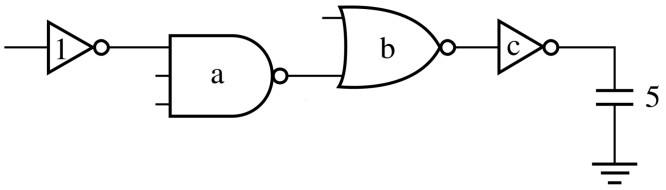

Figure 2: Example of the logic path of slide 49

4 Example

Let's calculate the delay of the path of figure 2, which you can find in slide 49.

1. We choose a pmos/nmos ratio r=2 and size each transistor so they drive the same current than the minimum inverter as explained before. Important to mention that the size depicted in a gate (a, b and c) is relative to a minimum inverter, not W/L. It means that pmos and nmos scale with the same factor, so ratio r is not affected.

2. Now we can calculate the logical effort g.

$$
\begin{aligned}
g_1 &= \frac{C_{g_1}}{C_{g_{INV}}} = 1 \\
g_2 &= \frac{C_{g_2}}{C_{g_{INV}}} = \frac{r \cdot C_{ref} + 3 \cdot C_{ref}}{1 \cdot C_{ref} + r \cdot C_{ref}} = 5/3 \\
g_3 &= \frac{C_{g_3}}{C_{g_{INV}}} = \frac{2r \cdot C_{ref} + 1 \cdot C_{ref}}{1 \cdot C_{ref} + r \cdot C_{ref}} = 5/3 \\
g_4 &= \frac{C_{g_4}}{C_{g_{INV}}} = 1
\end{aligned}
$$

3. We proceed to compute the electrical effort f.

$$
\begin{aligned}
f_1 &= \frac{C_{ext_1}}{C_{g_1}} = \frac{a \cdot 5 \cdot C_{ref}}{1 \cdot 3 \cdot C_{ref}} = \frac{a \cdot g_2}{1 \cdot g_1} \\
f_2 &= \frac{C_{ext_2}}{C_{g_2}} = \frac{b \cdot 5 \cdot C_{ref}}{a \cdot 5 \cdot C_{ref}} = \frac{b \cdot g_3}{a \cdot g_2} \\
f_3 &= \frac{C_{ext_3}}{C_{g_3}} = \frac{c \cdot 3 \cdot C_{ref}}{b \cdot 5 \cdot C_{ref}} = \frac{c \cdot g_4}{b \cdot g_3} \\
f_4 &= \frac{C_{ext_4}}{C_{g_4}} = \frac{5 \cdot C_{ref}}{c \cdot 3 \cdot C_{ref}} = \frac{5}{c \cdot g_4}
\end{aligned}
$$

4. Then we use Equation 3 for the individual delays, assuming $\gamma = 1$.

$$t_{pd_1} = t_{pd_0} \cdot (p + \frac{g_1 \cdot f_1}{\gamma}) = t_{pd_0} \cdot (1 + a \cdot g_2)$$
$$t_{pd_2} = t_{pd_0} \cdot (p + \frac{g_2 \cdot f_2}{\gamma}) = t_{pd_0} \cdot (3 + \frac{b}{a} \cdot g_3)$$
$$t_{pd_3} = t_{pd_0} \cdot (p + \frac{g_3 \cdot f_3}{\gamma}) = t_{pd_0} \cdot (2 + \frac{c}{b} \cdot g_4)$$
$$t_{pd_4} = t_{pd_0} \cdot (p + \frac{g_4 \cdot f_4}{\gamma}) = t_{pd_0} \cdot (1 + \frac{5}{c})$$

5. Finally, we compute the path delay as the summation of each gate delay.

$$t_{pd_{path}} = \sum_{i=1}^{4} t_{pd_i} \tag{4}$$