Seat. No. _____

KADI SARVA VISHWAVIDYALAYA

BE SEMESTER-IV (New) Examination April-2025

Subject Name: Computer Organization & Architecture
Subject Code: CT403-N
Date: 26/04/2025 **Time: 10:00 am – 01:00 pm** **Total Marks: 70**

Instructions:

1. Answer each section in separate answer sheet.
2. Use of scientific calculator is permitted.
3. All questions are Compulsory.
4. Indicate clearly, the option you attempt along with its respective question number.
5. Use the last page of main supplementary of rough work.

Section-I

Q-1 **(A)** Design a common bus system for four registers using mux, also describe it briefly. [5]

(B) List out Memory reference instructions and explain it with Expression. [5]

(C) Define the list of registers below for the basic computer with respect to its functionality (DR, AR, AC, IR, PC, TR, INPR, OUTR). [5]

OR

(C) Explain hardware implementation of One stage Logic Circuit of Logic Micro Operations using 4x1 mux. [5]

Q-2 **(A)** What is an Interrupt? Explain Interrupt cycle with its flowchart. [5]

(B) Explain subroutine with an example. [5]

OR

(A) Draw Only Flowchart for second pass of assembler. [5]

(B) Explain pseudo instructions. [5]

Q-3 **(A)** Explain the Input and Output programming in detail. [5]

(B) Explain different Addressing Modes of instructions. [5]

OR

(A) Explain Characteristics of RISC. [5]

(B) Explain Memory Stack organization using PUSH and POP [5]

Section-II

Q-4	(A)	What is pipelining? Explain a four-segment pipeline.	[5]
	(B)	Write a short note on Design of Accumulator Logic	[5]
	(C)	Explain Instruction Pipeline.	[5]
		OR	
	(C)	Explain RISC Pipeline stages	[5]
Q-5	(A)	Explain Binary Adder in detail.	[5]
	(B)	Explain the Three/Two/One/Zero address instructions	[5]
		OR	
	(A)	Explain any one type of data manipulation instructions	[5]
	(B)	What are the primary memories, distinguish them in tabular form.	[5]
Q-6	(A)	Draw and Explain General Register Organization.	[5]
	(B)	Write a short note on auxiliary memory.	[5]
		OR	
	(A)	Explain Major hazards (difficulties) in pipelined execution	[5]
	(B)	Explain any one mapping method of cache memory.	[5]

---X---