EEE 3308 – Lab #7 – MOSFET Switches and Logic Circuits

Objectives

Understand transistors as voltage-controlled switches instead of amplifiers. You will examine MOSFETS as switches and explore their characteristics make various useful circuits using MOSFETS, including NAND, NOR, and transmission gates.

Equipment

- Multiple resistors, capacitors, wire connections, clips, and your proto-board
- Digilent Analog Discovery (DAD) Board
- 2 each CD4007UBE MOSFET array ICs

Pre-Lab Experiments

Overview

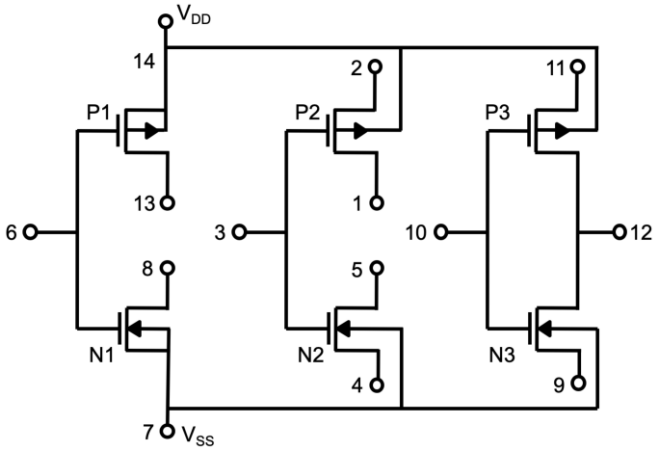
For this lab we will be using CD4007UBE transistor arrays. These arrays have both NMOSFET and PMOSET devices. Make sure you understand how both of these work before beginning the pre-lab. Please post any questions on the discussion forums provided for this week's lab.

We will start by characterizing each MOSFET as a voltage-controlled switch, measuring on-resistance, turn on/off voltage, and the voltage transfer curve (VTC). We will compare our results with the characteristics of an ideal voltage controlled switch.

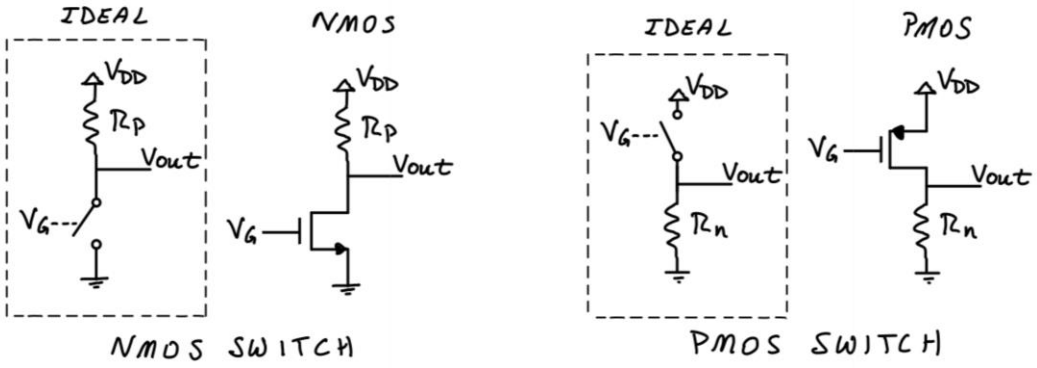
After characterizing the MOSFETs' switch properties we will learn to implement logic functions with switches using pull-up or pull-down networks. Using these principles, we will build inverter, NAND, and NOR gates. Building transmission gates is optional.

[NOTE: The lab will go smoother if you build a two-input CMOS NAND gate with one of your CD4007's and a two-input CMOS NOR gate with the other, then partially disassemble those circuits to make your measurements in the first parts of the lab.]

CD 4007 Pin Diagram



1) MOSFET Switch Characterization



You need 2 CD4007UBE transistor arrays. Review the data sheet for this component. For this part of the pre-lab you will need to build the NMOS and PMOS switch circuits in the diagram above as well as some other circuits. It is best to build these circuits using a pair of CD4007UBE chips, one for the NMOS switches and one for the PMOS switches. Use $R_p = R_n = 10$ K.

Notice that Pin 7 is connected to the source terminal of the left-most NMOS FET and to the bulk terminal for the whole chip, but is not connected to the sources of the other NMOS FETs. Pin 7 must be connected to V_{SS} to ensure the NMOS bulk connections are biased correctly. Similarly, Pin 14 is connected to the source terminal of the left-most PMOS FET and to the bulk/well terminals for the PMOS FETs, but is not connected to the sources of the other PMOS FETs. Pin 14 must be connected to V_{DD} to ensure that the PMOS bulk terminals are biased correctly.

Once you have built both circuits proceed to the following:

A. For the ideal switch circuits (enclosed by the dashed lines) what would the output be if the switch is in the open and in the closed positions?

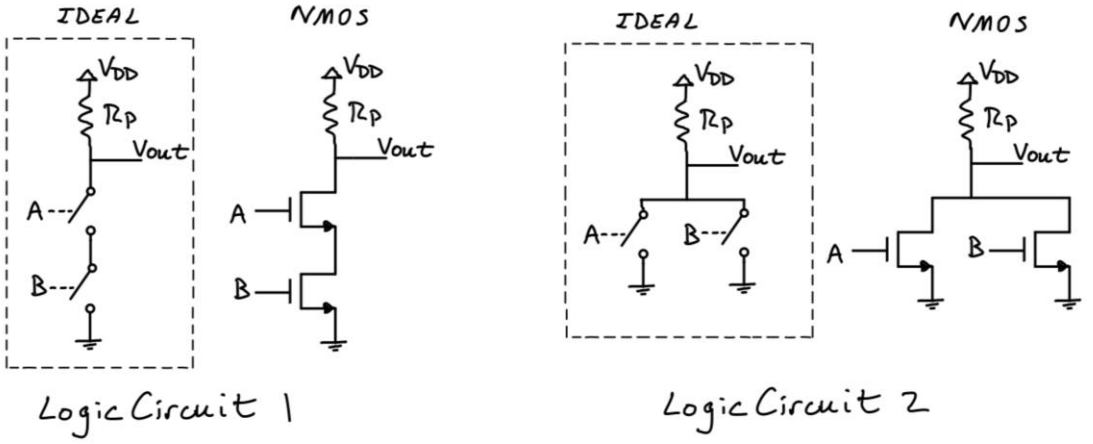
B. Find the VTC for both the NMOS and the PMOS switch circuits by sweeping V_G with V_{DD} = 5V and R_p = 10 Kohms.

C. What kind of logic gates do these circuits implement?

D. Measure Vout for the NMOS and PMOS switch circuits for the cases with $V_G = V_{DD}$ and $V_G = V_{SS}$ (= 0 V) Report the four voltages. The value of the $|V_{DS}|$ when the FET is turned on is sometimes called $V_{DS(on)}$. (Obviously, $V_{DS(on)}$ depends on the I_D and VG values with which it is measured.)

E. Calculate and report the ratio of your measured $|V_{DS(on)}|$ to I_D for your NMOS and PMOS FETs. This value is sometimes called $R_{DS(on)}$.

2) NMOSFET Pull-Down Logic Networks



Pull down (NMOS) logic circuits achieve output voltage levels or logic states by either pulling the output of the circuit to ground or by acting as an open circuit. Resistor R_p would be called a "pull-up resistor."

Consider Logic Circuit 1 above. In the ideal circuit when both switches are turned on, V_{out} is connected to ground. In this case the switches provide a path for current to "pull" the output voltage to ground. However, if either of the switches is open, then zero current flows through R_p, so V_{out} equals V_{DD}.

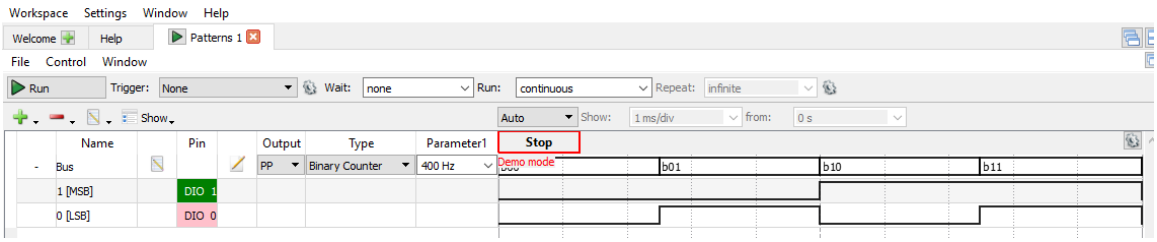
Now consider Logic Circuit 2 above. In the ideal circuit when either switch is turned on, V_{out} is connected to ground. In this case the switches provide a path for current to "pull" the output voltage to ground. Only in the case when both switches are open does zero current flows through R_p so that Vout equals V_{DD}.

A. Create tables that contain all the possible input voltage combinations for A and B for the ideal switch versions of Logic Circuits 1 and 2. You may remember this as a voltage table from EEL3701C (Digital Logic).

B. What type of logic gate is Circuit 1?

Using the CD4007UBE chips you used in Section 1, build Logic Circuits 1 and 2 shown above. **Build Logic Circuit 1 using one of the 4007 arrays, and build Logic Circuit 2 using the other array**. **Change V_{DD} to 3.3V** and V_{SS} = 0V. Make sure to connect Pin 14 to V_{DD} and Pin 7 to V_{SS} = 0V. **The change to 3.3 V is necessary to work with Patterns in the DAD.** An alternative is to use the open drain (OD) output type with a 10K pull-up resistor to V_{DD} = 5V.)

C. Use the Patterns tool on your DAD board to configure the DIO1 and DIO0 as a bus to count in binary as shown below. Set the Patterns This will test all possible input voltage combinations. **Capture the output and input waveforms using the Logic Analyzer function in the DAD.**



D. Attach a 1uF capacitor to the output of Logic Circuit 1 and repeat step C. However, this time capture the output waveform on your DAD Board's scope.

E. Measure the rise time and the fall time of the output waveform. Rise and fall times are usually considered the times it takes the output to go from 10% to 90% of the final value.

F. What would happen to the rise time if R_p were doubled? Would the fall time be affected?

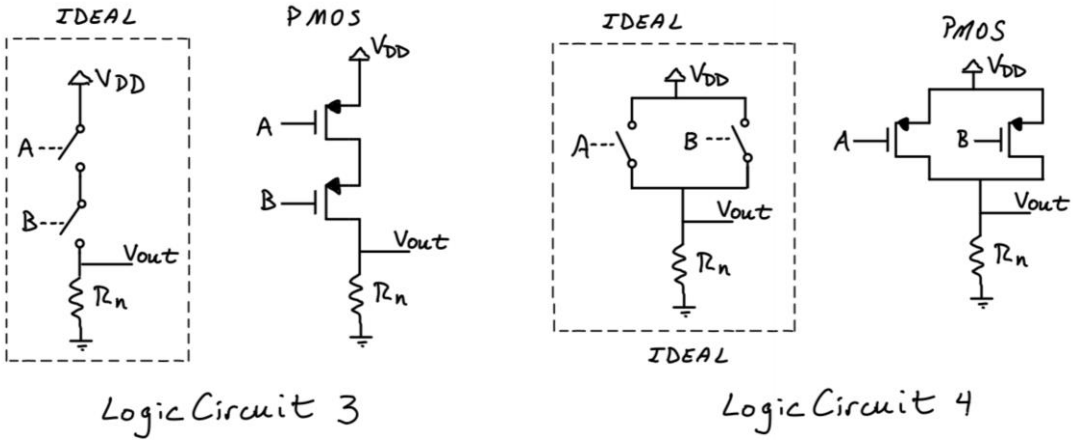
G. Now attach the largest capacitor you have in your kit to the output of Logic Circuit 1 and measure the rise and fall times. Which time is shorter? Why?

H. What type of logic gate is Circuit 2?

I. Repeat steps C through H for Logic Circuit 2 and compare the rise and fall times.

J. Which of the rise/fall times is the longest? Why?

3) PMOSFET Pull-Up Logic Networks



Logic Circuit 3 Logic Circuit 4

Pull up (PMOS) logic circuits achieve output voltage levels or states by either pulling the output of the circuit to V_{DD} or by acting as an open circuit. Resistor R_n would be called a "pull-down resistor."

Examine Logic Circuit 3. When both switches are turned on, the switches provide a path for current to "pull" the output voltage up to V_{DD}. However, if either switch is open, then the current flowing through R_n is zero and thus Vout is equal to V_{SS} = 0V.

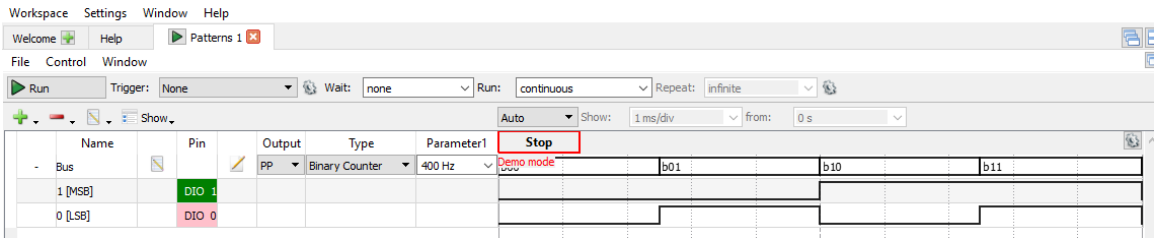
In Logic Circuit 4. if either switch is turned on, it will provide a path for current to "pull" the output voltage up to V_{DD}. Only if both switches are open will no current flow through R_n, so that Vout is equal to V_{SS} = 0V.

A. Create tables that contain all the possible input voltage combinations for A and B for the ideal switch versions of Logic Circuits 3 and 4.

B. What type of logic gate is Circuit 3?

Build Logic Circuit 3 using the 4007 array that you used to build Logic Circuit 1. **Build Logic Circuit 4 using the array you used to build Logic Circuit 2.** Use V_{DD} = 5V and V_{SS} = ground = 0V, and make sure that Pins 7 and 14 are properly connected.

C. Use the Patterns tool on your DAD board to configure DIO1 and DIO0 as a bus to count in binary as shown below. This will test all possible input voltage combinations. **Capture the output and input waveforms using the Logic Analyzer in the DAD.**



D. Attach a 1uF capacitor to the output of Logic Circuit 3 and repeat step C, but this time, capture the output waveform on your DAD Board's scope.

E. Measure the 10% to 90% rise and fall times of the output waveform.

F. What would happen to the fall time if R_n were doubled? Would the fall time be affected?

G. Now attach the largest capacitor you have in your kit to the output of Logic Circuit 3 and measure the rise time. Which rise time is shorter and why?

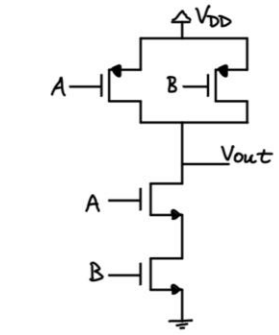
H. What type of logic gate is Circuit 3?

I. Repeat steps C through G for Logic Circuit 4 and compare the rise times

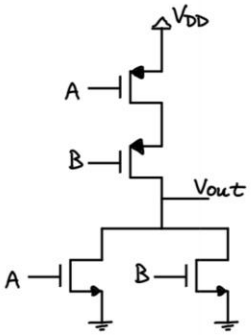
J. Which of the rise/fall times is the longest? Why?

In-Lab Experiments:

4. NAND and NOR Gates



Logic Circuits 1 & 4 Combined



Logic Circuits 2 & 3 Combined

Now combine **Logic Circuit 1 and Logic Circuit 4 all on the same 4007 array that you used to build Logic Circuit 1**. Remove R_n and R_p and connect the "A" inputs to each other, the "B" input to each other and the output pins to each other.

A. Attach a large-value capacitor to the output of the circuit and capture the output waveform on your DAD Board's scope.

B. Measure the 30% to 70% rise and fall times of the output waveform.

C. What type of CMOS logic gate have you built?

D. Which of the rise/fall times is the longest? Why?

Now combine **Logic Circuits 2 and 3 all on the same 4007 array.**

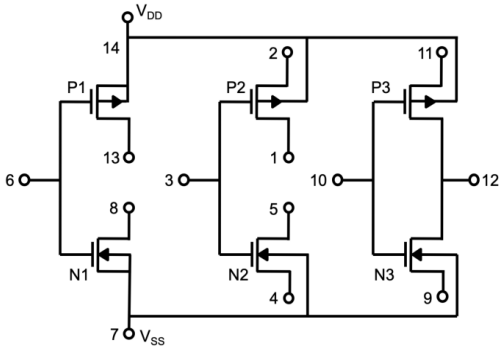
E. Attach a large-value capacitor to the output of the circuit and capture the output waveform on your DAD Board's scope.

F. Measure the 10% to 90% rise and fall times of the output waveform.

G. What type of CMOS logic gate have you built?

H. Which of the rise/fall times is the longest? Why?

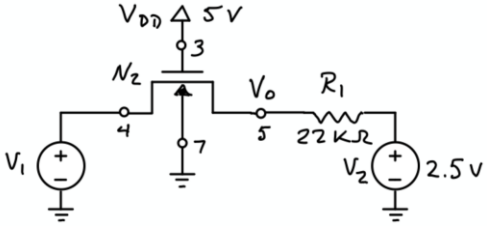
5. Transmission Gates (Optional Pre-Lab; Extra Credit of additional 25%)



In many electronics applications we need to control analog as well as digital signals. The circuit here allows bidirectional signal flow, with control signal C and its complement input "C-bar" used to turn the FETs on or off.

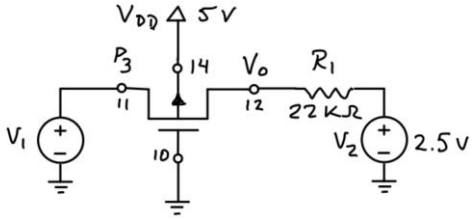
Use FETs N_2 and P_3 on the same chip to implement the circuit shown at right. Pins 1, 2 and 9 will float (not be connected to anything). We will test switches using N_2 and P_3 independently and then combine them to form a CMOS transmission gate.

A. Tie the NMOS bulk terminal (pin 7) to V_{SS} = ground and the PMOS bulk terminal (pin 14) to V_{DD} = 5V, not to the sources of the switch FETs.

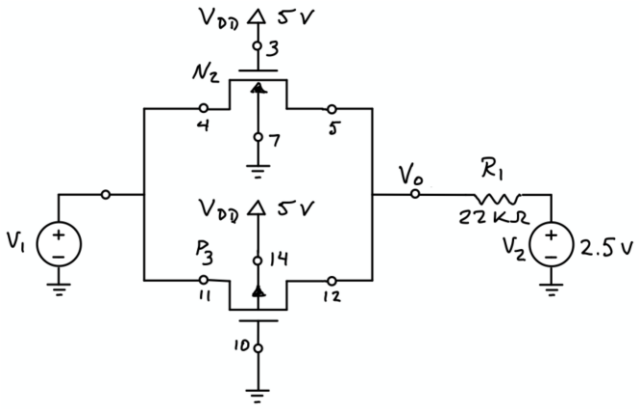


B. Connect the source of NMOS FET N_2 as shown in the test circuit above. For the set of V_1 = [0.0 1.0, 2.0, 3.0, 4.0, 5.0] V, record the corresponding values of V_o in a table.

C. Calculate the corresponding current $I = V_o/R_1$ for each data point using the measured value of R_1, estimate the "on conductance" $g_{DS(on)} = I/|V_{DS}| = I/(V_1 - V_o)$ for each data point, and include this data in your table.

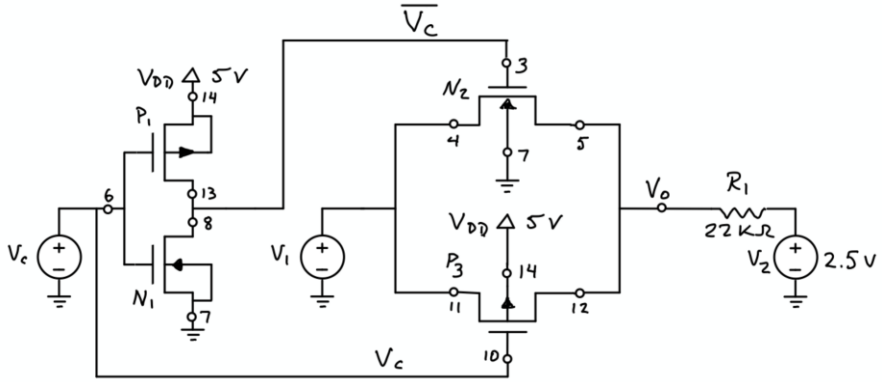


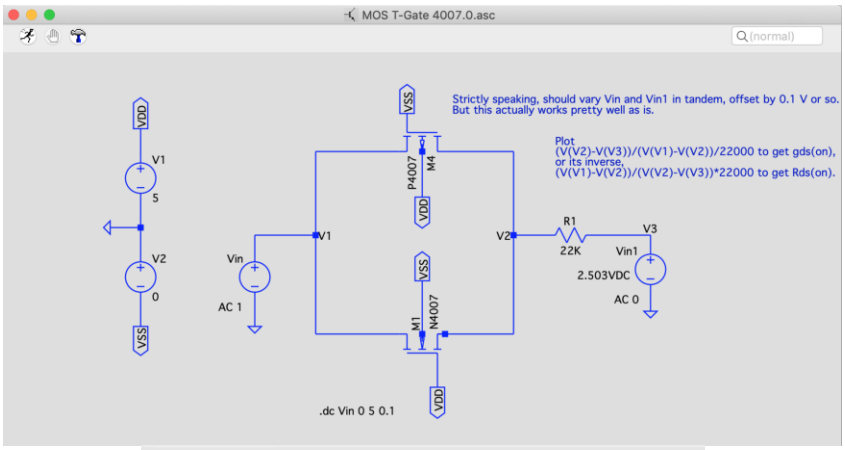
D. Repeat the process for the PMOS test circuit shown above, measuring V_o, I and $g_{DS(on)}$ for the set of V_1 = [0.0 1.0, 2.0, 3.0, 4.0, 5.0] V.

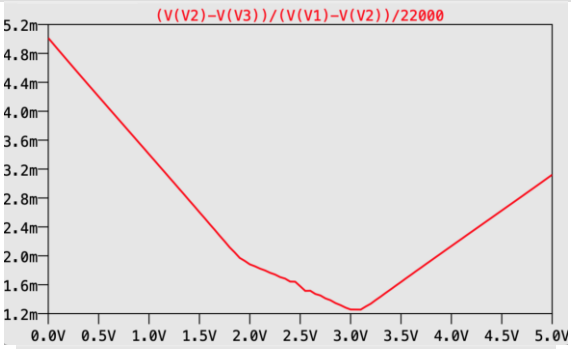


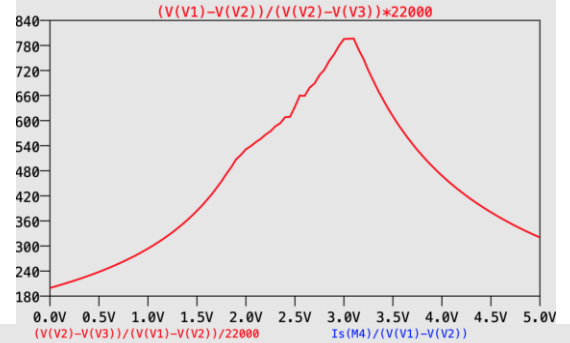
E. Connect the drains and sources of the FETs in parallel as shown above. Measure V_o, I and $g_{DS(on)}$ for the set of V_1 = [0.0 1.0, 2.0, 3.0, 4.0, 5.0] V. Calculate $R_{DS(on)} = 1/g_{DS(on)}$ for each data point.

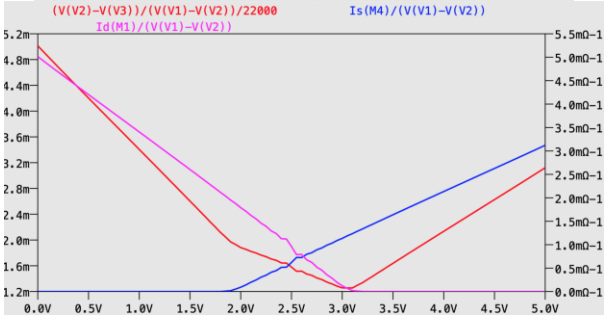
F. Add an inverter using FETs N_1 and P_1 to form a full transmission gate as shown below. Show that the control input V_C allows the gate to be switched on and off.

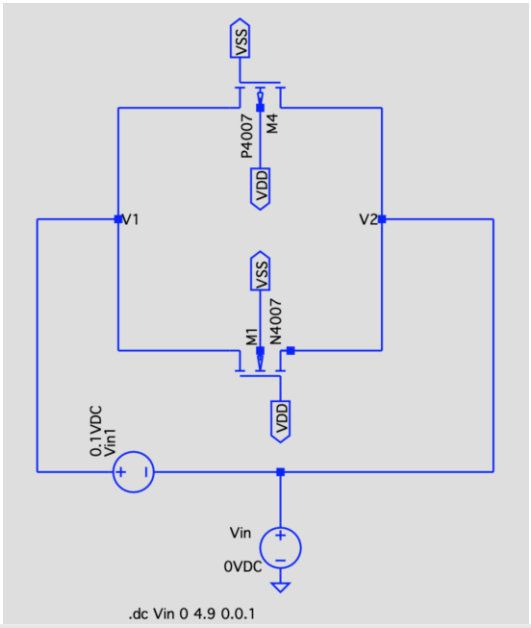


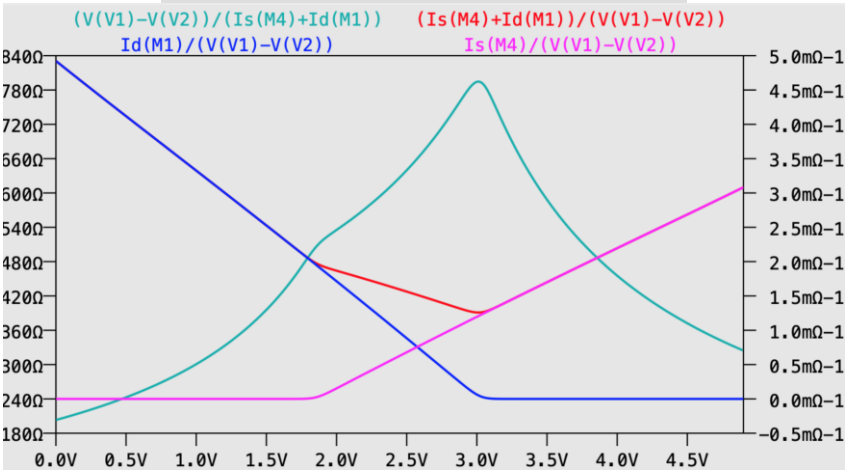

MOS T-Gate 4007.0.asc
(normal)
Strictly speaking, should vary Vin and Vin1 in tandem, offset by 0.1 V or so.
But this actually works pretty well as is.
Plot
(V(V2)-V(V3))/(V(V1)-V(V2))/22000 to get gds(on),
or its inverse,
(V(V1)-V(V2))/(V(V2)-V(V3))*22000 to get Rds(on).
VDD
V1
5
V2
0
VSS
Vin
AC 1
V1
VSS
P4007
M4
VDD
V2
R1
22K
V3
Vin1
2.503VDC
AC 0
VSS
M1
N4007
VDD
.dc Vin 0 5 0.1


(V(V2)-V(V3))/(V(V1)-V(V2))/22000
5.2m
4.8m
4.4m
4.0m
3.6m
3.2m
2.8m
2.4m
2.0m
1.6m
1.2m
0.0V 0.5V 1.0V 1.5V 2.0V 2.5V 3.0V 3.5V 4.0V 4.5V 5.0V


(V(V1)-V(V2))/(V(V2)-V(V3))*22000
840
780
720
660
600
540
480
420
360
300
240
180
0.0V 0.5V 1.0V 1.5V 2.0V 2.5V 3.0V 3.5V 4.0V 4.5V 5.0V


(V(V2)-V(V3))/(V(V1)-V(V2))/22000
Is(M4)/(V(V1)-V(V2))
Id(M1)/(V(V1)-V(V2))
5.2m
4.8m
4.4m
4.0m
3.6m
3.2m
2.8m
2.4m
2.0m
1.6m
1.2m
5.5mΩ-1
5.0mΩ-1
4.5mΩ-1
4.0mΩ-1
3.5mΩ-1
3.0mΩ-1
2.5mΩ-1
2.0mΩ-1
1.5mΩ-1
1.0mΩ-1
0.5mΩ-1
0.0mΩ-1
0.0V 0.5V 1.0V 1.5V 2.0V 2.5V 3.0V 3.5V 4.0V 4.5V 5.0V


VSS
P4007
M4
VDD
V1
V2
VSS
M1
N4007
VDD
0.1VDC
Vin1
Vin
0VDC
.dc Vin 0 4.9 0.0.1


(V(V1)-V(V2))/(Is(M4)+Id(M1))
(Is(M4)+Id(M1))/(V(V1)-V(V2))
Id(M1)/(V(V1)-V(V2))
Is(M4)/(V(V1)-V(V2))
840Ω
780Ω
720Ω
660Ω
600Ω
540Ω
480Ω
420Ω
360Ω
300Ω
240Ω
180Ω
5.0mΩ-1
4.5mΩ-1
4.0mΩ-1
3.5mΩ-1
3.0mΩ-1
2.5mΩ-1
2.0mΩ-1
1.5mΩ-1
1.0mΩ-1
0.5mΩ-1
0.0mΩ-1
-0.5mΩ-1
0.0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V