FAIRCHILD SEMICONDUCTOR®

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How to use the design tool for FSFR-series

2008 WW FAE training

PLM Display in PCK

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www.fairchildsemi.com

the power franchise™

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Motivations

- It’s a time to release all products of FSFR-series.
- To help WW FAEs to understand easily LLC topology including FSFR-series
- To help WW FAEs to design customers’ set fast and correctly
- To help customers to design LLC stage by themselves

Motivations

- It is different a little from the design sequences in AN4151-Half-bridge LLC Resonant Converter Design using FSFR-series Fairchild Power Switch (FPS™).

Design Example 1

Single Output Application for LCD TV

Design Example 1

- Single output application for LCD TV
- Specifications
  - Output: 24V/8A
  - Input: 360Vdc ~ 400Vdc (nominal 380Vdc)
- Let's start to design using "LLC design tool Ver 1.0"

Design Example 1

◆ Step 1: Fill out the input/output specifications

Multi-output could be possible up to three.

LLC Half-Bridge Converter Design Tool for FSFR series by Fairchild Semiconductor					ver 1.0
Specification & Parameter		Input	Dim.	Output	Dim.
1. Output Specifications	Output Voltage1	24	V		
	Output Current 1	8	A		
	Output Voltage 2	0	V		
	Output Current 2	0	A		
	Output Voltage 3	0			
	Output Current 3	0			
	Output Power			192.0	W
	Select Configuration of Output Rectifier	1			
	Maximum V_F of Output Diode	1	V		
2. Input Specifications	Maximum Input Voltage	400	V		
	Nominal Input Voltage	380	V		
	Estimated Efficiency	0.95			
	Input Power			202.1	W
	DC-Link Capacitor	680	uF		
	Ripple voltage @ Nominal Input			16	V
	Minimum Input Voltage	360	V		

If this is larger than the gap between Vin,nom and Vin,mim, increase the DC-Link Capacitor.

If the PFC circuit is used, then these two rows have no meaning.

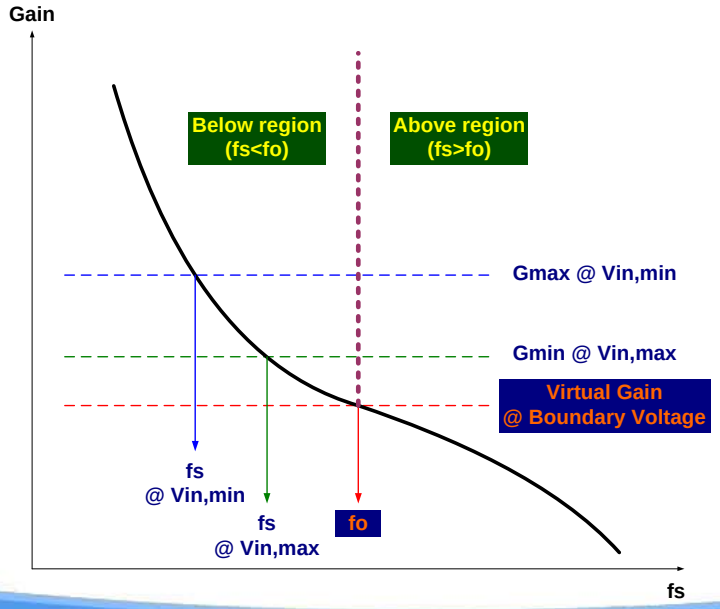
If the secondary side configuration is a center tapped, input *"1"*.
If the secondary side configuration is a bridge type, input *"2"*.

Design Example 1

◆ Step 2: Select m (Lp/Lr)

It is recommended to choose *4~8 of m*.
The conduction loss would be decreased as m increases.

3. Gain & Turns ratio	m=	6			
	Boundary Voltage	411	V		
	Minimum Gain			1.10	
	Margin of Maximum Gain	15	%		
	Required Maximum Gain			1.44	
	Turn-ratio (Np/Ns1)			9.00	
	Turn-ratio (Np/Ns2)			-	
	Turn-ratio (Np/Ns3)			-	



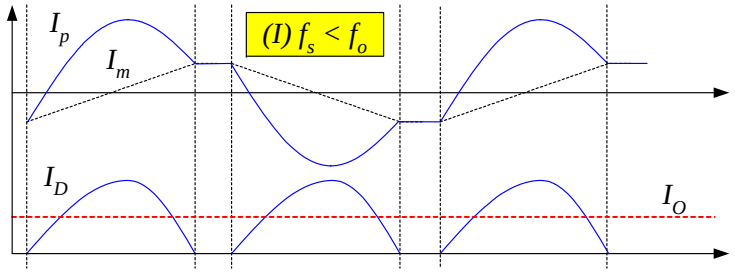
1. To make all switching frequencies depending on the input voltage below the resonant frequency (fs<fo), let the *Boundary Voltage* higher than the maximum input voltage.
If *Boundary Voltage* is less than Vin,max, above region operation could be with Vin,max.

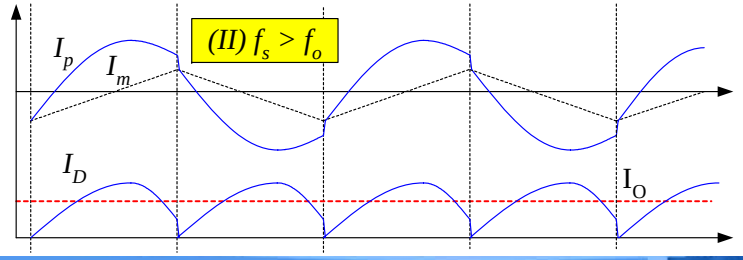
2. To make turns ratio be a natural number, tune the *Boundary Voltage* up.

Design Example 1

◆ Step 2: Select m (Lp/Lr)

3. Gain & Turns ratio	m=	6			
	Boundary Voltage	411	V		
	Minimum Gain			1.10	
	Margin of Maximum Gain	15	%		
	Required Maximum Gain			1.44	
	Turn-ratio (Np/Ns1)			9.00	
	Turn-ratio (Np/Ns2)			-	
	Turn-ratio (Np/Ns3)			-	





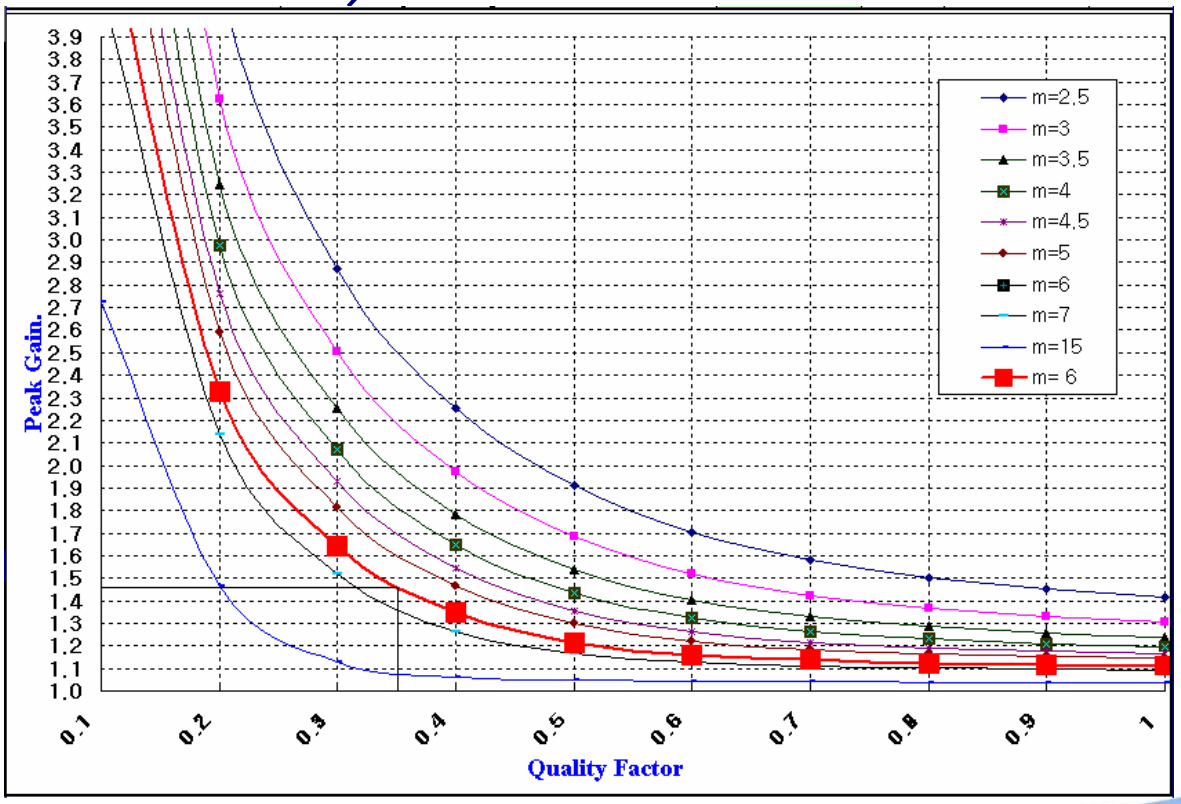
To respond properly to load changes, there should be an enough margin. ***15~20%*** is recommended.

The peak gain in the gain curve must exceed the ***Required Maximum Gain*** at full load condition.

Design Example 1

◆ Step 3: Select Q factor

This graph is obtained when m is selected.
Find out an appropriate ***Q factor*** guaranteeing the
Required Maximum Gain on ***the red curve***.



Design Example 1

◆ Step 3: Select Q factor

4. Resonant Parameters	AC Resistor			214.2	ohm
	DC Resistor			3.3	ohm
	Q factor	0.350			
	Expected Resonant Frequency	100	kHz		
	Recommended Cr			21.2	nF
	Recommended Lr			119.4	uH
	Selected Cr	22.0	nF		
	Selected Lr	120.0	uH		
	Estimated Lp			720.0	uH

Automatically calculated.

Lr and Cr could be calculated using;

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \qquad Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{AC}}$$

To guarantee the Required Maximum Gain, ***Q factor*** has to be small satisfactorily.

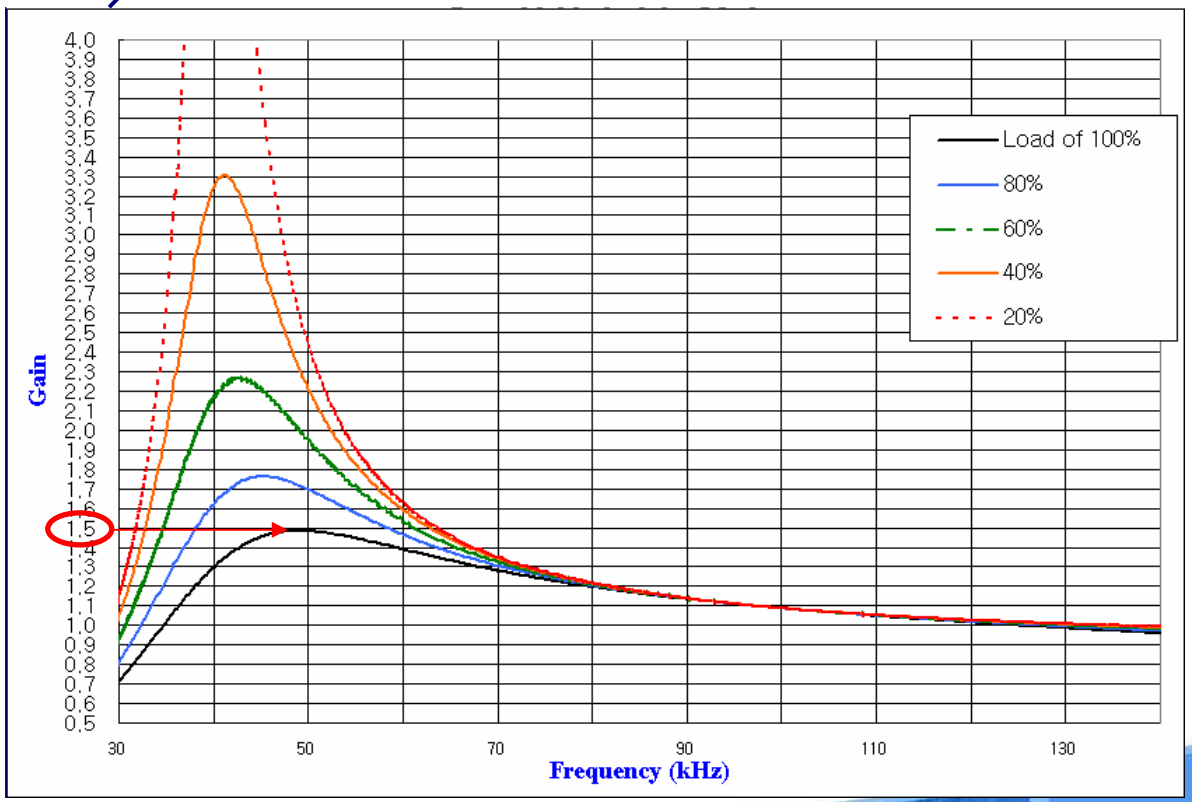
Put the desired resonant frequency down.

Choose Lr and Cr referring to the ***Recommended Values***

Design Example 1

◆ Step 4: Check the peak gain with the gain curve

Gain Curve depending on the load condition.
Check whether *the peak gain @ full load > Required Maximum Gain*
If not, go back to Step 3 and reduce Q factor.



Design Example 1

◆ Step 5: Just check out Section 5 and 6

Section 5 is only for the reference.
Remind Lp and Lr are not Lm and Llkg.

5. Transformer Parameters for Simulation	Maganitization Inductance			657.3	uH
	Leakage Inductance of Primary-side			62.73	uH
	Inductance of Secondary-side1			8.11	uH
	Leakage Inductance of Secondary-side1			0.77	uH
	Inductance of Secondary-side2			-	uH
	Leakage Inductance of Secondary-side2			-	uH
	Inductance of Secondary-side3			-	uH
	Leakage Inductance of Secondary-side3			-	uH
6. Operating Parameters	Phase Angle of Lr & Cr			615.5	krad/s
	Phase Angle of Lp & Cr			251.3	krad/s
	Resonant Freq. of Lr & Cr			**98.0**	**kHz**
	Resonant Freq. of Lp & Cr			40.0	kHz
	Operating Freq. @ Max. Input Voltage			91.7	kHz
	Operating Freq. @ Nom. Input Voltage			**83.1**	**kHz**
	Operation Freq. @ Min. Input Voltage			73.7	kHz

The real value of resonant frequency.

Estimated operating frequency
depending on the input voltage.
Check out all are below resonant frequency.

Design Example 1

◆ Step 6: Obtain components' values in the vicinity of RT pin

Referring to the gain curve, put down the minimum operating frequency. Keep it in your mind that *the set must do not enter the ZCS mode.*

7. Parameter of Control Part	Minimum Operating Frequency of IC		55	kHz		
	Maximum Operating Frequency of IC		130	kHz		
	Rmin				9.5	kohm
	Rmax				6.2	kohm
	Softstart Time		30.00	msec		
	Rss				1.7	kohm
	Css				44.3	uF
	Recommended Sense Resistor				0.22	ohm

To avoid triggering of OCP at startup, there is *50% margin* of the estimated peak primary current.

These are selected typically as *1.5k and more than 33uF.*

Design Example 1

◆ Step 7: Just check out Section 8

The estimated rms value of the primary current.
The more m, the smaller Irms.
If the transformer is too hot, there are two solutions;
First, go back to Step 2 and incrase m.
Second, increase wire gauge as large as possible.

8. Current on Input & Ouput Stage	I_{RMS} of Primary-side				1.1	Arms
	I_{PEAK} of Primary-side				1.6	A
	I_{RMS} of Output 1				9.6	Arms
	I_{RMS} of Output 2				-	Arms
	I_{RMS} of Output 3				-	Arms

It will be used to select the ***sense resistor***.
To avoid triggering of OCP at startup, there is ***50% margin*** of the estimated peak primary current.

Design Example 1

◆ Step 8: Select the secondary diode

9. Secondary Side Diode Specification	Margin of Rated Voltage	50	%		
	Margin of Rated Current	100	%		
	Rated Current & Voltage of Output 1 Diode			72.0	V
				8.6	A
	Rated Current & Voltage of Output 2 Diode			-	V
				-	A
	Rated Current & Voltage of Output 3 Diode			-	V
				-	A

3 페이지

The voltage rating is *(2*Vo)*1.5* as your input.
The current rating has *100%* margin.

Design Example 1

◆ Step 9: Transformer Design

To guarantee safe operation, ***0.2T~0.26T of Bmax*** is recommended.

Used core information

Minimum Np. ***Np must be greater than this.***

10. Transformer Specifications	Expected B_{MAX}	0.26	Tesla		
	Ae of Core	107	㎟		
	Min. Number of Primary Winding Turns			33.6	Turns
	Number of Expected Primary Winding Turns	36	Turns		
	Number of Output 1 Winding Turns			4.0	Turns
	Number of Output 2 Winding Turns			-	Turns
	Number of Output 3 Winding Turns			-	
	Primaryside Inductance			720.0	uH
	Leakage Inductance			120.0	uH
	Current Density	4	A/㎟		
	Area of Primary Winding Wire			0.28	㎟
	Area of Output 1 Winding Wire			1.56	㎟
	Area of Output 2 Winding Wire			-	㎟
	Area of Output 2 Winding Wire			-	㎟

Select the current density and the adequate wire.
If the window area of the used core is insufficient with the recommended winding wire,
increase the current density.

Design Example 1

- Design Results
  - Transformer Construction
  - Cr = 22nF
  - Secondary diode
    - FYP2010DN
  - Rmin=9k + 0.5k
  - Rmax=6k
  - Rss=1.5k
  - Css=47uF
  - Rsense=0.22

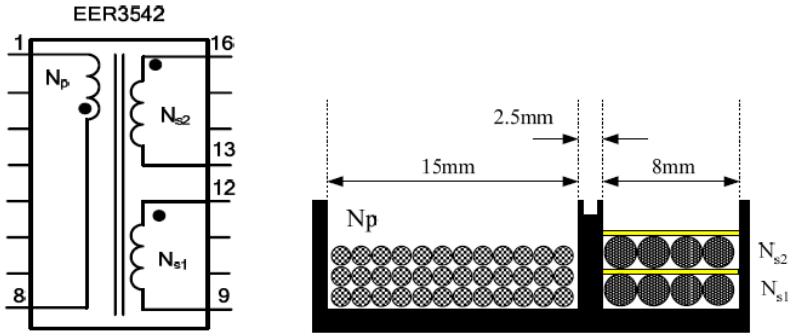


Figure 3. Transformer specification.

	Pin(S → F)	Wire	Turns	Winding Method
N_p	8 → 1	0.12φ×30 (Litz wire)	36	Section winding
N_{s1}	12 → 9	0.1φ×200 (Litz wire)	4	Section winding
N_{s2}	16 → 13	0.1φ×200 (Litz wire)	4	Section winding

Table 3. Winding Specification

Core: EER3542 (Ae=107 mm^2)
Bobbin: EER3542 (Horizontal)

Electrical Characteristics

	Pin	Spec.	Remark
Primary side Inductance (Lp)	1 – 8	720μH ± 5%	100kHz, 1V
Primary side effective leakage (Lr)	1 – 8	130μH max	Short one of the secondary windings

Table 4. Electrical Characteristics

Design Example 1

- Considerations
  - 4~8 of m is recommended.
  - Let Boundary Voltage above Vin,max.
  - Select Q factor for “Peak Gain > Required Maximum Gain.”
  - Set fs,min to avoid ZCS region operation.
  - Set the voltage margin for selecting the secondary diode.
  - 0.2T~0.26T of Bmax is recommended.
  - Np must be greater than Minimum Np.
  - If the temperature of transformer is too high,
    - Go back to Step 2, and increase m.
    - Go back to Step 9, and decrease Current Density.

Design Example 2

Dual Output Application for PDP TV

Design Example 2

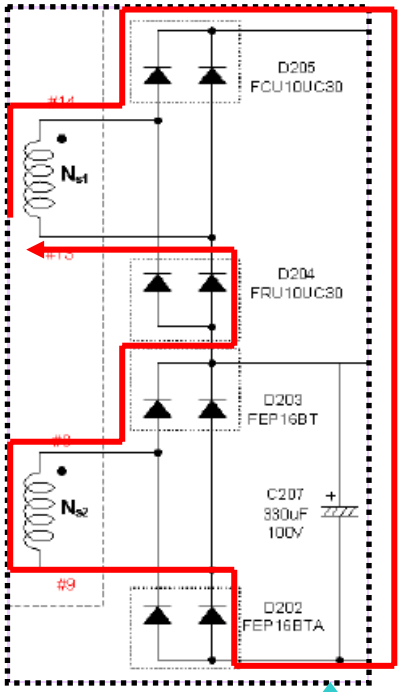
- Dual output application for PDP TV
- Specifications
  - Output: 210V/1.4A, 60V/1.5A (380W)
  - Input: 300Vdc ~ 400Vdc (nominal 390Vdc)
- Let's start to design using "LLC design tool Ver 1.0"

Design Example 2

◆ Step 1: Fill out the input/output specifications

The specifications for two outputs are inserted.

LLC Half-Bridge Converter Design Tool for FSFR series by Fairchild Semiconductor					ver 1.0
Specification & Parameter		Input	Dim.	Output	Dim.
1. Output Specifications	Output Voltage1	210	V		
	Output Current 1	1.4	A		
	Output Voltage 2	60	V		
	Output Current 2	1.5	A		
	Output Voltage 3	0			
	Output Current 3	0			
	Output Power			384.0	W
	Select Configuration of Output Rectifier	2			
	Maximum V_F of Output Diode	2	V		
2. Input Specifications	Maximum Input Voltage	400	V		
	Nominal Input Voltage	390	V		
	Estimated Efficiency	0.95			
	Input Power			404.2	W
	DC-Link Capacitor	680	uF		
	Ripple voltage @ Nominal Input			32	V
	Minimum Input Voltage	300	V		



In this case, *stacked winding* and *bridge-type rectifying* will be used so that the selecting number is *"2"* and *VF is two* for 210V output.

Design Example 2

◆ Step 2: Select m (Lp/Lr)

It is not required to be a natural number.
A rational number is OK.

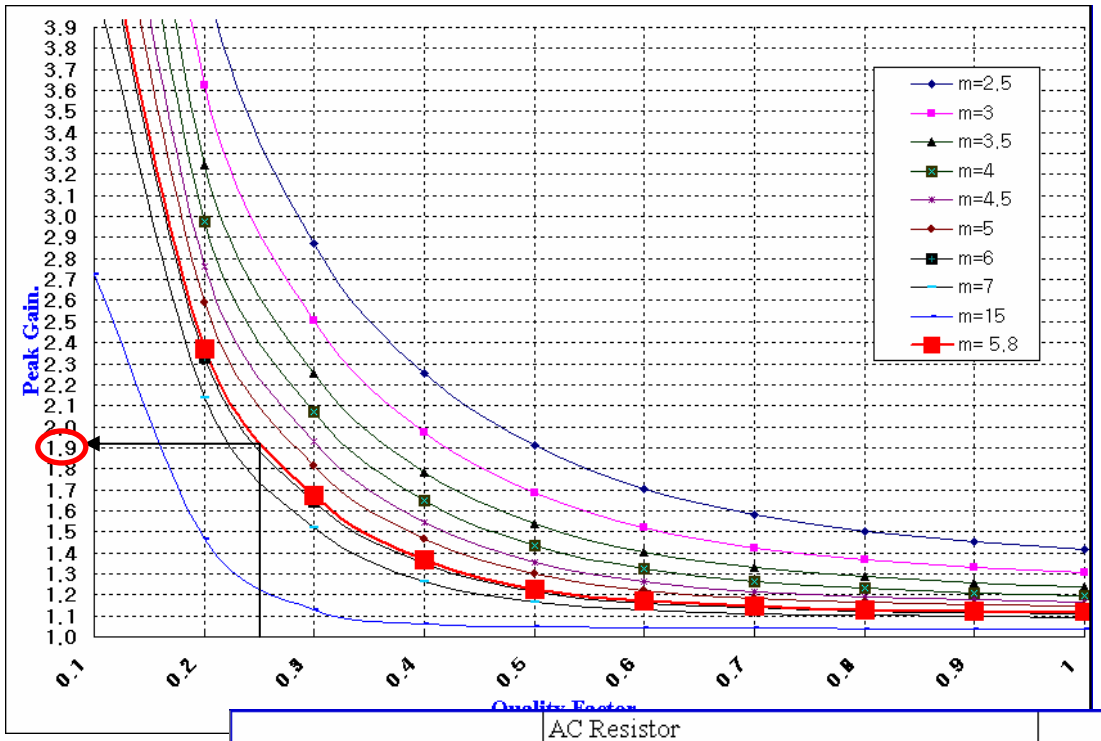
3. Gain & Turns ratio	m=	5.8			
	Boundary Voltage	400	V		
	Minimum Gain			1.10	
	Margin of Maximum Gain	30	%		
	Required Maximum Gain			1.91	
	Turn-ratio (Np/Ns1)			1.03	
	Turn-ratio (Np/Ns2)			3.44	
	Turn-ratio (Np/Ns3)			-	

In this case, the operation @ Vin,max is *the border of below/above* operation.

Margin as you want.

Design Example 2

◆ Step 3: Select Q factor

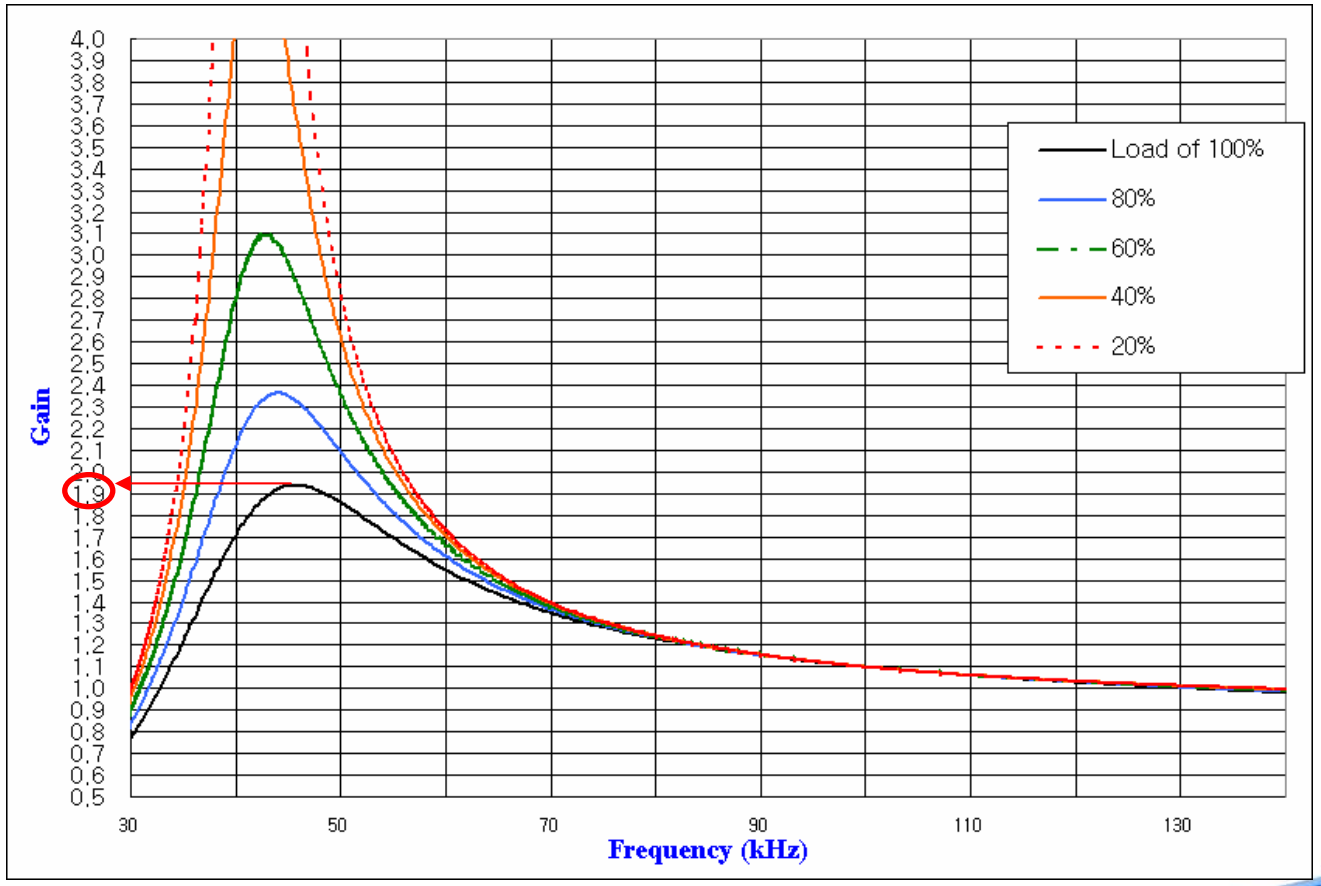


To guarantee the Required Maximum Gain, Q factor has to be small satisfactorily.

4. Resonant Parameters	AC Resistor			102.1	ohm
	DC Resistor			119.3	ohm
	Q factor	0.250			
	Expected Resonant Frequency	100	kHz		
	Recommended Cr			62.4	nF
	Recommended Lr			40.7	uH
	Selected Cr	62.0	nF		
	Selected Lr	41.0	uH		
	Estimated Lp			237.8	uH

Design Example 2

◆ Step 4: Check the peak gain with the gain curve



Design Example 2

◆ Step 5: Just check out Section 5 and 6

5. Transformer Parameters for Simulation	Maganitization Inductance			216.3	uH
	Leakage Inductance of Primary-side			21.47	uH
	Inductance of Secondary-side1			204.97	uH
	Leakage Inductance of Secondary-side1			20.34	uH
	Inductance of Secondary-side2			18.33	uH
	Leakage Inductance of Secondary-side2			1.82	uH
	Inductance of Secondary-side3			-	uH
	Leakage Inductance of Secondary-side3			-	uH
6. Operating Parameters	Phase Angle of Lr & Cr			627.2	krad/s
	Phase Angle of Lp & Cr			260.4	krad/s
	Resonant Freq. of Lr & Cr			**99.9**	**kHz**
	Resonant Freq. of Lp & Cr			41.5	kHz
	Operating Freq. @ Max. Input Voltage			103.0	kHz
	Operating Freq. @ Nom. Input Voltage			**96.5**	**kHz**
	Operation Freq. @ Min. Input Voltage			64.5	kHz

The estimated operating frequency @ Vin,max is *100kHz which is boundary.*

Design Example 2

◆ Step 6: Obtain components' values in the vicinity of RT pin

Referring to the gain curve, put down the minimum operating frequency. Keep it in your mind that *the set must do not enter the ZCS mode.*

7. Parameter of Control Part	Minimum Operating Frequency of IC		50	kHz		
	Maximum Operating Frequency of IC		130	kHz		
	Rmin				10.4	kohm
	Rmax				5.9	kohm
	Softstart Time		20.00	msec		
	Rss				1.7	kohm
	Css				30.3	uF
	Recommended Sense Resistor				0.09	ohm

Design Example 2

◆ Step 7: Just check out Section 8

The estimated rms value of the primary current.
The more m, the smaller Irms.
If the transformer is too hot, there are two solutions;
First, go back to Step 2 and incrase m.
Second, increase wire gauge as large as possible.

8. Current on Input & Ouput Stage	I_{RMS} of Primary-side				2.7	Arms
	I_{PEAK} of Primary-side				3.9	A
	I_{RMS} of Output 1				1.7	Arms
	I_{RMS} of Output 2				1.8	Arms
	I_{RMS} of Output 3				-	Arms

Design Example 2

◆ Step 8: Select the secondary diode

9. Secondary Side Diode Specification	Margin of Rated Voltage	50	%		
	Margin of Rated Current	100	%		
	Rated Current & Voltage of Output 1 Diode			315.0	V
				1.5	A
	Rated Current & Voltage of Output 2 Diode			90.0	V
				1.6	A
	Rated Current & Voltage of Output 3 Diode			-	V
				-	A

3 페이지

It is not a center-tapped configuration.
The voltage rating is ***Vo*1.5*** as your input.
The current rating has ***100%*** margin.

Design Example 2

◆ Step 9: Transformer Design

Np must be greater than Minimum Np.

10. Transformer Specifications	Expected B_{MAX}	0.2	Tesla		
	Ae of Core	232	mm²		
	Min. Number of Primary Winding Turns			21.6	Turns
	Number of Expected Primary Winding Turns	23	Turns		
	Number of Output 1 Winding Turns			22.4	Turns
	Number of Output 2 Winding Turns			6.7	Turns
	Number of Output 3 Winding Turns			-	
	Primaryside Inductance			237.8	uH
	Leakage Inductance			41.0	uH
	Current Density	4	A/mm²		
	Area of Primary Winding Wire			0.68	mm²
	Area of Output 1 Winding Wire			0.42	mm²
	Area of Output 2 Winding Wire			0.45	mm²
	Area of Output 2 Winding Wire			-	mm²

Due to the stacked winding,
Ns2 is 7 → 60V output
Ns1 is 16 → 150V output
Ns2+Ns1 is 23 → 210V output.

Design Example 2

- Design Results
  - Transformer Construction
  - Cr = 62nF
  - Secondary diode
    - FEP16BT(A)
    - FRU10UC30
    - FCU10U30
  - Rmin=10k
  - Rmax=6.2k
  - Rss=1.5k
  - Css=33uF
  - Rsense=0.05

- ✓ Core: EED4547 (Material: PL7 and Ae = 232 mm^2)
- ✓ Bobbin: Sectional bobbin with 14pin

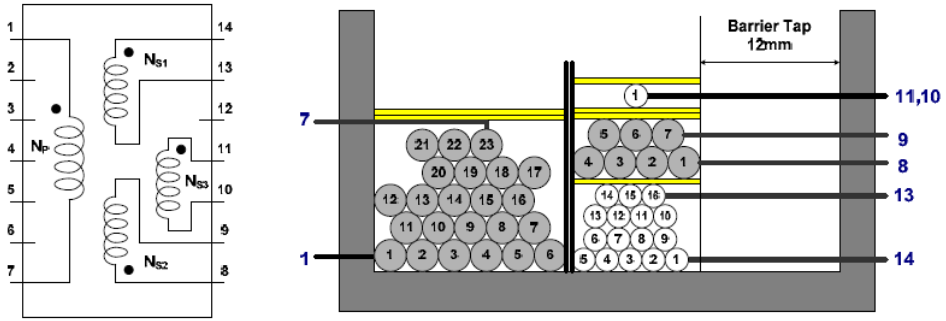


Fig. 6. Transformer specifications.

Table 3. Winding specifications.

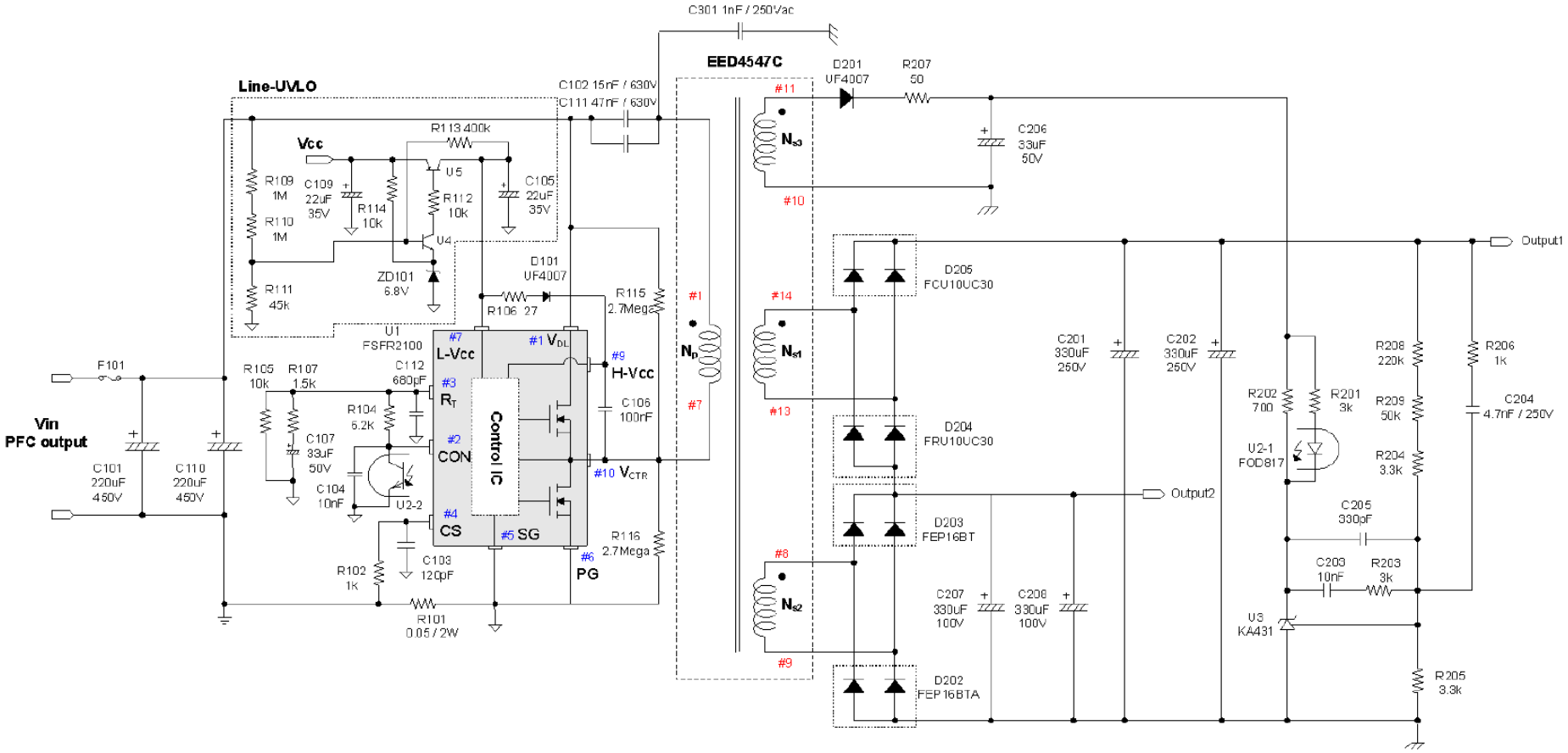
No	Winding	Pin(S → F)	Wire	Turns	Winding Method
1	N_p	1 → 7	Litz wire 0.1φ×100	23 Ts	Solenoid winding
2	N_{S1}	14 → 13	Litz wire 0.1φ×30	16 Ts	Solenoid winding Barrier Tap 12mm
3	N_{S2}	8 → 9	Litz wire 0.1φ×100	7 Ts	Solenoid winding Barrier Tap 12mm
4	N_{S3}	11 → 10	0.4 φ×1	1 Ts	Solenoid winding Barrier Tap 12mm

Table 4. Electrical characteristics.

Parameter	Pin	Spec.	Remark
Inductance	1-2	240uH ± 5%	100kHz, 1V
Leakage	1-2	40uH ± 5%	Short all output pins

Design Example 2

◆ Circuit Diagram



Design Example 2

- Considerations
  - VF could be changed depending on the transformer construction.
  - 4~8 of m is recommended. No need to be a natural number.
  - Let Boundary Voltage above Vin,max. ← Recommendation
  - Select Q factor for “Peak Gain > Required Maximum Gain.”
  - Set fs,min to avoid ZCS region operation.
  - Set the voltage margin for selecting the secondary diode.
  - 0.2T~0.26T of Bmax is recommended.
  - Np must be greater than Minimum Np.
  - If the temperature of transformer is too high,
    - Go back to Step 2, and increase m.
    - Go back to Step 9, and decrease Current Density.

Thank you !