Implementation of Digital Phase Locked Loop using CMOS Technology

Abstract: The requirement for low power and rapid circuits are expanding in present day hardware. The generation of carrier and locking of phase have become significant for transceiver circuits. The frequency divider which is dependent on the phase locked loop (PLL) is a fundamental building block of the transceiver. The frequency divider that produces carrier for the down-conversion/up-conversion functions, it works at high frequency and it expends a massive portion of the whole power of the circuit. The frequency divider dependent on phase locked loop (PLL) comprises of voltage-controlled oscillator (VCO), phase detector, loop filter and frequency divider. The voltage-controlled oscillator (VCO) and frequency divider expends the utmost power. This project presents a CMOS digital phase locked loop which is proposed with low power utilization voltage-controlled oscillator (VCO) circuit and frequency divider circuit using 45nm CMOS technology. The overall performance has been simulated and examined using Tanner EDA platform. Using this, we are reducing time delay, area and power consumption as compared to that of conventional circuits.