NAGA ROHITHA.B

Rohithabn12@gmail.com | 8639070952

EXPERIENCE

CAPGEMINI| Associate Engineer
OCT 2022 – FEB 2024 | Bengaluru.

- Achieved successful outcomes by maintaining accurate documentation and meeting strict deadlines.
- Captured technical schematics for use in project planning and execution.
- Designed ethernet component circuits and printed circuit board stack up and PCB area Analysis, designed block diagrams and completing interfacing components & Data sheet observations.

PROJECTS

Implementation of digital Phase Lock Loop using CMOS Technology

It is used for frequency synthesizer circuits. The main goal of a PLL is to synchronize the output oscillator signal with a reference signal. Even if the two signals have the same frequency, their peaks and troughs may not occur in the same place. Simply put, they do not reach the same point on the waveform at the same time.

Design and implementation of Low power SOC Memory BIST

Developed a Built-In Self-Test (BIST) mechanism for system-on-chip (SoC) memory, focusing on low power consumption and efficient fault detection

EDUCATION

GITAM UNIVERSITY BENGALURU
MASTERS OF TECHNOLOGY
VLSI (very large scale integration)
Expected May 2026

SWARNANDHRA COLLEGE OF ENGINEERING AND TECHNOLOGY NARASAPURAM
BACHLORES OF TECHNOLOGY
06/2018 -06/2022

- **Electronics and communication engineering**

SKILL

C Programming
VERILOG
VHDL(Basic)
MATLAB
LINUX
MULTISIM
CADANCE
TOP-SPICE

PERSONAL INFO

Date of Birth :12-06-00
Nationality: Hindu
Gender: Female
Marital status: Unmarried

ACHIEVEMENTS

Worked as a School representative in (2015-2016)

ACHARANA Charitable trust: Worked as volunteer and conducted many events successfully during college Narasapuram. (2019 - 2022)

LINKS

LinkedIn: https://www.linkedin.com/in/rohitha-bn-776909215/?utm_source=share&utm_campaign=share_via&utm_content=profile&utm_medium=android_app