Bo-Yuan Huang

Curriculum Vitae

Contact

Email: bo-yuan.huang@intel.com
Phone: (+1) 917-770-2804

https://bo-yuan-huang.github.io

Research Interests

I am interested in all aspects of security, automated reasoning, and design methdology, automation, and verification of heterogeneous computing systems.

Education

Princeton University, USA
Ph.D., Electrical and Computer Engineering, 2021

Thesis: Instruction-Level Abstraction for Program Compilation and Verification in Accelerator-Rich Platforms
Advisor: Prof. Sharad Malik
Committee: Prof. Margaret Martonosi and Prof. Naveen Verma

Princeton University, USA
M.A., Electrical Engineering, 2017

National Taiwan University, Taiwan
B.S., Electrical Engineering, 2014

Experience

2021 – present

Intel Corporation, Security Research
Offensive Security Researcher
Researching formal information flow veriifcation applied to SoC interconnect fabrics
Researching hardware security vulnerability detection using ML-based static analysis
Researching automated formal firmware verification for RoT virtualization platforms

2015 – 2021

Princeton University, Department of Electrical and Computer Engineering
Research Assistant
Advisor: Prof. Sharad Malik
Thesis researching the Instruction-level Abstraction model and its applications in design automation and verification of SW/FW/HW in heterogeneous computing platforms
Led multi-institutes research on modular and verifiable end-to-end compilation flow for deep-learning applications (DSL to ASIC)

Summer 2019

Microsoft Research, New Security Ventures & Research in Software Engineering
Research Intern
Supervisor: Dr. Patrice Godefroid and Dr. Marina Polishchuk
Designed grammar-based fuzzing algorithm with dynamic learning for stateful REST API
Implemented REST API data fuzzer for cloud services on top of RESTler

Summer 2018

Microsoft Research, Research in Software Engineering
Research Intern
Supervisor: Dr. Patrice Godefroid and Dr. Barry Bond
Designed white-box fuzzing algorithm for attacker-memory-safety of OS kernels
Implemented kernel-aware symbolic memory checker on top of SAGE

Summer 2017 **Intel Corporation,** Security Center of Excellence
Security Research Intern
Developed formal modeling and verification framework for concurrent firmware
Exploited TOC/TOU security vulnerability in an inter-IPs communication protocol

Summer 2016 **Intel Corporation,** Security Center of Excellence
Technical Intern
Word-level bounded model checking of SoC Secure Boot flow with QEMU IA semantics

2014 – 2015 **Coast Guard Administration**
Second Lieutinant
Designed and developed the first search and rescue procedure assisting system for Taiwan coastal area based on USCG drift theory

2013 – 2014 **National Taiwan University,** Applied Logic and Computation Lab
Undergraduate Research Assistant
Advisor: Prof. Jie-Hong Roland Jiang
Asynchronous QDI circuit synthesis from signal transition protocols

Summer 2013 **TSMC,** Advanced Process Transferring Group
Software Engineer Intern
Developed automation and visualization tools for GDS and design pattern analysis

2012 – 2013 **National Taiwan University,** Wireless and Mobile Networking Lab
Undergraduate Research Assistant
Advisor: Prof. Hung-Yu Wei
Protocol design and game theoretic solutions for device-to-device radio resource allocation

Teaching Experience

Fall 2018 **Princeton ECE 206/COS 306 - Contemporary Logic Design**
Head Assistant Instructor
This course teaches digital logic design and introductory computer organization. I was the head assistant instructor (AI) for this 170-students course. I organized the graduate and undergraduate AI team, taught precepts, held laboratory hours, prepared exam materials, and graded assignments/exams. I received ***Best Teaching Assistant Award***.

Fall 2016, 2017 **Princeton ECE 206/COS 306 - Contemporary Logic Design**
Assistant Instructor
I was twice an AI for this course and I taught precepts, held laboratory hours, prepared exam materials, and graded assignments/exams.

Co-Supervision of Undergraduate and Graduate Students

- Intel Intern – Elijah Bryant (Universal Language for Information Flow Tracking, 2022)
- Intel Intern – Isabella Siu (LLVM-based Firmware Instrumentation, 2022)
- REU Program – Sarah Schabar (Crypto-accelerator-rich SoC Analysis, 2021)
- REU Program – Isabella Siu (Secure Bootloader Verification, 2021)
- ECE Junior Thesis – Phoebe Lin (Parallel SAT Solver, 2021)
- CS Visiting Scholar – Yueling Zhang (HDL Synthesis and Hardware Abstraction, 2018)
- ECE Senior Thesis – David Gilhooley (Verified Boot in Trusted Platform Module, 2016)

Awards and Honors

2020	ACM TODAES Best Paper Award
2019	Teaching Assistant Award, Princeton University
2017, 2018	NSF SSFT Travel Grant
2017	SRC TECHCON Best in Session Award
2016	NSF VMW Full Scholarship, CAV
2015	SEAS Travel Grant, Princeton University
2015	Francis Robbins Upton Fellowship, Princeton University
2014	First Prize: Outstanding Undergraduate Independent Research, NTU
2014	Second Prize: TSMC Special Research Competition
2013	TSMC Undergraduate Research Grant
2013	Ministry of Science and Technology Research Grant
2012	First Prize: TSMC Semiconductor Elite Program
2012	First Prize: Microsoft WP Platform Workshop Innovation Award
2011,2012,2013,2014	President's Awards, NTU

Publications

Journal Articles

Bo-Yuan Huang, Hongce Zhang, Pramod Subramanyan, Yakir Vizel, Aarti Gupta, and Sharad Malik. Instruction-Level Abstraction (ILA): A Uniform Specification for System-on-Chip (SoC) Verification. *ACM Transactions on Design Automation of Electronic Systems (TODAES),* 2019. ***Best Paper Award***.

Pramod Subramanyan, **Bo-Yuan Huang**, Yakir Vizel, Aarti Gupta, and Sharad Malik. Template-based Parameterized Synthesis of Uniform Instruction-Level Abstractions for SoC Verification. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD),* 2018.

Shih-Tang Su, **Bo-Yuan Huang**, Chih-Yu Wang, Che-Wei Teh, and Hung-Yu Wei. Protocol Design and Game Theoretic Solutions for Device-to-Device Radio Resource Allocation. *IEEE Transactions on Vehicular Technology (TVT),* 2017.

Conference Proceedings

Yu Zeng, **Bo-Yuan Huang**, Hongce Zhang, Aarti Gupta, and Sharad Malik. Generating Architecture Level Abstractions from RTL Designs for Processors and Accelerators. Part I: Determining Architectural State Variables. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* 2021.

Patrice Godefroid, **Bo-Yuan Huang**, and Marina Polishchuk. Intelligent REST API Data Fuzzing. *ACM Joint European Software Engineering Conference and Symposium on the Foundations of Software Engineering (FSE),* 2020.

Bo-Yuan Huang, Hongce Zhang, Aarti Gupta, and Sharad Malik. ILAng: A Modeling and Verification Platform for SoCs using Instruction-Level Abstractions. *International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS),* 2019.

Yue Xing, **Bo-Yuan Huang**, Aarti Gupta, and Sharad Malik. A Formal Instruction-Level GPU Model for Scalable Verification. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* 2018.

Bo-Yuan Huang, Sayak Ray, Aarti Gupta, Jason Fung, and Sharad Malik. Formal Security Verification of Concurrent Firmware in SoCs using Instruction-Level Abstraction for Hardware. *ACM/ESDA/IEEE Design Automation Conference (DAC),* 2018.

Bo-Yuan Huang, Yi-Hsiang Lai, and Jie-Hong Roland Jiang. Asynchronous QDI Circuit Synthesis from Signal Transition Protocols. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD),* 2015.

Workshop Proceedings

Bo-Yuan Huang, Steven Lyubomirsky, Thierry Tambe, Yi Li, Mike He, Gus Smith, Gu-Yeon Wei, Aarti Gupta, Sharad Malik, Zachary Tatlock. From DSLs to Accelerator-Rich Platform Implementations: Addressing the Mapping Gap. *Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE),* 2021.

Hongce Zhang, **Bo-Yuan Huang**, Yue Xing, Aarti Gupta, Sharad Malik. Hardware-Software Interface Specification for Verification in Accelerator-Rich Platforms. *Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE),* 2021.

Bo-Yuan Huang, Hongce Zhang, Pramod Subramanyan, Yakir Vizel, Aarti Gupta, and Sharad Malik. Instruction-Level Abstraction (ILA): Democratizing Instructions for SoCs. *SRC TECHCON*, 2017. ***Best in Session Award***.

Bo-Yuan Huang, Shih-Tang Su, Chih-Yu Wang, Che-Wei Teh, and Hung-Yu Wei. Resource Allocation in D2D Communication - A Game Theoretic Approach. *IEEE International Conference on Communications Workshops (ICC),* 2014.

(In Submission)

Priyam Biswas, Sayak Ray, Stephan Heuser, **Bo-Yuan Huang**, Rana Elnaggar, and Jason Fung. Effectiveness of Artificial Intelligence in Detecting Hardware Security Issues: Challenges, Status Quo, and Directions. *Workshop on Attacks and Solutions in Hardware Security (ASHES).*

Bo-Yuan Huang, Sayak Ray, Nagaraju Kodalapura, Jason Fung. Checking the Checker: Formal Verification for Security Evaluation of Root-of-Trust Firmware. *Design, Automation, and Test in Europe Conference (DATE).*

Bo-Yuan Huang, Steven Lyubomirsky, Yi Li, Mike He, Thierry Tambe, Gus Henry Smith, Akash Gaonkar, Vishal Canumalla, Andrew Cheung, Gu-Yeon Wei, Aarti Gupta, Zachary Tatlock, and Sharad Malik. Application-Level Validation of Accelerator Designs Using a Formal Software/Hardware Interface. *Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS).*

Akash Gaonkar, **Bo-Yuan Huang**, Yi Li, Mike He, Steven Lyubomirsky, Gus Henry Smith, Vishal Canumalla, Andrew Cheung, Thierry Tambe, Gu-Yeon Wei, Aarti Gupta, Zachary Tatlock, and Sharad Malik. Modular and Semi-Automatic Formal Verification of Hardware Offloading in High Performance Programs using Constrained Horn Clauses. *Computer-Aided Verification (CAV).*

Patent

Patrice Godefroid, Bo-Yuan Huang, and Marina Polishchuk. Intelligently fuzzing data to exercise a service. Patent, May 2022. US 11321219 B2.

Talks & Tutorials

June 2022	Tutorial – "Generalizing the ISA to the ILA: A Software/Hardware Interface for Accelerator-rich Platforms." *International Symposium on Computer Architecture (ISCA)*
May 2022	Tutorial – "Generalizing the ISA to the ILA: A Software/Hardware Interface for Accelerator-rich Platforms." *Annual Symposium of the Applications Driving Architectures (ADA) Center*
May 2021	Invited Talk – "Instruction-Level Abstraction & ILAng: A Modeling and Verification Platform for SoCs." *Paul G. Allen School of Computer Science & Engineering, University of Washington.* (Host: Prof. Luis Ceze)
April 2021	Invited Talk – "Instruction-Level Abstraction for Accelerator-rich Architectures' Specification and Verification." *Graduate Institute of Electronics Engineering, National Taiwan University.* (Host: Prof. Chien-Mo Li)
April 2021	Invited Talk – "Instruction-Level Abstraction for Software Development and Verification in Accelerator-rich Computing Systems." *Security and Privacy Lab, Intel Labs.* (Host: Dr. Carlos V Rozas)

Professional Service

2017-2022	External Review Committee, DAC
2020	Program Committee, Artifact Evaluation, CAV
	Reviewer for IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), ICC, ICCAD, and FMCAD

Community Service

2022	Program Manager, Princeton-Intel Research Experience for Undergraduate (REU) Program
2021	Mentor, Princeton-Intel Research Experience for Undergraduate (REU) Program
2019 – 2021	Mentor, ReMatch Undergraduate Summer Research Program
2017 – 2019	Mentor, Princeton Early Career Mentoring Program
2017 – 2019	Speaker, Graduate Student Orientation Workshop Series
2017 – 2018	Vice President, Princeton Association of Taiwanese Students

This curriculum vitae was last updated on 14th August, 2022.