BOCHEN YE

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EDUCATION

Eindhoven University of Technology Sep 2022 - Now
Msc. Electrical Engineering(track: Electronic System) Eindhoven, NL

- **GPA**: 7.5/10
- **Relevant Course**: Digital integrated circuit design, Embedded computer architecture, Electronic design automation, Applied combinatorial algorithms, Intelligent architectures(focus on DNN/Hardware co-design), Systems on silicon(focus on SoC backend), Neuro computation(focus on Neuromorphic computing).

Hefei University of Technology Sep 2018 - Jul 2022
BEng. Integrated Circuit Design and Integration System Hefei, China

- **GPA**: 83.1/100 (TOP 22%)
- **Relevant Class**: Analysis and Design of Integrated Digital Circuit, Microprocessor architecture and design, Introduction to SoC design, Verilog HDL and FPGA implementation and so on.
- **Honors and awards**: Scholarship(21/22), get an A in graduation thesis.

INTERNSHIP EXPERIENCE

Digital Design Intern(Master thesis) Mar 2024 - Now
NXP Semicoductors Nijmegen, NL

- Define a custom digital communication protocol between two ICs.
- Develop and verify an IP module implementing the new communication protocol by using **SystemVerilog**.
- Build a prototype demonstrator with FPGA(s).
- This internship supervised by Manil Dev Gomony(Bell Lab & TU/e) and Kimmo Salo(NXP).

IP modeling and Design Intern Jul 2023 - Oct 2023
Synopsys(then Intrinsic ID) Eindhoven, NL

- Study on a trellis-based Reed-Muller codec and use Python modeling it as a digital IP module(software).
- Design the architecture of codec and implementation by **VHDL**(hardware).
- Verify on **Arty-z7 FPGA(zynq)** with Vivado and Vitis(Embeded System).
- Under the condition of 50MHz, the hardware resource consumption is reduced from 938 LUT to 843 LUT after several improvements. At the same time, the decoding delay is reduced to 6 clock cycles and can be decoded continuously.
- This internship supervised by Manil Dev Gomony(Bell Lab & TU/e) and Roel Maes(Intrinsic ID).

NoC Design Intern Oct 2021 - May 2022
Institute of VLSI Design of HFUT Hefei, China

- Study the knowledge of Network-on-Chip(NoC) Router Based on Packet Connected Circuit(PCC).
- Implement the router and routing algorithm of PCC-NoC by using **Verilog**.
- Verify it on FPGA and use UART(with FIFO) to communicate with PC and use Python to verify result automatically.
- This project as my bachelor graduation project got A and advised by Zhenmin Li(HFUT).

PROJECTS

Tiny LeViT Hardware Accelerator Apr 2024 - Now

- This is my hobby project using by System Verilog.
- Used row stationary (RS) and systolic array to accelerate the convolutional layer.

Low power synthesis and physical design of SOC based on MIPS and AES Apr 2023 - Jun 2023

- The **SoC** include five-stage pipelined mMIPS processor core, AES encryption module, AHB and APB bus. Used Cadence Incisive to simulation and functional verification.
- Used Cadence **Genus** for logic synthesis with low power strategies which is reduce 3% power consumption under 125MHz.
- Used Cadence **Innovus** for place and route with two power domain which is reduce 8% power consumption under 200MHz.

Inference acceleration of deep neural network based on TCU accelerator Feb 2023 - Apr 2023

- Trained a multilayer perceptron for handwritten digit classification(MNIST) using the **PyTorch** framework.
- Optimized a VGG5 for image classification using various quantization and pruning techniques. Explored the impact of these techniques on both accuracy and compute cost.
- Use open source Tensil AI for generating tensor computing units(TCU), compiling and accelerating ResNet20 by systolic array on PYNQ .

Full Custom 16-bit Brent-Kung Adder Design Nov 2022 - Jan 2023

- Completed CMOS circuit design and layout design for a 45nm full custom 16-bit Brent-Kung adder. Used Cadence **Virtuoso** Circuit for design and layout design, used **Calibre** for DRC and LVS verification of the layout. The circuit can be functionally verified by simulation at 500MHz, 90°C with an output rise and fall time of less than 100ps, and the layout results can be functionally verified at a post-simulation of 500MHz.

Five-stage pipelined RISC-V processor with full hazard handling Feb 2023 - Mar 2023

- Implemented a **RISC-V** five-stage pipeline processor with full hazard handling. The RTL level design used by Verilog and simulated in Modelsim for simulation. The processor can run the basic RV32i instructions, solves data conflicts, structure conflicts, and control conflicts, and supports stalling, flushing and forwarding.

Implementation of image processing kernels on CUDA Dec 2022 - Jan 2023

- Mapping Grayscale processing and convolution 2D kernels from C to **CUDA** and optimize the loop, then running on the Nvidia GPU A100. The result is that the processing time of 13 images is accelerated from 4872ms to 27ms.

Design of Lightweight System Based on SystemC Dec 2020 - Jan 2021

- Studying the structural design of soc, and use **SystemC** to write Bus and UART serial interface, function processing module, arbiter module, data receiving and sending module to form a lightweight system and verify it. Drive data enters two processing modules, and one of the results is selected by the arbiter in the bus and sent to the receiving module through UART interface and displayed.

SKILLS AND LANGUAGE

- **Professional:** Verilog/VHDL/SystemVerilog · FPGA · Linux · Cadence(Virtuoso, Incisive, Genus, Innovus)
- **Miscellaneous:** Python · C/C++ · SystemC · MS Office · LaTex · CUDA · Pytorch · Perl/TCL/Shell
- **Language:** Chinese Mandarian: Native, **English:** TOEFL(iBT) 92