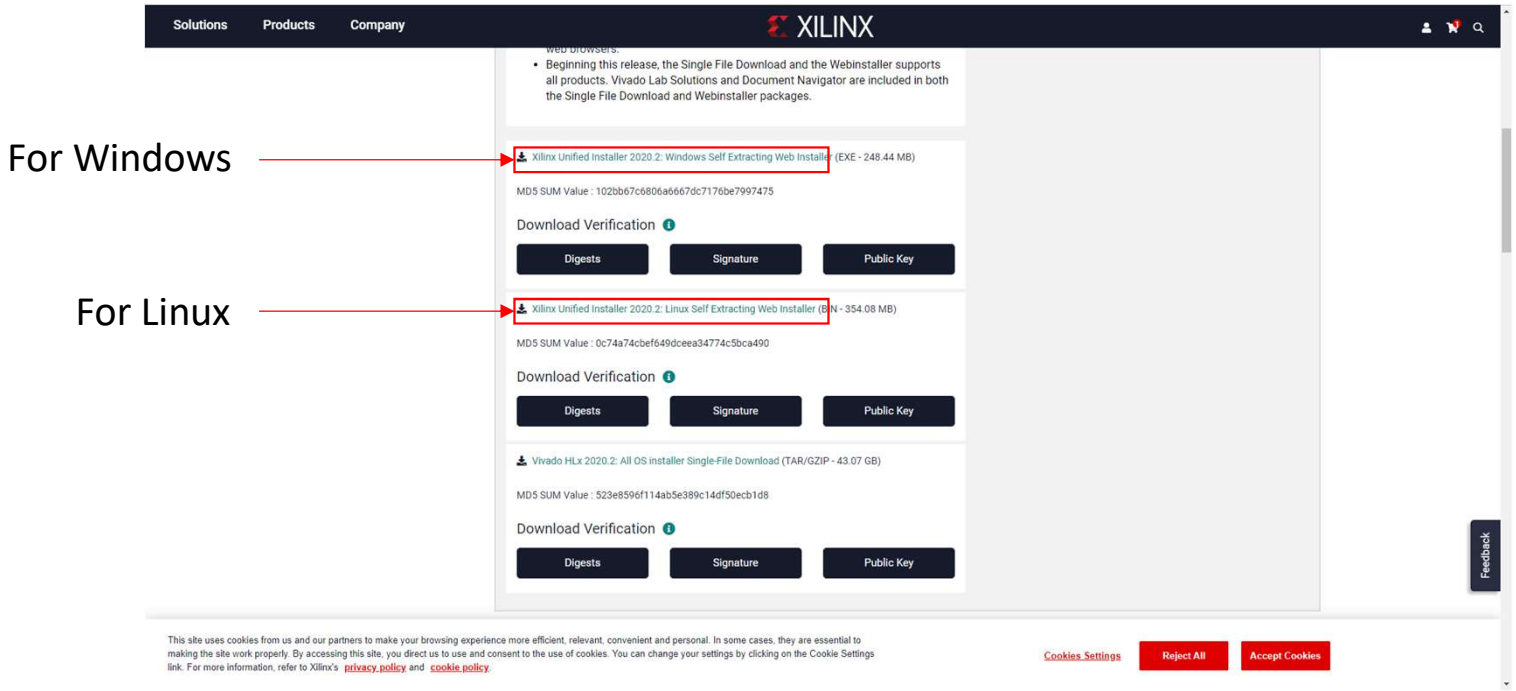
Lab2 guide

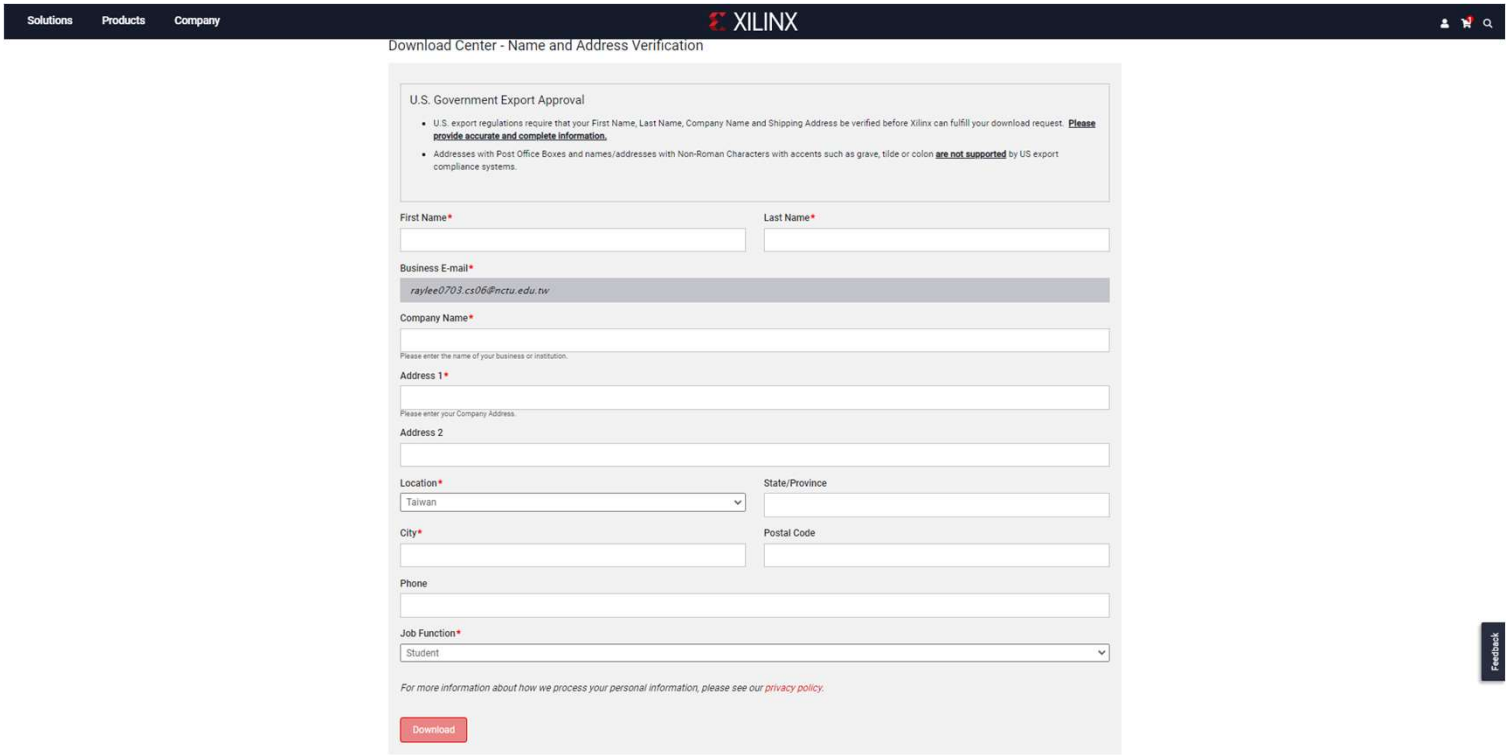
Vivado Installation Guide

Access Xilinx website to download Vivado: (https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/2020-2.html)



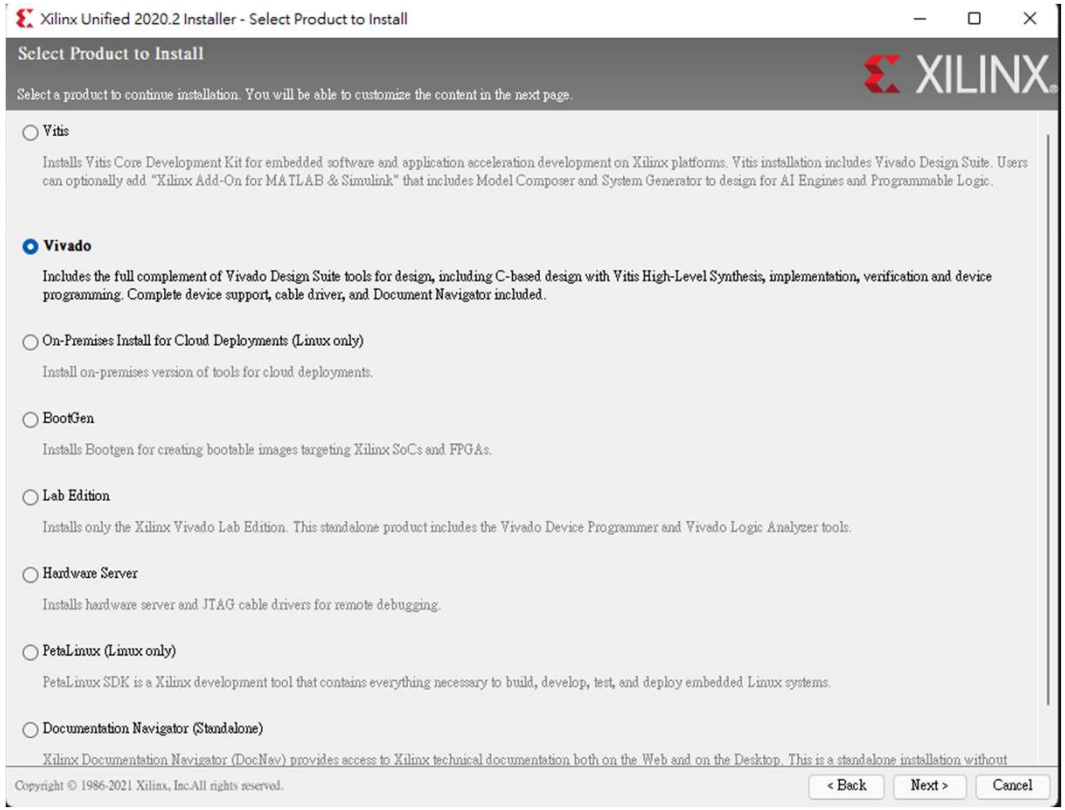
Vivado Installation Guide

- Fill in the personal information and click “Download”



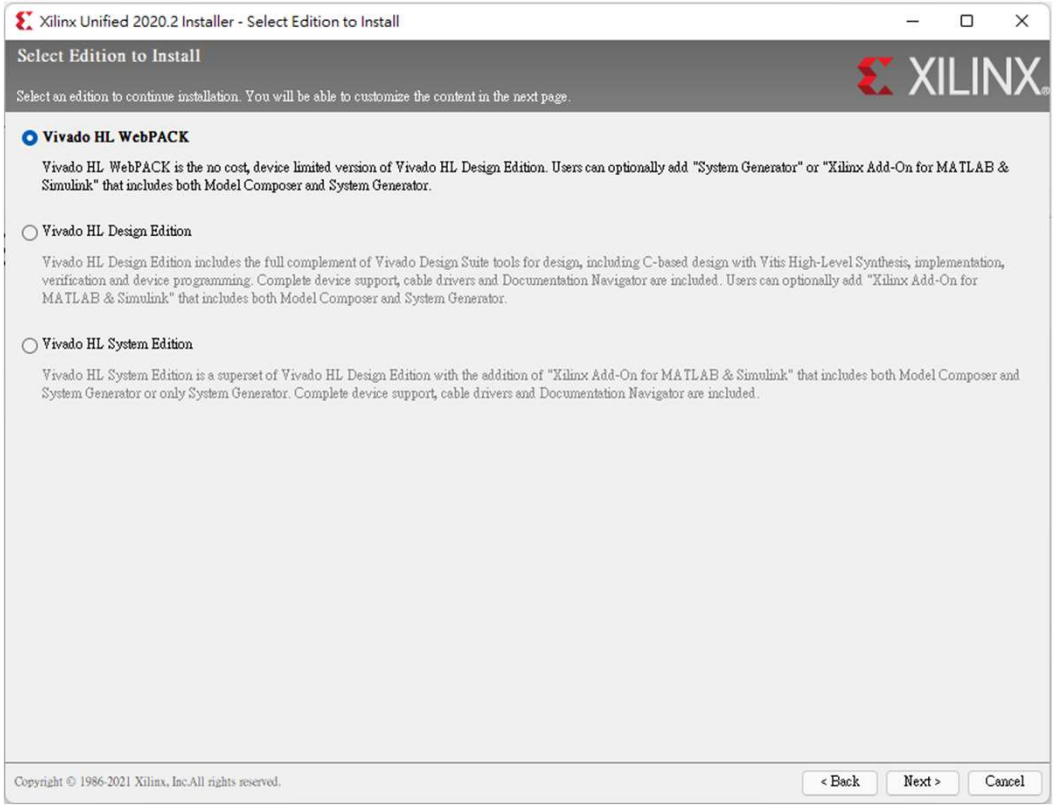
Vivado Installation Guide

- Select “Vivado”



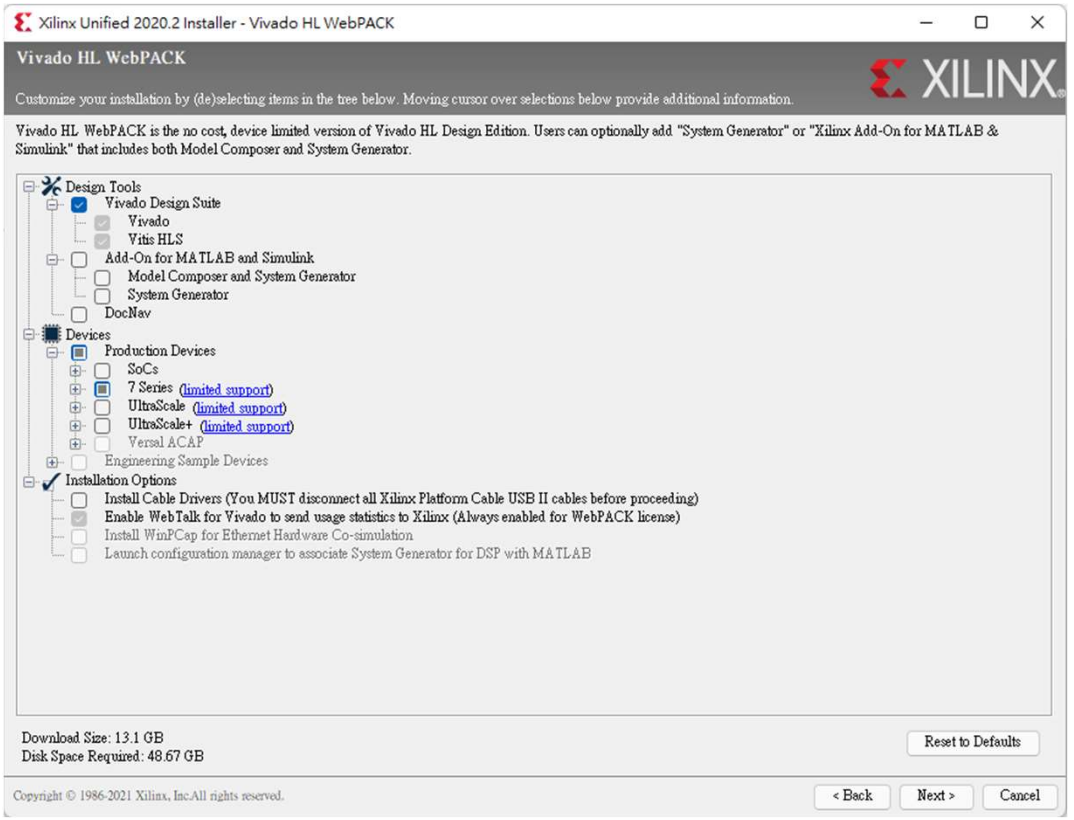
Vivado Installation Guide

- Select “Vivado HL WebPACK” for free license version

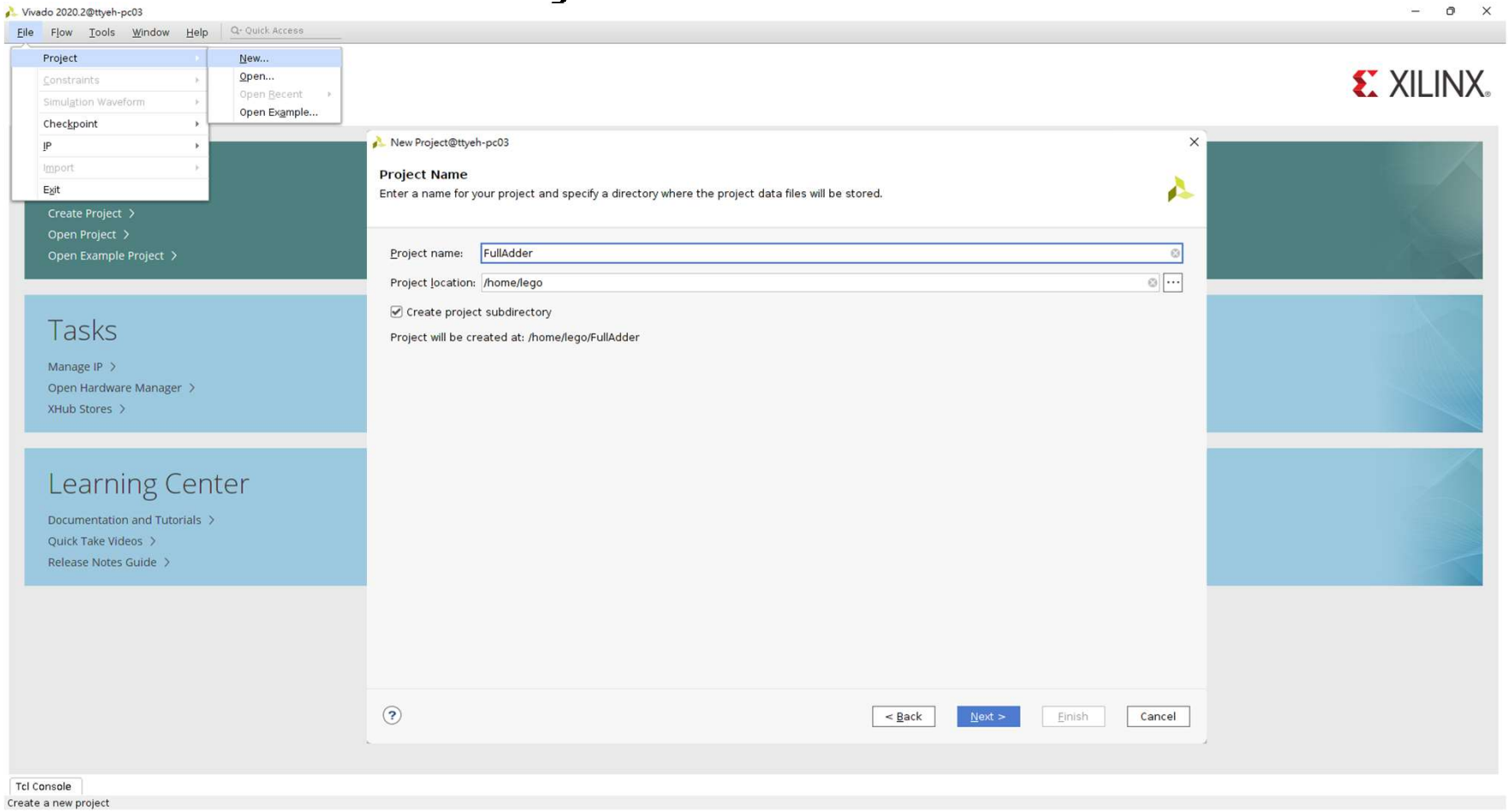


Vivado Installation Guide

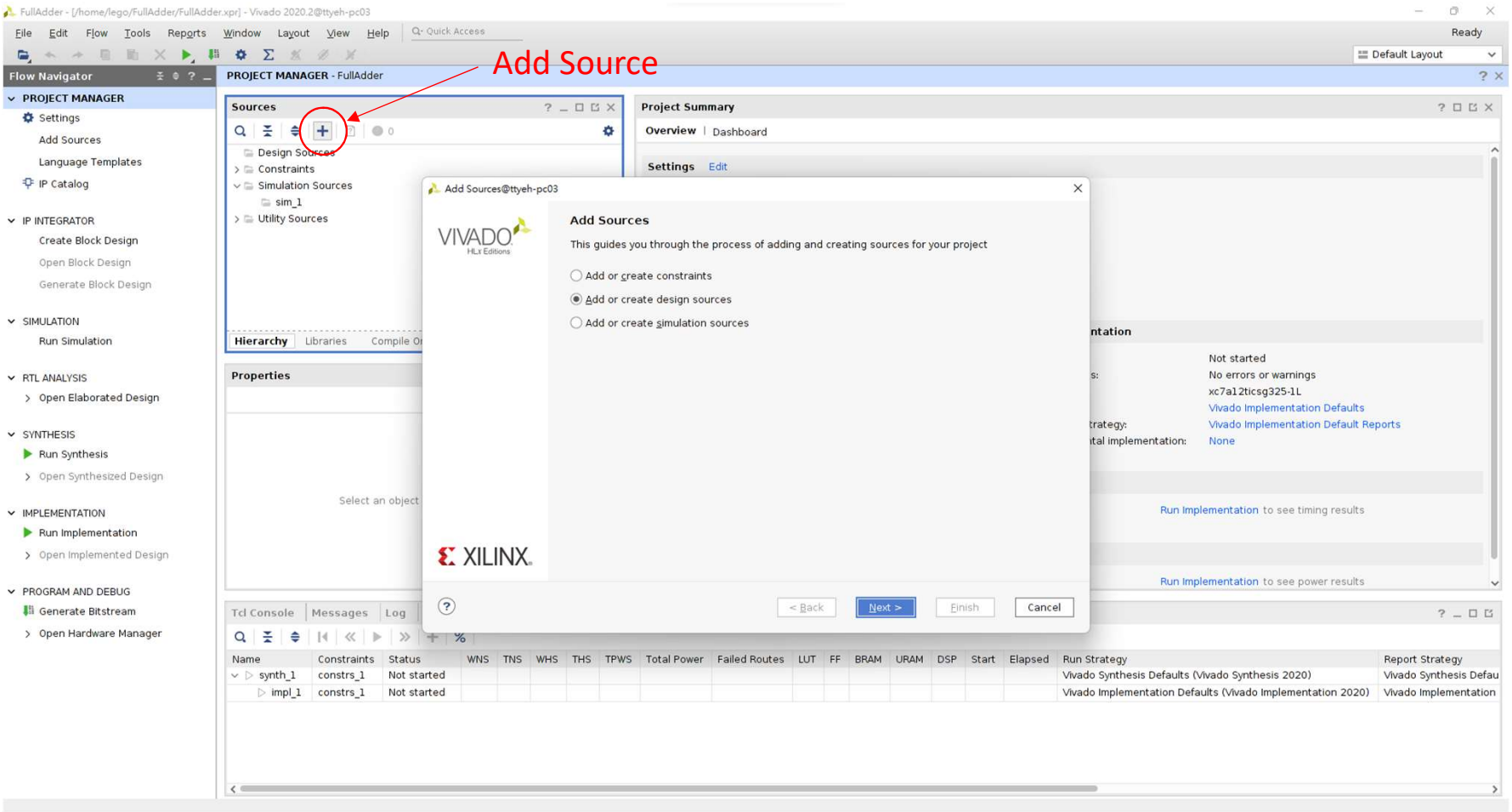
- Uncheck features we don’t need.



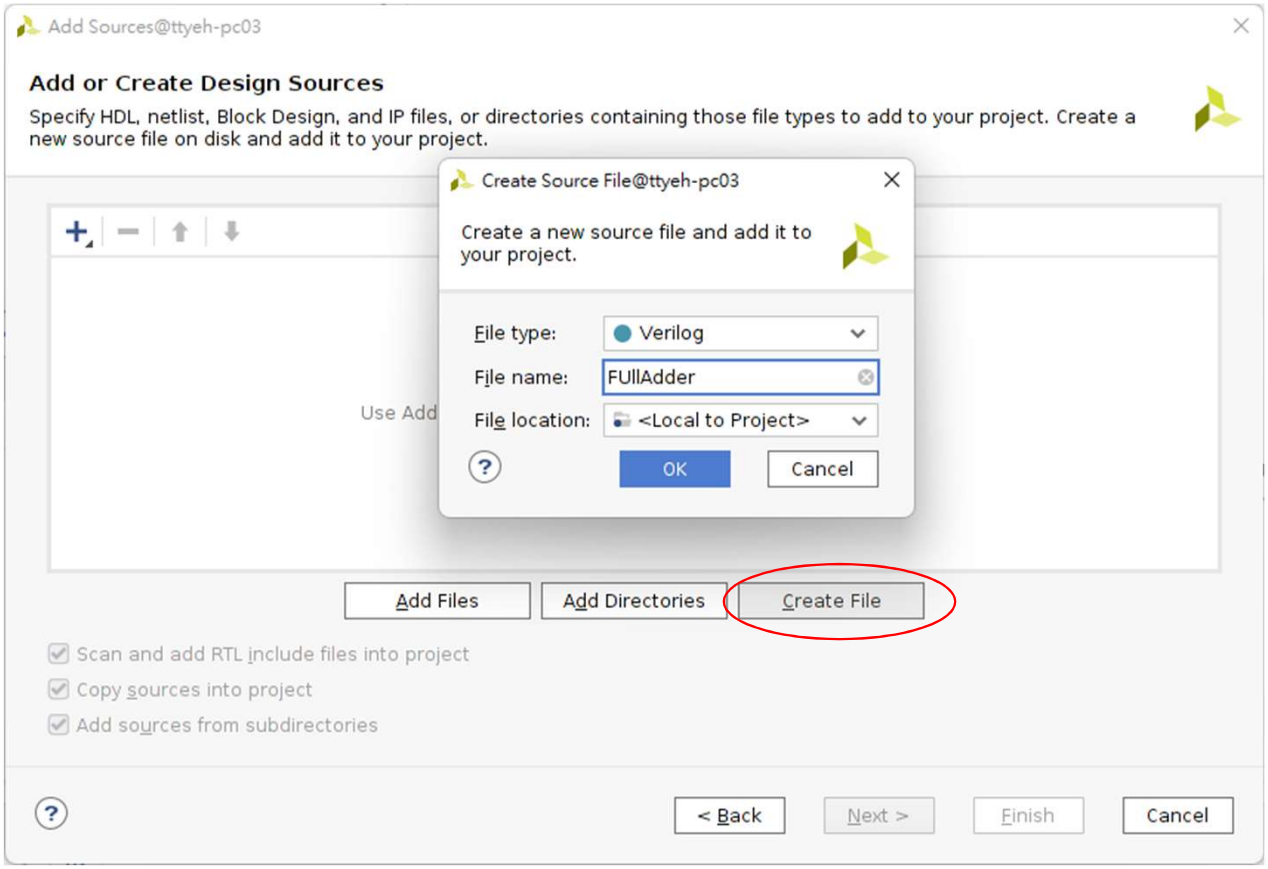
Create a New Project in Vivado



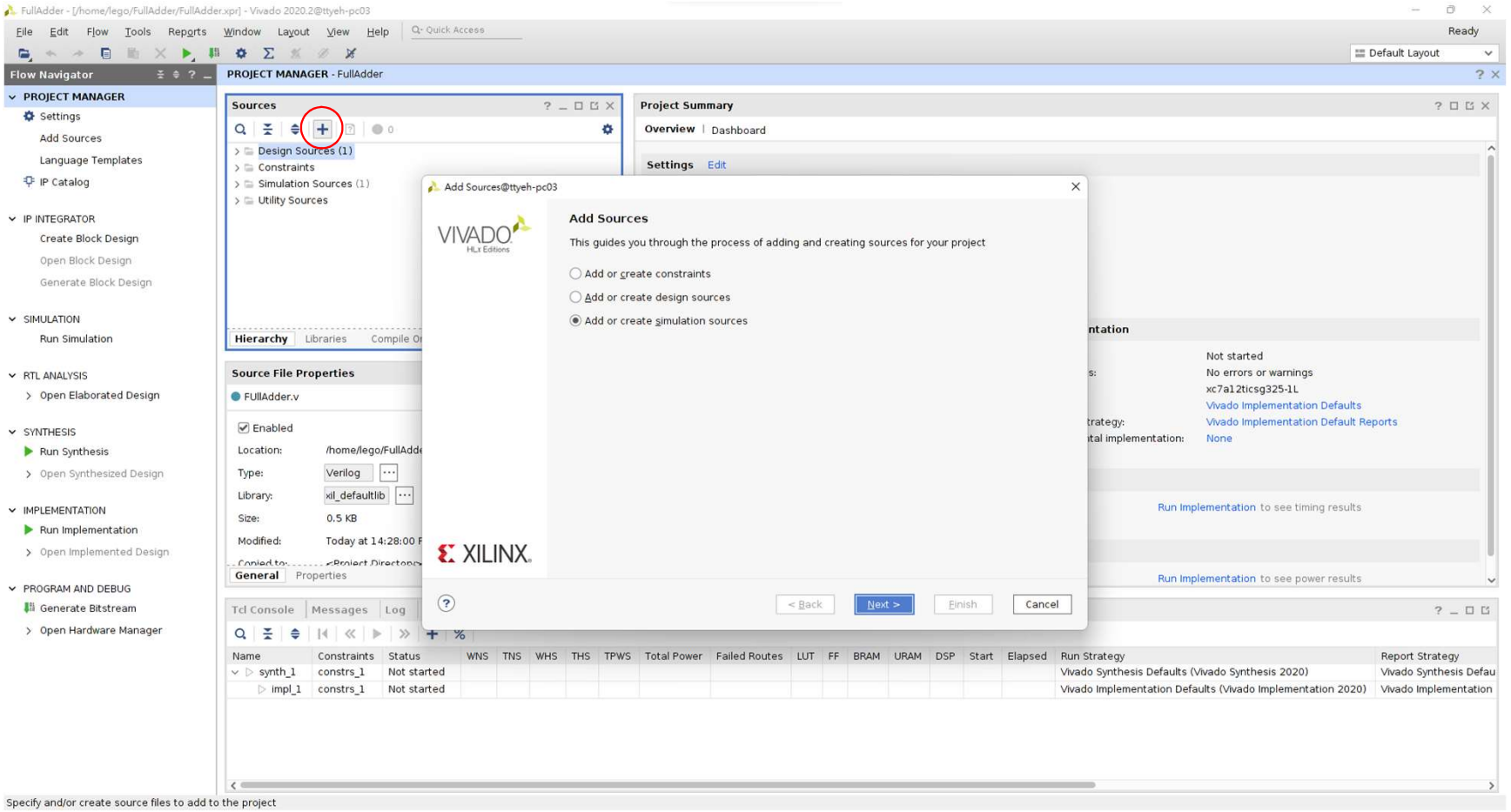
Create a Design



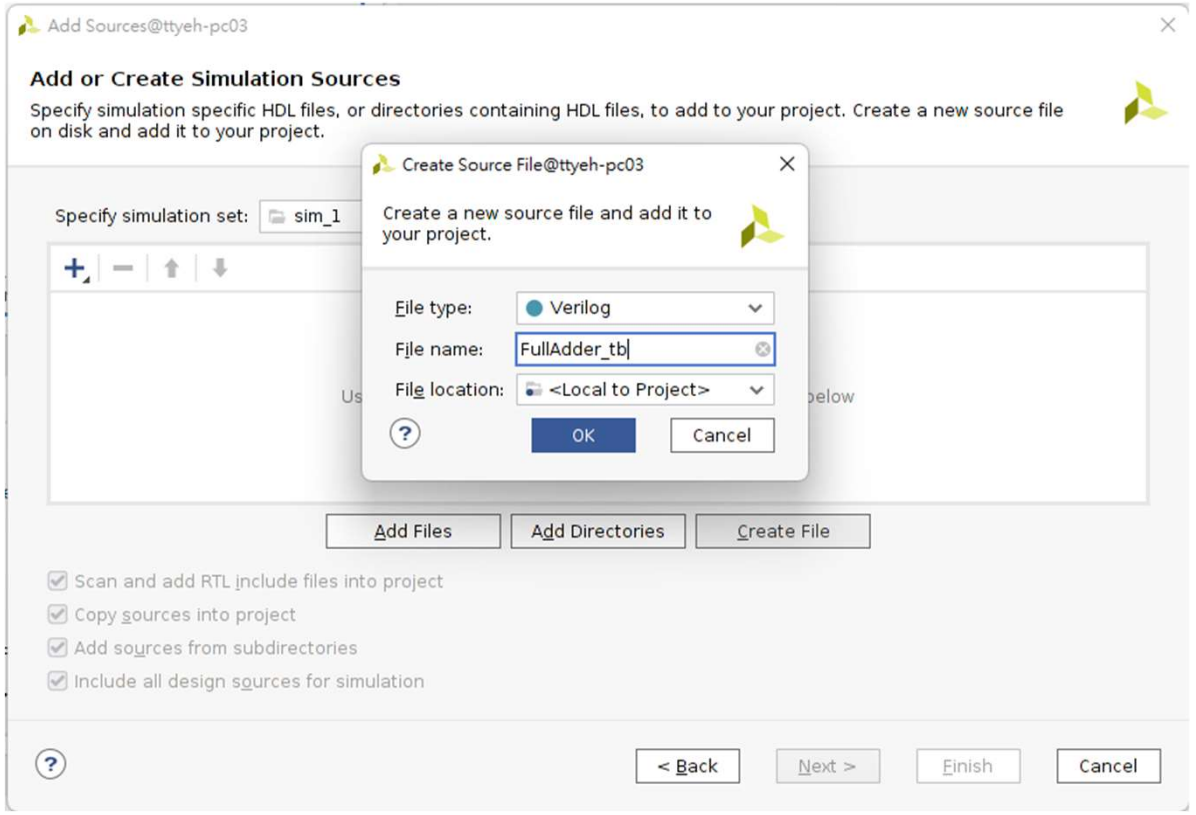
Create a Design



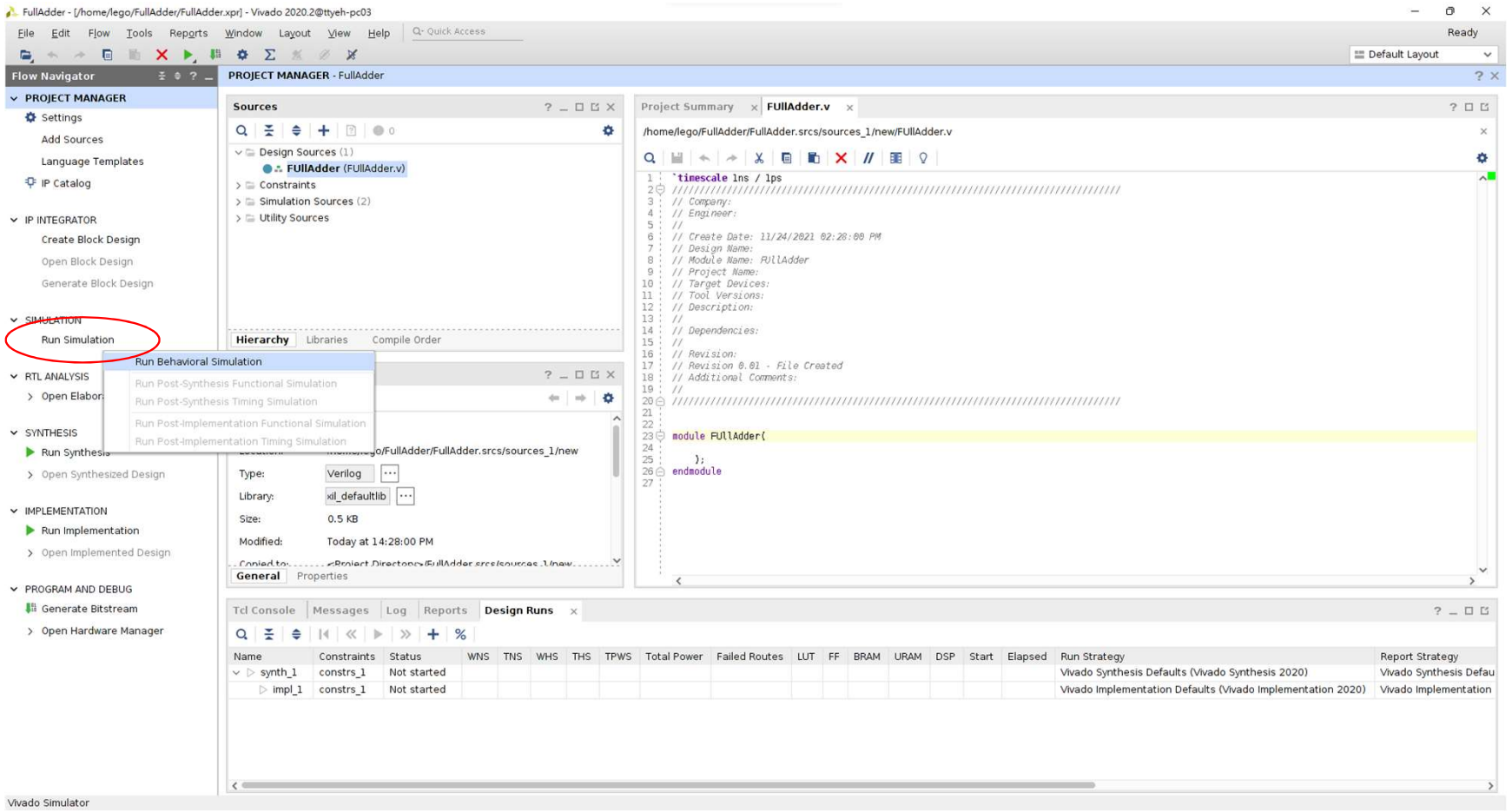
Creating Testbench Source Code



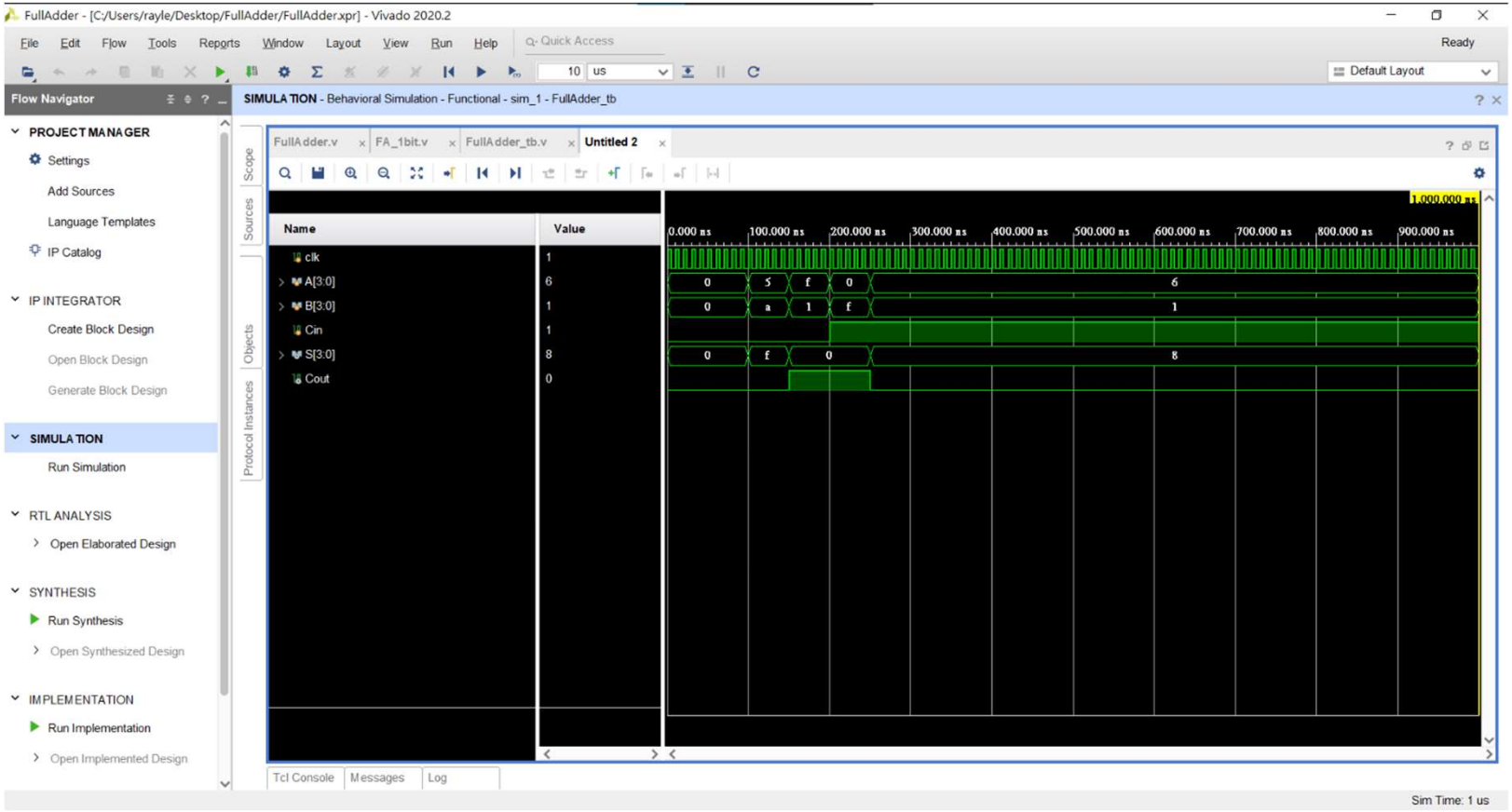
Creating Testbench Source Code



Run the Simulation

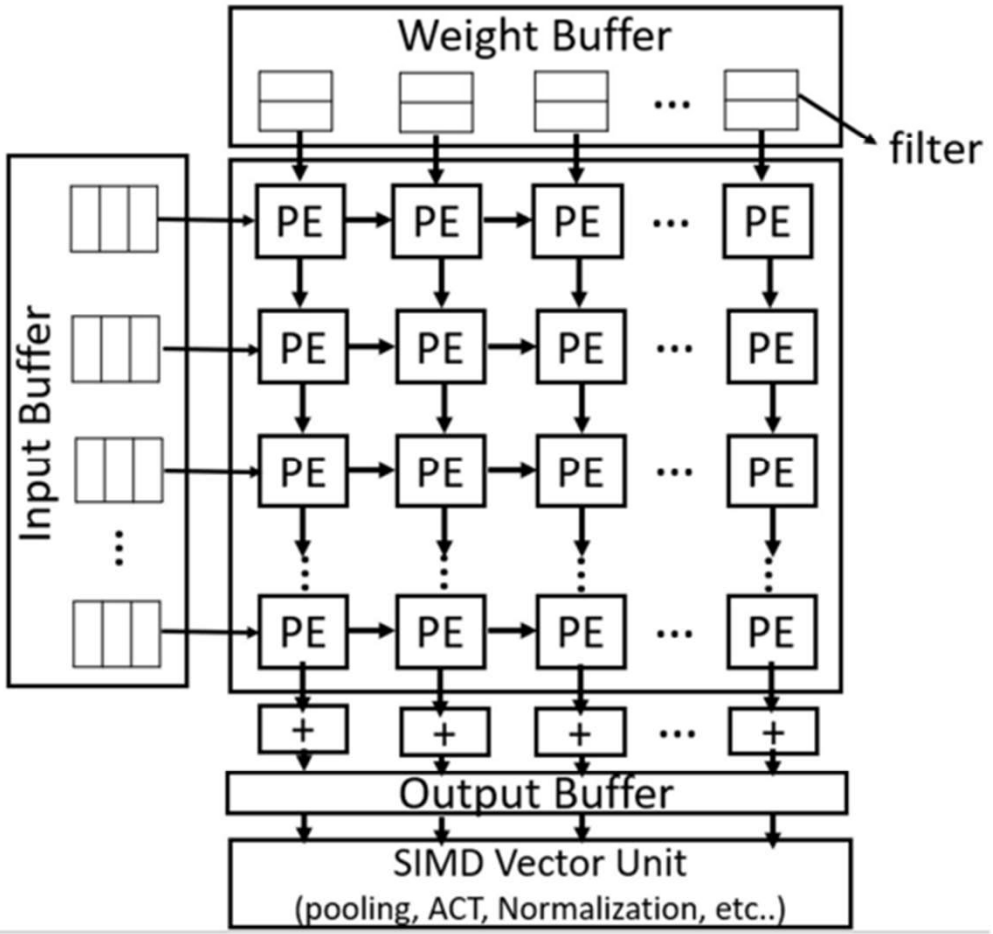


Vivado Simulator Window

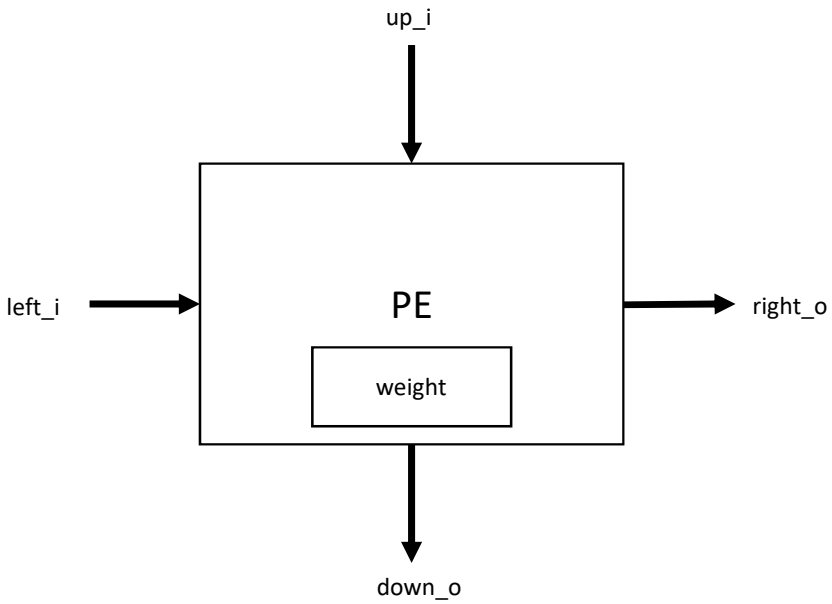


TPU Micro-architecture

- Each PE performs Multiply-and Accumulate (MAC) operation
- The unified memory buffer is decomposed into input, weight, and output buffer
- Each weight buffer stores weights of a filter
- At each cycle, inputs are pushed in the PE horizontally
- Partial sums flow vertically



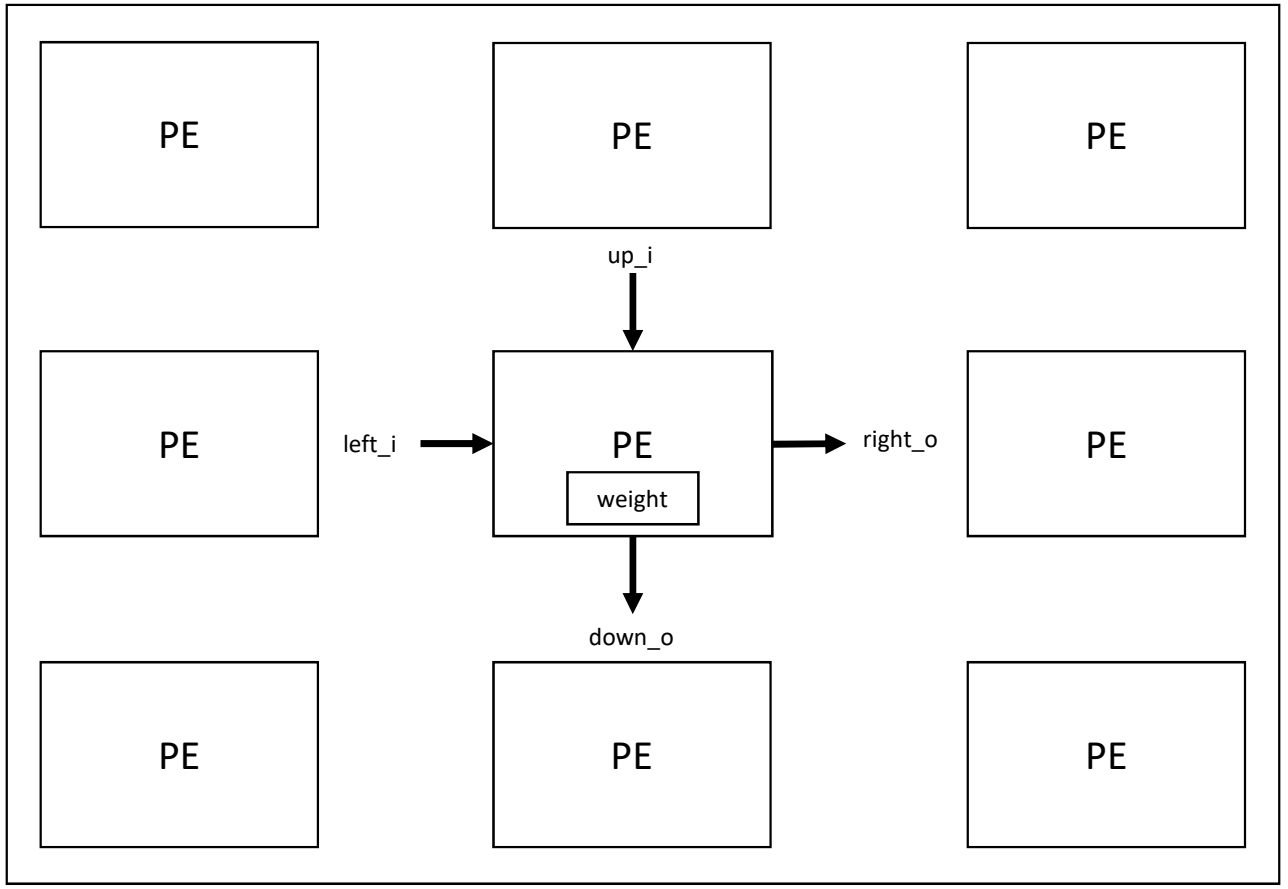
PE module



MAC:

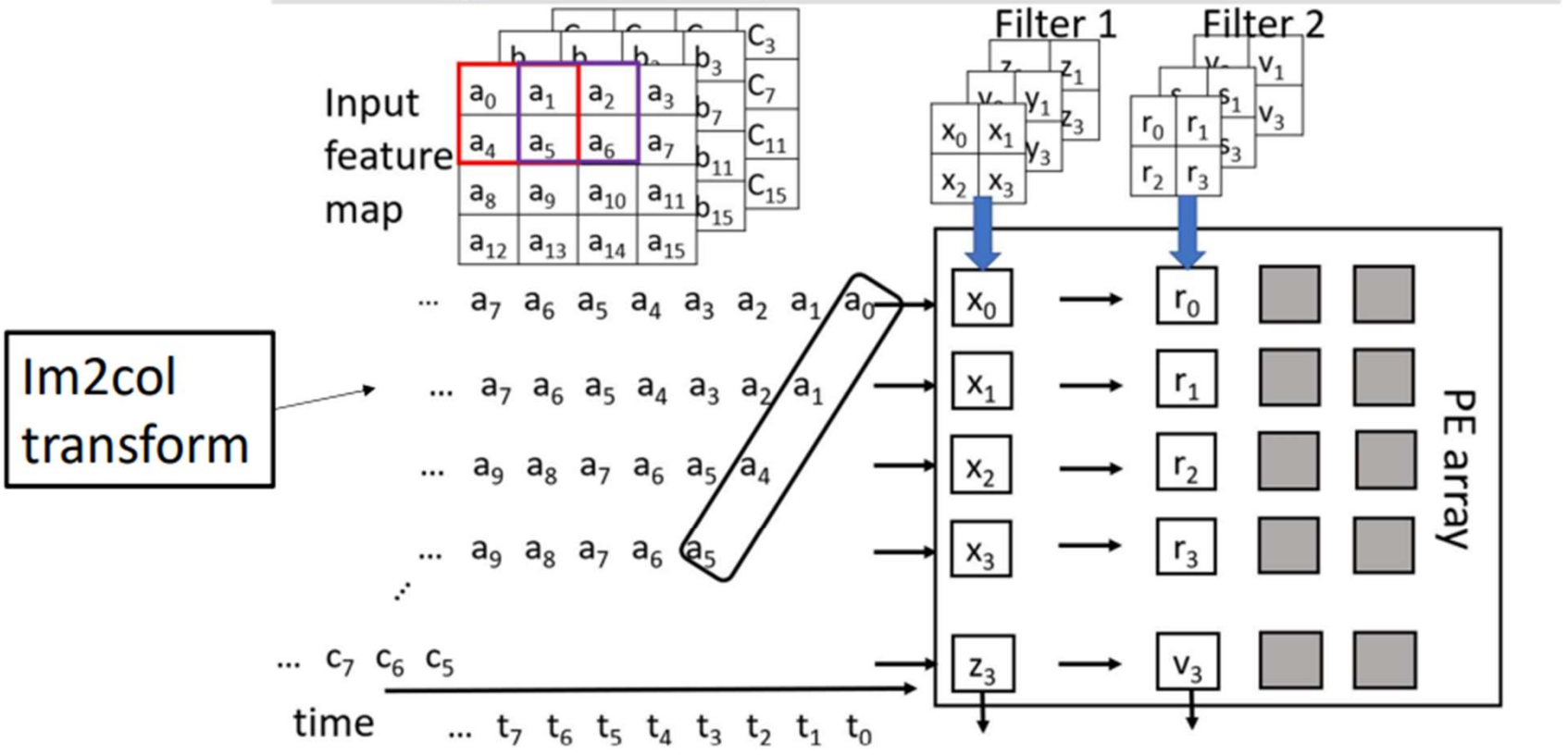
down_o = left_i * weight + up_i
right_o = left_i

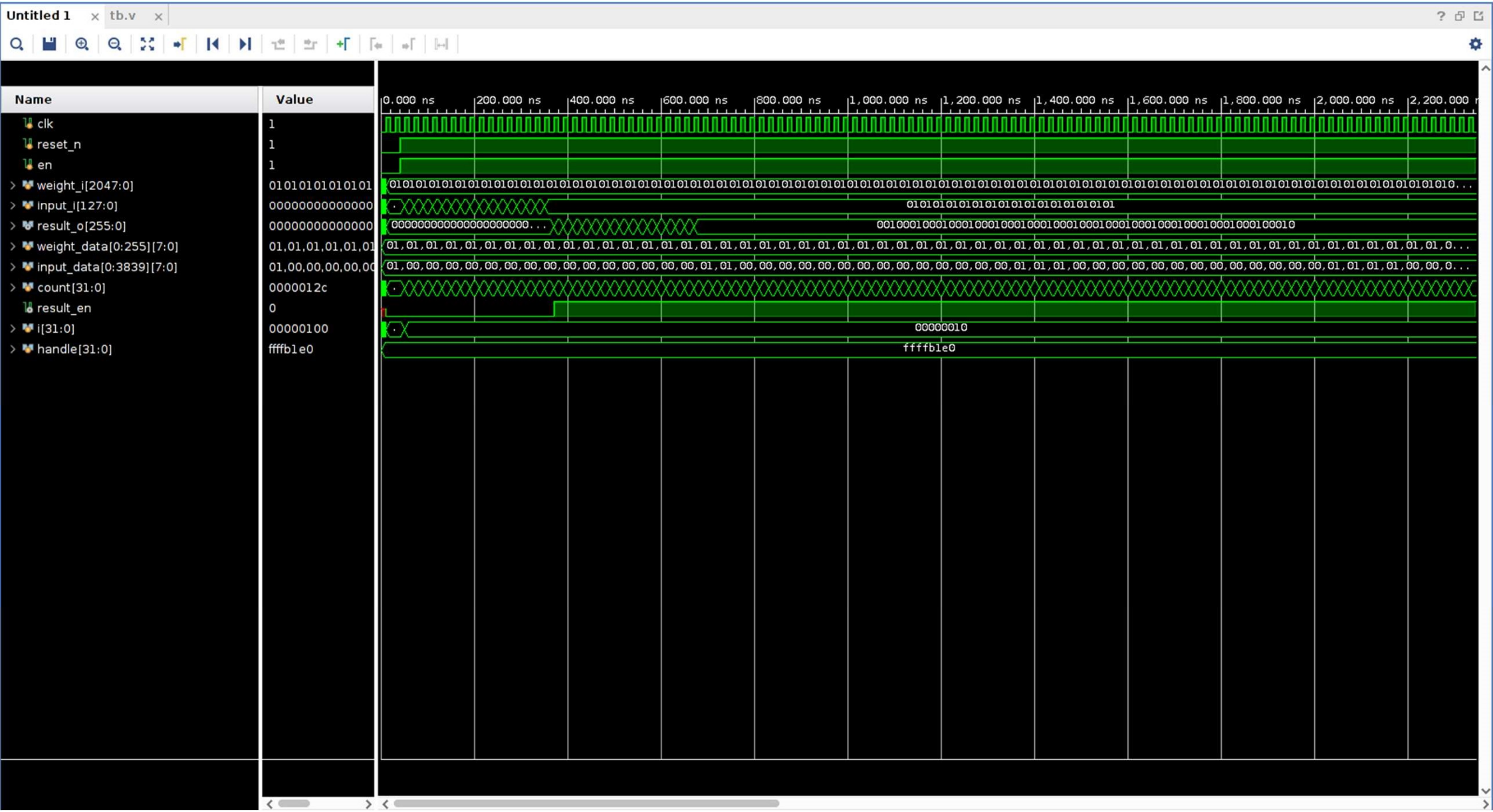
Systolic Array Module



Case Study

- The CONV weight stationary data flow




Untitled 1
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Value
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reset_n
1
en
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input_i[127:0]
00000000000000
result_o[255:0]
00000000000000
weight_data[0:255][7:0]
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input_data[0:3839][7:0]
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count[31:0]
0000012c
result_en
0
i[31:0]
00000100
handle[31:0]
ffffble0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1,200.000 ns
1,400.000 ns
1,600.000 ns
1,800.000 ns
2,000.000 ns
00000010
ffffble0