

## Computer-Aided VLSI System Design

### Homework 5 Report

**Due Tuesday, Dec. 3, 13:59**

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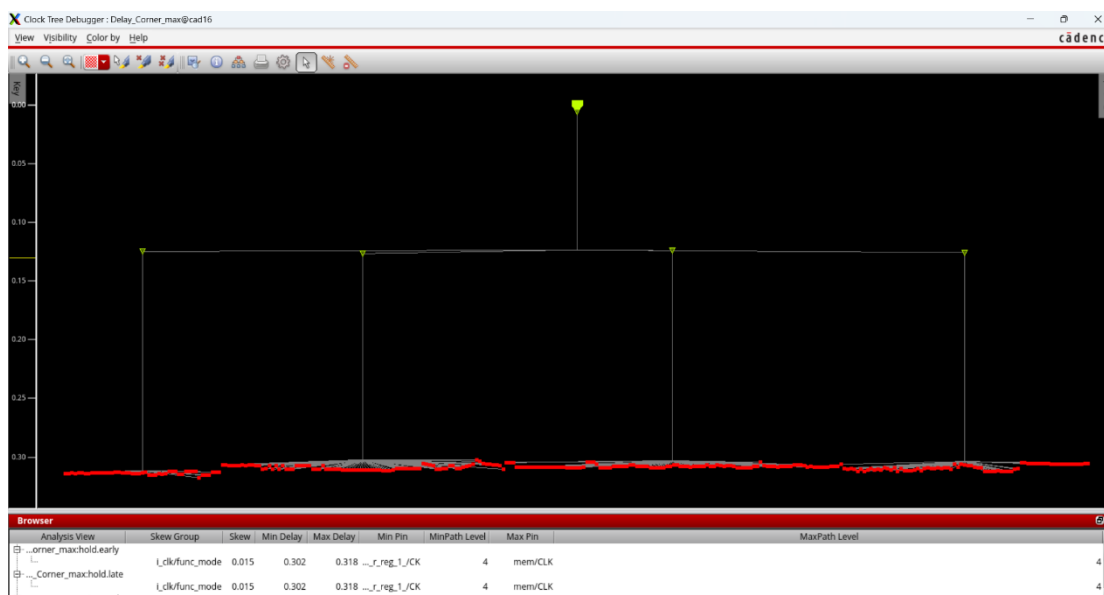
### APR Results

1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry...)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity...)	0
	Die Area ( $\mu\text{m}^2$ )	489062.43
	Core Area ( $\mu\text{m}^2$ )	290445.51
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	5.0ns
Follow your design in HW3? (If not, specify student ID of the designer or 'from TA')		from TA

## Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).



2. Attach the snapshot of DRC and LVS checking after routing. (5%)

DRC:

```

2. 140.112.20.59 (r13015 cad16)
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 176.800 176.800} 1 of 16
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {176.800 0.000 353.600 176.800} 2 of 16
VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {353.600 0.000 530.400 176.800} 3 of 16
VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {530.400 0.000 699.200 176.800} 4 of 16
VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 176.800 176.800 353.600} 5 of 16
VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {176.800 176.800 353.600 353.600} 6 of 16
VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {353.600 176.800 530.400 353.600} 7 of 16
VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {530.400 176.800 699.200 353.600} 8 of 16
VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 353.600 176.800 530.400} 9 of 16
VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {176.800 353.600 353.600 530.400} 10 of 16
VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {353.600 353.600 530.400 530.400} 11 of 16
VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {530.400 353.600 699.200 530.400} 12 of 16
VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 530.400 176.800 699.460} 13 of 16
VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {176.800 530.400 353.600 699.460} 14 of 16
VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {353.600 530.400 530.400 699.460} 15 of 16
VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {530.400 530.400 699.200 699.460} 16 of 16
VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.4 ELAPSED TIME: 1.00 MEM: 16.4M) ***
innovus 15>

```

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LVS:

```
innovus 15> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Wed Nov 27 13:12:00 2024

Design Name: core
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (699.2000, 699.4600)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 13:12:00 **** Processed 5000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Nov 27 13:12:00 2024
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.5 MEM: 11.906M)

innovus 15>
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)
- setup time:

```
2 140.112.20.59 (r13015 cad16) x +
Total number of fetched objects 4995
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 5194, 0.1 percent of the nets selected for SI analysis
End delay calculation. (MEM=1678.87 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1678.87 CPU=0:00:00.1 REAL=0:00:00.0)

-----
timeDesign Summary
-----

Setup views included:
av_func_mode_max

+-----+-----+-----+-----+-----+-----+
| Setup mode | all | reg2reg | in2reg | reg2out | in2out | default |
+-----+-----+-----+-----+-----+-----+
| WNS (ns): | 0.407 | 0.407 | 0.543 | 1.326 | N/A | 0.000 |
| TNS (ns): | 0.000 | 0.000 | 0.000 | 0.000 | N/A | 0.000 |
| Violating Paths: | 0 | 0 | 0 | 0 | N/A | 0 |
| All Paths: | 649 | 319 | 427 | 16 | N/A | 0 |
+-----+-----+-----+-----+-----+-----+

+-----+-----+-----+
| DRVs | Real | Total | |
|---|---|---|---|
| | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+

Density: 37.293%
Total number of glitch violations: 0
-----
Reported timing to dir timingReports
Total CPU time: 4.99 sec
Total Real time: 6.0 sec
Total Memory Usage: 1678.953125 Mbytes
Reset AAE Options
innovus 14>
```

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hold time:

```

2. 140.112.20.59 (r13015 cad16)
End delay calculation (fullDC). (MEM=1699.36 CPU=0:00:01.9 REAL=0:00:01.0)
Loading CTE timing window with TwFlowType 0...(CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 1699.4M)
Add other clocks and setupCteToAAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.1, REAL = 0:00:00.0, MEM = 1699.4M)
Starting SI iteration 2
AAE INFO: 1 threads acquired from CTE.
Calculate late delays in OCV mode...
Calculate early delays in OCV mode...
Start delay calculation (fullDC) (1 T). (MEM=1706.14)
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_max -- Total Number of Nets Analyzed = 17.
Total number of fetched objects 4995
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 5194, 0.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=1675.29 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1675.29 CPU=0:00:00.1 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:03.1 real=0:00:03.0 totSessionCpu=0:19:32 mem=1675.3M)

-----
timeDesign Summary
-----

Hold views included:
av_func_mode_max

+-----+-----+-----+-----+-----+-----+
| Hold mode | all | reg2reg | in2reg | reg2out | in2out | default |
+-----+-----+-----+-----+-----+-----+
| WNS (ns) | 0.746 | 0.746 | 2.498 | 3.408 | N/A | 0.000 |
| TNS (ns) | 0.000 | 0.000 | 0.000 | 0.000 | N/A | 0.000 |
| Violating Paths: | 0 | 0 | 0 | 0 | N/A | 0 |
| All Paths: | 649 | 319 | 427 | 16 | N/A | 0 |
+-----+-----+-----+-----+-----+-----+

Density: 37.293%

Reported timing to dir timingReports
Total CPU time: 4.9 sec
Total Real time: 6.0 sec
Total Memory Usage: 1636.667969 Mbytes
Reset AAE Options
innovus 14>

```

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4. Show the critical path after post-route optimization. What is the path type? (10%)  
(The slack of the critical path should match the smallest slack in the timing report)  
Path type: reg2reg

```

innovus 3> report_timing -max_path 1
#####
# Generated by: Cadence Innovus 17.11-s000_1
# OS: Linux x86_64 (Host ID cad16)
# Generated on: Thu Nov 28 20:31:46 2024
# Design: core
# Command: report_timing -max_path 1
#####
Path 1: MET Setup Check with Pin grad_angle_r_reg_0_1/QN
Endpoint: grad_angle_r_reg_0_1/Q (^) checked with leading edge of 'l_clk'
Beginpoint: Gx_r_reg_0_0/QN (^) triggered by leading edge of 'l_clk'
Path Groups: {reg2reg}
Analysis View: av_func_mode_max
Other End Arrival Time 0.302
+ Setup 0.128
+ Phase Shift 5.000
+ CPBR Adjustment 0.000
+ Required Time 5.175
+ Arrival Time 4.767
= Slack Time 0.407
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) -0.001
= Beginpoint Arrival Time -0.001

+-----+-----+-----+-----+-----+-----+
| Instance | Arc | Cell | Delay | Arrival Time | Required Time |
+-----+-----+-----+-----+-----+-----+
| Gx_r_reg_0_0 | CK ^ -> QN ^ | DFFRX1 | 0.519 | -0.001 | 0.406 |
| Gx_r_reg_0_0 | CK ^ -> Y v | NOR3BXL | 0.498 | 0.518 | 0.925 |
| FE_RC_9_0 | D ^ -> Y v | NAND4X1 | 0.161 | 1.168 | 1.576 |
| U2000 | A0 v -> Y ^ | OAI33X4 | 0.529 | 1.697 | 2.104 |
| U1967 | A ^ -> Y v | INVX3 | 0.112 | 1.809 | 2.216 |
| U1962 | A v -> Y ^ | NAND2X1 | 0.106 | 1.915 | 2.322 |
| U1964 | A ^ -> Y v | NAND2X2 | 0.079 | 1.993 | 2.400 |
| U1960 | A v -> Y ^ | CLKINXV1 | 0.126 | 2.119 | 2.526 |
| U1606 | B ^ -> Y ^ | XNOR2X2 | 0.189 | 2.308 | 2.715 |
| U1605 | A ^ -> Y ^ | OR2X4 | 0.155 | 2.462 | 2.870 |
| U3578 | A ^ -> Y v | INVX3 | 0.042 | 2.504 | 2.911 |
| U3823 | A1 v -> Y ^ | OAI21X2 | 0.159 | 2.664 | 3.071 |
| U3396 | C ^ -> Y v | XOR3X4 | 0.385 | 2.969 | 3.376 |
| add_0_root_add_0_root_add_518_3/U1_4 | B v -> C0 v | ADDPHX4 | 0.268 | 3.229 | 3.637 |
| add_0_root_add_0_root_add_518_3/U1_5 | CI v -> C0 v | ADDPHX4 | 0.188 | 3.418 | 3.825 |
| add_0_root_add_0_root_add_518_3/U1_6 | CI v -> C0 v | ADDPHX4 | 0.182 | 3.599 | 4.007 |
| add_0_root_add_0_root_add_518_3/U1_7 | CI v -> C0 v | ADDPHX4 | 0.178 | 3.778 | 4.185 |
| add_0_root_add_0_root_add_518_3/FE_RC_24_0 | A v -> Y v | XOR2X2 | 0.146 | 3.924 | 4.331 |
| U4050 | B0 v -> Y v | OAI22X4 | 0.236 | 4.160 | 4.567 |
| U4292 | B0 v -> Y v | OAI21X2 | 0.171 | 4.330 | 4.737 |
| U2979 | A v -> Y ^ | NAND2X2 | 0.123 | 4.453 | 4.860 |
| U1569 | C ^ -> Y ^ | AND3X8 | 0.155 | 4.608 | 5.016 |
| FE_RC_10_0 | A ^ -> Y v | NOR2X2 | 0.046 | 4.655 | 5.062 |
| U1440 | B0 v -> Y ^ | AOI211X2 | 0.113 | 4.767 | 5.175 |
| grad_angle_r_reg_0_1 | D ^ -> Y v | DFFRHQX2 | 0.800 | 4.767 | 5.175 |
+-----+-----+-----+-----+-----+-----+
innovus 4>

```

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5. Attach the snapshot of GDS stream out messages. (10%)

```

metal layer METAL3      16
metal layer METAL4      21
metal layer METAL5      79

Via Instances           2940

Metal Fills             0

Via Instances           0

Metal FillOPCs          0

Via Instances           0

Text                    35
metal layer METAL2      20
metal layer METAL3      15

Blockages               0

Custom Text             0

Custom Box              0

Trim Metal              0

Merging with GDS libraries
Scanning GDS file library/gds/tsmc13gfsg_fram.gds to register cell name .....
Scanning GDS file library/gds/sram_4096x8.gds to register cell name .....
Merging GDS file library/gds/tsmc13gfsg_fram.gds .....
***** Merge file: library/gds/tsmc13gfsg_fram.gds has version number: 5.
***** Merge file: library/gds/tsmc13gfsg_fram.gds has units: 1000 per micron.
***** unit scaling factor = 1 *****
Merging GDS file library/gds/sram_4096x8.gds .....
***** Merge file: library/gds/sram_4096x8.gds has version number: 5.
***** Merge file: library/gds/sram_4096x8.gds has units: 1000 per micron.
***** unit scaling factor = 1 *****
#####Streamout is finished!
innovus 17>

```

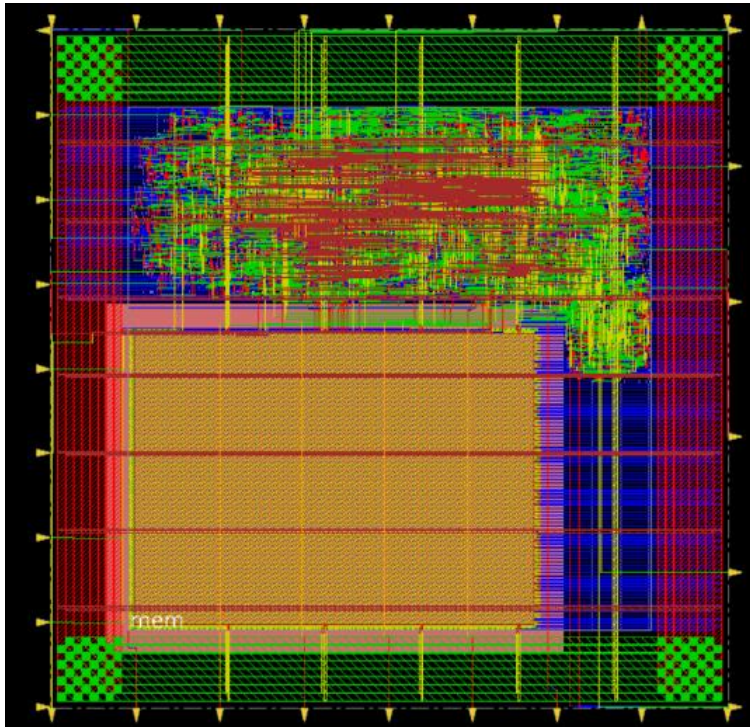
6. Attach the snapshot of the final area result. (5%)

```

innovus 20> analyzeFloorplan
**WARN: (IMPAPPU-9006): Command 'analyzeFloorplan' is obsolete. Please use commands 'placeDesign + trialRoute + create_ps_per_micron_model + timeDesign -prot
o + load_timing_debug_report -proto' to analyze congestion and timing for the floorplan.
Start to collect the design information.
Build netlist information for Cell core.
Finished collecting the design information.
Average module density = 1.000.
Density for the design = 1.000.
= stdcell area 81320 sites (138033 um^2) / alloc_area 81320 sites (138033 um^2).
Pin Density = 0.09687.
= total # of pins 16576 / total area 171112.
***** Analyze Floorplan *****
Die Area(um^2)          : 489062.43
Core Area(um^2)         : 290445.51
Chip Density (Counting Std Cells and MACROs and IOs): 53.654%
Core Density (Counting Std Cells and MACROs): 90.345%
Average utilization     : 100.000%
Number of instance(s)   : 13474
Number of Macro(s)      : 1
Number of IO Pin(s)     : 33
Number of Power Domain(s) : 0
***** Estimation Results *****
innovus 21>

```

7. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

I use Automatic Floorplan to place the SRAM. In this design, there is only one 4096x8 SRAM, and it is placed in the corner of the core for efficient power routing(close to the power ring) and minimize congestion(central core region for std cells).