Computer-Aided VLSI System Design
Homework 5 Report

Due Tuesday, Dec. 3, 13:59

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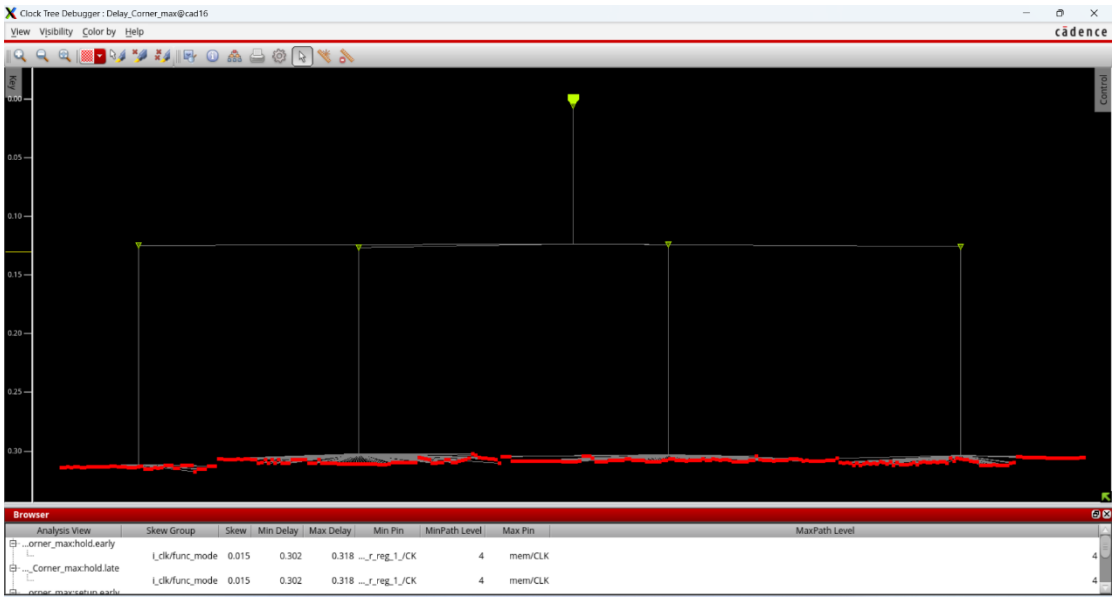
APR Results

1. Fill in the blanks below.

Design Stage	Description	Value
P&R	Number of DRC violations (ex: 0) (Verify -> Verify Geometry…)	0
	Number of LVS violations (ex: 0) (Verify -> Verify Connectivity…)	0
	Die Area (um^2)	489062.43
	Core Area (um^2)	290445.51
Post-layout Simulation	Clock Period for Post-layout Simulation (ex. 10ns)	5.0ns
Follow your design in HW3? (If not, specify student ID of the designer or 'from TA')		from TA

Questions and Discussion

1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).



2. Attach the snapshot of DRC and LVS checking after routing. (5%)

DRC:

```
2. 140.112.20.59 (r13015 cad16)
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area: {0.000 0.000 176.800 176.800} 1 of 16
  VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 0.000 353.600 176.800} 2 of 16
  VERIFY DRC ..... Sub-Area : 2 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 0.000 530.400 176.800} 3 of 16
  VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 0.000 699.200 176.800} 4 of 16
  VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 176.800 176.800 353.600} 5 of 16
  VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 176.800 353.600 353.600} 6 of 16
  VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 176.800 530.400 353.600} 7 of 16
  VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 176.800 699.200 353.600} 8 of 16
  VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 353.600 176.800 530.400} 9 of 16
  VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 353.600 353.600 530.400} 10 of 16
  VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 353.600 530.400 530.400} 11 of 16
  VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 353.600 699.200 530.400} 12 of 16
  VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {0.000 530.400 176.800 699.460} 13 of 16
  VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {176.800 530.400 353.600 699.460} 14 of 16
  VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {353.600 530.400 530.400 699.460} 15 of 16
  VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
  VERIFY DRC ..... Sub-Area: {530.400 530.400 699.200 699.460} 16 of 16
  VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.

  Verification Complete : 0 Viols.

 *** End Verify DRC (CPU: 0:00:01.4  ELAPSED TIME: 1.00  MEM: 16.4M) ***

innovus 15>
ase support MobaXterm by subscribing to the professional edition here:  https://mobaxterm.mobatek.net
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LVS:

```
innovus 15> VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Wed Nov 27 13:12:00 2024

Design Name: core
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (699.2000, 699.4600)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 13:12:00 **** Processed 5000 nets.

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Nov 27 13:12:00 2024
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.5  MEM: 11.906M)

innovus 15>
```

3. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)

setup time:

```
2. 140.112.20.59 (r13015 cad16)

Total number of fetched objects 4995
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 5194,  0.1 percent of the nets selected for SI analysis
End delay calculation. (MEM=1678.87 CPU=0:00:00.1 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1678.87 CPU=0:00:00.1 REAL=0:00:00.0)

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 av_func_mode_max

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | default |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.407  |  0.407  |  0.543  |  1.326  |   N/A   |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |    0    |
|          All Paths:|   649   |   319   |   427   |   16    |   N/A   |    0    |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 37.293%
Total number of glitch violations: 0
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 4.99 sec
Total Real time: 6.0 sec
Total Memory Usage: 1678.953125 Mbytes
Reset AAE Options
innovus 14>
se support MobaXterm by subscribing to the professional edition here:  https://mobaxterm.mobatek.net
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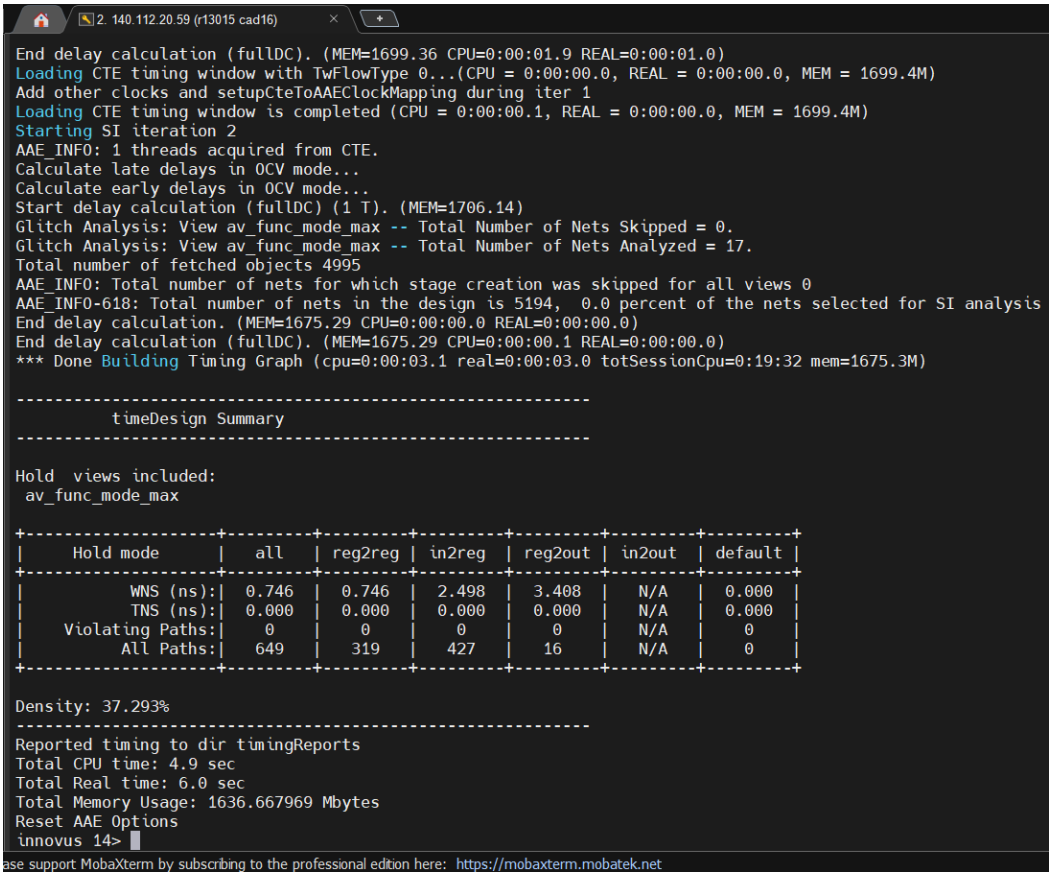
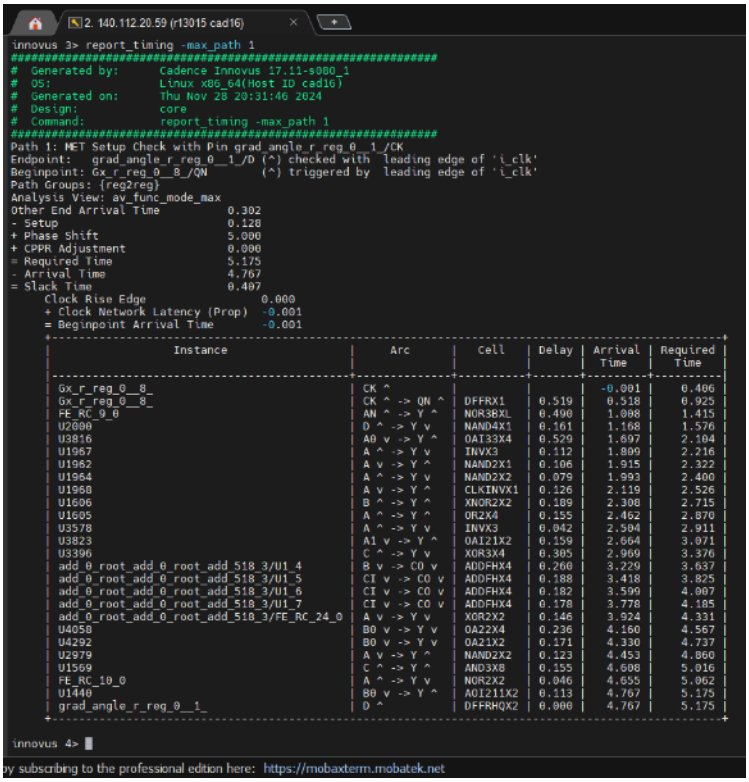
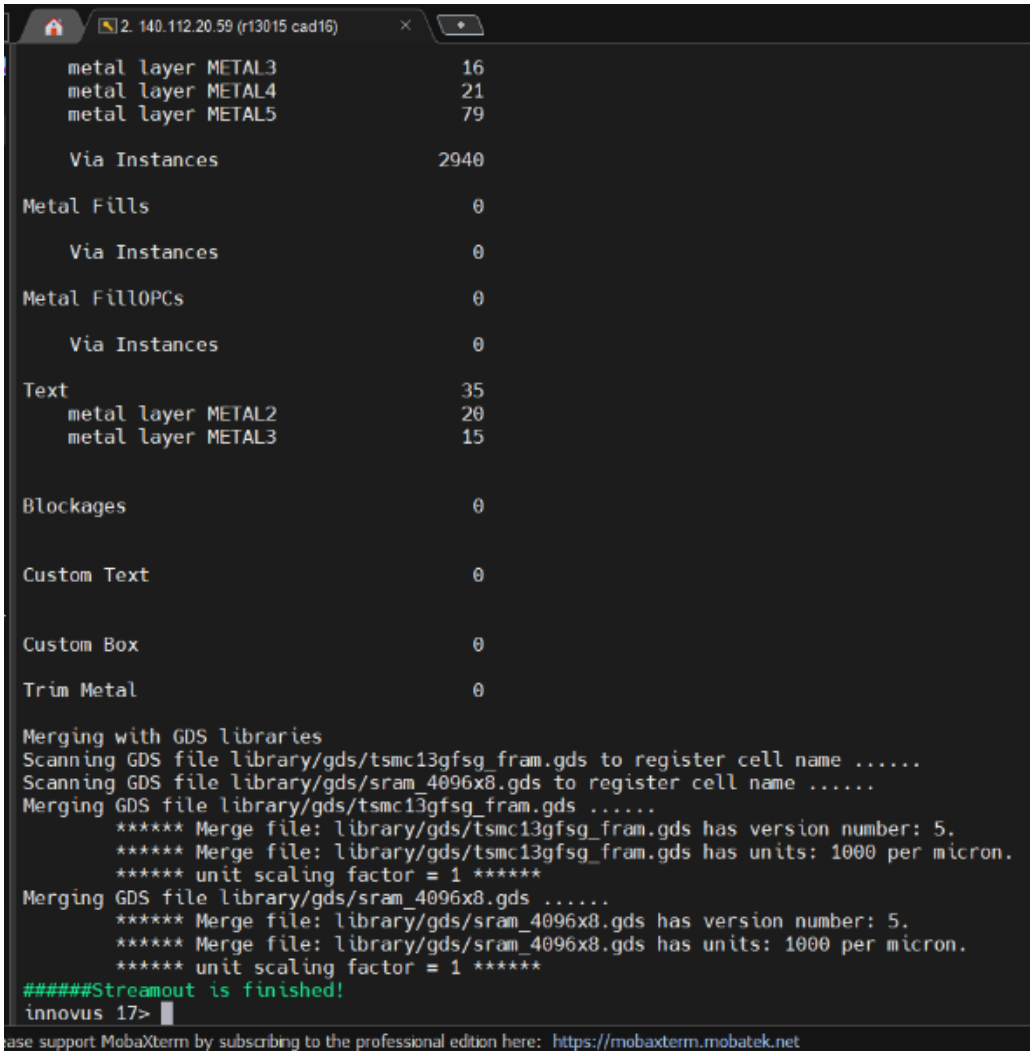
hold time:



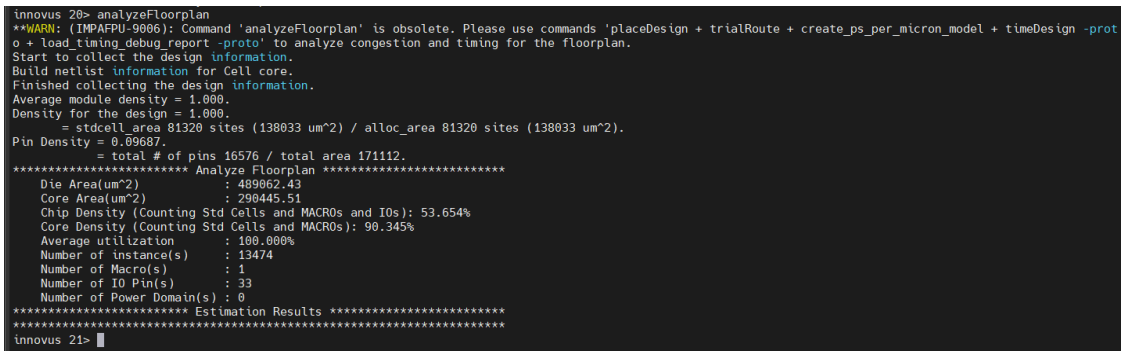
4. Show the critical path after post-route optimization. What is the path type? (10%) (The slack of the critical path should match the smallest slack in the timing report)
Path type: reg2reg



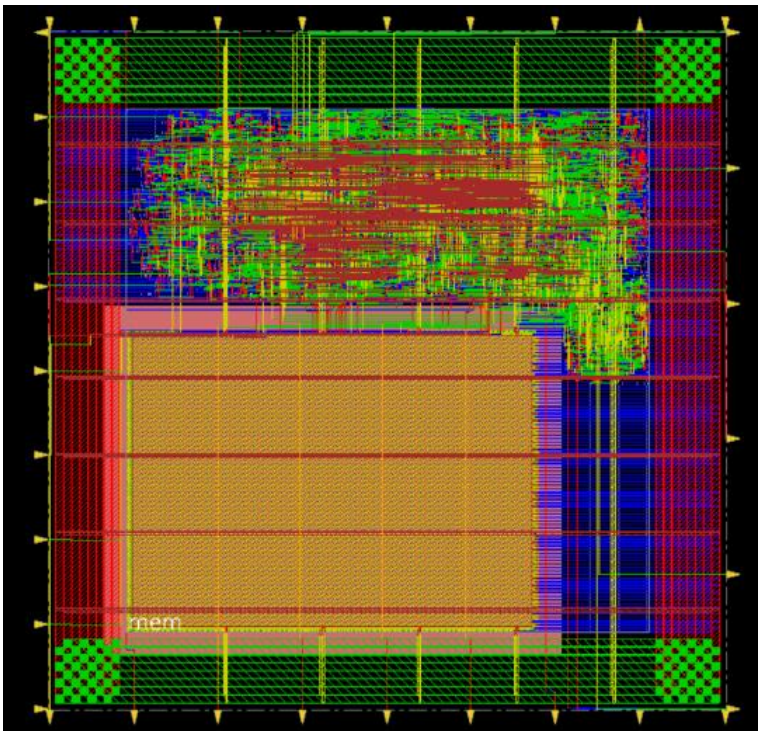
5. Attach the snapshot of GDS stream out messages. (10%)



6. Attach the snapshot of the final area result. (5%)



7. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)



8. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

   I use Automatic Floorplan to place the SRAM. In this design, there is only one 4096x8 SRAM, and it is placed in the corner of the core for efficient power routing(close to the power ring) and minimize congestion(central core region for std cells).