**Computer-Aided VLSI System Design**

**Homework 5 Report**

**Due Tuesday, Dec. 3, 13:59**

**Student ID: r13943015**

**Student Name: 張根齊**

**APR Results**

1. Fill in the blanks below.

|  |  |  |
| --- | --- | --- |
| Design Stage | Description | Value |
| P&R | Number of DRC violations (ex: 0)  (Verify -> Verify Geometry…) | 0 |
| Number of LVS violations (ex: 0)  (Verify -> Verify Connectivity…) | 0 |
| Die Area (um2) | 489062.43 |
| Core Area (um2) | 290445.51 |
| Post-layout  Simulation | Clock Period for Post-layout Simulation (ex. 10ns) | 5.0ns |
| Follow your design in HW3?  (If not, specify student ID of the designer or ‘from TA’) | | from TA |

**Questions and Discussion**

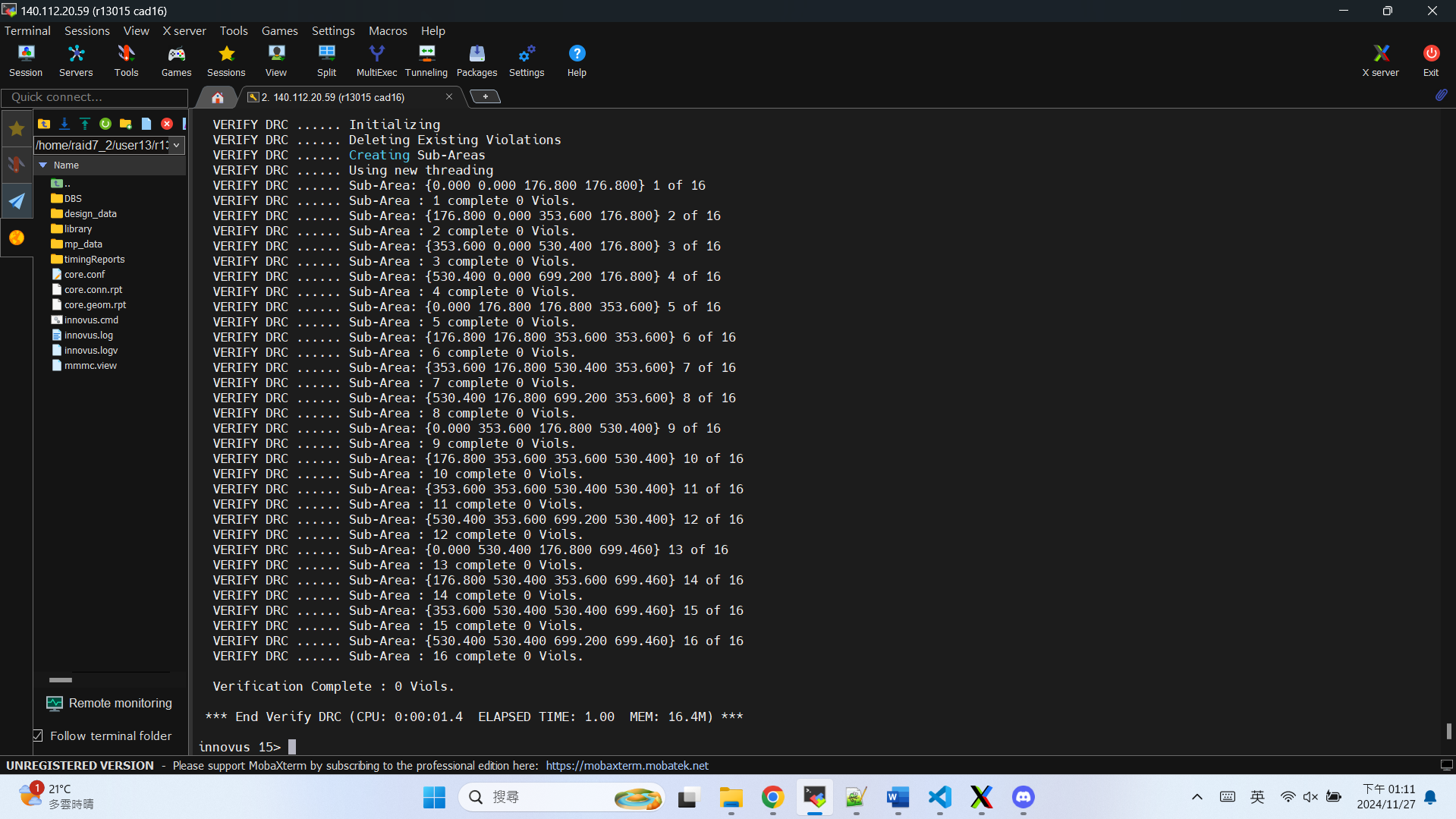
1. Attach the snapshot of CCOpt Clock Tree Debugger result (5%).

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自動產生的描述

1. Attach the snapshot of DRC and LVS checking after routing. (5%)

DRC:



LVS:

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自動產生的描述

1. Attach the snapshot of the timing report for **setup time and hold time** with no timing violation (post-route). (5%)

setup time:

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自動產生的描述

hold time:

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自動產生的描述

1. Show the critical path after post-route optimization. What is the path type? (10%)

(The slack of the critical path should match the smallest slack in the timing report)

Path type: reg2reg

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自動產生的描述

1. Attach the snapshot of GDS stream out messages. (10%)

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自動產生的描述

1. Attach the snapshot of the final area result. (5%)

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自動產生的描述

1. Attach the snapshot of your final layout **after adding core filler**. (Remember to switch to **Physical view** and make Pin Shapes visible) (10%)

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自動產生的描述

1. What is your strategy for floorplanning (especially for placing the SRAMs)? What is the reason behind it? (10%)

I use Automatic Floorplan to place the SRAM. In this design, there is only one 4096x8 SRAM, and it is placed in the corner of the core for efficient power routing(close to the power ring) and minimize congestion(central core region for std cells).