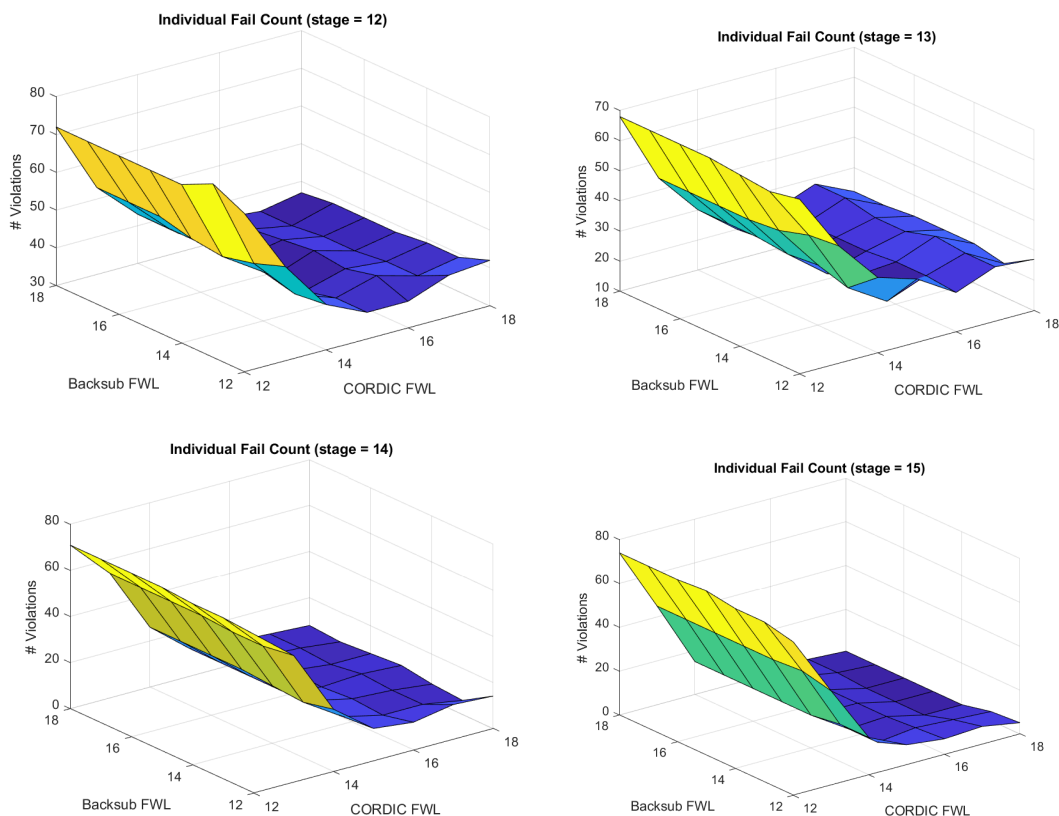# DSP in VLSI
FINAL

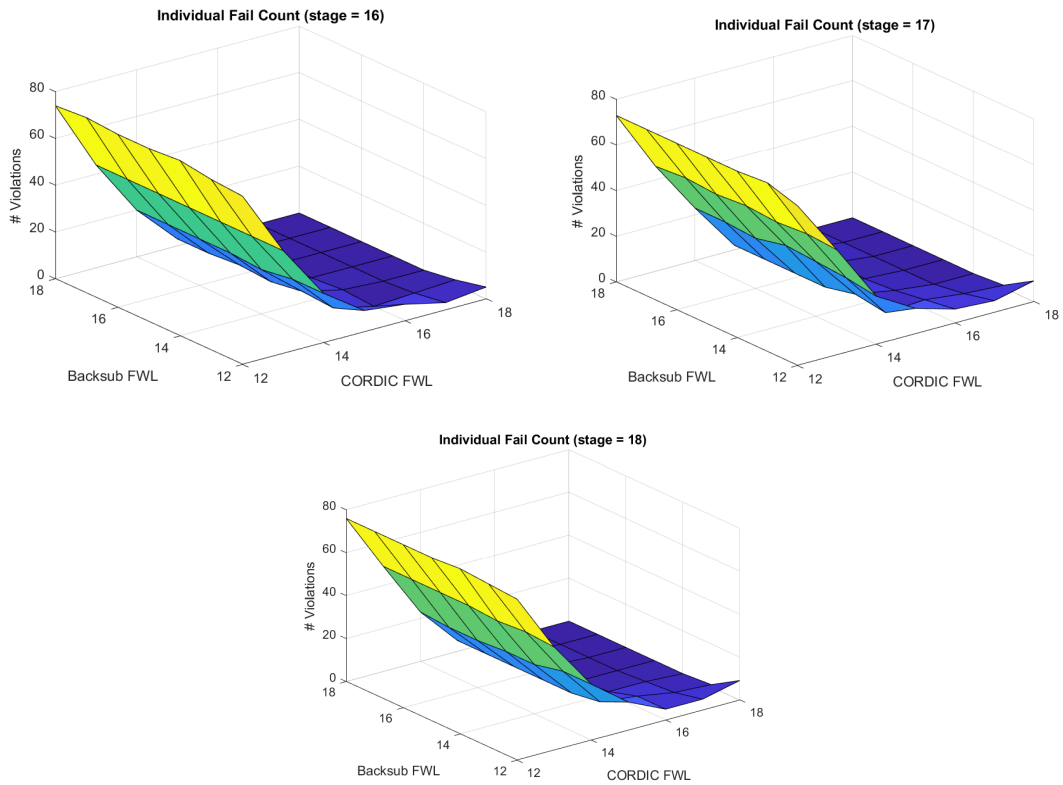電子所ICS組, R13943015, 張根齊
電子所ICS組, R12943180, 范宇清

Q1. The word-length must be set so that the root mean square error (RMSE) $\sqrt{\frac{1}{4}\sum_{i=1}^{4}(\hat{x}_i - x_i)^2} < 10^{-3}$

for your 100 sets of linear equations. Show how you decide the wordlengths of CORDIC modules, dividers, and multipliers. Draw the figure of RMSE versus wordlength.

There are a total of **3 design parameters** in our design: **stages** number of each CORDIC module, **FWL** of all **CORDIC** module, and the **FWL** for **back substitution** (including the divider, multipliers, and adders). To overall find the best design spec, we iteratively simulate patterns over each combination of design parameters and eventually get the following result. The range of 3 parameters are all from 12 to 18.

Individual Fail Count (stage = 16)

Individual Fail Count (stage = 17)

Individual Fail Count (stage = 18)

The CORDIC stages and CORDIC FWL are the key parameters which dominate the precision.

```
analysis_stage15.csv

Report > analyze_random > analysis_stage15.csv > data
  1    CORDIC_FWL, BACKSUB_FWL, RMSE_Indiv_Fail, RMSE_Total_Val        , RMSE_Total_FailFlag
 20         14,          16,            15, 0.000681966285898201,                    0
 21         14,          17,            15, 0.000681388797502839,                    0
 22         14,          18,            15, 0.000681467010730661,                    0
 23         15,          12,             9, 0.000473241740210384,                    0
 24         15,          13,             4, 0.000327966568236815,                    0
 25         15,          14,             4, 0.00033837862450638 ,                    0
 26         15,          15,             5, 0.000324927912213456,                    0
 27         15,          16,             5, 0.000323249976135281,                    0
 28         15,          17,             5, 0.0003240311151564   ,                    0
 29         15,          18,             5, 0.00032299140029015  ,                    0
```

```
analysis_stage16.csv

Report > analyze_random > analysis_stage16.csv > data
  1    CORDIC_FWL, BACKSUB_FWL, RMSE_Indiv_Fail, RMSE_Total_Val        , RMSE_Total_FailFlag
 24         15,          13,             4, 0.000350453230021682,                    0
 25         15,          14,             5, 0.000331267723853197,                    0
 26         15,          15,             3, 0.000311239530417109,                    0
 27         15,          16,             4, 0.000314274517909229,                    0
 28         15,          17,             3, 0.000313824529710361,                    0
 29         15,          18,             3, 0.000313276943889977,                    0
 30         16,          12,             7, 0.000348225479902188,                    0
 31         16,          13,             0, 0.000220344519291717,                    0
 32         16,          14,             1, 0.000198986986758106,                    0
 33         16,          15,             0, 0.000184923118508792,                    0
 34         16,          16,             0, 0.000174856157614307,                    0
 35         16,          17,             0, 0.000176343997379709,                    0
 36         16,          18,             0, 0.000175866193513629,                    0
```

Since the performance of stages of 15 / 16 and FWL = 15 can meet the requirement, we select stages = 15, CORDIC FWL = 15, and back substitution FWL = 15. (To meet the requirement of TA's pattern)

2. Draw the RMSE versus set index (1~100) to construct your bit-true model. If RMSEs of P sets are larger than 10-3, a deduction of $0.5P$ points will be applied. If more

than 6 sets cannot satisfy the criterion, the evaluation of AT product (area and processing time) is put in the last level.
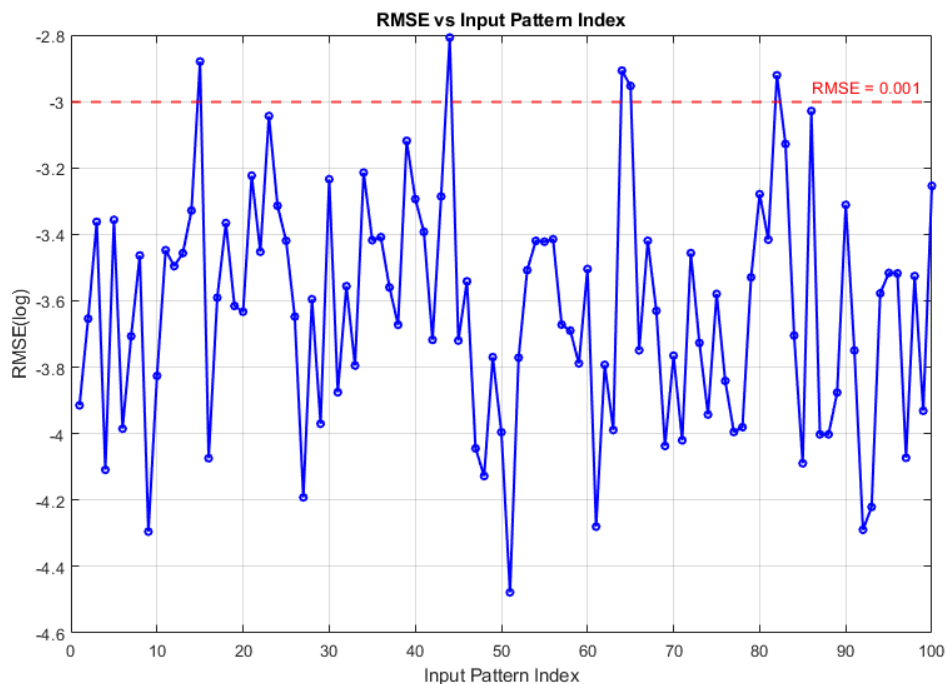

3. Explain your hardware design concept in the report. Draw the block diagram of back substitution in your design.

Instead of divider, we calculate reciprocals of diagonal elements to reduce the number of dividers. When the skew of R matrix is 1, only 1 divider is required since the diagonal elements won't overlap each other (r11 r22 r33 R11 r44 R22 R33 r11 R44).

When we utilize the pipeline technique in reciprocal module and CORDIC modules, both are critical paths. The output skew of CORDIC's output would increase and other elements in R matrix need to wait reciprocal for further computation. To solve this problem, we add extra delay lines to adjust the skew
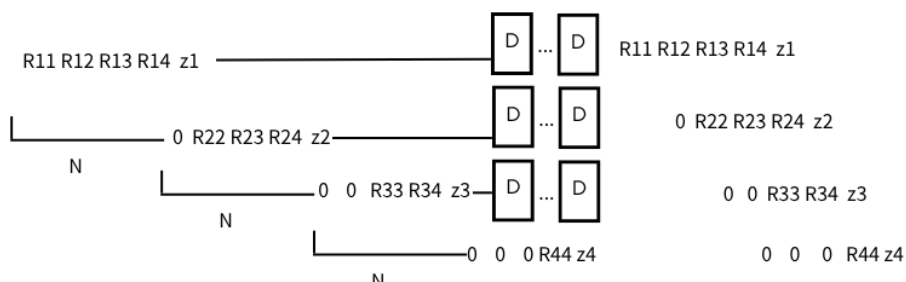
The overall diagram of back substation is shown as the following figure
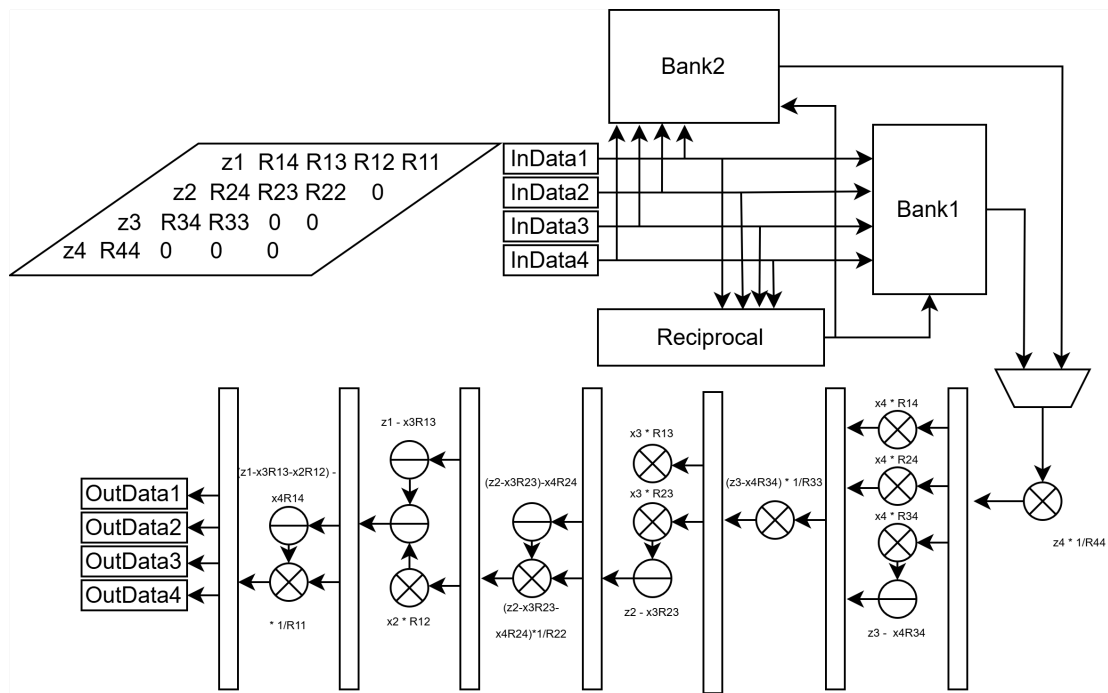
4. Please show the hardware simulation results with the input patterns provided on the NTUCool. If the number of clock cycles in the simulation is large, then cut the whole timing diagram into several segments and paste them. Also, you need to keep and show the time stamp in your simulation figure for verifying the setting of the clock period.

(a) Please provide the timing diagram of behavior simulation and calculate the RMSE of the 4 sets of solutions. If RMSEs of S sets are larger than 10-3, a deduction of S points will be applied. If more than 3 sets cannot satisfy the criterion, the evaluation of AT product (area and processing time) is put in the last level.

- Timing diagram of behavior simulation (clk period = 12ns):
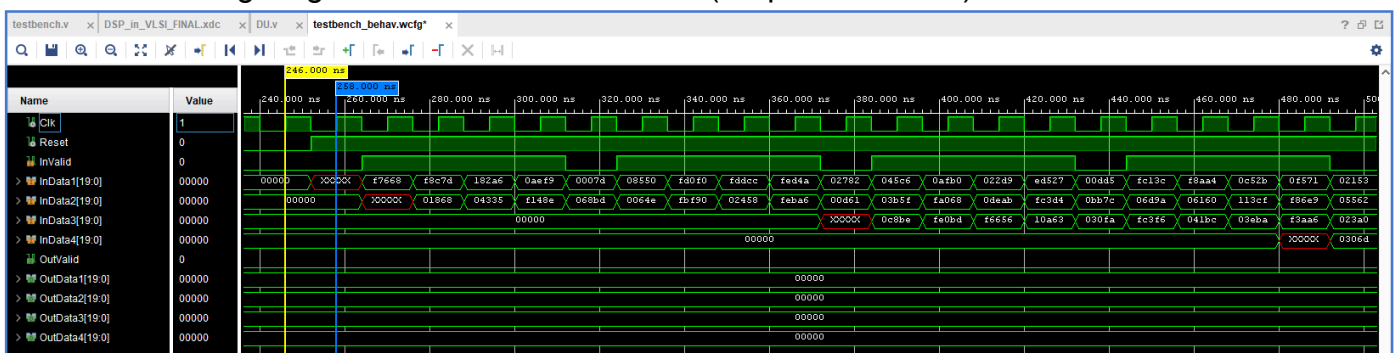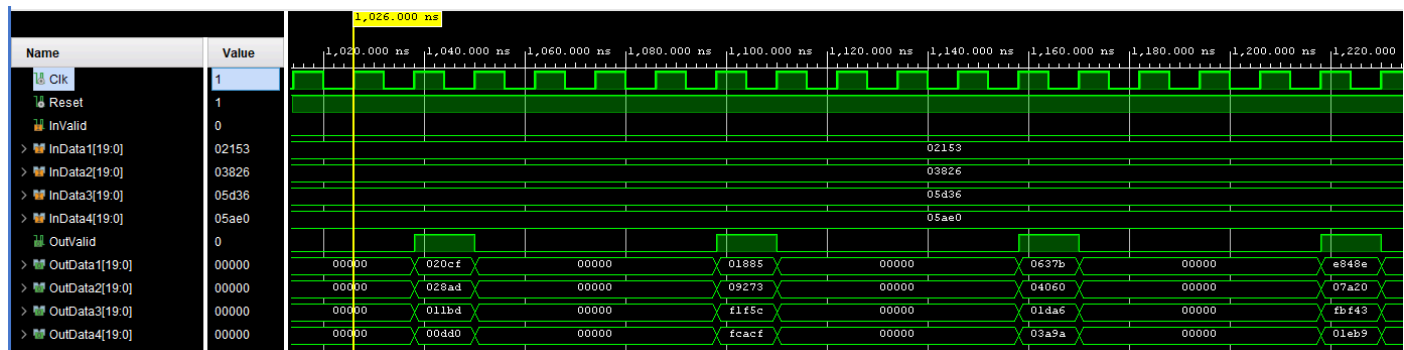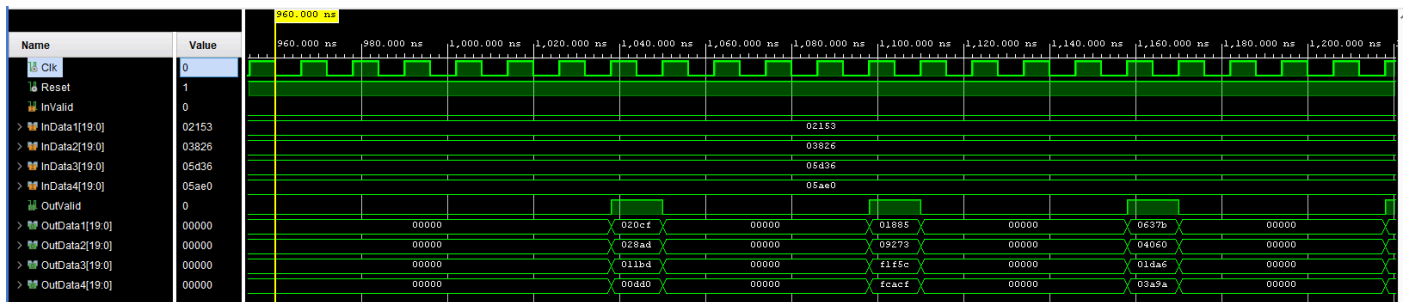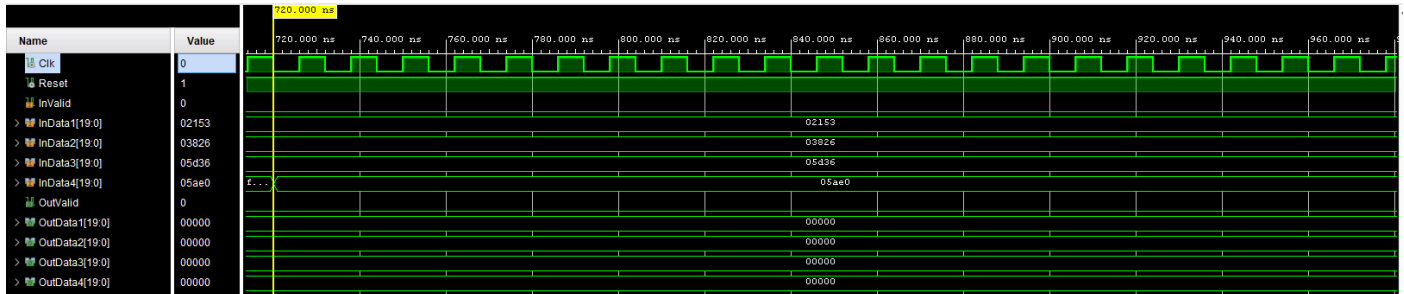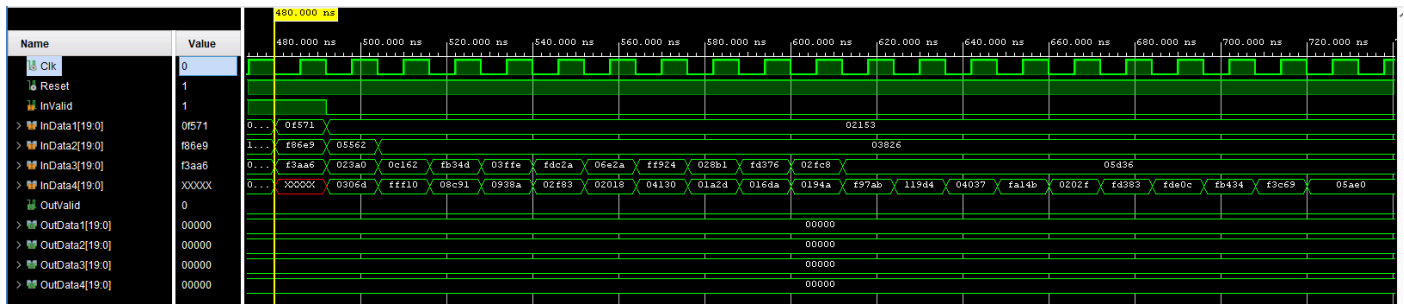
- RMSE (all < 10^-3):

```
Set 1 RMSE: 0.000066
Set 2 RMSE: 0.000300
Set 3 RMSE: 0.000146
Set 4 RMSE: 0.000975
```

(b) Please provide the timing diagram of the post-synthesis simulation. You need to indicate the clock period setting (Ts) in your post-synthesis simulation and the values of M. The processing time is calculated by MTs. Explain your latency L in your design.

- Timing diagram of the post-synthesis simulation (clk period = 12ns):
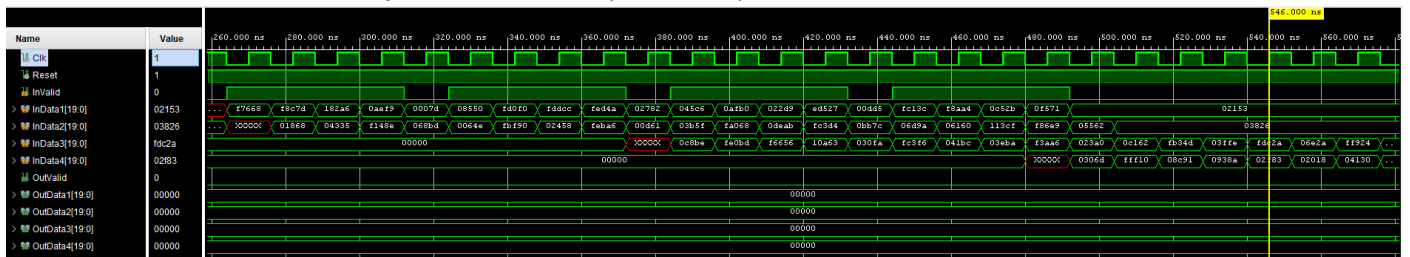
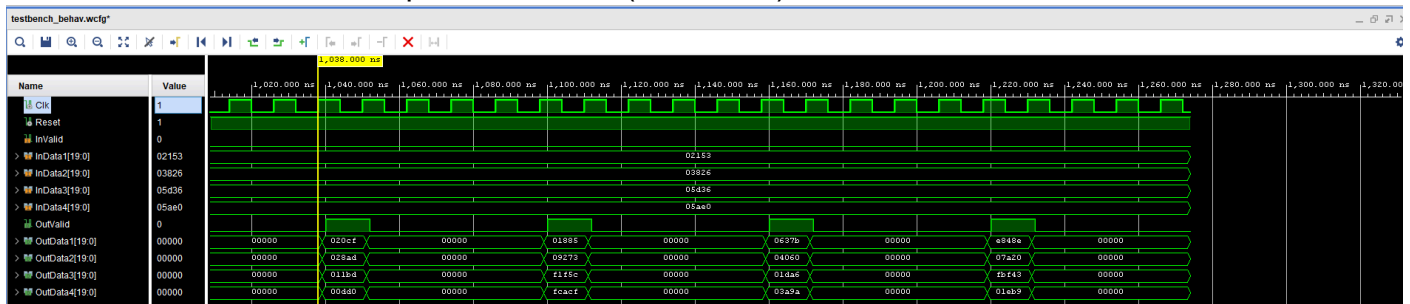- The values of M (minimal M, M = 5):
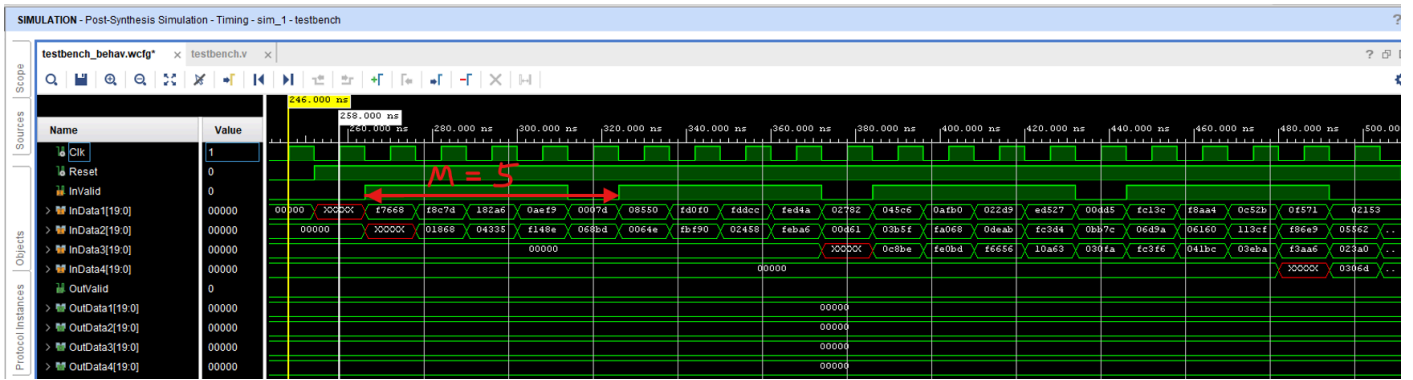
- Processing time:

$$MTs = 5 * 12\text{ns} = 60 \text{ ns}$$

- Latency L:
  - Last input of test set1 (at 546ns):

  - First output of test set1 (at 1038ns):


  - L latency:
    L = (1038ns - 546ns)/12ns = 41cycles
    1. CORDIC Systolic:
        From input to CORDIC output, the total latency is 26 cycles, including pipeline stages (blue), the input register (light blue), and the CORDIC output register (purple). Each CORDIC processing element (PE) is divided into a 9-stage pipeline. Since there are skew buffers, the total pipeline latency is 3 × 8 = 24 cycles. Additionally, there is 1 cycle for the input register and 1 cycle for the output register. Therefore, the total latency of the CORDIC systolic array is 24 + 1 + 1 = **26 cycles**.
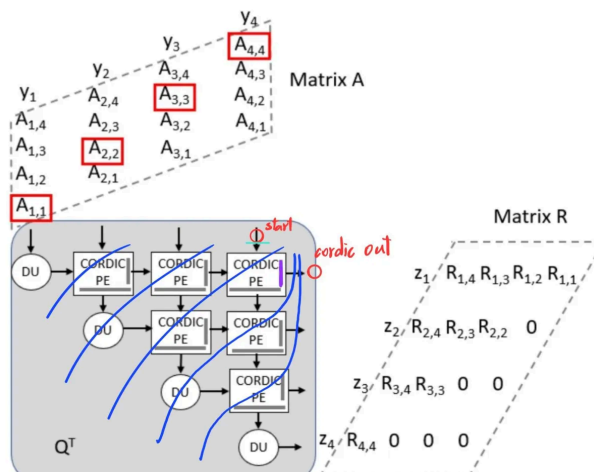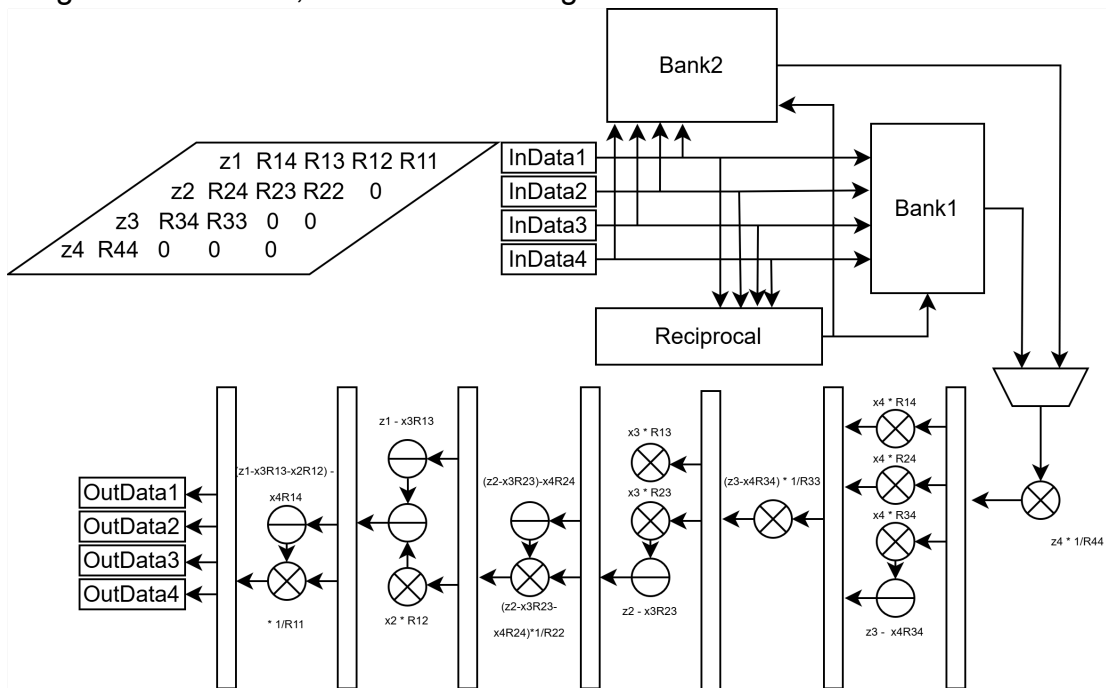
2. Back Substitution:
One register is inserted into the input of the back substitution module.
All the input would delay an extra 6+1 cycles to wait for the pipelined reciprocal module and save them to a bank of registers.
Eventually, the bank register need 7 cycles to run all multiplication and addition to generate x1 ~ x4, as shown in the figure.
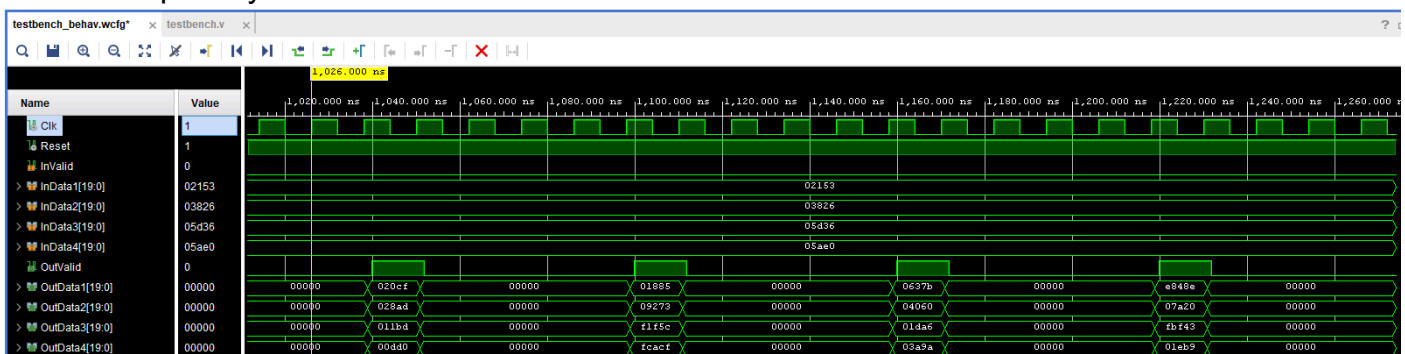

(c) Show that your post-synthesis simulation results are the same as the behavior simulation results.
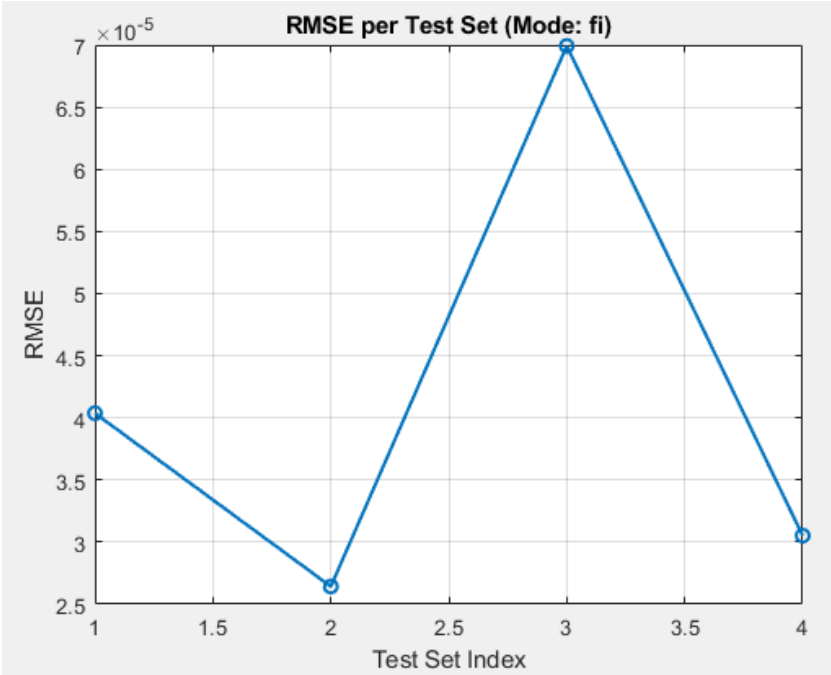- behavior simulation
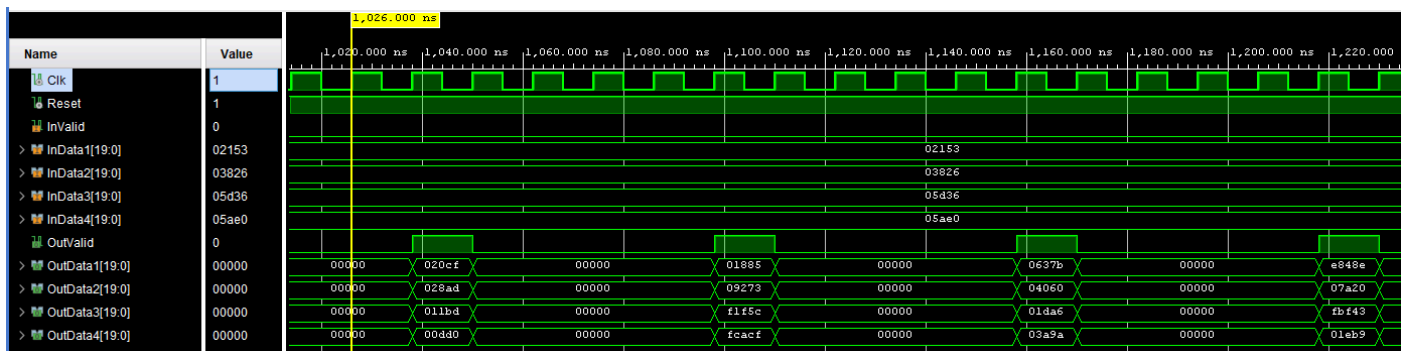
- post-synthesis simulation

5. Show that your implementation is consistent with your fixed-point

simulation by drawing the figure indicating the errors of the results using linear equations on NTUCool.

6. Show your synthesis report. If you use VIVADO, please use the following equation to combine all the resource consumptions into one metric [1]:

$$NA = LUTs + DSPs \times 280 + FFs$$

If you use ADFP, please simply show the total area after synthesis.

We use VIVADO. Our resource metric = 10434 + 10 * 280 + 4443 = **17677**

Resource	Estimation	Available	Utilization %
LUT	10434	134600	7.75
LUTRAM	318	46200	0.69
FF	4443	269200	1.65
DSP	10	740	1.35
IO	164	400	41.00
BUFG	1	32	3.13

7. Now calculate your AT product by Area (or NA) × processing time (MTs). We will classify the AT product into 3 levels and evaluate the implementation results of your AT product (Note: 15% of the score is decided by the level of the AT product. The remaining 85% is decided by the

simulations, functionality, descriptions, and timing diagram….)

$$NA * MTs = 17677 * 60 = \mathbf{1060620}$$

8. Highlight any of your design innovations. List the working items and weightings of two members.

- **design innovations**

In the CORDIC systolic array, during the initial vectoring mode, we record the rotation mode (μ_i = 1, 0, -1) of each CORDIC stage to form a rotation sequence. This sequence is then used in the subsequent rotation mode operations to determine the corresponding rotations, eliminating the need to explicitly compute the vectoring mode angle θ. Additionally, we applied pipelining to the CORDIC systolic array. The unpipelined version has a maximum path delay of 83 ns. After dividing it into a 9-stage pipeline, the maximum path delay is reduced to 10.7 ns.

One of the key innovations in back substitution is the use of the reciprocal module. If we use the divider, we cannot pipeline the divider while also meeting the highest throughput. Since the division of x1 would need to wait for the division of x2 and so on. Furthermore, to guarantee the highest throughput and minimum cycle time, we pipeline the computation chain so that no critical path exceed 12 ns

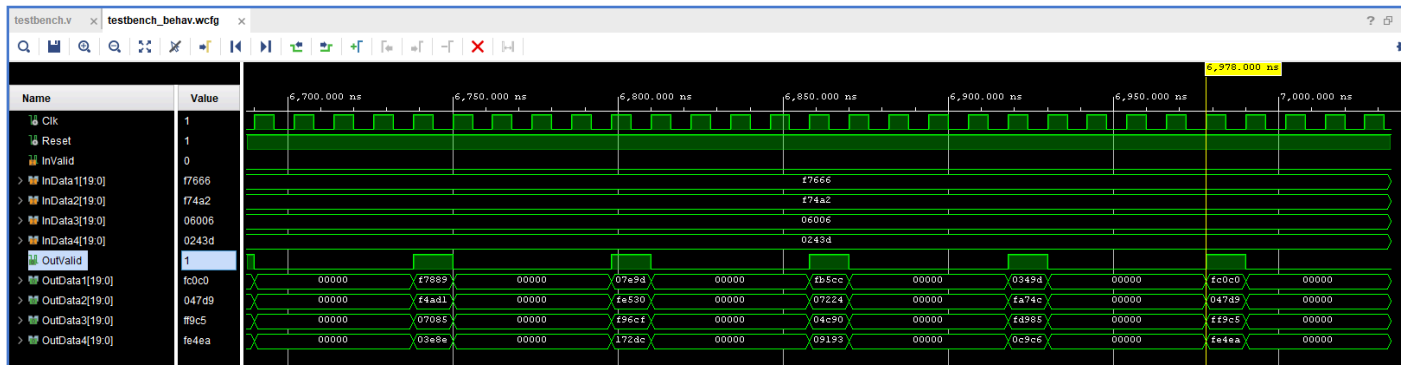- **working items and weightings of two members**

Task	Member	weightings
Software	范宇清	100%
Hardware – Cordic systolic array	張根齊	100%
Hardware – Back substitution	范宇清	100%

9. Additional Requirement

- Start time: at 264ns
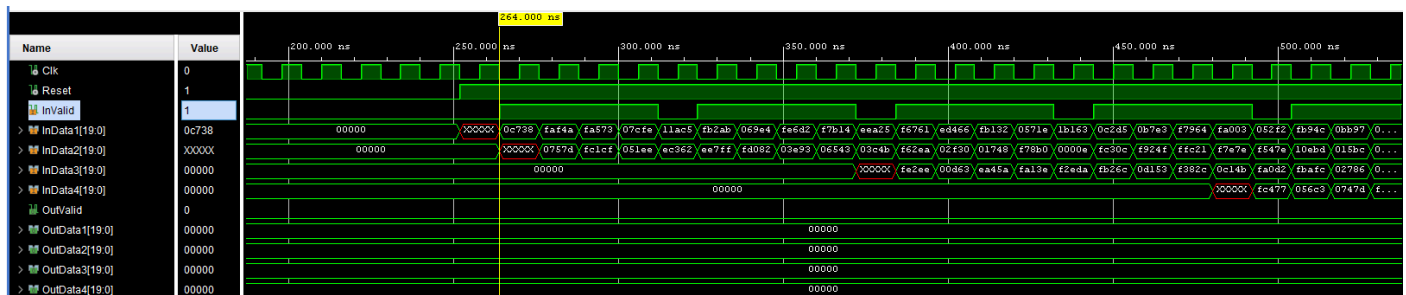
- End time: at 6978ns

- Average processing time = (6978 - 264) / 100 = 67.14ns