DSP in VLSI

HW4

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1. (Step 1) Please show how you calculate the scaling factor, write down the N value that you use and the result of $S(N)$.

   Scaling factor 算式:

$$S = \prod_{i=0}^{N-1} \frac{1}{\sqrt{1 + 2^{-2i}}}$$

   Matlab code:

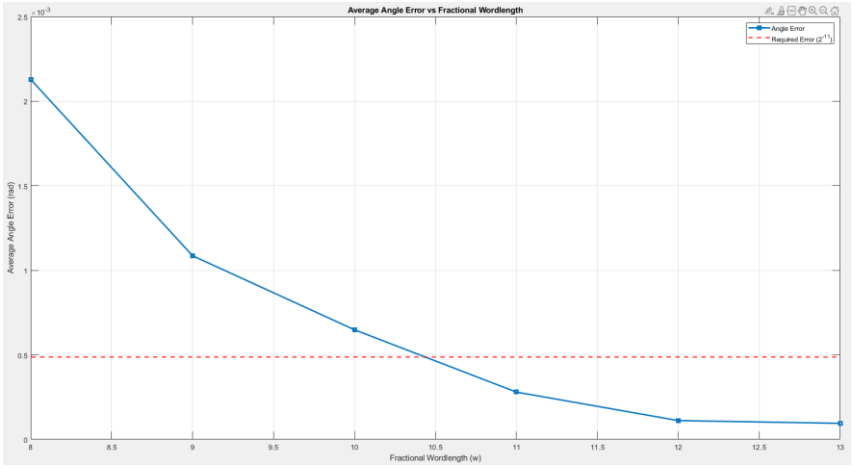
   I use N = 24, result of $S(N)$ is 0.6072529350.

```
N = 24;

S = 1;
for i = 0:N-1
    S = S * (1 / sqrt(1 + 2^(-2*i)));
end
```

2. (Step 2) Draw the figure of average absolute error versus fractional word-length (10%) to show how you determine the setting of word-length of the fractional part. Write down the integer word-length of $X(i)$ and $Y(i)$ that you use all the stages. Please explain it. (5%)

   2.1 Average absolute error versus fractional word-length: choose w = 11.



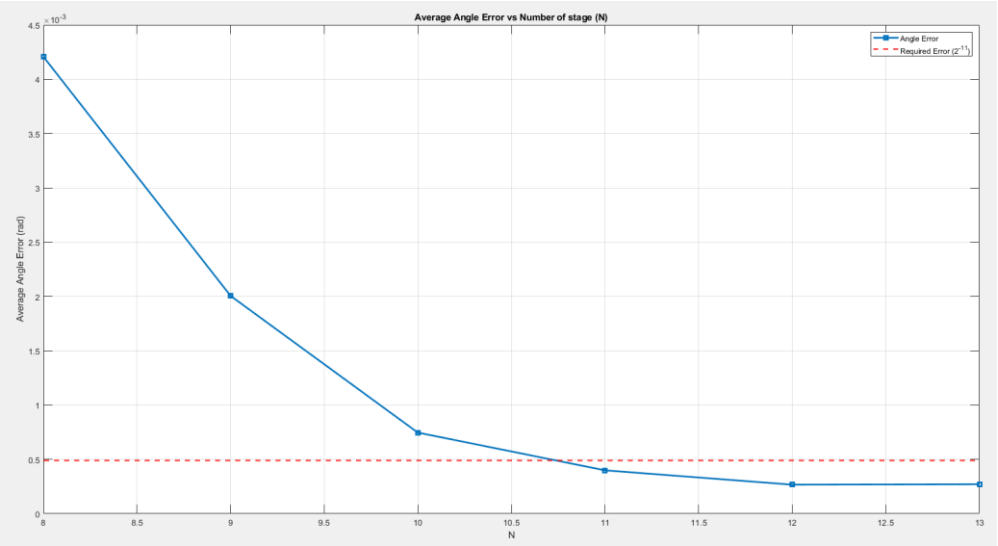
2.2 integer word-length of $X(i)$ and $Y(i)$ = 3 bits

The integer word length of $X(i)$ and $Y(i)$ is set to 3 bits to ensure that no overflow occurs during the N = 24 stages, which could otherwise lead to errors. I have verified using MATLAB that a 3-bit integer word length is sufficient to prevent overflow.

3. (Step 3) Please draw a figure to denote the average phase errors of 11 quantized input pairs (X, Y) versus different numbers of micro-rotations N (10%) and draw a figure to show the resulted phase errors of 11 quantized input pairs versus the word-length of quantized elementary angles (10%). Explain how you determine it. Also list a table of the elementary angles (both in floating-point representation and binary fixed-point representation). (5%)

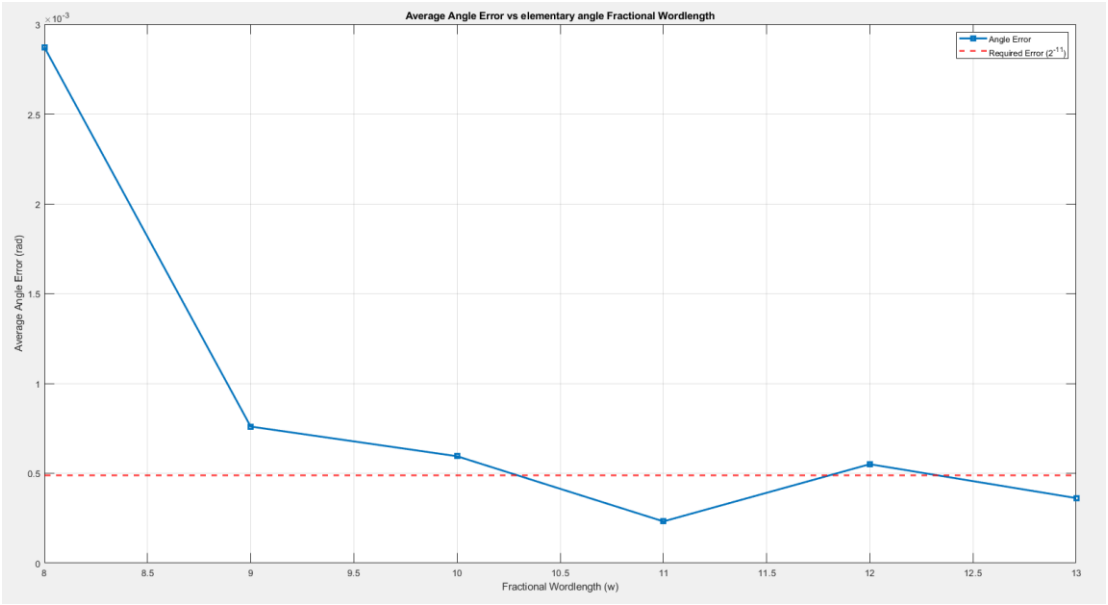
3.1 Average phase errors of 11 quantized input pairs (X, Y) versus different numbers of micro-rotations N:

Choose N = 11.



3.2 phase errors of 11 quantized input pairs versus the word-length of quantized elementary angles:

Choose frac word-length of elementary angles = 11. And integer word-length of elementary angles = 3 to ensure that no overflow occurs.



3.3 Table of the elementary angles:

Floating-point representation:

```
atan_table_final[1] = 0.785398
atan_table_final[2] = 0.463648
atan_table_final[3] = 0.244979
atan_table_final[4] = 0.124355
atan_table_final[5] = 0.062419
atan_table_final[6] = 0.031240
atan_table_final[7] = 0.015624
atan_table_final[8] = 0.007812
atan_table_final[9] = 0.003906
atan_table_final[10] = 0.001953
atan table final[11] = 0.000977
```

Binary fixed-point representation (3bit int, 11bit frac):

```
atan_table_final_fix[1] = 00011001001000
atan_table_final_fix[2] = 00001110110110
atan_table_final_fix[3] = 00000111110110
atan_table_final_fix[4] = 00000011111111
atan_table_final_fix[5] = 00000010000000
atan_table_final_fix[6] = 00000001000000
atan_table_final_fix[7] = 00000000100000
atan_table_final_fix[8] = 00000000010000
atan_table_final_fix[9] = 00000000001000
atan_table_final_fix[10] = 00000000000100
atan_table_final_fix[11] = 00000000000010
```

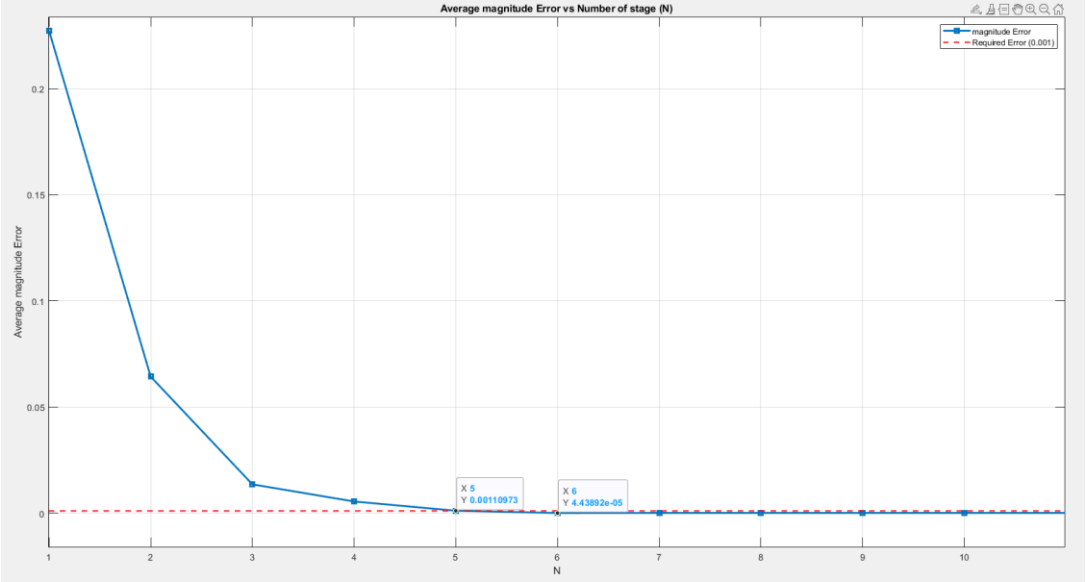
4. (Step 4) Please show how you decide the number of micro-rotations for the magnitude function with error tolerance of 0.1%. (10%)

$$\frac{|X+jY|-S(N)X(N)}{|X+jY|} < 1-\cos\left(\theta_e(N-1)\right) = 1-\frac{1}{\sqrt{1+2^{-2(N-1)}}}. \qquad (12)$$

I use equation 12 to find sufficient N such that magnitude error < 0.1%. Matlab code is shown as below, and the minimum N to meet the requirement is 6.

```
N_report4 = 1:11;
for N = N_report4
    if 0.001 > (1 - 1/(sqrt(1 + 2^(-2*(N - 1)))))
        meet = 1;
    else
        meet = 0;
    end
    fprintf('N = %d, meet = %d\n', N , meet);
end
```

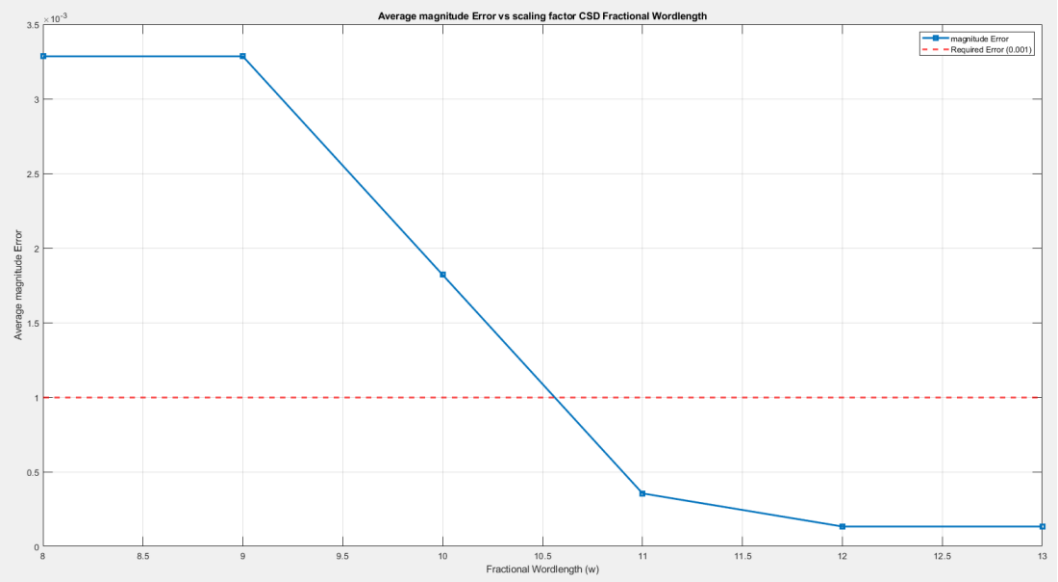
I also draw the figure to verify equation 12.



5. (Step 5) Write a program to show the setting of fractional word-length of CSD versus error. Draw the figure. (10%). Depict your design for the shift-and-add block according to your CSD representation. How many adders do you use? (10%)

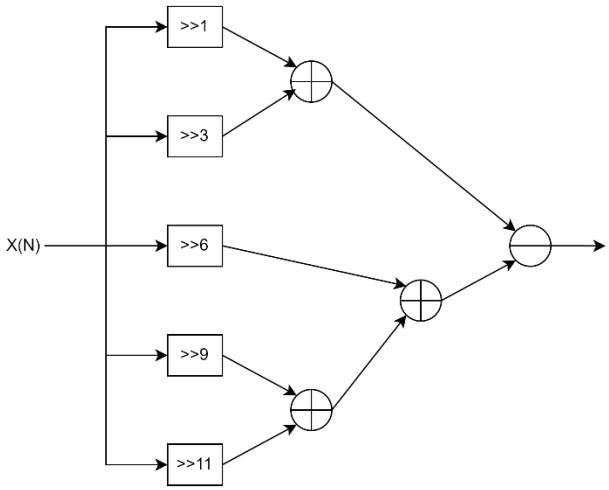
5.1 fractional word-length of CSD versus magnitude error

Choose CSD frac word-length = 11.



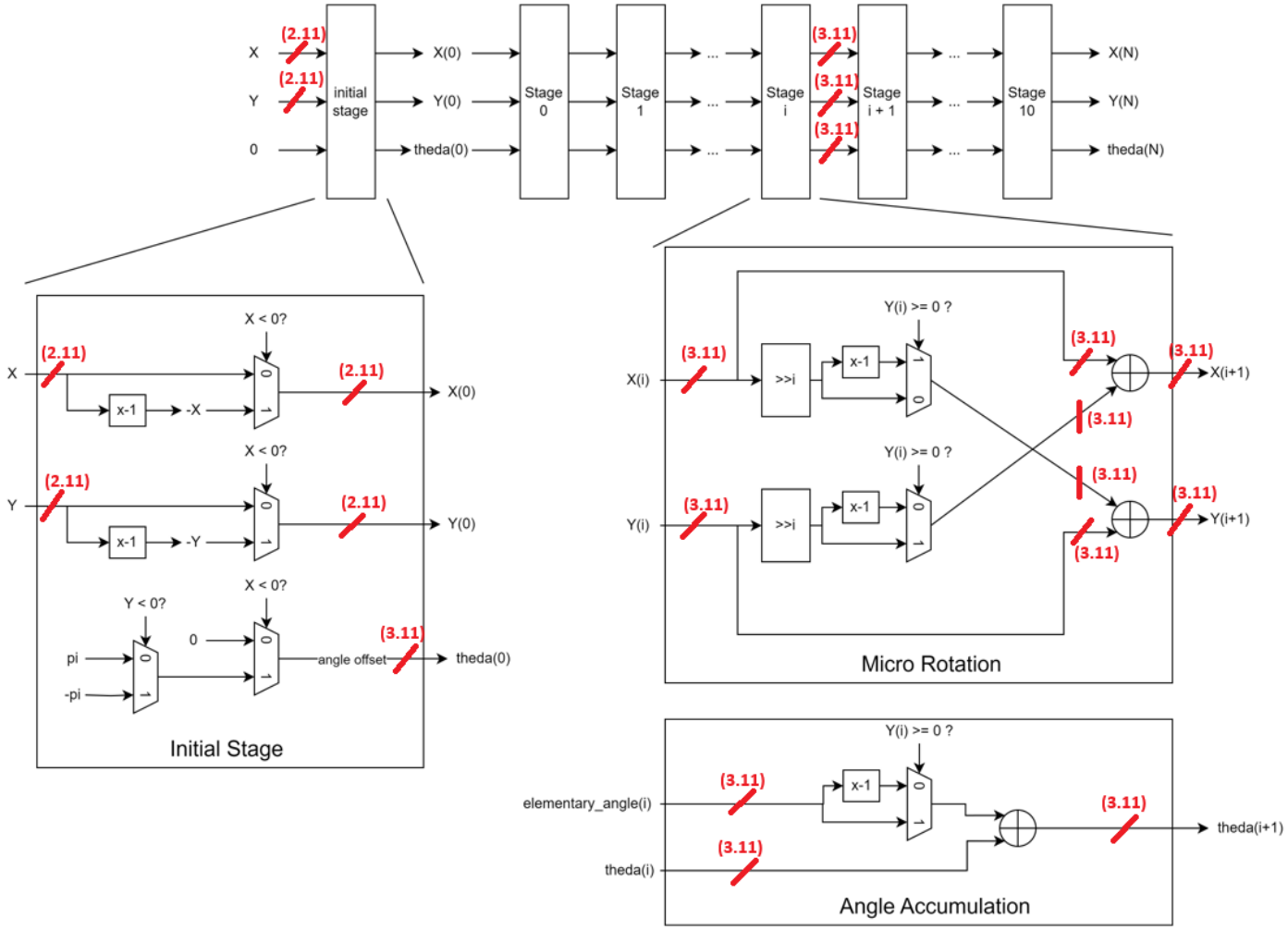
5.2 Shift-and-add block: Total 4 adder (3 add and 1 sub)

CSD block diagram calculate X(N) * Scaling_factor.



6. (Step 6) Depict your design of the initial stage and the complete CORDIC architecture for the arctangent function. Mark the word-length in the block diagram. (10%)

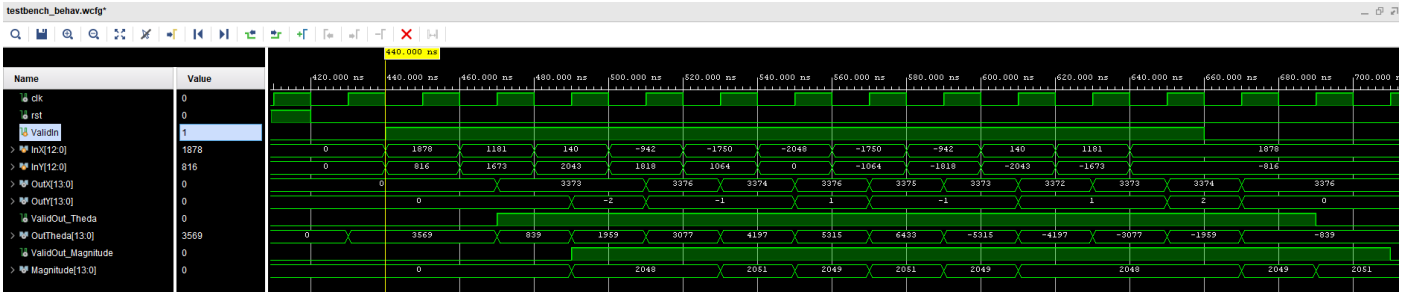
(x, y) means x bits integer and y bits fraction. All data are signed number.



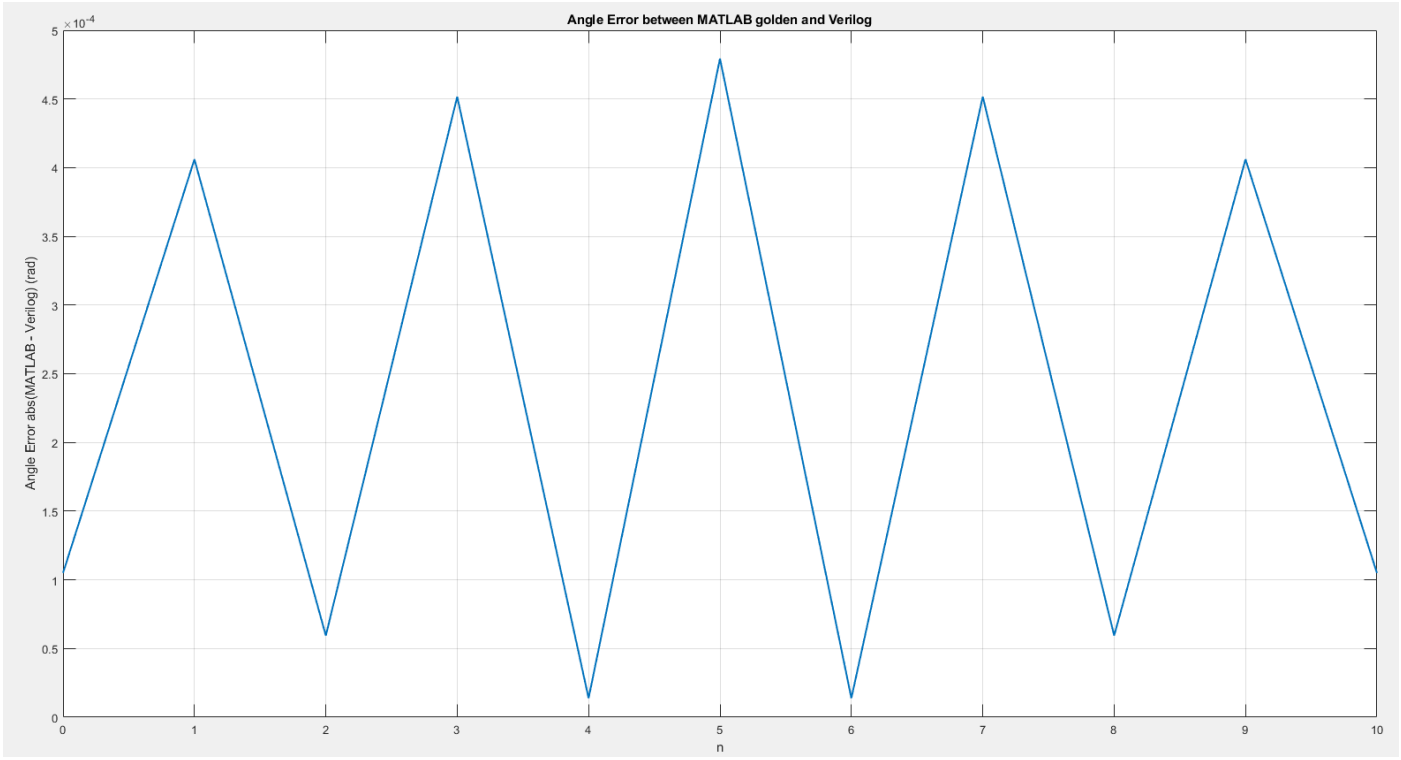
7. (Step 6) Implement your design with only DFFs inserted at the inputs and outputs. Show the timing diagram of behavior simulation. (20%) Compare the results with the arctangent function and draw the error versus index n to show that your implementation meets the precision requirements of error less than 2^−11. (10%)

7.1 timing diagram of behavior simulation

Value of timing diagram is in signed decimal, divided it by 2^11 is true value. (11bit fraction)



7.2 The angle error between matlab golden(double) and RTL output(fixed point)

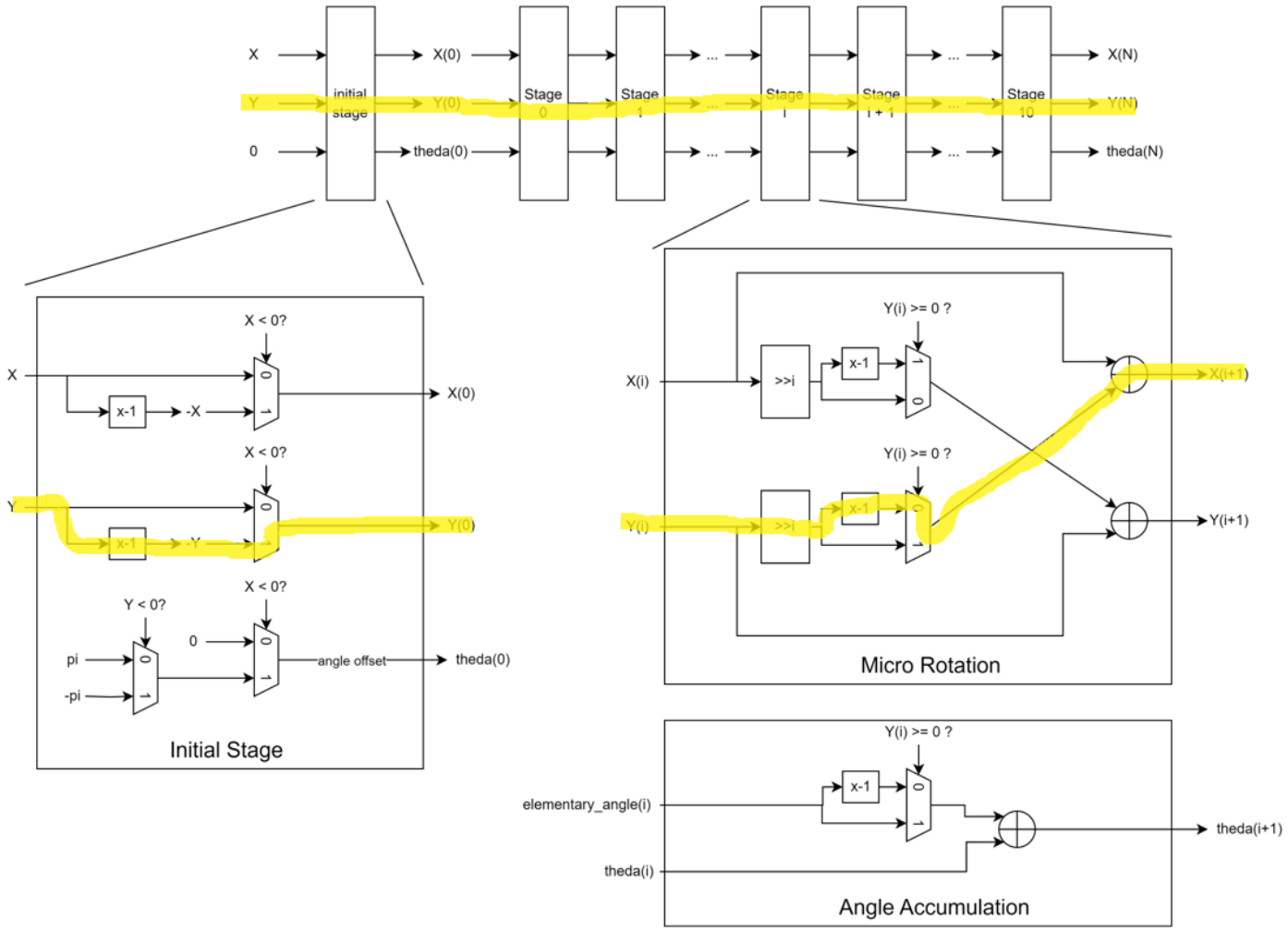


Average angle error meets the requirement 2^-11.

```
>> main
Scaling factor for N = 24 is 0.6072529350
average angle error = 0.000232, average angle error < 2^-11 = 1
>>
```

8. (Step 6) Draw the critical path in your block diagram and synthesize your circuits to show the critical path and max delay (or operating frequency). (10%)

8.1 critical path marked with yellow

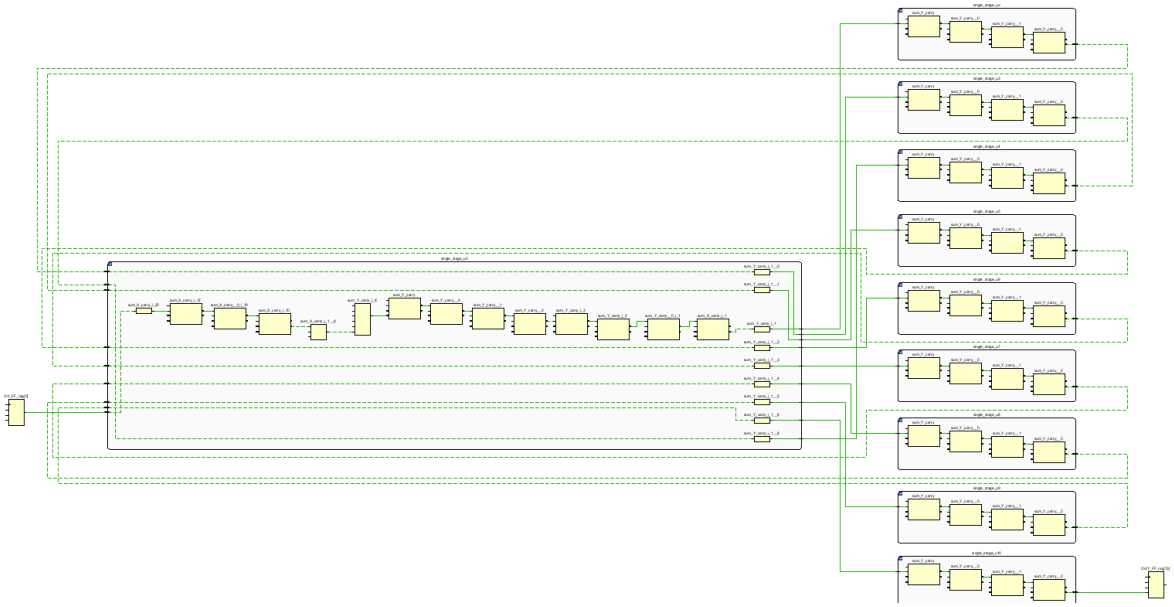


8.2 critical path and max delay

max delay is 26.687ns, operation frequency = 37.4MHz.

Name	Path 1
Slack	3.195ns
Source	InY_FF_reg[0]/C (rising edge-triggered cell FDCE clocked by clk {rise@0.000ns fall@15.000ns period=30.000ns})
Destination	OutY_FF_reg[13]/D (rising edge-triggered cell FDCE clocked by clk {rise@0.000ns fall@15.000ns period=30.000ns})
Path Group	clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	30.000ns (clk rise@30.000ns - clk rise@0.000ns)
Data Path Delay	26.687ns (logic 17.586ns (65.897%) route 9.101ns (34.103%))
Logic Levels	59 (CARRY4=47 LUT1=10 LUT3=1 LUT6=1)
Clock Path Skew	-0.145ns
Clock Un...rtainty	0.035ns

Critical path is from InY input flip flop to OutY output flip flop.



9. (Step 7) Calculate how to insert sufficient pipeline register to meet the requirement of operating frequency. (5%). Insert the pipeline registers in your design. Synthesize your implementation again to obtain the timing slack with the timing constraint of (1/fs) and show that the slack is positive. (5%) Check the critical path report from the synthesizer to show that your pipeline insertion is effective. (5%). Show the timing diagram of post-synthesis simulation with correct setting of clock period. (20%) Verified the error between the post-synthesis results and the floating-point arctangent results. Draw the error versus index n. (10%)

9.1 calculate pipeline register to meet the requirement of operating frequency

$$original\ maximum\ delay = 26.687ns$$

$$required\ maximum\ delay < \frac{1}{75MHz} = 13.333ns$$

$$required\ pipeline\ stage > \frac{26.687}{13.333} = 2.002$$

$$choose\ pipeline\ stage = 3$$

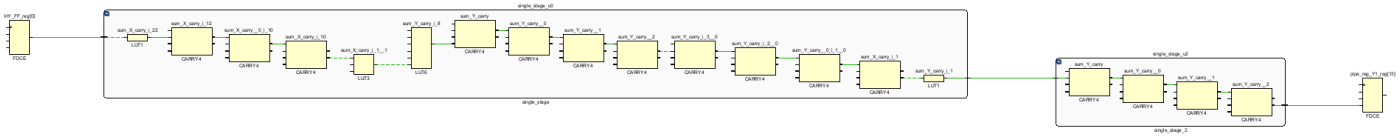
9.2 pipeline design max delay is 9.234ns

maximum operating frequency = 108MHz, but I choose clock period = 13ns, so actual operating frequency = 76.9MHz, which faster than the requirement 75MHz.

Summary

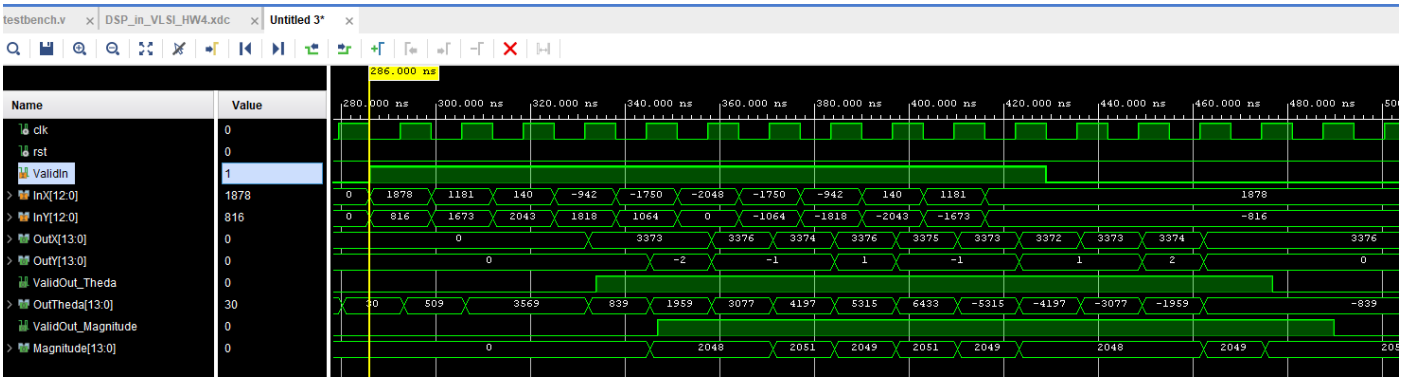
Name	Path 1
Slack	3.648ns
Source	InY_FF_reg[0]/C (rising edge-triggered cell FDCE clocked by clk {rise@0.000ns fall@6.500ns period=13.000ns})
Destination	pipe_reg_Y1_reg[13]/D (rising edge-triggered cell FDCE clocked by clk {rise@0.000ns fall@6.500ns period=13.000ns})
Path Group	clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	13.000ns (clk rise@13.000ns - clk rise@0.000ns)
Data Path Delay	9.234ns (logic 5.890ns (63.786%) route 3.344ns (36.214%))
Logic Levels	19 (CARRY4=15 LUT1=2 LUT3=1 LUT6=1)
Clock Path Skew	-0.145ns
Clock Un...rtainty	0.035ns

9.3 critical path is from InY to pipeline register.

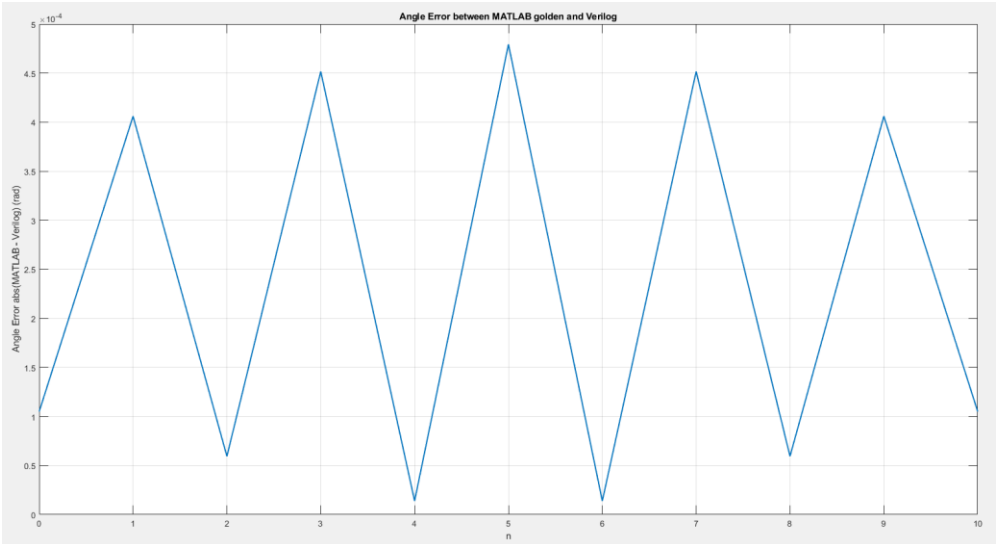


9.4 timing diagram of post-synthesis simulation (clock period = 13ns)

Value of timing diagram is in signed decimal, divided it by 2^11 is true value. (11bit fraction)



9.5 error between the post-synthesis results and the floating-point arctangent results



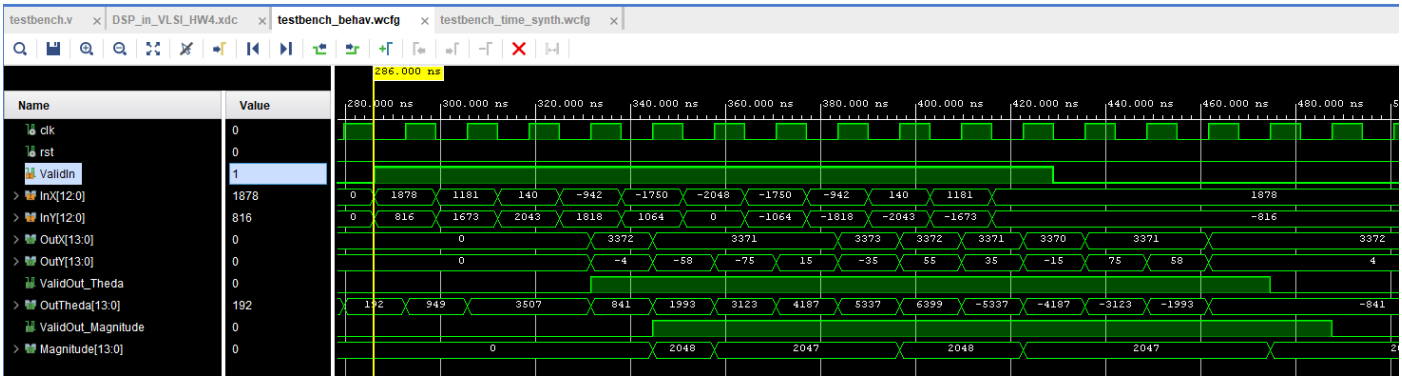
Average angle error meets the requirement 2^-11.

```
>> main
Scaling factor for N = 24 is 0.6072529350
average angle error = 0.000232, average angle error < 2^-11 = 1
>>
```

10. (Step 8) Based on the design in Step 7, change it to calculate the magnitude function. Show the timing diagram of behavior simulation and post-synthesis simulation with correct setting of clock period (1/fs). (20%). Verified the error between the post-synthesis results and the floating-point arctangent results. Draw the error versus index n. (10%)

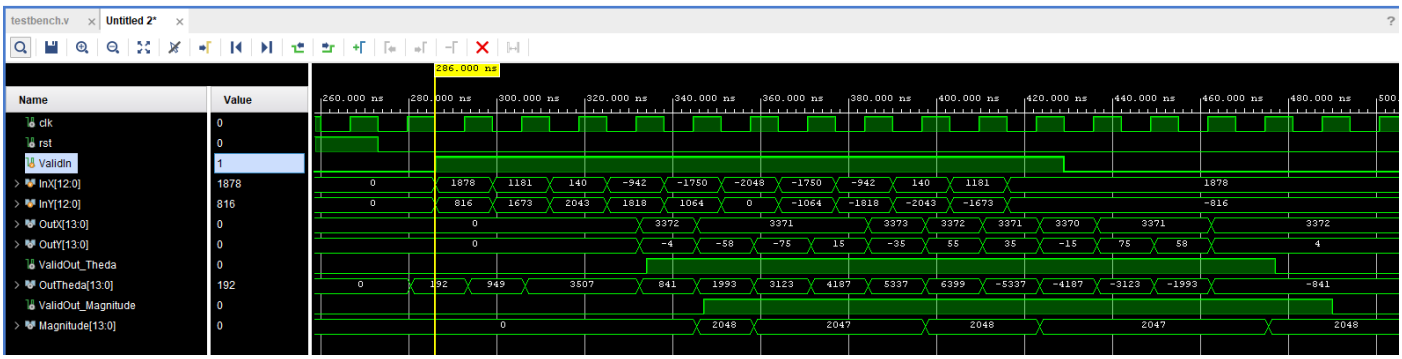
10.1 timing diagram of behavior simulation (clock period = 13ns)

Value of timing diagram is in signed decimal, divided it by 2^11 is true value. (11bit fraction)

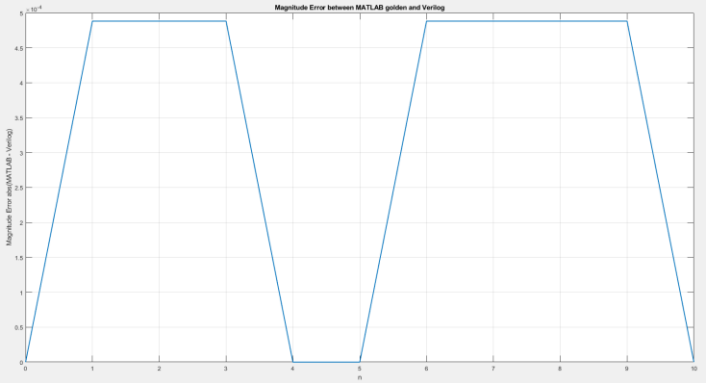


10.2 timing diagram of post-synthesis simulation (clock period = 13ns)

Value of timing diagram is in signed decimal, divided it by 2^11 is true value. (11bit fraction)



10.3 error between the post-synthesis results and the floating-point results



Average magnitude error meets the requirement 0.1%.

```
average magnitude error = 0.000311, average magnitude error < 0.001 = 1
```