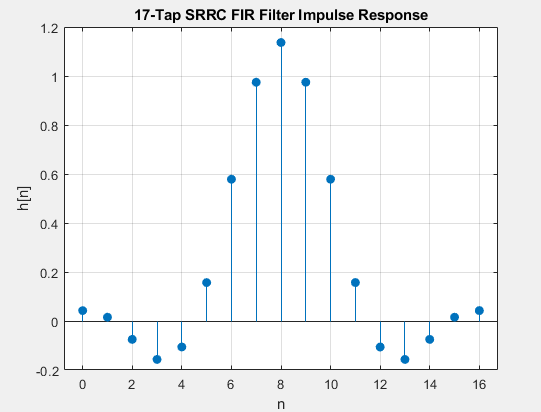
DSP in VLSI

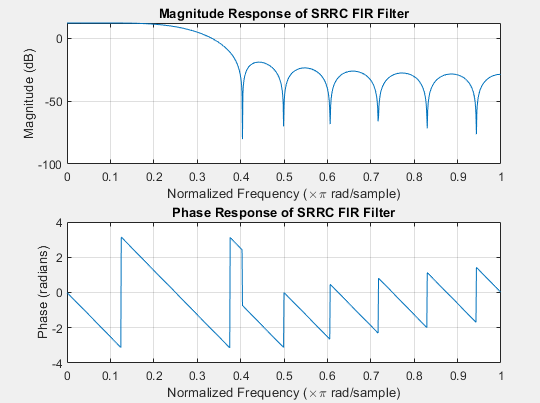
HW2

電子所ICS組, R13943015, 張根齊

1. (Step 1) Please use Matlab/Python to draw the impulse response and frequency response (containing magnitude and phase) of the 17-tap square-root raised-cosine FIR filter. Note that you need to use dB scale for the magnitude of the frequency response and use radian for the phase of frequency response versus normalized frequency. The x-axis must be marked with the correct label (20%). Please explain whether the filter is high-pass, band-pass or low-pass and why. (5%) 1.1 impulse response:



1.2 Frequency response:

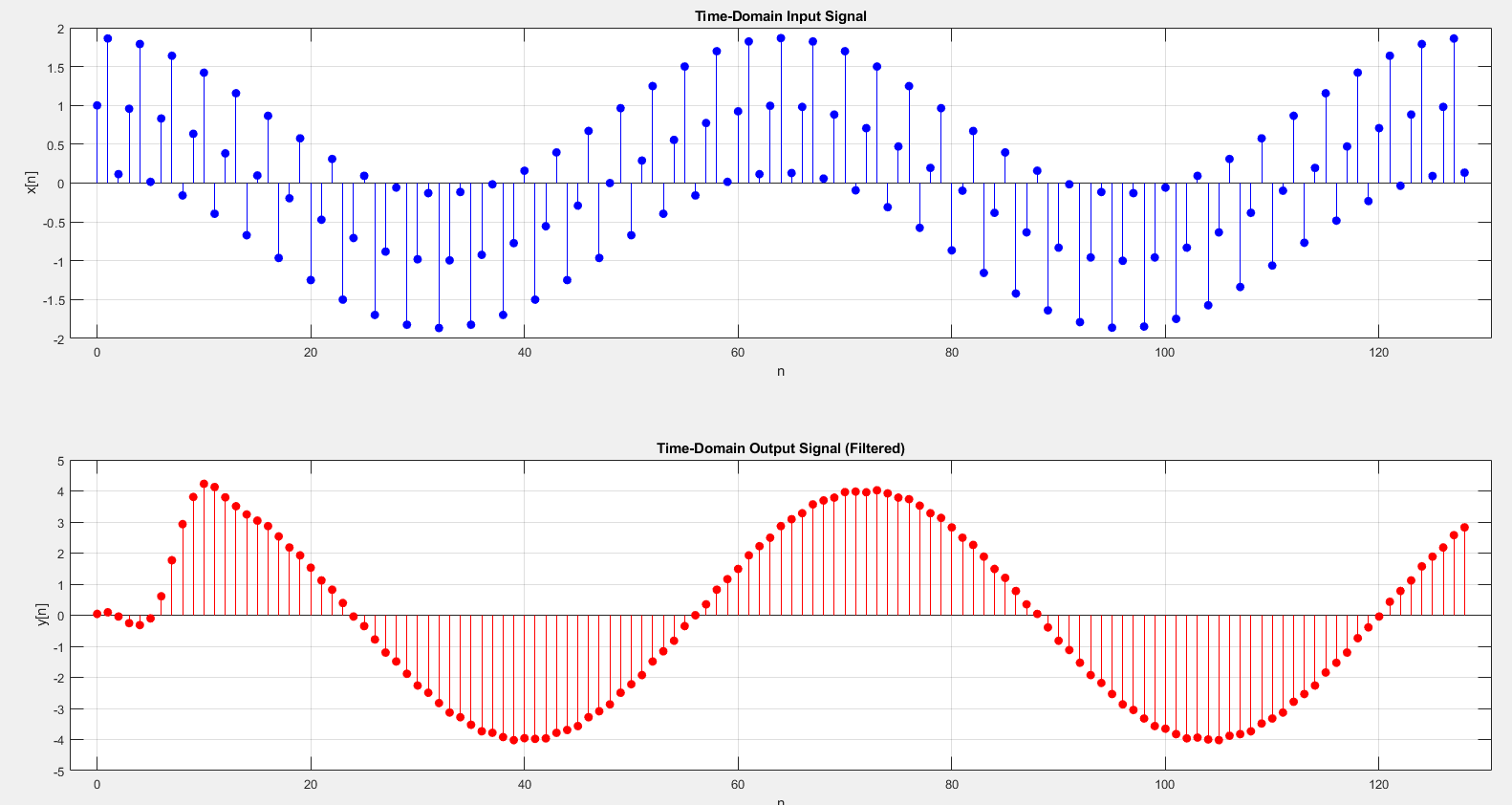


1.3 high-pass, band-pass or low-pass:

I think it is a low-pass filter because the magnitude of the FIR filter at low frequency (0π) is higher than at high frequency (1π).

2. (Step 2) Draw the time-domain input and output waveforms after you feed 128-point input (20%)

Output time domain waveform is obtained by transposed form FIR filter.



3. (Step 3) To show how you determine the word-length, please use the word-length of coefficients as the X-axis and error as the Y-axis. Scan the quantization error versus the word-lengths for at least 6 settings. (Four figures each having at least 6 word-length settings in its x-axis). According the following simulation results, mark the final word-length settings in the block diagram of the transposed form FIR filter. (20%)

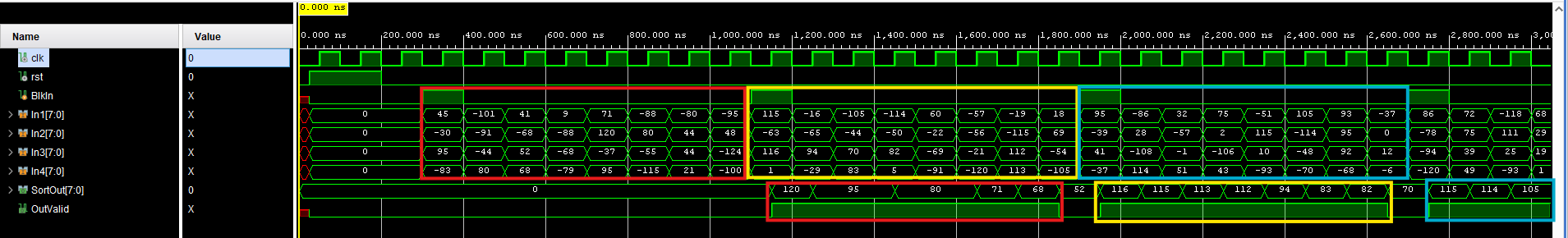
a. Output error versus input word-lengths

b. Output error versus coefficient word-lengths

c. Output error versus word-lengths after multiplication

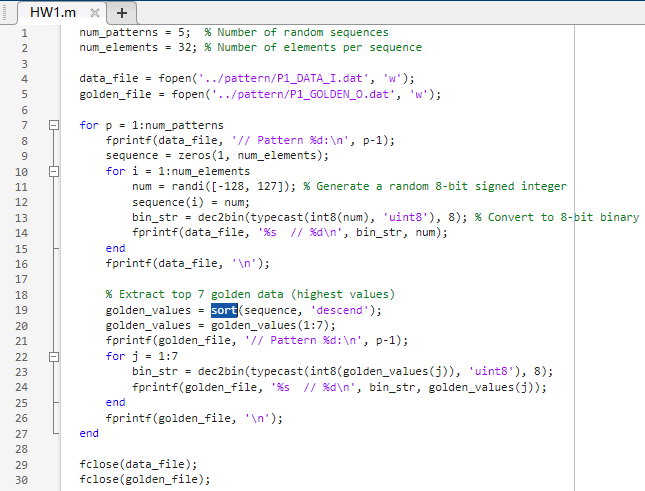
d. Output error versus word-lengths after addition

1. Show that your design can generate required top-7 output in descending order every 8 clock cycles as indicated in Fig. 3 in the timing diagram with proper input signal “BlkIn” and output indicator “OutValid”. If it is too long, please cut it down into several segments to make the numerical expressions in the timing diagram clear. If the numerical expressions are hard to distinguish, correct evaluation may not be 5 given. (30%)

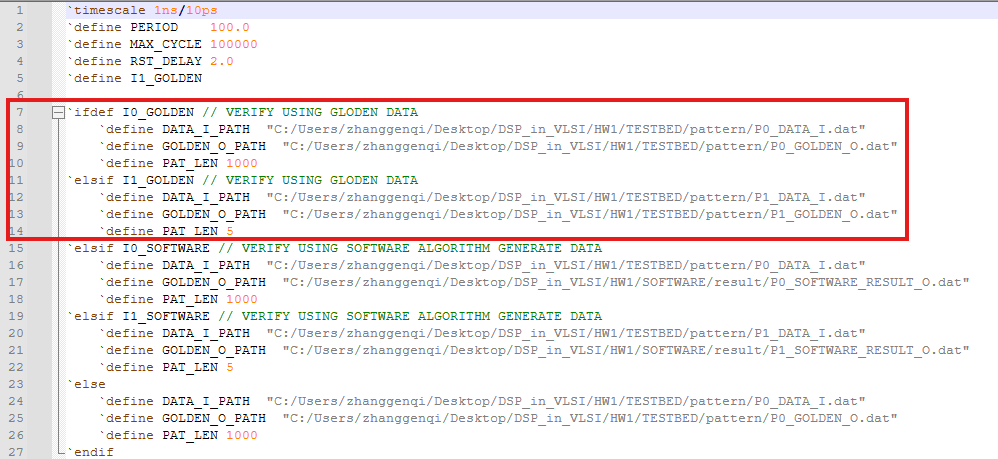
****

1. Please use Matlab command “sort” to verify your results of your randomly generated sequence and compare to the Verilog simulation results (10%).

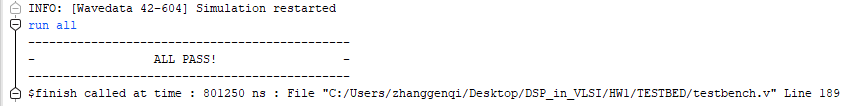
Matlab generate test pattern code:

****

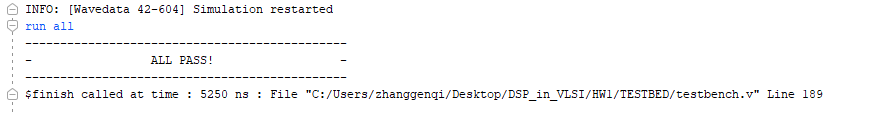
Testbench test pattern selection:

****

I0\_GOLDEN result:

****

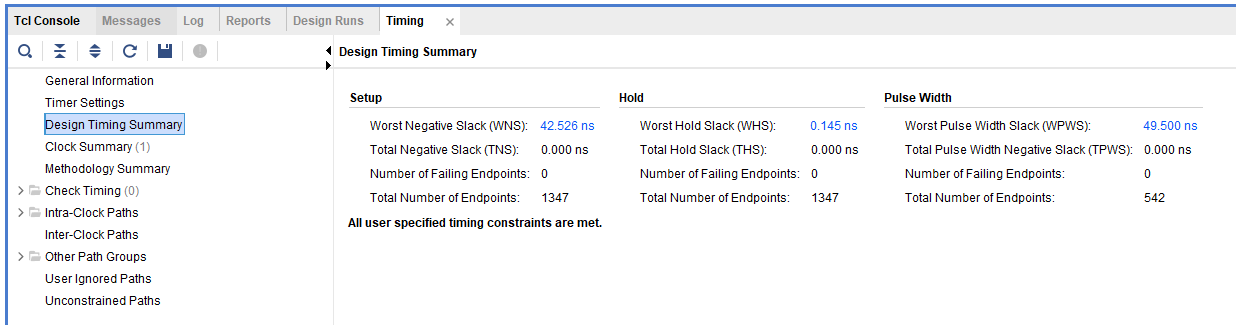
I1\_GOLDEN result:

****

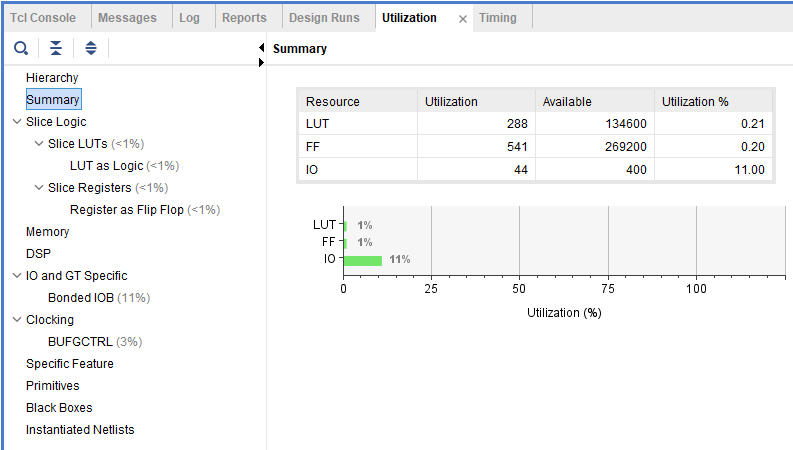
1. Synthesis your design in Q4. Show the number of adders/subtractors/comparators in your design. Sum them up together to see if it matches with your block diagram. (10%) (Because you may use counters to control your circuits, we will not ask that the two values should be exactly the same. However, there should not be a large difference.)

Clk period: 100ns

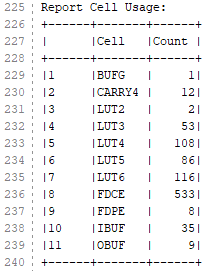
Synthesis timing result:



Synthesis utilization result:

****

Number of adders/subtractors/comparators: 12 (matched)

****