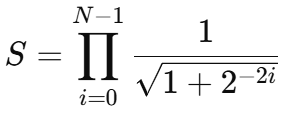
DSP in VLSI

HW4

電子所ICS組, R13943015, 張根齊

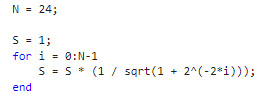
1. (Step 1) Please show how you calculate the scaling factor, write down the 𝑁 value that you use and the result of 𝑆(𝑁).

Scaling factor算式:



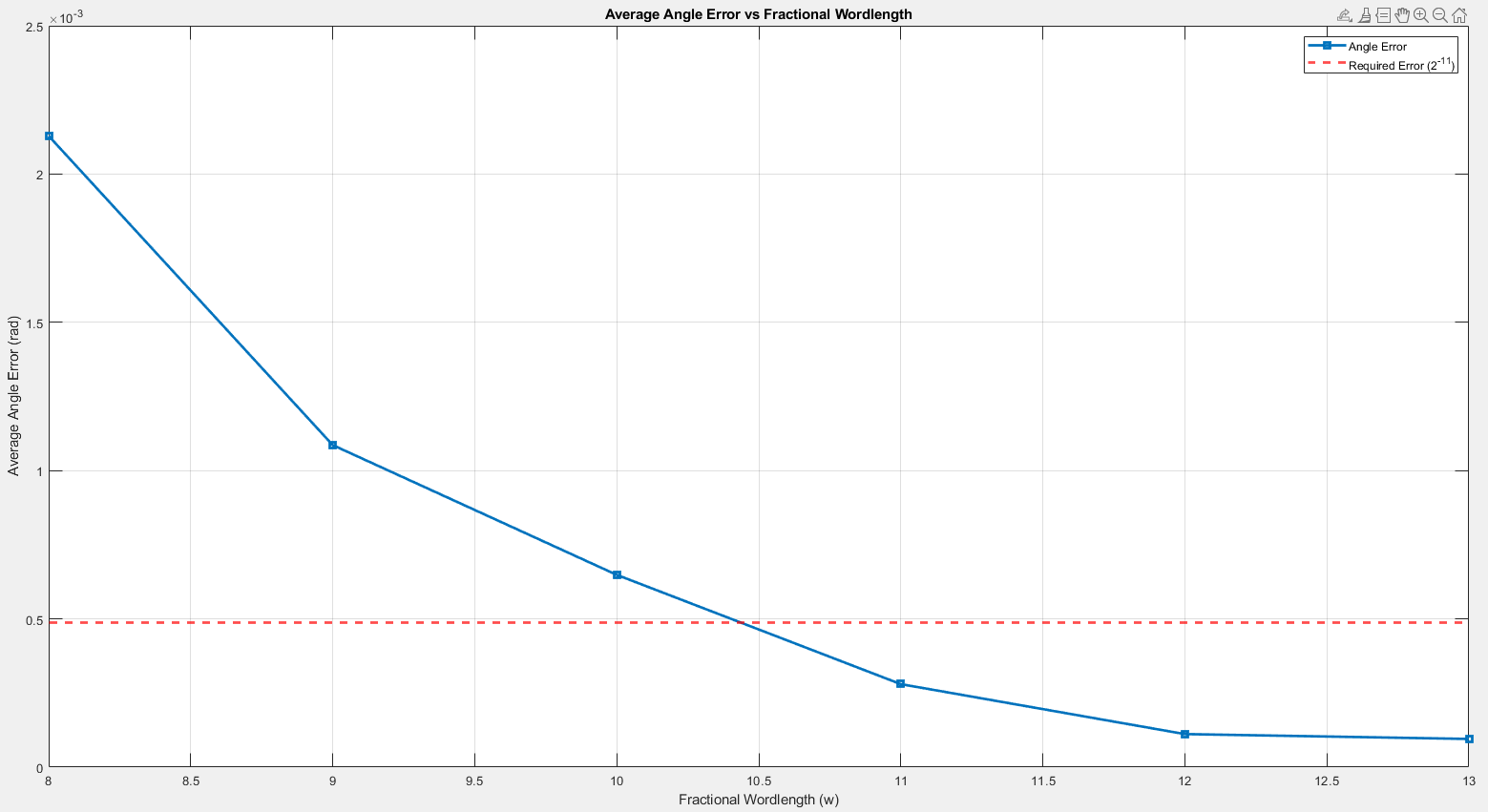
Matlab code:

I use N = 24, result of 𝑆(𝑁) is 0.6072529350.



1. (Step 2) Draw the figure of average absolute error versus fractional word-length (10%) to show how you determine the setting of word-length of the fractional part. Write down the integer word-length of 𝑋(𝑖) and 𝑌(𝑖) that you use all the stages. Please explain it. (5%)

2.1 Average absolute error versus fractional word-length: choose w = 11.

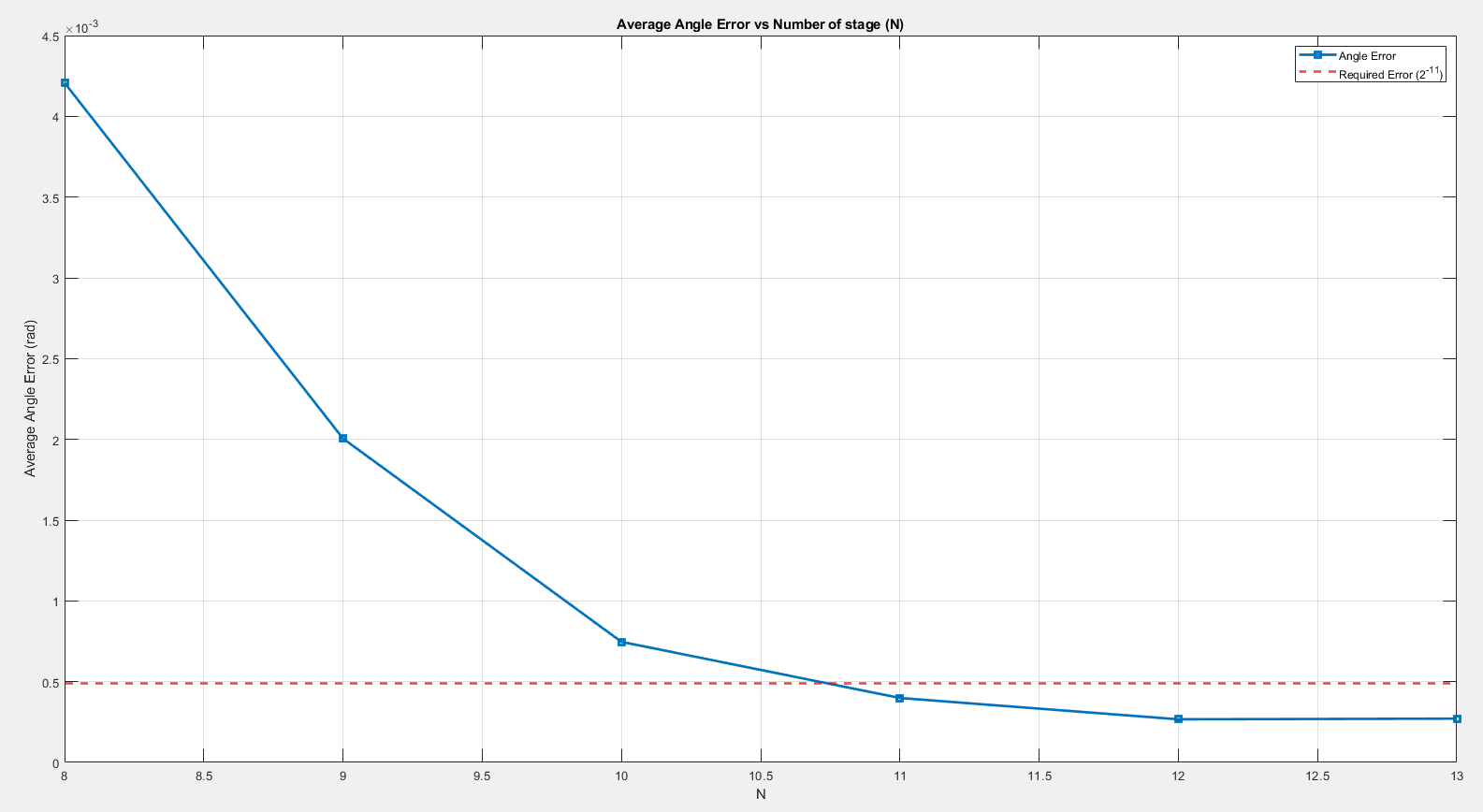


2.2 integer word-length of 𝑋(𝑖) and 𝑌(𝑖) = 3 bits

The integer word length of 𝑋(𝑖) and 𝑌(𝑖) is set to 3 bits to ensure that no overflow occurs during the 𝑁 = 24 stages, which could otherwise lead to errors. I have verified using MATLAB that a 3-bit integer word length is sufficient to prevent overflow.

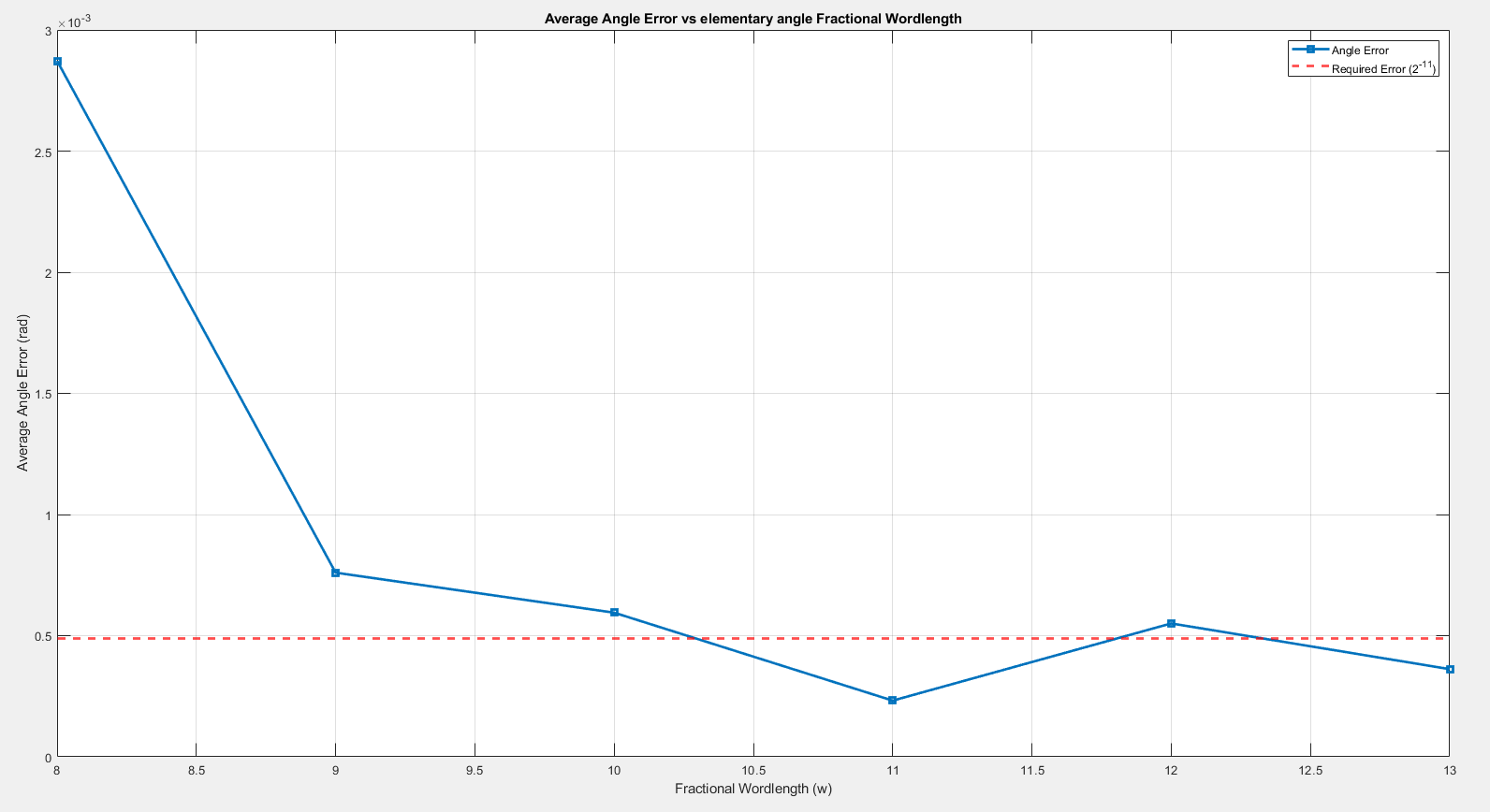
3. (Step 3) Please draw a figure to denote the average phase errors of 11 quantized input pairs (𝑋, 𝑌) versus different numbers of micro-rotations 𝑁 (10%) and draw a figure to show the resulted phase errors of 11 quantized input pairs versus the word-length of quantized elementary angles (10%). Explain how you determine it. Also list a table of the elementary angles (both in floating-point representation and binary fixed-point representation). (5%) 3.1 Average phase errors of 11 quantized input pairs (𝑋, 𝑌) versus different numbers of micro-rotations 𝑁:

Choose N = 11.



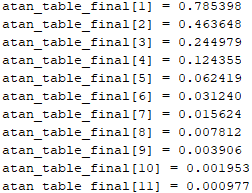
3.2 phase errors of 11 quantized input pairs versus the word-length of quantized elementary angles:

Choose frac word-length of elementary angles = 11. And integer word-length of elementary angles = 3 to ensure that no overflow occurs.

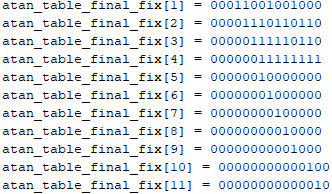


3.3 Table of the elementary angles:

Floating-point representation:



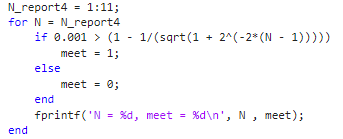
Binary fixed-point representation (3bit int, 11bit frac):



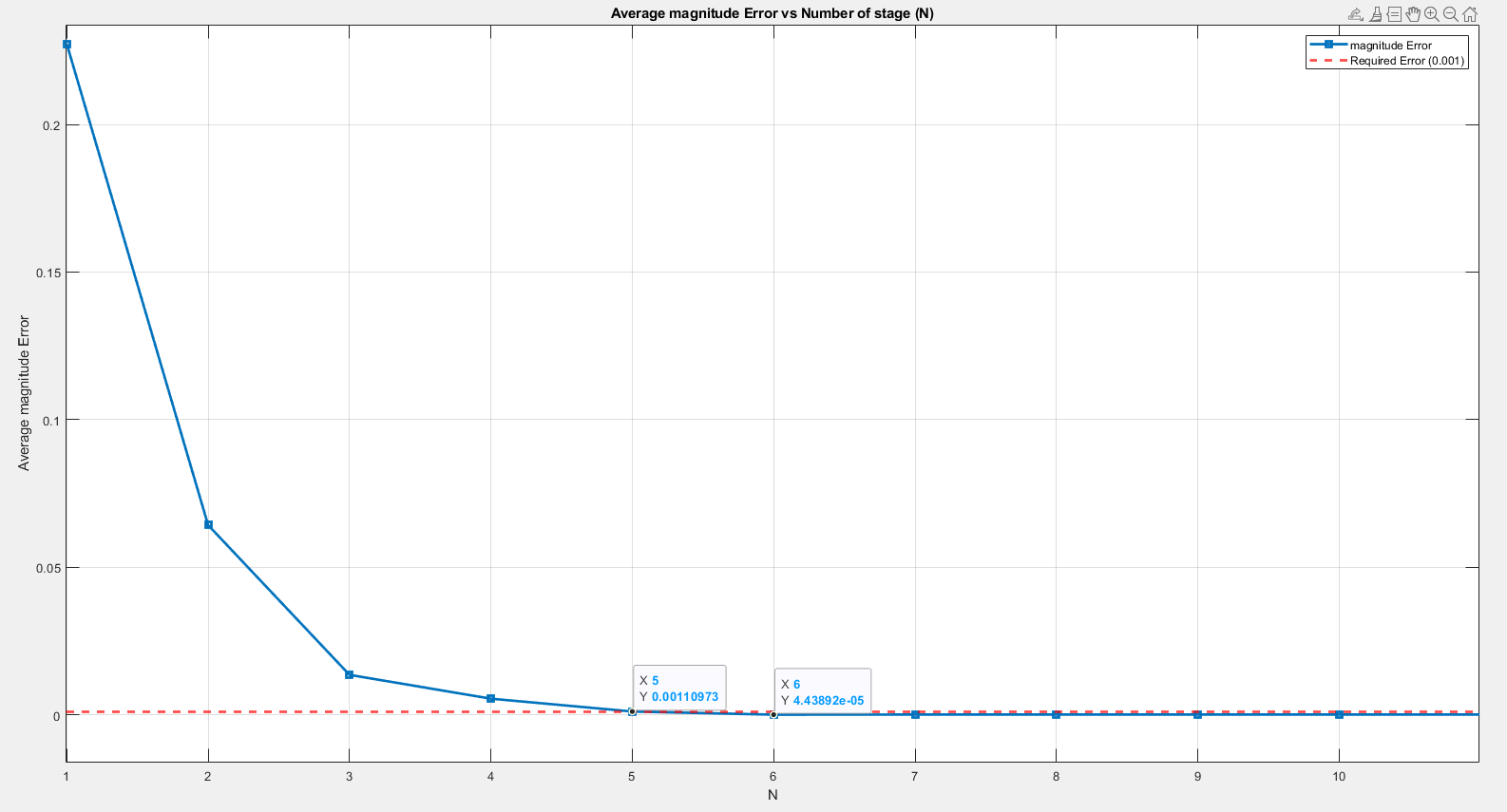
1. (Step 4) Please show how you decide the number of micro-rotations for the magnitude function with error tolerance of 0.1%. (10%)



I use equation 12 to find sufficient N such that magnitude error < 0.1%. Matlab code is shown as below, and the minimum N to meet the requirement is 6.



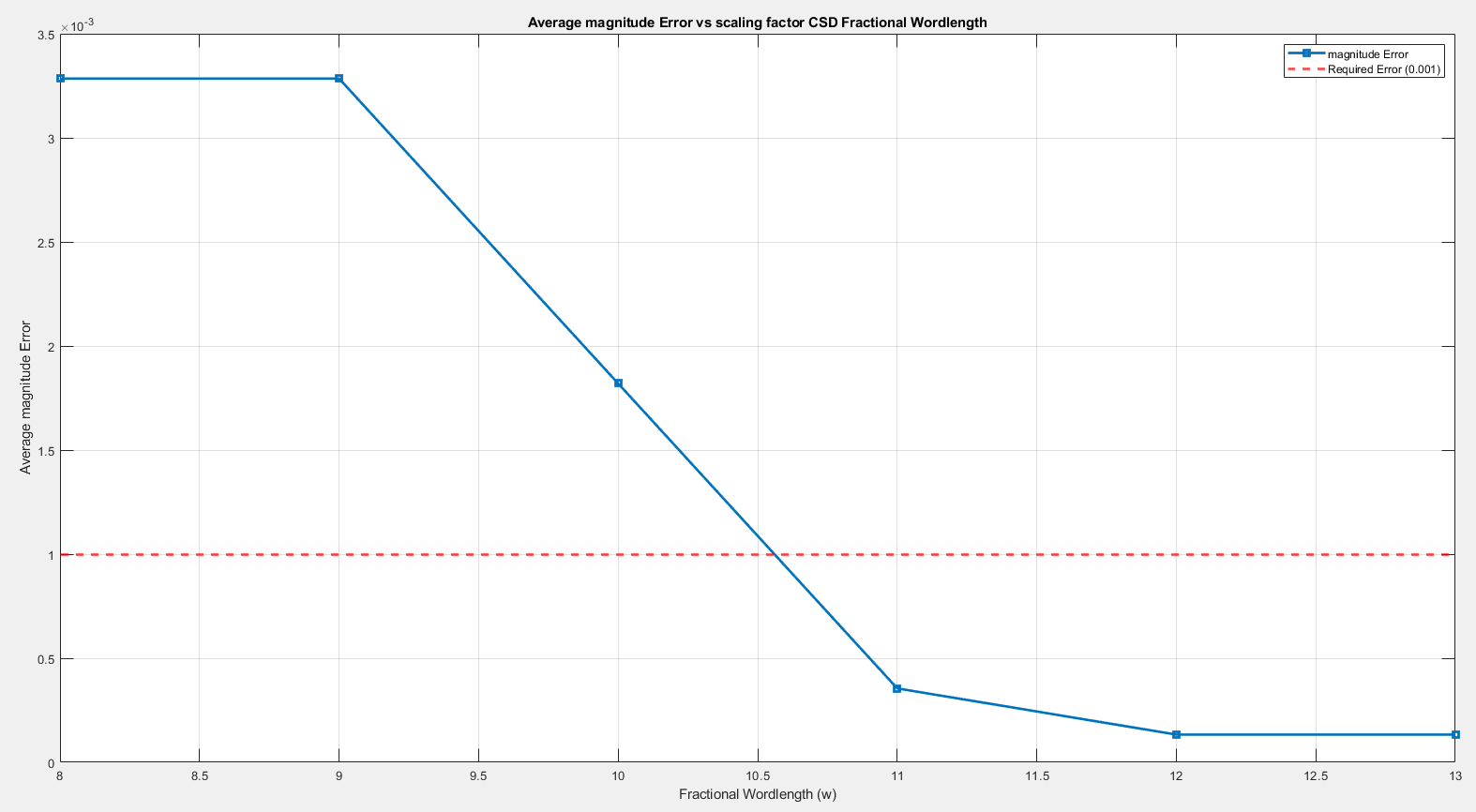
I also draw the figure to verify equation 12.



1. (Step 5) Write a program to show the setting of fractional word-length of CSD versus error. Draw the figure. (10%). Depict your design for the shift-and-add block according to your CSD representation. How many adders do you use? (10%)

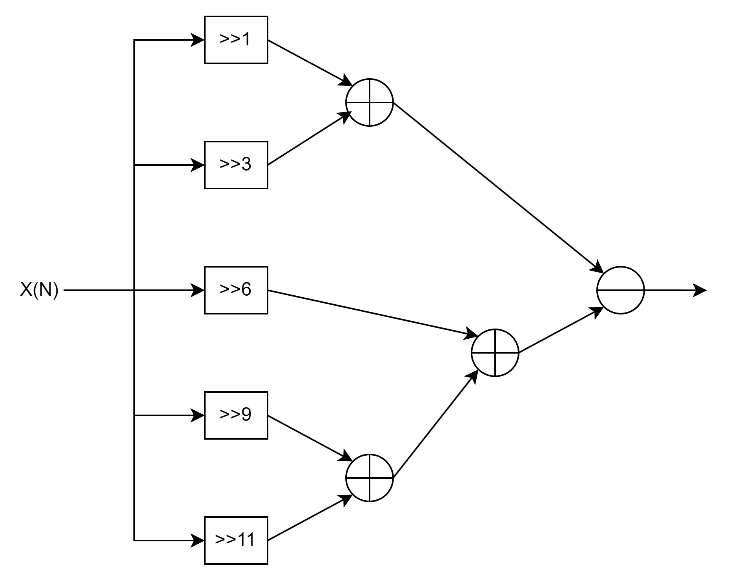
5.1 fractional word-length of CSD versus magnitude error

Choose CSD frac word-length = 11.



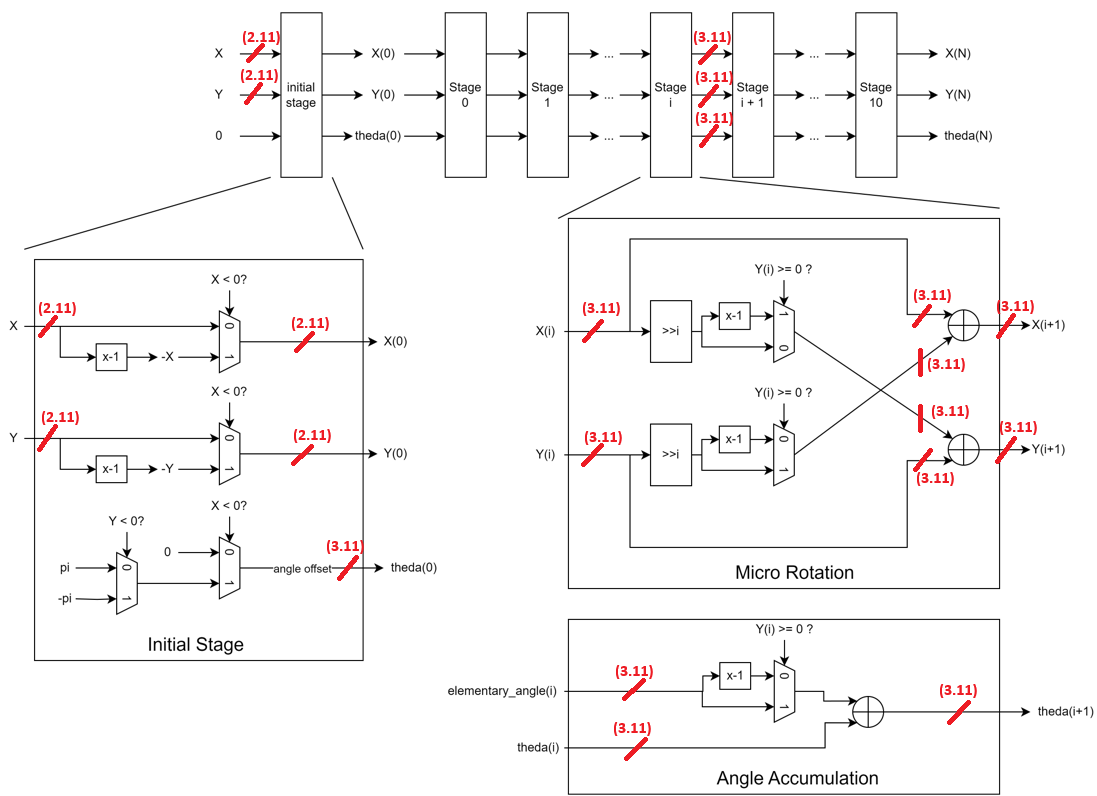
* 1. Shift-and-add block: Total 4 adder (3 add and 1 sub)

CSD block diagram calculate X(N) \* Scaling\_factor.



1. (Step 6) Depict your design of the initial stage and the complete CORDIC architecture for the arctangent function. Mark the word-length in the block diagram. (10%)

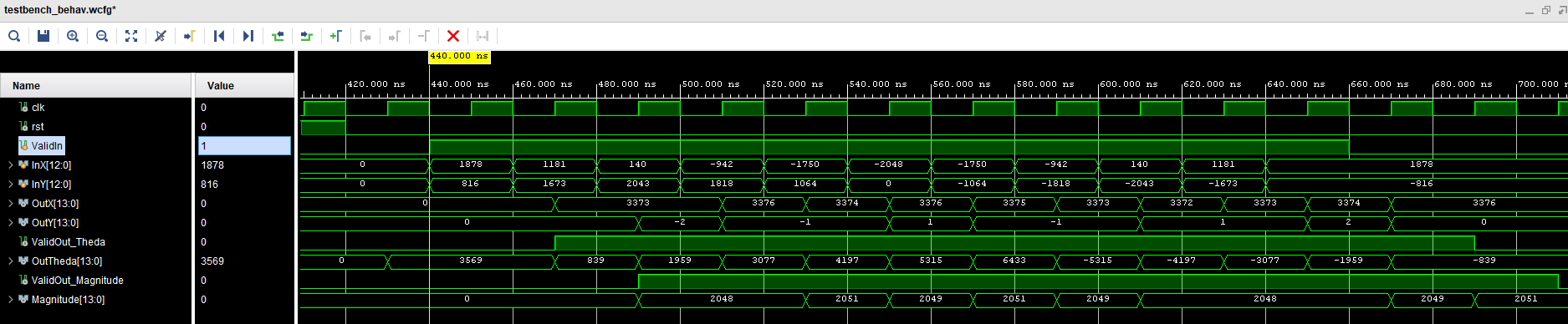
(x, y) means x bits integer and y bits fraction. All data are signed number.



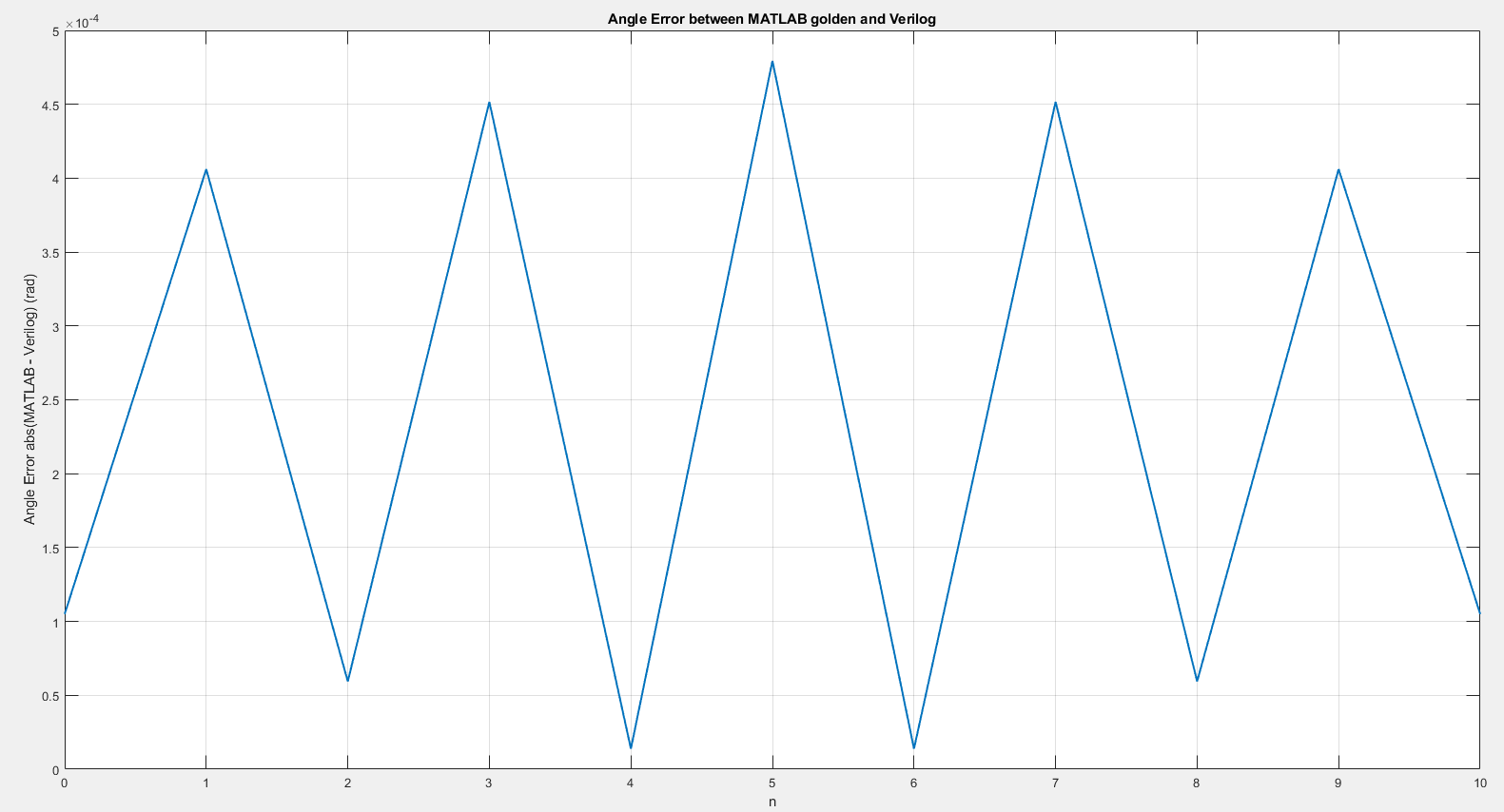
1. (Step 6) Implement your design with only DFFs inserted at the inputs and outputs. Show the timing diagram of behavior simulation. (20%) Compare the results with the arctangent function and draw the error versus index 𝑛 to show that your implementation meets the precision requirements of error less than 2^−11. (10%)

7.1 timing diagram of behavior simulation

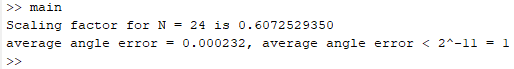
Value of timing diagram is in signed decimal, divided it by 2^11 is true value. (11bit fraction)



7.2 The angle error between matlab golden(double) and RTL output(fixed point)

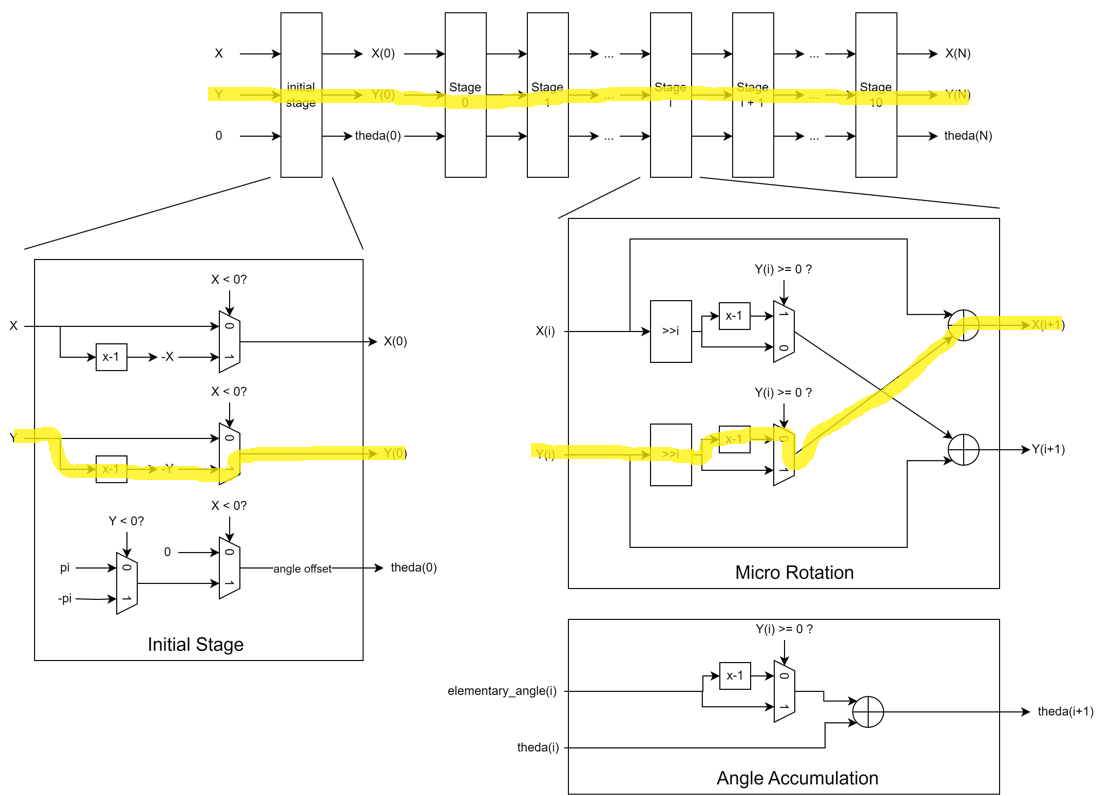


Average angle error meets the requirement 2^-11.



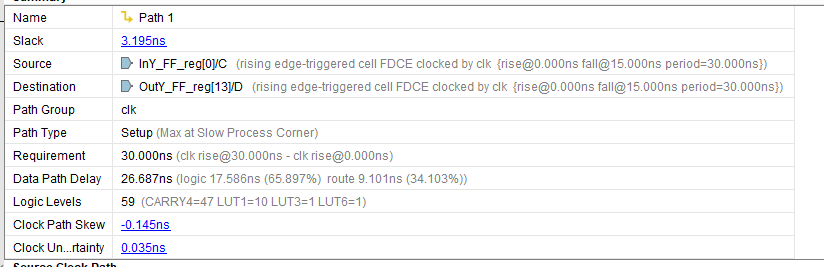
1. (Step 6) Draw the critical path in your block diagram and synthesize your circuits to show the critical path and max delay (or operating frequency). (10%)

8.1 critical path marked with yellow

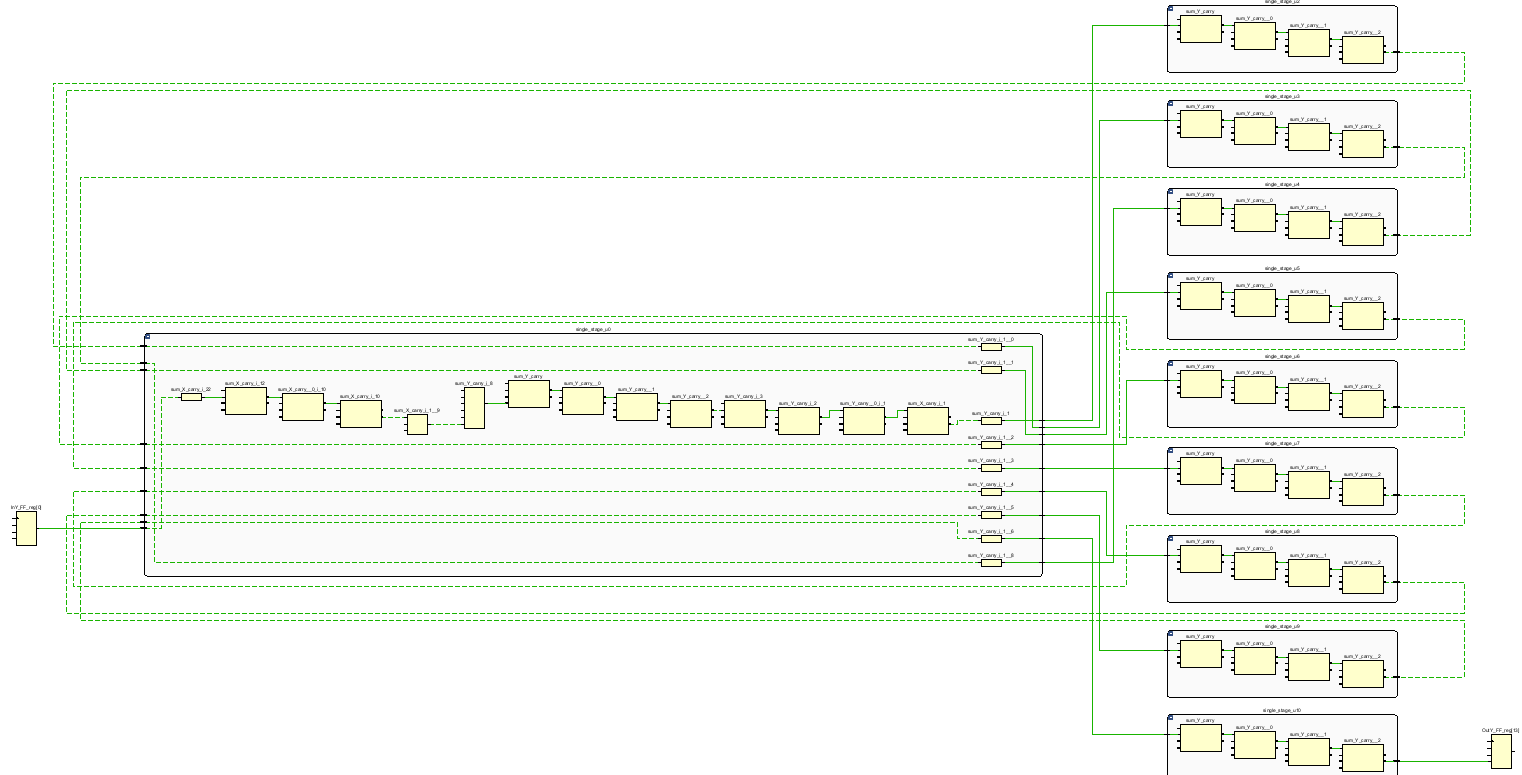


* 1. critical path and max delay

max delay is 26.687ns, operation frequency = 37.4MHz.



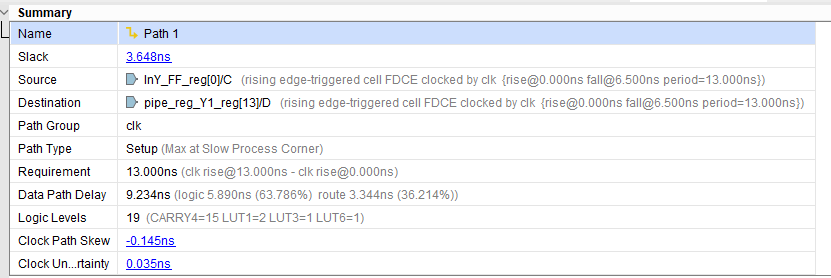
Critical path is from InY input flip flop to OutY output flip flop.



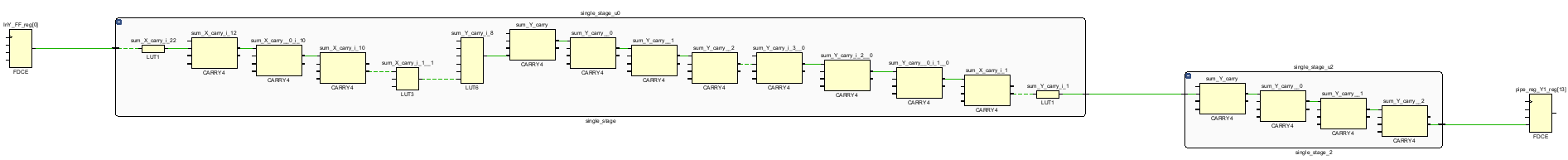
9. (Step 7) Calculate how to insert sufficient pipeline register to meet the requirement of operating frequency. (5%). Insert the pipeline registers in your design. Synthesize your implementation again to obtain the timing slack with the timing constraint of (1/fs) and show that the slack is positive. (5%) Check the critical path report from the synthesizer to show that your pipeline insertion is effective. (5%). Show the timing diagram of post-synthesis simulation with correct setting of clock period. (20%) Verified the error between the post-synthesis results and the floating-point arctangent results. Draw the error versus index 𝑛. (10%) 9.1 calculate pipeline register to meet the requirement of operating frequency

9.2 pipeline design max delay is 9.234ns

maximum operating frequency = 108MHz, but I choose clock period = 13ns, so actual operating frequency = 76.9MHz, which faster than the requirement 75MHz.

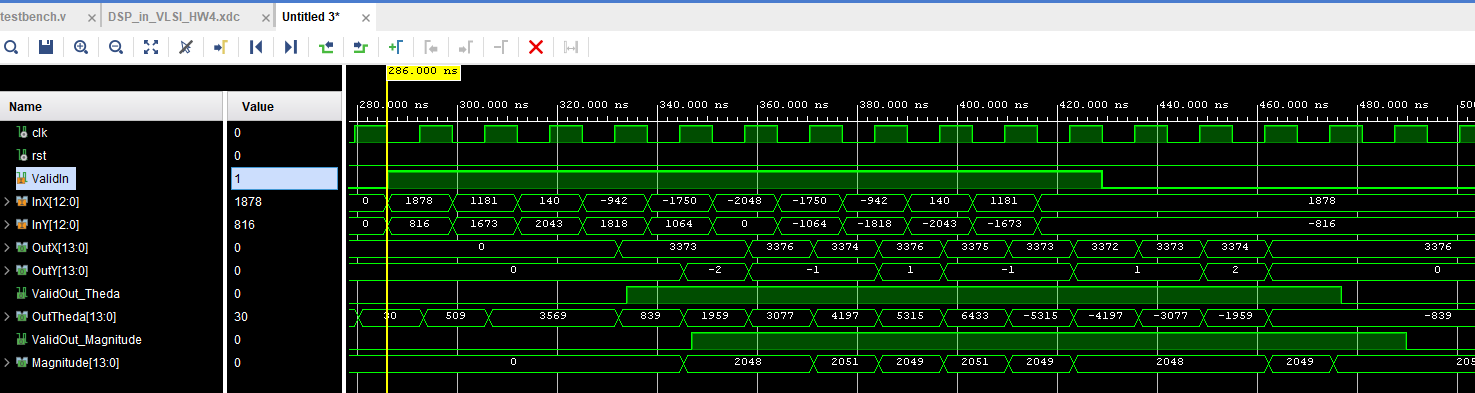


9.3 critical path is from InY to pipeline register.

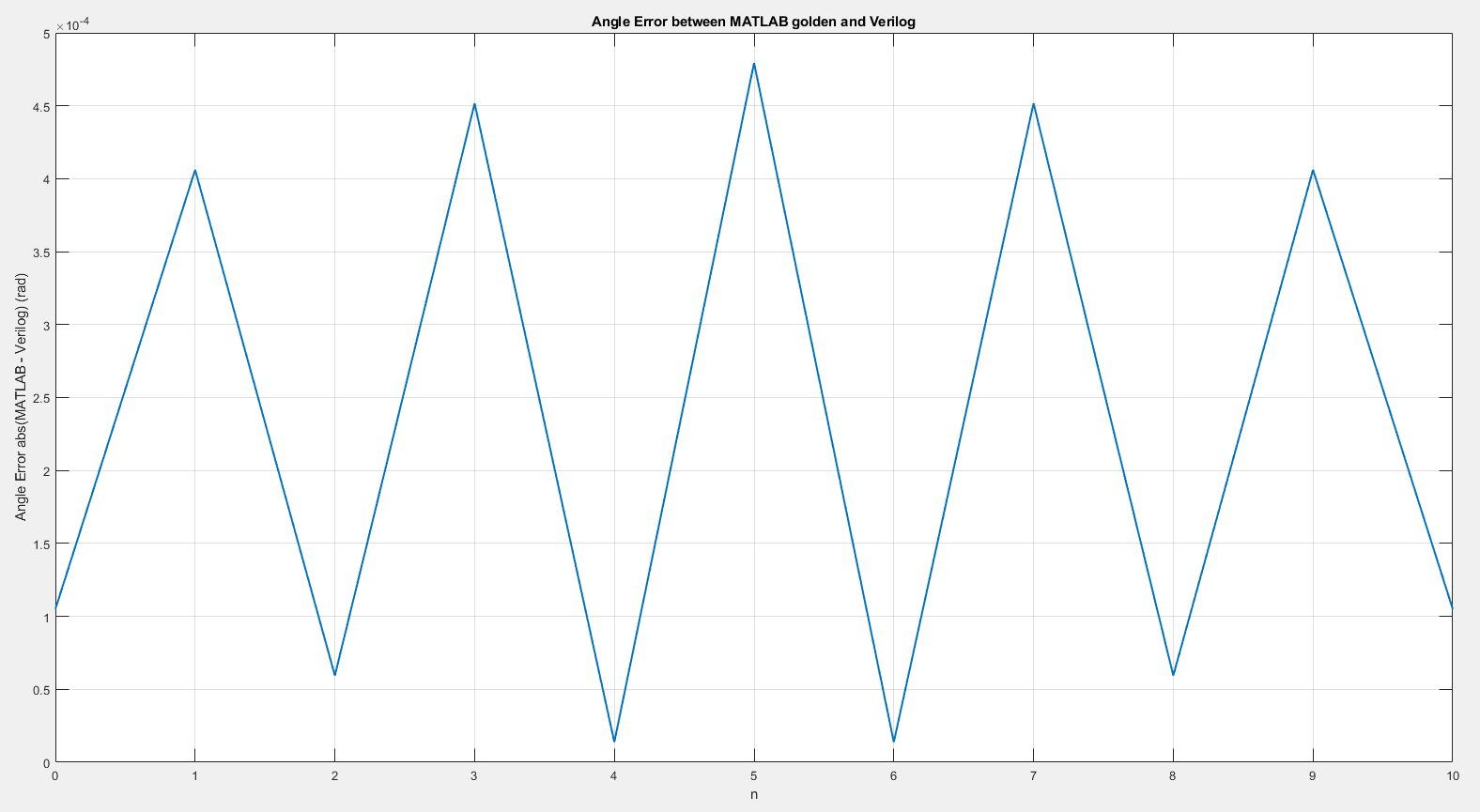


9.4 timing diagram of post-synthesis simulation (clock period = 13ns)

Value of timing diagram is in signed decimal, divided it by 2^11 is true value. (11bit fraction)



9.5 error between the post-synthesis results and the floating-point arctangent results

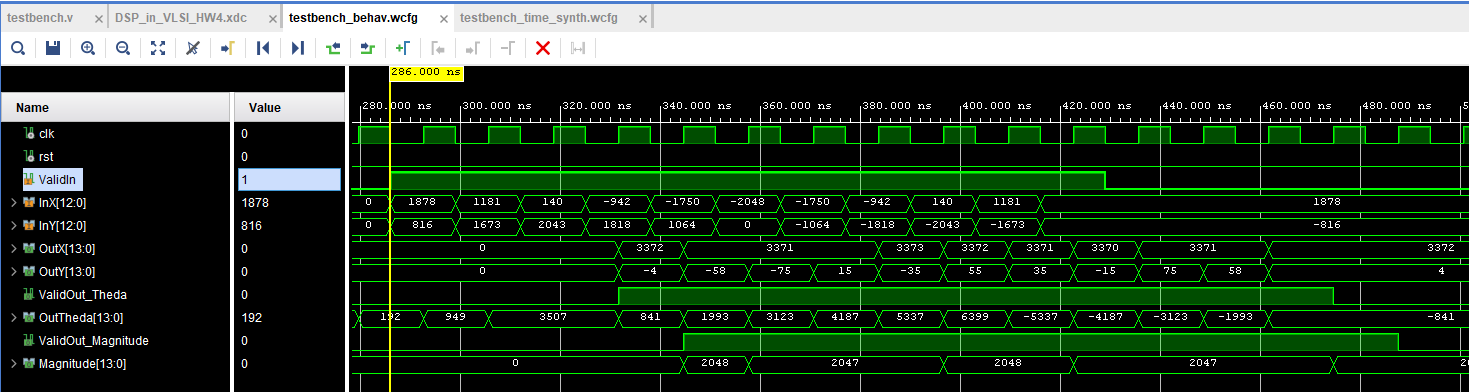


Average angle error meets the requirement 2^-11.



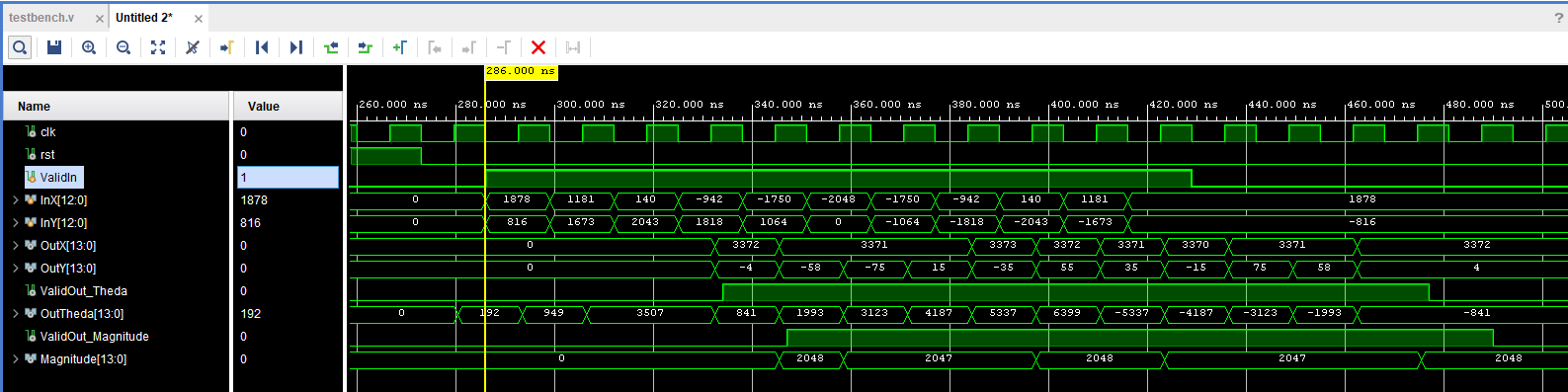
10. (Step 8) Based on the design in Step 7, change it to calculate the magnitude function. Show the timing diagram of behavior simulation and post-synthesis simulation with correct setting of clock period (1/fs). (20%). Verified the error between the post-synthesis results and the floating-point arctangent results. Draw the error versus index 𝑛. (10%) 10.1 timing diagram of behavior simulation (clock period = 13ns)

Value of timing diagram is in signed decimal, divided it by 2^11 is true value. (11bit fraction)

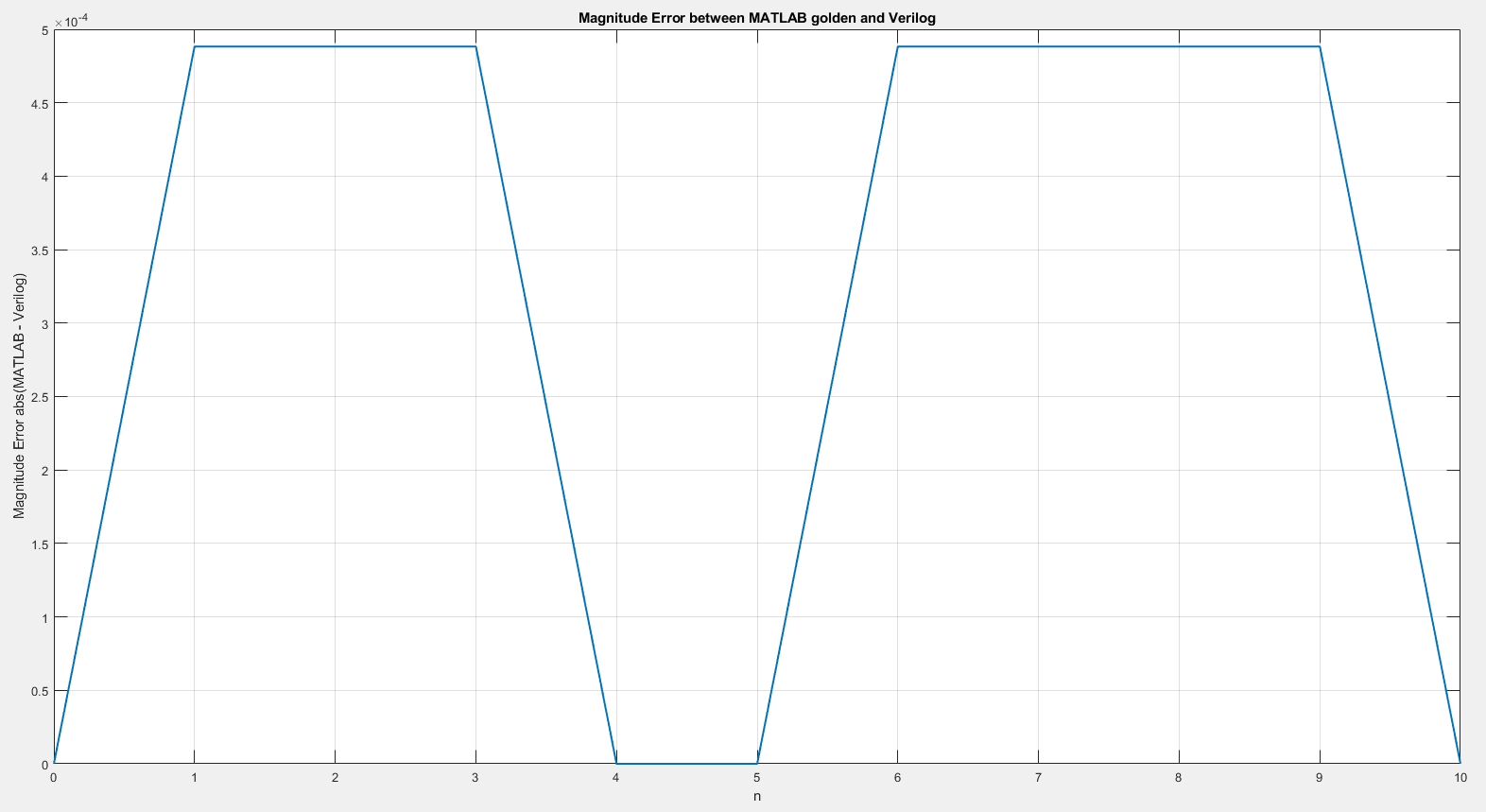


10.2 timing diagram of post-synthesis simulation (clock period = 13ns)

Value of timing diagram is in signed decimal, divided it by 2^11 is true value. (11bit fraction)



10.3 error between the post-synthesis results and the floating-point results



Average magnitude error meets the requirement 0.1%.

