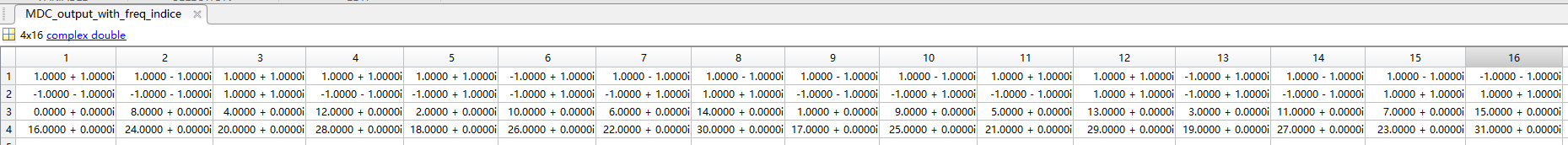
DSP in VLSI

HW5

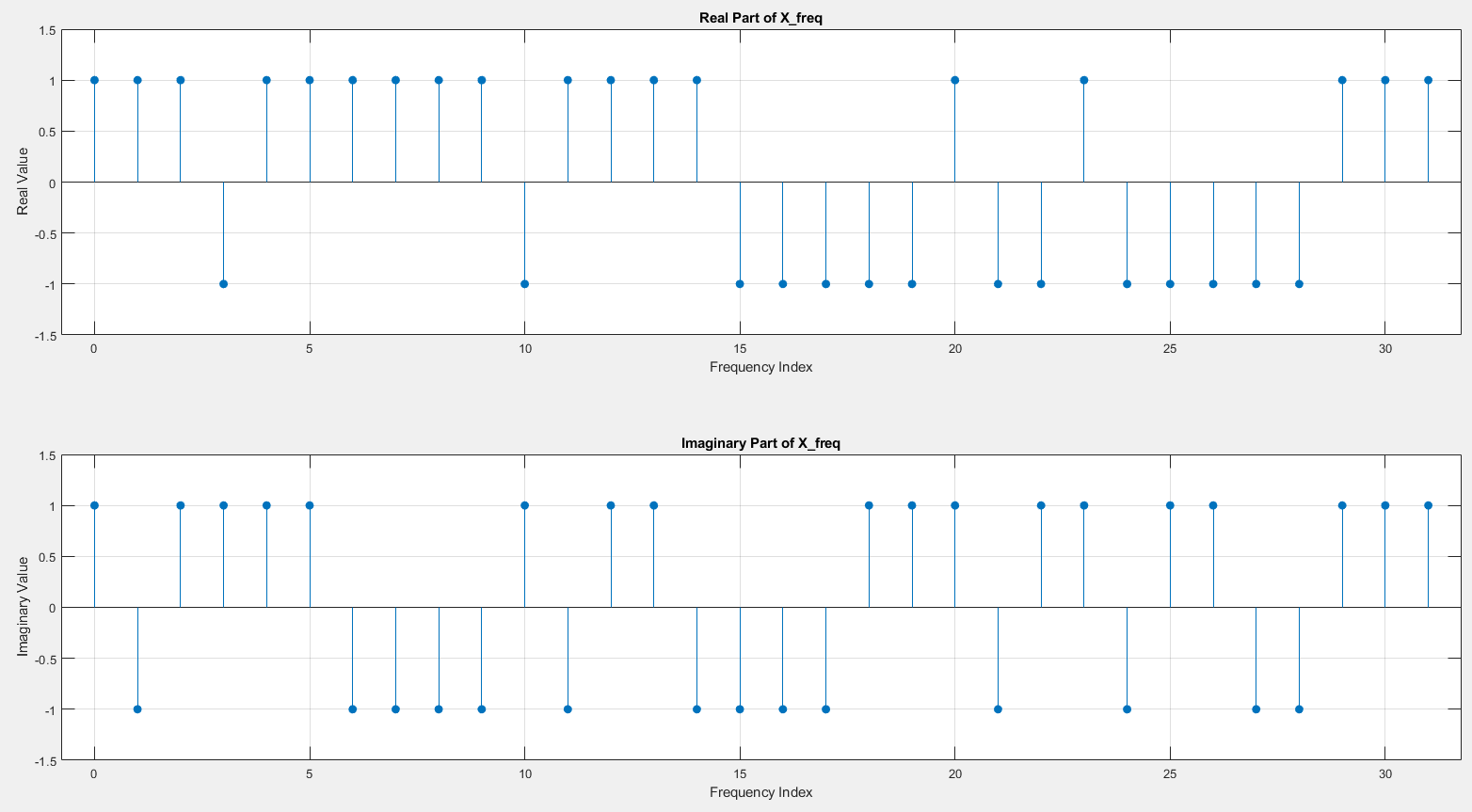
電子所ICS組, R13943015, 張根齊

1. (Step 1) Please use FFTInput32.mat as the inputs. Use your MDC FFT Matlab/Python program to generate the 32 FFT outputs. The program outputs should be in a 2 × 16 array. Because they are in bit-reversed order, write a program to generate their associated frequency domain indices. Now, you have an 4 × 16 array containing the frequency domain indices and the MDC outputs. List the array. (Maybe you can copy the results in Work Space and paste onto your report.) (10%)  
row 1 and row 2 are 32 FFT outputs (complexed number). And row3, row4 are corresponding frequency domain indices. (integer number)

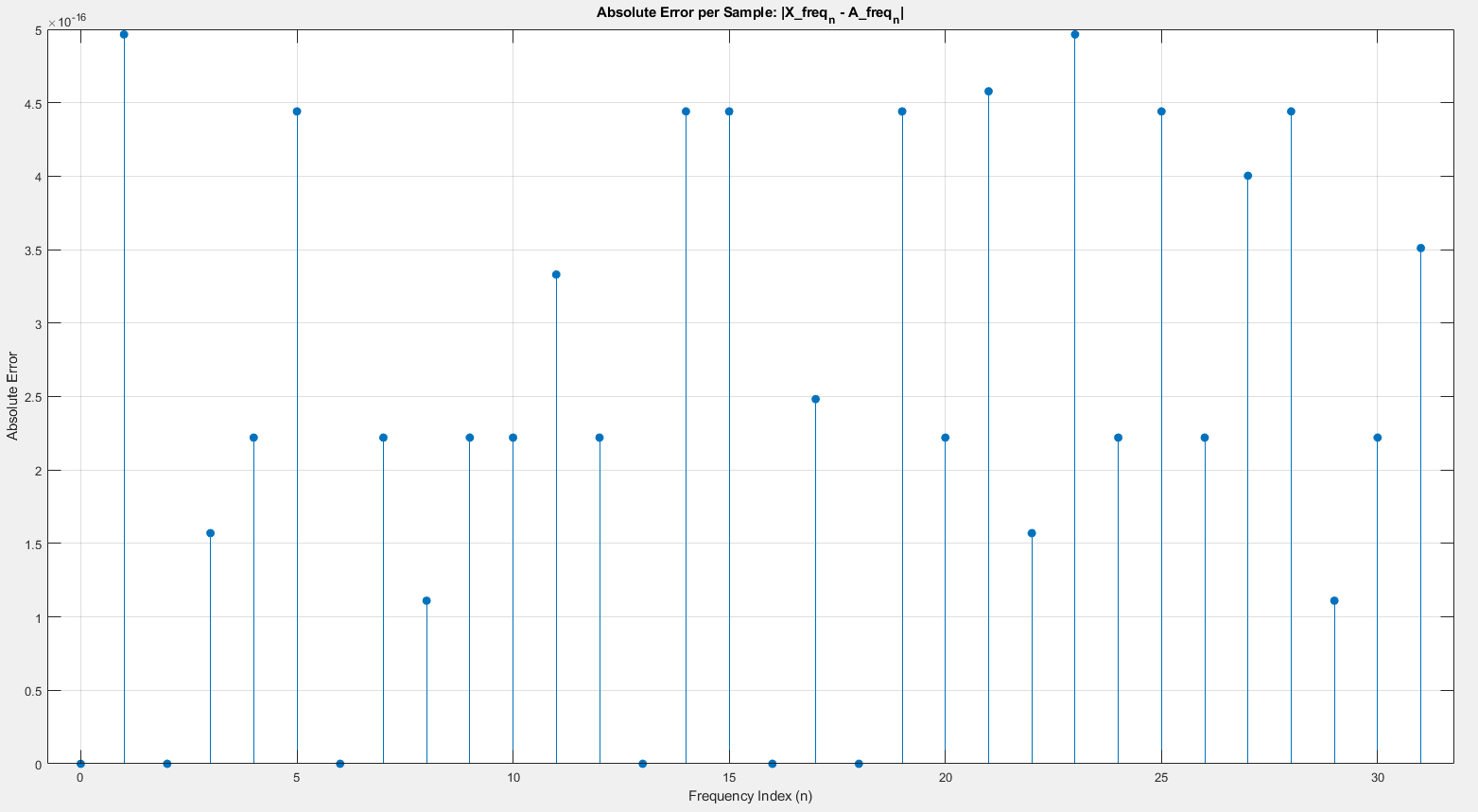


2. (Step 2) Please use FFTInput32.mat as the inputs. Show that your program for output re-ordering is correct. Draw the real part and imaginary part of 𝑋0~𝑋31. (10%) Compare the results of 𝑋0~𝑋31 to A0~A31 . Draw the absolute error of each sample. The error should be small than 10^-10 because of double-precision floating-point operations. If the error is not acceptable, the first 20 points will be deducted, too. (10%)

2.1 Draw the real part and imaginary part of 𝑋0~𝑋31



2.2 Draw the absolute error of each sample



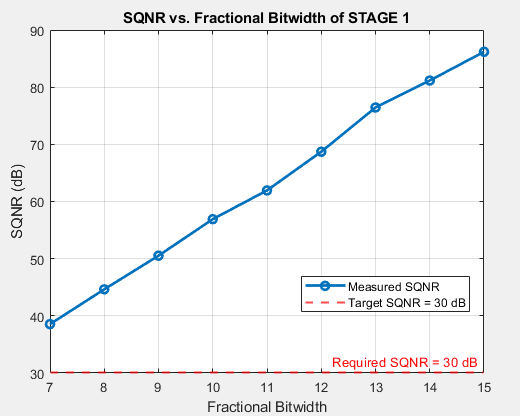
Average error (< 10^-10):



3. (Step 3) Generate your own inputs of 96 samples. Draw the SQNR versus fractional part word-length N stage by stage. (30%)

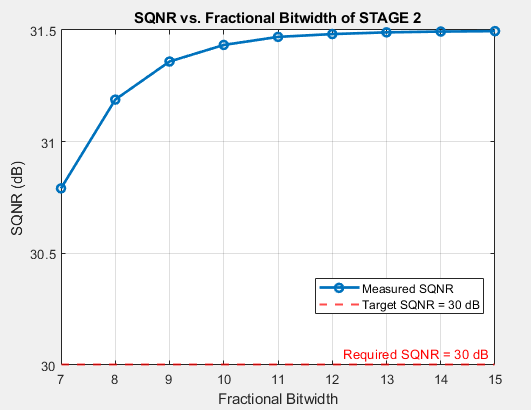
(a) Quantize the first stage. Evaluate the FFT output SQNR versus fractional part word-length N for N=7, 8, 9, 10, …, 13, 14,15 for stage 1. Draw the figure.

Choose stage 1 fractional bit-width = 10 (reserved margin).



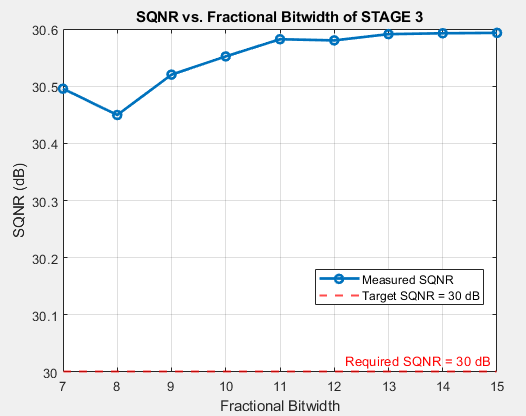
(b) Fix the setting for stage 1. Quantize the second stage. Evaluate the FFT output SQNR versus fractional part word-length N for N=7, 8, 9, 10,…, 13, 14,15 for stage 2. Draw the figure.

Choose stage 2 fractional bit-width = 10 (reserved margin):



(c) Fix the setting for stage 1 and 2. Quantize the third stage. Evaluate the FFT output SQNR versus fractional part word-length N for N=7, 8, 9, 10,…, 13,14,15 for stage 3 and so on. Draw the figure

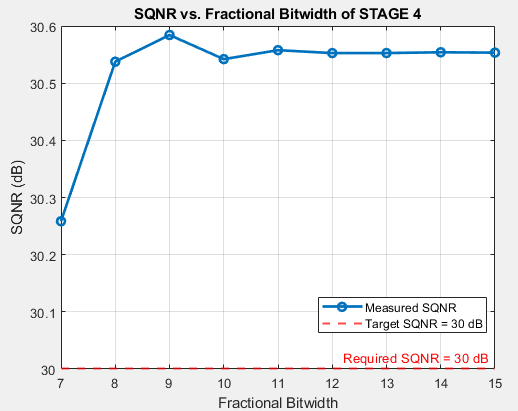
Choose stage 3 fractional bit-width = 10 (reserved margin):



(d) Repeat until stage 5. So, you have five figures.

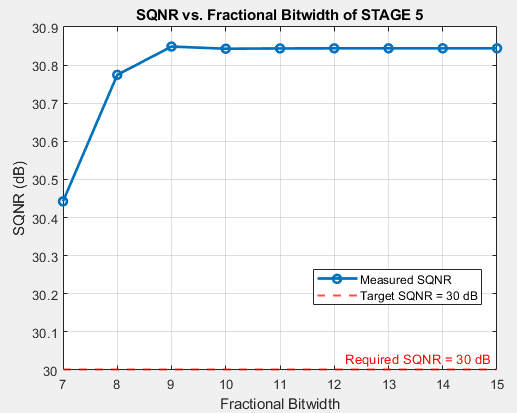
d-1: stage 4:

Choose stage 4 fractional bit-width = 10 (reserved margin):



d-2: stage 5:

Choose stage 5 fractional bit-width = 10 (reserved margin):



(e) Then, decide the fractional part word-length for twiddle factors of all the stages. Draw the FFT output SQNR versus fractional part word-length of twiddle factors.

Choose twiddle factors fractional bit-width = 10:

