CSE 2301 Final Exam Review

Fall 2021

1. Convert the decimal number -31.415 to IEEE 754 format with 8 bits of precision

   31 converted to binary is 11111

   0.415 in binary is approximately 0.0110

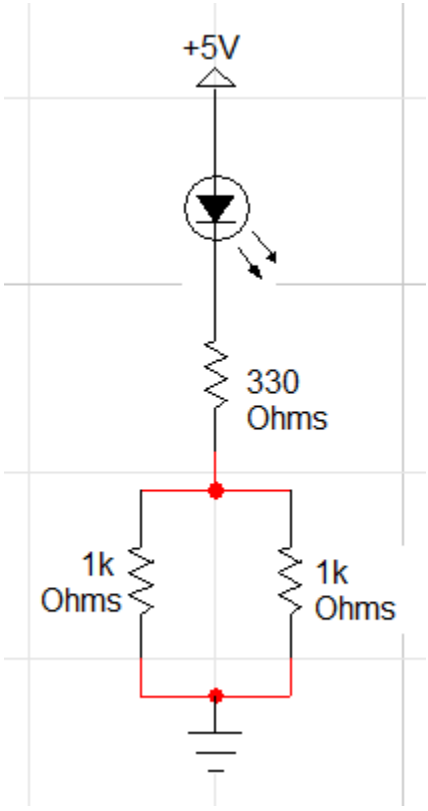
   Therefore, 31.415 is approximately 11111.0110 = 1.11110110 * 2^4

   The exponent is 4 however there is a 127-bias applied to yield 131 in decimal which is 10000011.

   Since we are interested in the negative number, we use a 1 for the sign bit to get the following result:

   11000001111110110…

2. Find the current flowing through the LED in the following circuit assuming that when the LED is on, there is 2V across it.



Since the anode of the LED is more positive than the cathode, we will assume that the LED is on and there is 2V across it from cathode to anode.

Therefore, we have 5V-2V=3V across the resistive network.

The resistors in parallel equate to 500 Ohms and are in series with the 330 Ohm resistor. Therefore, the total resistance of the network is 330 + 500 = 830 Ohms.

Using Ohms Law, I=V/R and the current flowing through the LED is 3.6mA

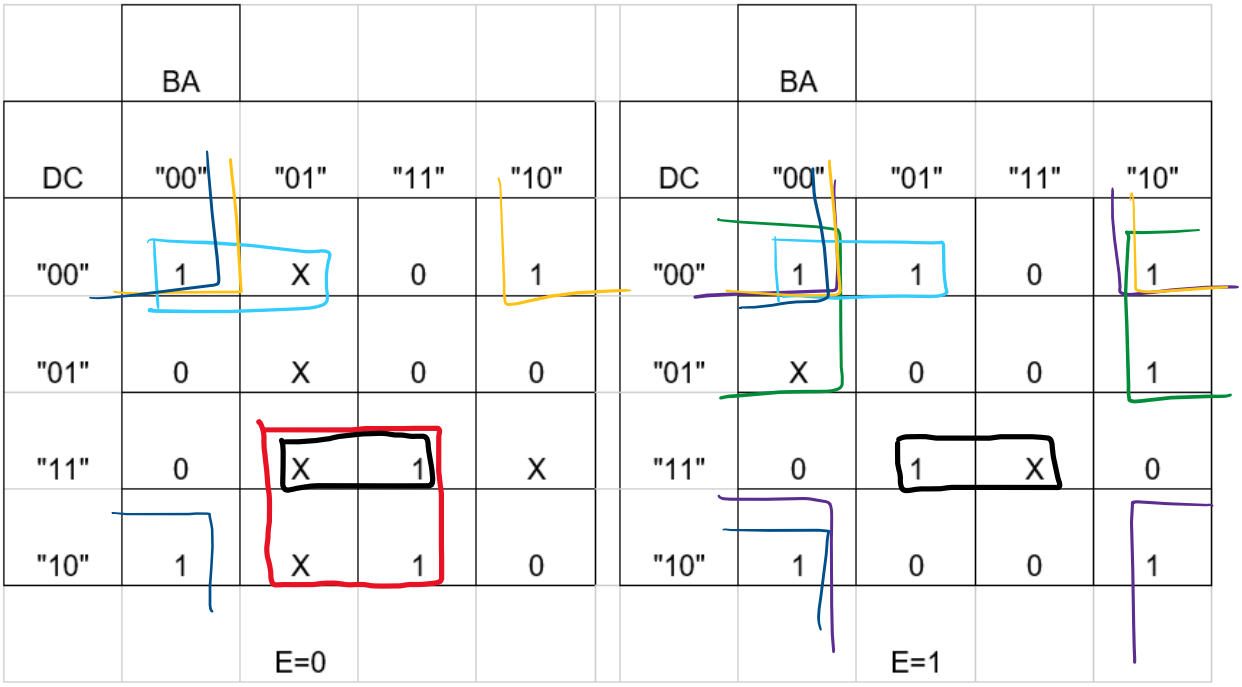
3. The number 01000010 is represented in BCD. Compute the negative version in 8-bit two's complement.

   Since the number is given in BCD, we first need to convert it to standard binary.

   We can recognize that this number is 42 in decimal and its binary equivalent is 00101010.

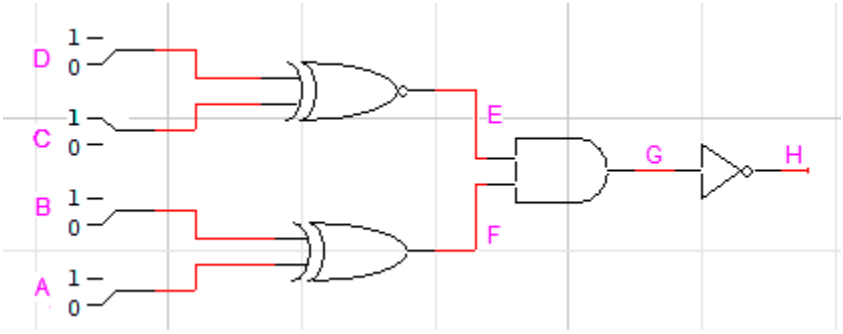
   Inverting the bits and adding 1, we obtain 11010110.

4. Compute the following operations in 4-bit binary. Ignore overflow.
   a. 1000 – 0011 = 0101
   b. 1011 + 1101 = 1000
   c. 0101 * 0100 = 0100
   d. 0101 / 0100 = 0001
5. The function *F* is defined by the sum of minterms
   ∑m(0, 2, 8, 11, 15, 16, 17, 18, 22, 24, 26, 29) and maxterms
   ∑m(3, 4, 6, 7, 10, 12, 19, 21, 23, 25, 27, 28, 30) where the rest of the terms are don't care states. Construct a K-map of this function and determine its minimized equation (Use EDCBA as inputs).

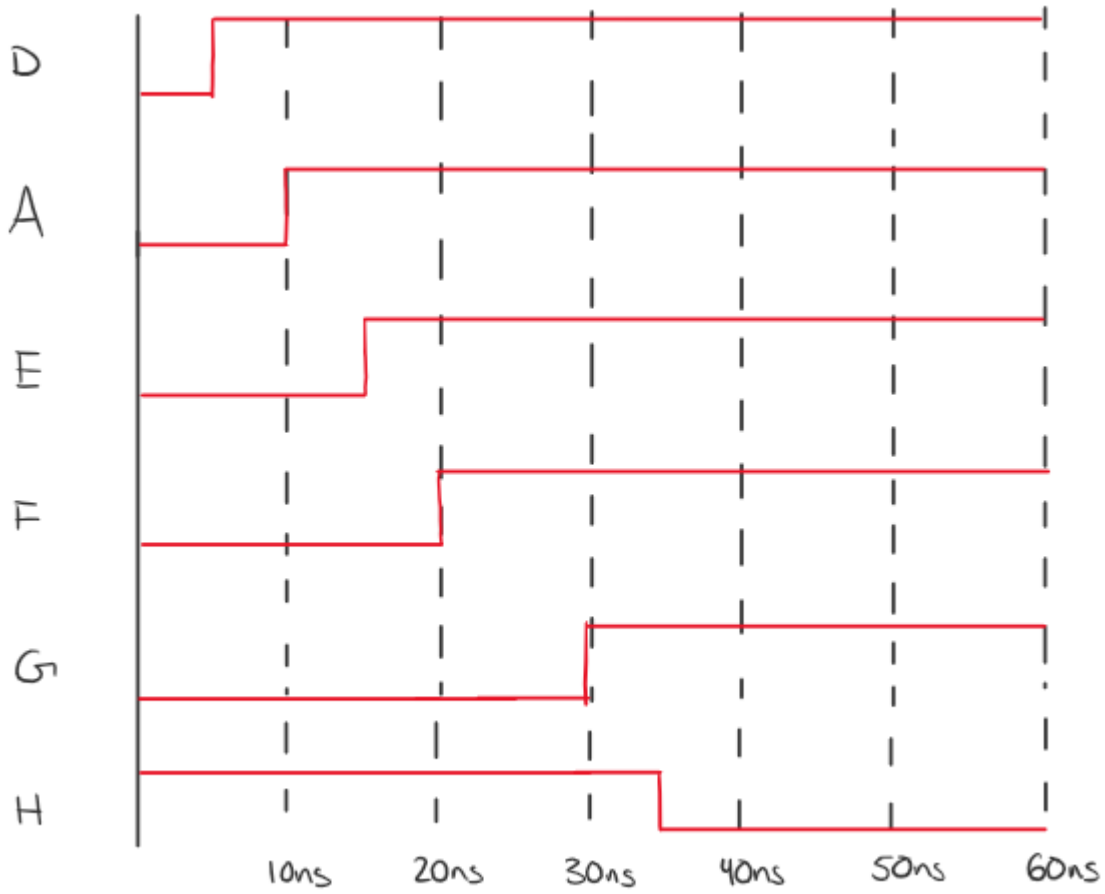


F = E'DA + DCA + C'B'A' + D'C'A' + D'C'B' + ED'A' + EC'A'

6. Consider the combinational logic circuit shown below



Draw a timing diagram where the input D changes to a 1 at t = 5ns and A changes to a 1 at t = 10ns. Assume that each gate has a propagation delay of 10ns except the NOT gate which has a delay of 5ns.

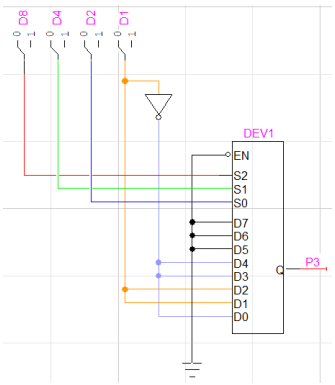


7. Complete the hamming code for the numbers 1 through 9 with odd parity

	P1	P2	D8	P3	D4	D2	D1
0	1	1	0	1	0	0	0
1	0	0	0	0	0	0	1
2	1	0	0	0	0	1	0
3	0	1	0	1	0	1	1
4	0	1	0	0	1	0	0
5	1	0	0	1	1	0	1
6	0	0	0	1	1	1	0
7	1	1	0	0	1	1	1
8	0	0	1	1	0	0	0
9	1	1	1	0	0	0	1

8. Using the table in the previous problem, implement the *P3* function for inputs *D8 D4 D2 D1* (only values 0 through 9) using an 8-1 MUX and draw the schematic. First start out by drawing the truth table. For don't care inputs, tie them to ground.

D8	D4	D2	D1	P3	Input
0	0	0	0	1	D1'
0	0	0	1	0	
0	0	1	0	0	D1
0	0	1	1	1	
0	1	0	0	0	D1
0	1	0	1	1	
0	1	1	0	1	D1'
0	1	1	1	0	
1	0	0	0	1	D1'
1	0	0	1	0	
1	0	1	0	X	X = 0
1	0	1	1	X	
1	1	0	0	X	X = 0
1	1	0	1	X	
1	1	1	0	X	X = 0
1	1	1	1	X	



9. Write the VHDL code for the problem above

```
if D8='0' and D4='0' and D2='0' then P3<=not D1
if D8='0' and D4='0' and D2='1' then P3<=D1
if D8='0' and D4='1' and D2='0' then P3<=D1
if D8='0' and D4='1' and D2='1' then P3<=not D1
if D8='1' and D4='0' and D2='0' then P3<=not D1
if D8='1' and D4='0' and D2='1' then P3<=0
if D8='1' and D4='1' and D2='0' then P3<=0
if D8='1' and D4='1' and D2='1' then P3<=0
```

10. Show all steps for multiplying 1010 (Multiplicand) and 0101 (Multiplier) using sequential multiplication. Do addition and shift operations in separate steps

Register A (Multiplicand)			
1	0	1	0

Step	C	Register B (Product)				Register Q (Multiplier)			
0	0	0	0	0	0	0	1	0	1
1	0	1	0	1	0	0	1	0	1
2	0	0	1	0	1	0	0	1	0
3	0	0	1	0	1	0	0	1	0
4	0	0	0	1	0	1	0	0	1
5	0	1	1	0	0	1	0	0	1
6	0	0	1	1	0	0	1	0	0
7	0	0	1	1	0	0	1	0	0
8	0	0	0	1	1	0	0	1	0

11. Write the truth tables for the following flip flops

a. J-K Flip Flop (and excitation/transition table)

J	K	Q0	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Q0	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

b. D Flip Flop

D	Q0	Q+
0	0	0
0	1	0
1	0	1
1	1	1

c. T Flip Fop

T	Q0	Q+
0	0	0
0	1	1
1	0	1
1	1	0

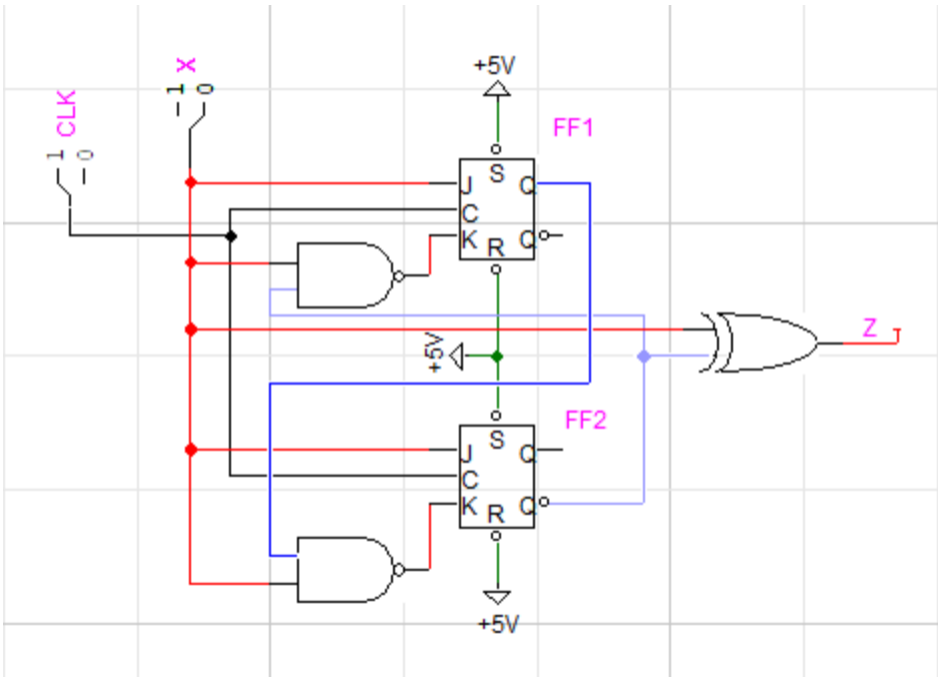
d. SR Flip Flop (and excitation/transition table)

S	R	Q0	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1

1	0	1	1
1	1	0	X
1	1	1	X

Q0	Q+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

12. Given the sequential circuit shown below, draw the state diagram.



a. Find equations for J1 K1 J2 K2 and Z

J1 = X

K1 = (X.Q2')'

J2 = X

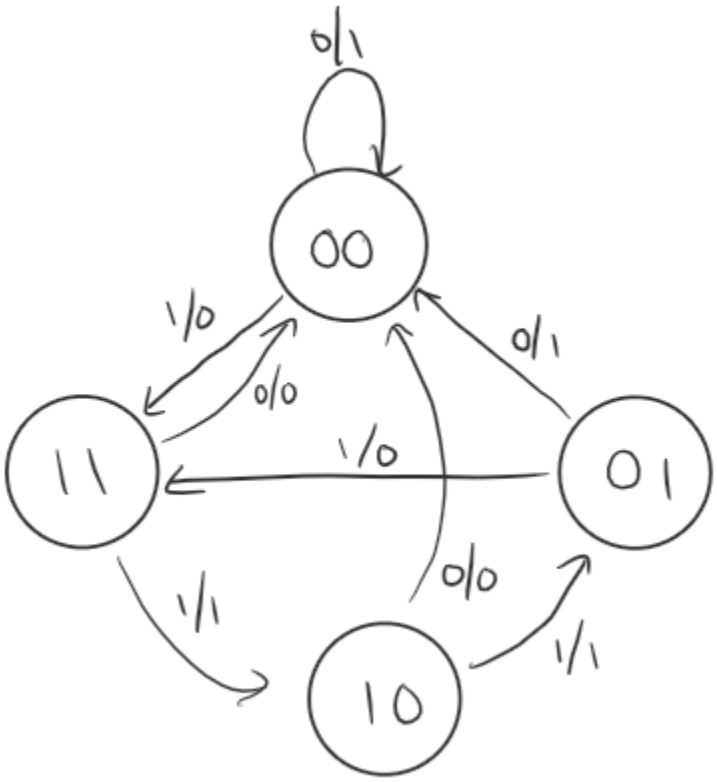
K2 = (X.Q1)'

Z = X xor Q2'

b. Fill out the transition table

Present State		Input	FF1		FF2		Future State		Output
Q2	Q1	X	J1	K1	J2	K2	Q2+	Q1+	Z
0	0	0	0	1	0	1	0	0	1
0	0	1	1	0	1	1	1	1	0
0	1	0	0	1	0	1	0	0	1
0	1	1	1	0	1	0	1	1	0
1	0	0	0	1	0	1	0	0	0
1	0	1	1	1	1	1	0	1	1
1	1	0	0	1	0	1	0	0	0
1	1	1	1	1	1	0	1	0	1

c. Draw the state diagram based on the transition table

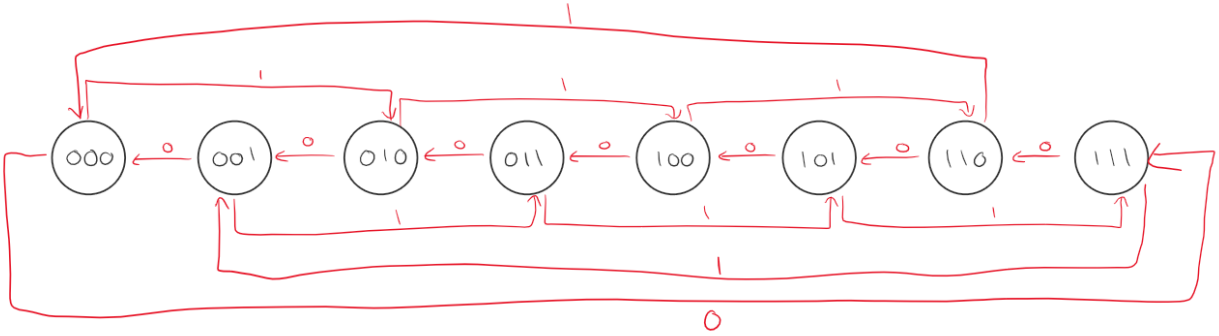


13. (Long) Design Problem: Design a counter using J-K flip flops that counts up by two when input A is a 1, and decrements by 1 when A is a 0. The counter should have a maximum value of 7.

    If A is a 1, we should see the sequence 0-2-4-6-0-2-4-6… or 1-3-5-7-1-3-5-7… Depending on if the initial state is odd or even.

    If A is a 0, we should see the sequence 7-6-5-4-3-2-1-0-7-6-5-4-3-2-1-0…

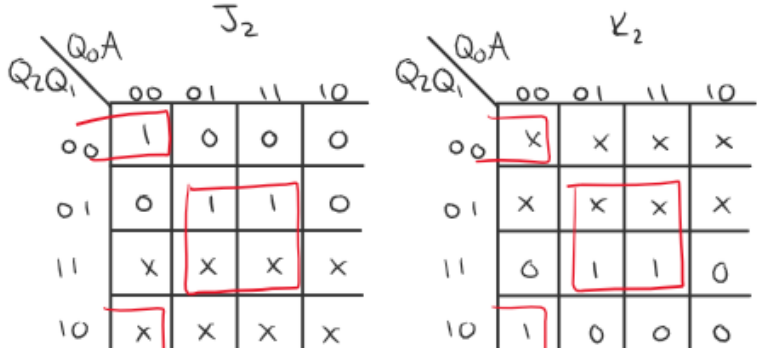
a. Draw the state diagram that models the circuit

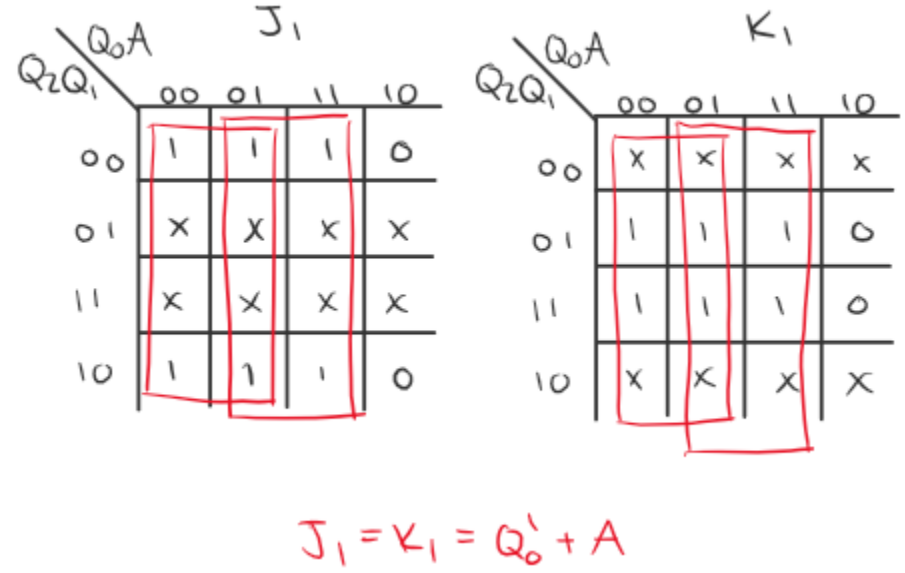


b. Fill out the transition table

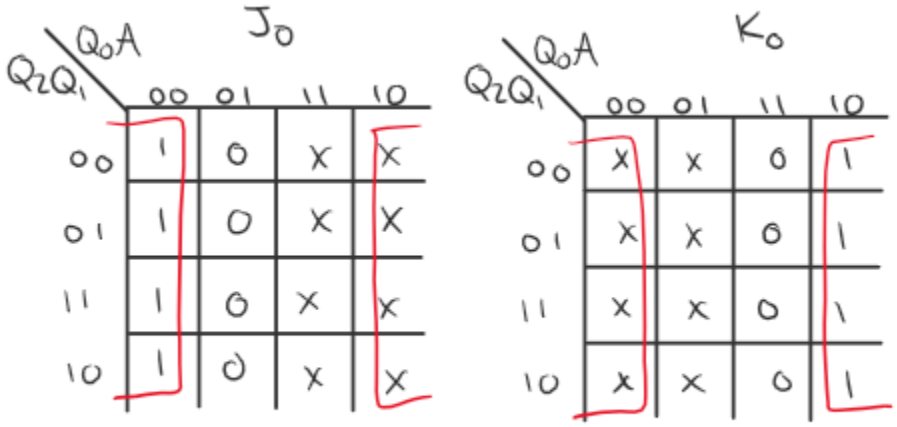
Q2	Q1	Q0	A	Q2+	Q1+	Q0+	J2	K2	J1	K1	J0	K0
0	0	0	0	1	1	1	1	X	1	X	1	X
0	0	0	1	0	1	0	0	X	1	X	0	X
0	0	1	0	0	0	0	0	X	0	X	X	1
0	0	1	1	0	1	1	0	X	1	X	X	0
0	1	0	0	0	0	1	0	X	X	1	1	X
0	1	0	1	1	0	0	1	X	X	1	0	X
0	1	1	0	0	1	0	0	X	X	0	X	1
0	1	1	1	1	0	1	1	X	X	1	X	0
1	0	0	0	0	1	1	X	1	1	X	1	X
1	0	0	1	1	1	0	X	0	1	X	0	X
1	0	1	0	1	0	0	X	0	0	X	X	1
1	0	1	1	1	1	1	X	0	1	X	X	0
1	1	0	0	1	0	1	X	0	X	1	1	X
1	1	0	1	0	0	0	X	1	X	1	0	X
1	1	1	0	1	1	0	X	0	X	0	X	1
1	1	1	1	0	0	1	X	1	X	1	X	0

c. Draw the K-maps and find equations for the flip flop inputs





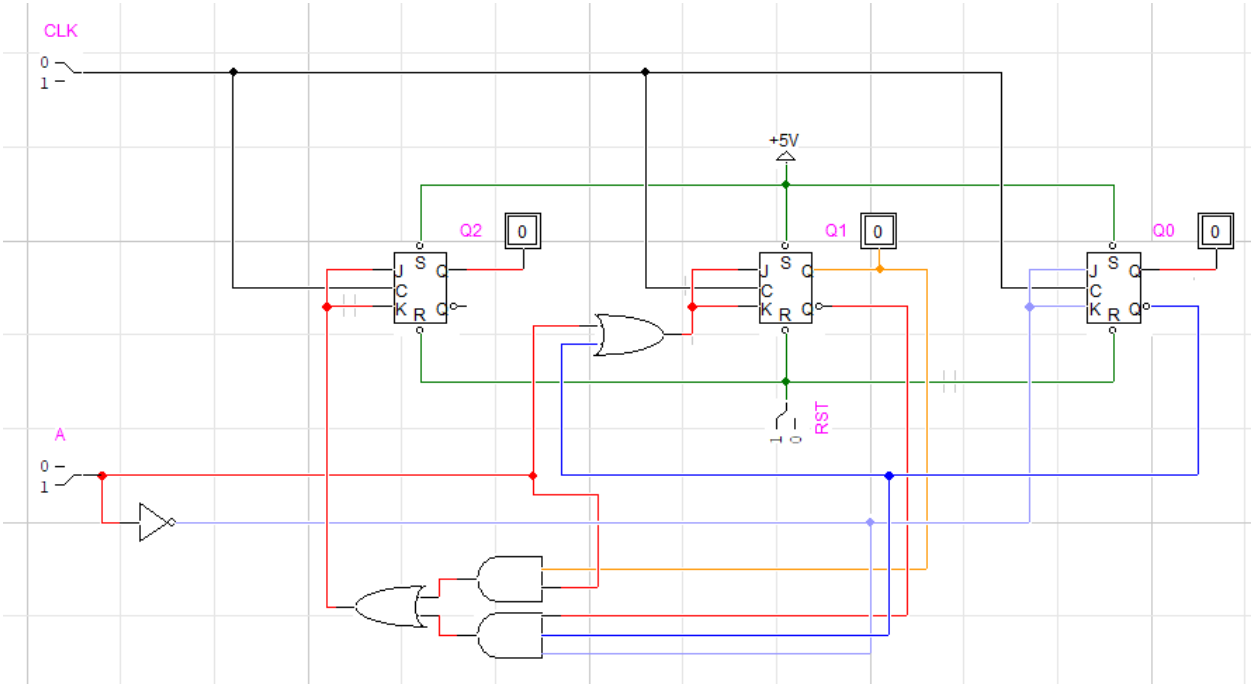
$$J_1 = K_1 = Q_0' + A$$



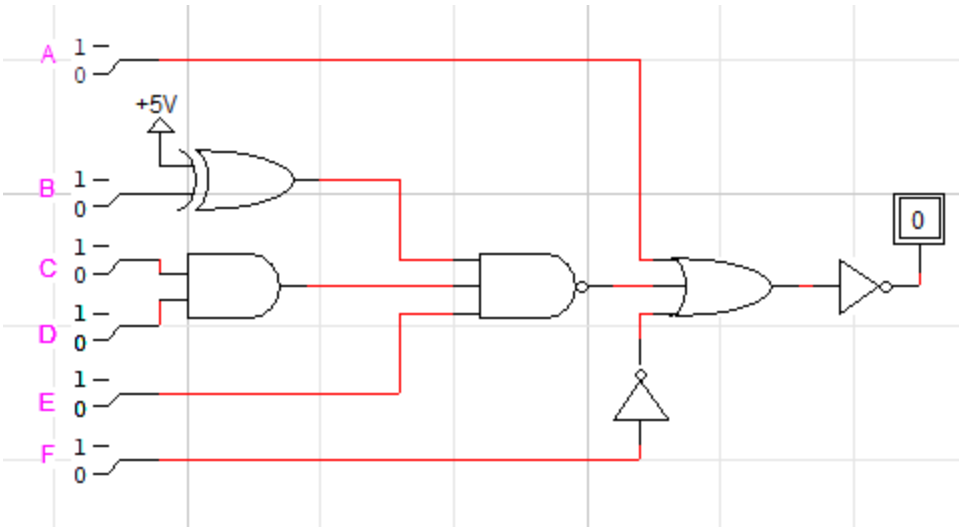
$$J_0 = K_0 = A'$$

Since J_n = K_n, we could easily implement the counter using T flip flops

d. Draw the final schematic of the counter



14. For the following circuit shown below, change the inputs *A B C E F* such that when we see a change in the output when we change the input *D*.

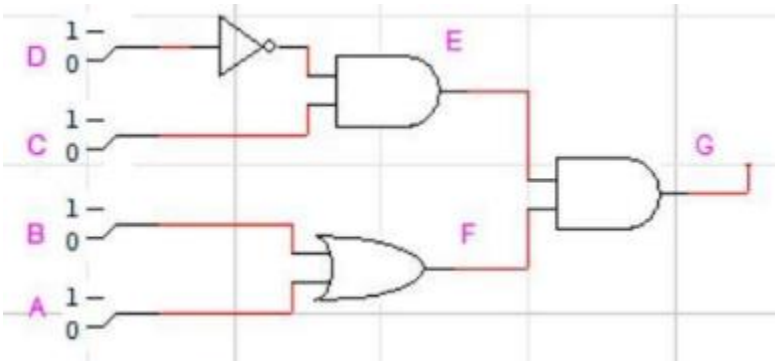


A = 0, B = 0, C = 1, E = 1, F = 1

15. Given the following code, draw the corresponding schematic

```
signal E std_logic;
signal F std_logic;

E<=C and not D;
F<=B or A;
G<=E and F;
```



16. We want to sample an audio wave that has a bandwidth of 10kHz. What frequency should we sample at to retain its quality? What is this criteria known as?

We should sample at twice the maximum frequency present in the input signal. Therefore, we should sample at approximately 20kHz as per the Nyquist Criterion.

17. Compare and contrast the Resistor String, Binary Weighted Resistor, and R/2R "ladder" DACs.

    Resistor string DAC – Simple and fast for less than 8 bits. Requires large number of resistors (2^n) and switches.

    Binary weighted resistor DAC – Simple and fast. Needs large range of resistor values. Needs very small switch resistance

    R/2R "ladder" DAC – Needs two precise values of R. Easy to manufacture. Fast response. Confusing analysis

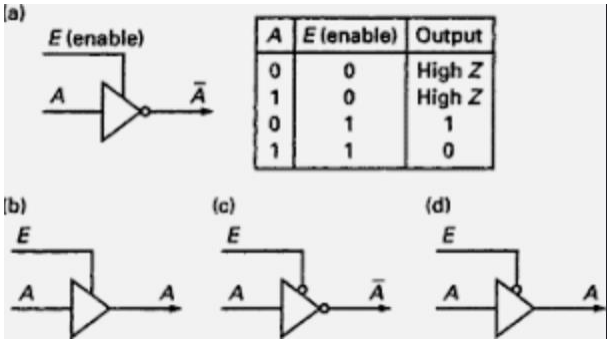
Rapid Fire Questions (Courtesy of Matt Piotrowski)

1. What do all the following acronyms stand for: TTL, SSI, MSI, LSI, VLSI, ULSI, PCB, RAID, EPROM, EEPROM, ALU, ADC, DAC, CRC, PLA, ASIC, FPGA, PRBS, MSB, LSB, NRZ, ROM, ASCII, VHDL
   Transistor-Transistor Logic, Small-Scale Integration, Medium-Scale Integration, Very Large Scale Integration, Ultra Large Scale Integration, Printed Circuit Board, Random Array of Independent Disks, Erasable Programmable Read-Only Memory, Electronically Erasable Programmable Read-Only Memory, Arithmetic Logic Unit, Analog to Digital Converter, Digital to Analog Converter, Cyclic Redundancy Check, Programmable Logic Array, Application-Specific Integrated Circuit, Field Programmable Gate Array, Pseudo-Random Binary Sequence, Most Significant Bit, Least Significant Bit, Non-return-to-Zero, Read-Only Memory, American Standard Code for Information Interchange, Very High Speed Integrated Circuit Hardware Description Language
2. How many bits are in a byte? 8
3. What does 4k mean? 4096
4. Truth table for an AND gate

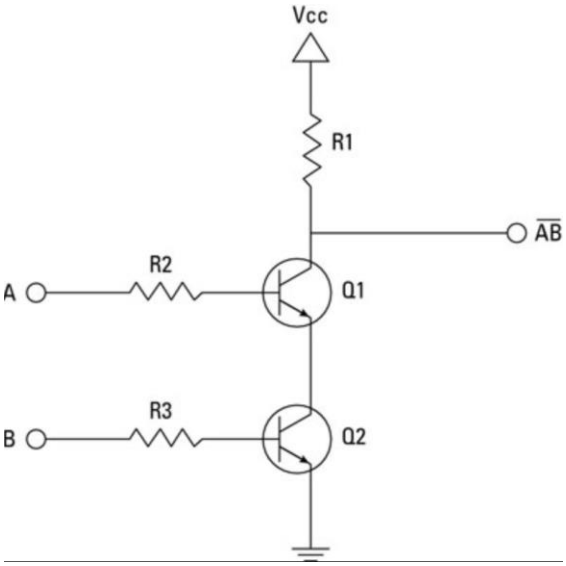
A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

5. What is DeMorgan's Law? (A.B)' = A'+B' (A+B)' = A'.B'

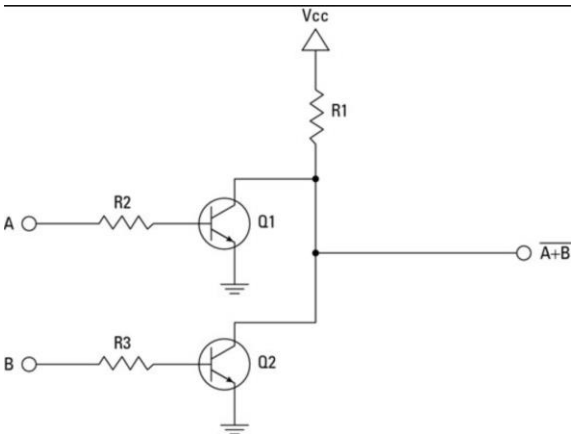
6. What is 7 in binary? 111
7. What is two's complement? A way to represent positive/negative numbers in binary and conform to standard mathematical operations.
8. What is the radix of hexadecimal? 16
9. What does the first bit in a FLOP represent? Sign
10. What is the difference between unipolar NRZ and unipolar RTZ? Non-Return to Zero vs Return to Zero
11. What do VCC, GND, and EN represent on a chip? Power, Ground, and Enable
12. Draw the 4 different three state gates?



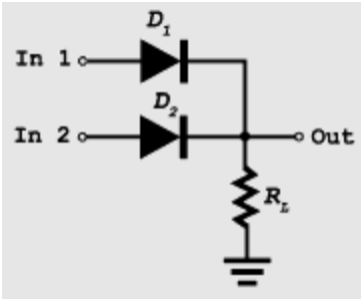
13. How is postal bar code weighted? How many 1's do you need in a valid sequence? 74210 You need two 1's for a valid POSTNET code
14. What is hamming distance? Number of bit differences between two binary numbers
15. How would you write a clock signal in VHDL? CLK <= not CLK after 10ns
16. What is the equation for Q(t+) for a JK Flip Flop? Q(t+) = JQ' + K'Q
17. Draw a NAND gate with transistors



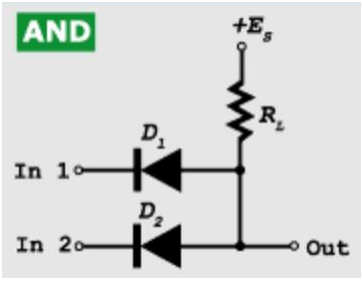
18. Draw a NOR gate with transistors



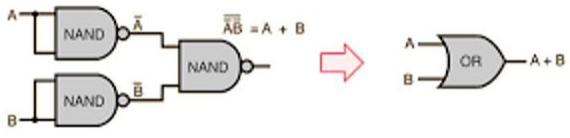
19. Draw an OR gate with diodes



20. Draw an AND gate with diodes



21. What is fan in? Number of input gates that can be connected without degraded performance
22. How do you multiply 0001 by 4? Shift left twice
23. What is the range of voltages that define a 0 and a 1 for a TTL gate? 0-0.8V and 2-5V
24. What condition creates an overflow for two's complement numbers? When the sign bits of the inputs are the same but differ from that of the output sign.
25. Draw an OR gate using NANDs only?



26. What is Ohm's Law? V=IR

27. What is quantization? Mapping a continuous (analog) signal to a set of discrete (digital) values.
28. What is volatile memory? Requires power to maintain data
29. What is the dynamic range of a signal? Ratio between the largest and smallest value that a signal produces.
30. What is an ADC and DAC? ADC is a converter that transforms a continuous analog signal to discrete digital levels. A DAC is a converter to convert discrete digital numbers into an analog equivalent.