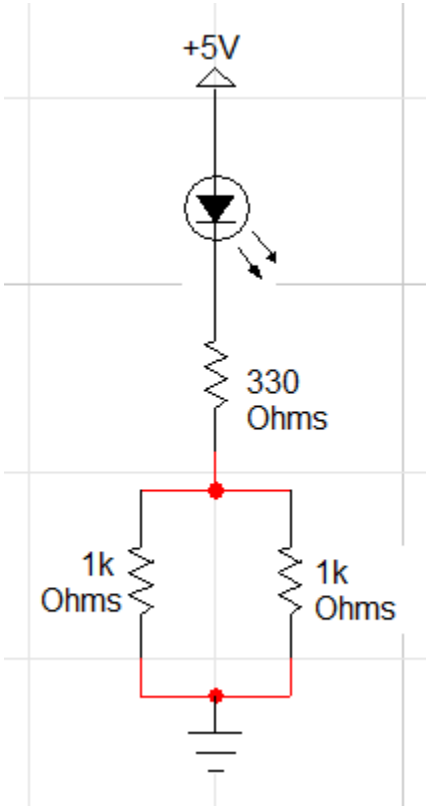
CSE 2301 Final Exam Review

Fall 2021

1. Convert the decimal number -31.415 to IEEE 754 format with 8 bits of precision

2. Find the current flowing through the LED in the following circuit assuming that when the LED is on, there is 2V across it.

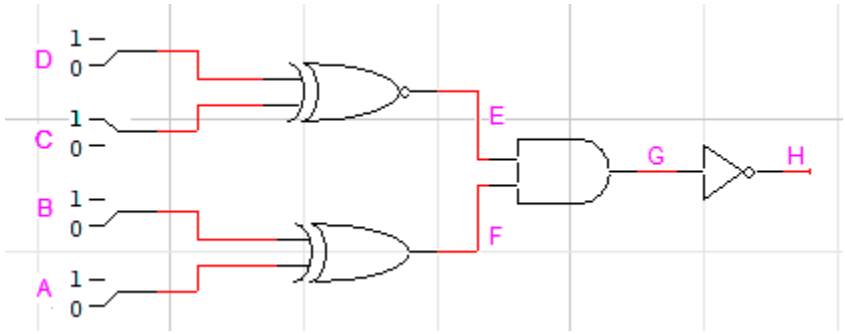


3. The number 01000010 is represented in BCD. Compute the negative version in 8-bit two's complement.

4. Compute the following operations in 4-bit binary. Ignore overflow.
    a. 1000 – 0011
    b. 1011 + 1101
    c. 0101 * 0100
    d. 0101 / 0100

5. The function *F* is defined by the sum of minterms
   ∑m(0, 2, 8, 11, 15, 16, 17, 18, 22, 24, 26, 29) and maxterms
   ∑m(3, 4, 6, 7, 10, 12, 19, 21, 23, 25, 27, 28, 30) where the rest of the terms are don't care states. Construct a K-map of this function and determine its minimized equation (Use EDCBA as inputs).

6. Consider the combinational logic circuit shown below



Draw a timing diagram where the input D changes to a 1 at t = 5ns and A changes to a 1 at t = 10ns. Assume that each gate has a propagation delay of 10ns except the NOT gate which has a delay of 5ns.

7. Complete the hamming code for the numbers 1 through 9 with odd parity

	P1	P2	D8	P3	D4	D2	D1
0			0		0	0	0
1			0		0	0	1
2			0		0	1	0
3			0		0	1	1
4			0		1	0	0
5			0		1	0	1
6			0		1	1	0
7			0		1	1	1
8			1		0	0	0
9			1		0	0	1

8. Using the table in the previous problem, implement the *P3* function for inputs *D8 D4 D2 D1* (only values 0 through 9) using an 8-1 MUX and draw the schematic. First start out by drawing the truth table. For don’t care inputs, tie them to ground.

<table>
<tr><th>D8</th><th>D4</th><th>D2</th><th>D1</th><th>P3</th><th>MUX</th></tr>
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9. Write the VHDL code of the MUX for the problem above

10. Show all steps for multiplying 1010 (Multiplicand) and 0101 (Multiplier) using sequential multiplication. Do addition and shift operations in separate steps

Register A (Multiplicand)			

Step	C	Register B (Product)				Register Q (Multiplier)			
0									
1									
2									
3									
4									

5									
6									

11. Write the truth tables for the following flip flops
    a. J-K Flip Flop (and excitation/transition table)

J	K	Q0	Q+

Q0	Q+	J	K

    b. D Flip Flop

D	Q0	Q+

    c. T Flip Fop

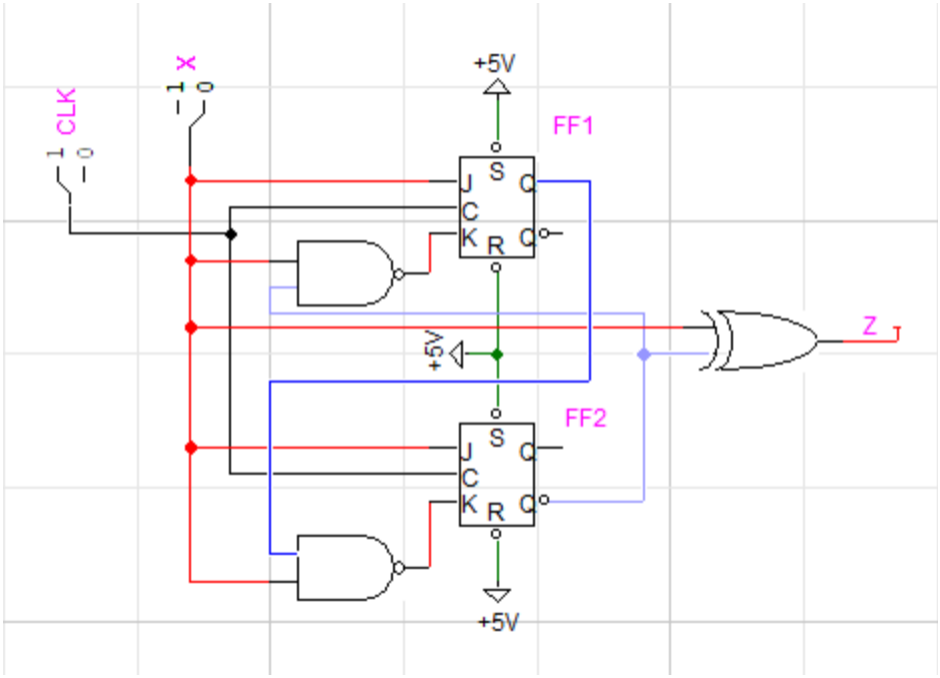
T	Q0	Q+

    d. SR Flip Flop (and excitation/transition table)

S	R	Q0	Q+

Q0	Q+	S	R

12. Given the sequential circuit shown below, draw the state diagram.



a. Find equations for J1 K1 J2 K2 and Z

b. Fill out the transition table

Present State		Input	FF1		FF2		Future State		Output
Q2	Q1	X	J1	K1	J2	K2	Q2+	Q1+	Z

c. Draw the state diagram based on the transition table

13. (Long) Design Problem: Design a counter using J-K flip flops that counts up by two when input A is a 1, and decrements by 1 when A is a 0. The counter should have a maximum value of 7.

    If A is a 1, we should see the sequence 0-2-4-6-0-2-4-6… or 1-3-5-7-1-3-5-7… Depending on if the initial state is odd or even.

    If A is a 0, we should see the sequence 7-6-5-4-3-2-1-0-7-6-5-4-3-2-1-0…

a. Draw the state diagram that models the circuit

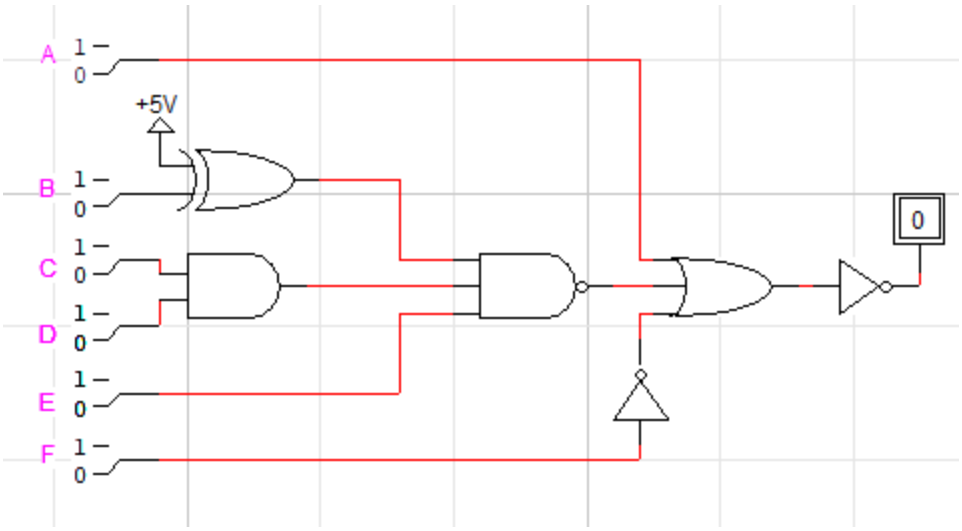
b. Fill out the transition table

Q2	Q1	Q0	A	Q2+	Q1+	Q0+	J2	K2	J1	K1	J0	K0

c. Draw the K-maps and find equations for the flip flop inputs

d. Draw the final schematic of the counter

14. For the following circuit shown below, change the inputs *A B C E F* such that we see a change in the output when we change the input *D*.



15. Given the following code, draw the corresponding schematic

```
signal E std_logic;
signal F std_logic;

E<=C and not D;
F<=B or A;
G<=E and F;
```

16. We want to sample an audio wave that has a bandwidth of 10kHz. What frequency should we sample at to retain its quality? What is this criterion known as?

17. Compare and contrast the Resistor String, Binary Weighted Resistor, and R/2R “ladder” DACs.

Rapid Fire Questions (Courtesy of Matt Piotrowski)

1. What do all the following acronyms stand for: TTL, SSI, MSI, LSI, VLSI, ULSI, PCB, RAID, EPROM, EEPROM, ALU, ADC, DAC, CRC, PLA, ASIC, FPGA, PRBS, MSB, LSB, NRZ, ROM, ASCII, VHDL

2. How many bits are in a byte?
3. What does 4k mean?
4. Truth table for an AND gate

A	B	OUT

5. What is DeMorgan's Law?
6. What is 7 in binary?
7. What is two's complement?

8. What is the radix of hexadecimal?
9. What does the first bit in a FLOP represent?
10. What is the difference between unipolar NRZ and unipolar RTZ?

11. What do VCC, GND, and EN represent on a chip?
12. Draw the 4 different three state gates?

13. How is postal bar code weighted? How many 1's do you need in a valid sequence?

14. What is hamming distance?
15. How would you write a clock signal in VHDL?
16. What is the equation for Q(t+) for a JK Flip Flop?
17. Draw a NAND gate with transistors

18. Draw a NOR gate with transistors

19. Draw an OR gate with diodes

20. Draw an AND gate with diodes

21. What is fan in?

22. How do you multiply 0001 by 4?
23. What is the range of voltages that define a 0 and a 1 for a TTL gate?
24. What condition creates an overflow for two's complement numbers?

25. Draw an OR gate using NANDs only?

26. What is Ohm's Law?
27. What is quantization?

28. What is volatile memory?
29. What is the dynamic range of a signal?

30. What is an ADC and DAC?