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Lab 11

Theory

A multiplexer is a “data selector”. A multiplexer works by receiving inputs then from what is selected, we can choose to output whatever is outputted. In this lab we can't use the “dual” functionality of our multiplexer chips as each multiplexer is used as its own voting system. Each system needs to be independent from each other, then combined in the 8-1 multiplexer. The 74ls153 chip's dual feature combines the selector bits of the multiplexers so they aren't independent. Our voting machine in this lab works by slitting up the voting system then combining them. We have 4 4-1 multiplexers, 2 of them dummies as we don't have enough multiplexers, and the majority votes from those are then inputted into the 8-1 multiplexer which outputs the majority. A method of when a majority outputs without having a real majority is when the 4-1 chips give out a majority however the 8-1 multiplexer doesn't so it outputs a negative. When both multiplexers have three states of high equalling 6 high inputs but the 8-1 multiplexer also has 4 inputs, two from the 4-1 and two into the 8-1 which if both were negative would then make the 8-1 output a negative.

Deliverables

W	**X**	**Y**	**F**	**D**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**0**
0	**1**	**0**	**0**	**D**
0	**1**	**1**	**1**	**D**
1	**0**	**0**	**0**	**D**
1	**0**	**1**	**1**	**D**
1	**1**	**0**	**1**	**1**
1	**1**	**1**	**1**	**1**

F is determined by if the selector bits, W and X, are a combination of 0 and 1 which would output 1. To determine D0-D3, we look at the combinations of F, if its 00 then D is 0, 01 D switch, 10 D' switch, and 11 would be 1.

D	C	B	A	F	D
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	D
0	1	1	1	1	D
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	D
1	0	1	1	1	D
1	1	0	0	0	D
1	1	0	1	1	D
1	1	1	0	1	1
1	1	1	1	1	1

F is determined by if the selector bits, D C and B, are a combination of 0 and 1 which would output 1. To determine D0-D7, we look at the combinations of F, if its 00 then D is 0, 01 D switch, 10 D' switch, and 11 would be 1.

Discussion

This lab was actually very enjoyable as multiplexers are one of my favorite logic components. I liked how since we didn't have enough multiplexers, we used just the normal switches to toggle the selector bits and output. I also enjoyed how straight forward this lab was.

Questions

1. What do we mean by term resolution for ADC and DAC? What do we mean by term aliasing?

Resolution in this context is how many bits are received in the conversion process and how “clear” or accurate the conversion was. Aliasing happens if a given frequency is greater than the Nyquist Criterion Frequency, causing distortions and errors.

2. A diagram to perform the binary sequential multiplication of the 4-bit Multiplier (0101) times the 4-bit Multiplicand (1011) is provided. 8 steps are required to complete this problem. Recall that add and shift are done in separate steps. Using the diagram, show each step in the binary sequential multiplication.

3. What does the term volatile mean in computer memories? Give the name of two volatile memory systems

Volatile means erasure of data once a device is shut down. 2 examples of volatile memory are RAM and Cache memory.

4. How many addresses can be accessed using a memory address word of 8 bits?

2^8