1 The voltage through the resistive part of the circuit is 3V.

$(\frac{1}{1k} + \frac{1}{2k})^{-1} = 667\ \Omega$ $\quad I = V/R$

$667 + 500\ \Omega = R_{total}$

$3/1167 = 0.00257 = 2.57\ mA$

2

1k + 1k (parallel) → 500Ω

2k + 500 (series) → 2.5kΩ

2.5k + 2.5k (parallel) → 1.25kΩ

1.25k + 250 (series) → 1.5kΩ = R_{total}

$I_{total} = 3.33\ mA$

*Resistance in both branches is the same, so current is split in half.

$P = I^2R$ $\quad P = (1.67mA)^2 \cdot 2.5k\Omega = 6.97\ mW$

3

$A + 0 = A$

$A + A' = 1$

$0 . 1 = 0$

$A . A' = 0$

$A \oplus A' = 1$

$1 \oplus A = A'$

4

$AB + BC =$ $B(A+C)$

$AB'C + ABC' =$ $A(B \oplus C)$

$A + AB + ABC =$ $A(1 + B(1+C))$

$AB'(C'+D) + A'B(C'+D) =$ $(A \oplus B)(C'+D)$

$AB + A'B' =$ $(A \odot B')$

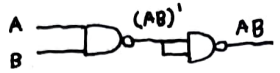
$(A+C)' + A'B =$ $A'C' + A'B =$ $A'(B+C')$

$A(B'CD)' =$ $A(B+C'+D')$

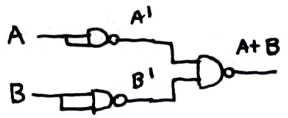
5

NOT

AND



OR

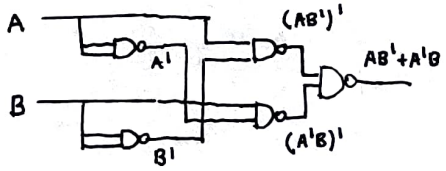


XOR

$AB' + A'B$

→ $((A'+B).(A+B'))'$

→ $((AB')'.(A'B)')'$



In retrospect this is more of a difficulty 4 question.

7

```
 1111
 1010 1110
+0111 1000
-----------
10010 0110
```

↑ "overflow" Intended. 2's complement is designed to work in this manner.

```
10101110
01010001
   ↓
01010010
  1
01010010
+01111000
---------
11001010
```

don't do this!

8

		economy
111_{10}	=	$10 \times 3 = 30$
1101111_2	=	$7 \times 2 = 14$
157_8	=	$8 \times 3 = 24$

		economy
73_{10}		
2201_3	=	$4 \times 3 = 12$
49_{16}	=	$16 \times 2 = 32$

9

$$\begin{array}{r} 1\,1 \\ 1\,0\,1\,0 \\ -\;1\,1 \\ \hline 1\,0\,1 = 5 \end{array} \qquad \begin{array}{r} 1\,0\,1 \\ \times\;1\,0\,0 \\ \hline 0\,0\,0 \\ 0\,0\,0 \\ +\;1\,0\,1 \\ \hline 1\,0\,1\,0\,0 = 20 \end{array}$$

$$\begin{array}{r} 1\,1\,1 \\ 1\,0\,1\,1 \\ +\;1\,1\,0\,1 \\ \hline 1\,1\,0\,0\,0 = 24 \end{array}$$

ALT: $4 = 2^2$ (Shift left 2)

$101 \rightarrow 10100$

$15/4$: shift right 2

$1111 \rightarrow 11 = 3$ (floored)

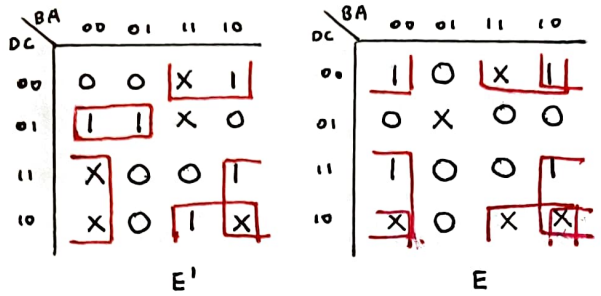
10

150_8 { 1101000_2, 104_{10}, 68_{16}

CF_{16} { 11001111_2, 317_8, 207_{10}

etc...

11

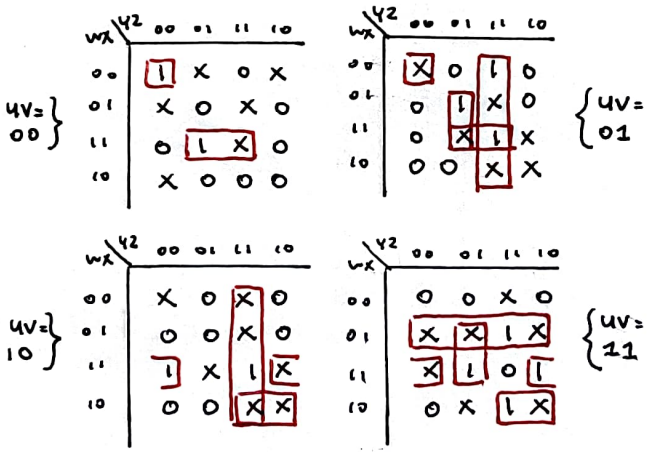


$$F = C'B + DA' + EC'A' + E'D'CB'$$

12

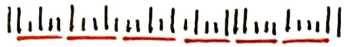
While I will not show the full map and reduction, the best formula I could find was (for a UVWXYZ plot)...

$$F = U'(W'X'Y'Z' + WXZ) + VX(Y'Z + UW') + (U \oplus V)YZ + UW(XZ' + X'Y)$$



A better reduction may be possible but is unlikely to be more than a marginal improvement.

13 The valve is 982407.
The third group was wrong.

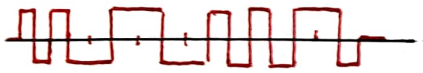


14 Option B

15 You can add $D'C'A$. This redundancy reduces the likelihood of a static hazard by providing additional checks on the same logic.

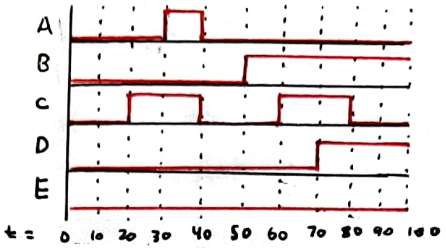
DC \ BA	00	01	11	10
00	1	1	1	0
01	1	1	0	0
10	0	0	0	0
11	0	0	1	0

16 Manchester



Unipolar RTZ

17



Note that this is inertial. If the values change again before the delay, any modification is negated. This chart would look much different for transport delay.

18 Forgot to include the circuit! That's my bad.

19 $F_1 = DBA + CB'$

* Putting DD' here would be incorrect, as they reduce to 0, and 0 has no effect on a canonical sum.

$F_2 = DBA + C'BA'$

* Because one of the minterms would be $D'CAA'$, this minterm cannot exist, and reduces to 0.

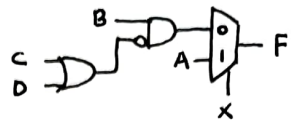
20 Inputs would be A-0-A-1-A-0-A-A from m_0 to m_7.

21

D	C	B	A	f	
0	0	0	0	0	m_0
0	0	0	1	0	
0	0	1	0	0	m_1
0	0	1	1	1	
0	1	0	0	1	m_2
0	1	0	1	1	
0	1	1	0	0	m_3
0	1	1	1	1	
1	0	0	0	0	m_4
1	0	0	1	0	
1	0	1	0	0	m_5
1	0	1	1	1	
1	1	0	0	0	m_6
1	1	0	1	0	
1	1	1	0	1	m_7
1	1	1	1	0	

* Because these equations are based on B, filling out the table for f is less straightforward. You must take DCA as the selector bits.

22



$B(C+D)' = 1(0+0)' = \underline{1}$

23

```
D <= not A and B after 10 ns;
E <= A or B;
F <= not C after 10 ns;
G <= D or (E or F);
```

24

0101011 → 01010101
11011111 → 11111111
00100011 → 01100011
00010000 → 00000000

25

From $C_0 \rightarrow C_7$...
10111000 (odd)

26

D Flip-Flop

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

JK Flip-Flop

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

SR Latch

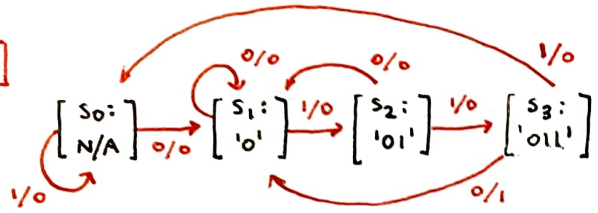
Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

*Note that, unlike set/reset on D flip-flops, an SR latch is not inverted. You still can't have both set and reset active. The resultant behavior is undefined.

27

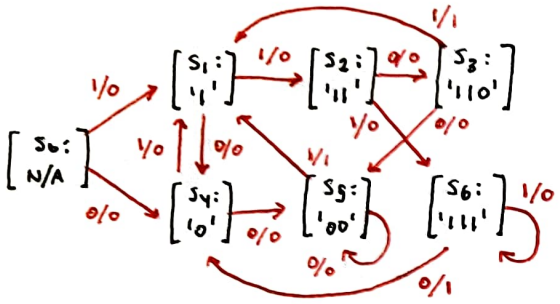
A debouncer is fundamentally set up like an SR latch, with the differences being that S and R are inverted. SR latches store 1-bit memory. When we tap one resistor, S = 1 and R=0, so Q goes low (remembers, inverted). Then, when we tap the other (with the ground), S=0 and R=1, so Q goes high.

28



You need only 2 D Flip-Flops for this.

29



30

Q_2	Q_1	Q_0	X	Q_2^+	Q_1^+	Q_0^+	Y
0	0	0	0	1	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	1	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	1	1	0
0	1	0	1	1	1	0	0
0	1	1	0	1	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	1	0	1	0	1	0
1	0	1	1	0	0	1	1
1	1	0	0	1	0	0	1
1	1	0	1	1	1	0	0
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

31

The associated equations are ...

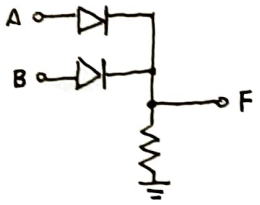
$$J_0 = K_0 = A'$$
$$J_1 = K_1 = Q_0' + A$$
$$J_2 = K_2 = Q_1 A + Q_1' Q_0' A'$$

32

First: INV
Second: OR
Third: AND

33 T, F, F, F, F

34 This is an AND gate.
OR gate shown...



35
i. 0000
ii. 1100
iii. 0001
iv. 1001
v. 1100
~~1~~100

36 $Q_3^+ = \overline{Q_2 \oplus Q_0}$

0000 → 1000 → 1100 → 0110 → 0011 → 0001 → 0000

0010 → 1001 → 0100 → 0010 → 1111 → 1111

0101 → 1010 → 1101 → 1110 → 0111 → 1011 → 0101

37 Left as an exercise. If anybody actually did this, show me what you got.

38 Set to 20 kHz.
Based on Nyquist criterion.

39

step	C	Reg B	Reg Q	
0	0	0 0 0 0	0 1 0 1	
1	0	1 0 1 0	0 1 0 (1)	Add
2	0	0 1 0 1	0 0 1 0	Shift
3	0	0 1 0 1	0 0 1 0	NOS
4	0	0 0 1 0	1 0 0 1	Shift
5	0	1 1 0 0	1 0 0 (1)	Add
6	0	0 1 1 0	0 1 0 0	Shift
7	0	0 1 1 0	0 1 0 0	NOS
8	0	0 0 1 1	0 0 1 0	Shift
				Done

* Reg A = 1010

0011 0010 = 50 ☑
5 × 10 = 50

40 F, T, F, F, F, F, T