HARDWARE 4:
BINARY MULTIPLIER

STUDENT RUBRIC

Demo Completion Requirements:

- ✓ This is a very straightforward lab. Since the design is given, the circuit should be fully functional. No credit for non-functional outputs, except in extreme cases.

REPORT RUBRIC

Scoring (out of 3 points):

- ✓ **[0.9 point]** Theory:
  - [0.9] How does binary multiplication work? Provide an example with two 4-bit unsigned values. Why do we use AND gates and adders for the hardware implementation? Your response should detail each step in the process and its hardware analogue (you may digress for repeated steps).

- ✓ **[0.9 points]** Deliverables:
  - [0.4] Include 5 test cases that cover a range of values for A_0-A_2 and B_0-B_3 in a table. It is not reasonable to test the circuit exhaustively. Briefly explain why you chose the values.
  - [0.5] Create a truth table with the headings Co, A1, B1, D, E, P1, S1, (Co'.D), and C1 as seen in the lab instructions. There will be 8 input states, where Co, A1, and B1 are the controls. Refer to the diagram on page 4.

- ✓ **[0.4 points]** Discussion section. Should conform to standard lab report guidelines.

- ✓ **[0.8 points]** Questions:
  - [0.8] Q1: If the logic gates have a propagation delay of about 10ns each, how long do you think it will take to complete a multiplication with this type of circuit? Make sure to consider the *sequential* internal structure of the SN7483 adder. An adder is not just one gate!