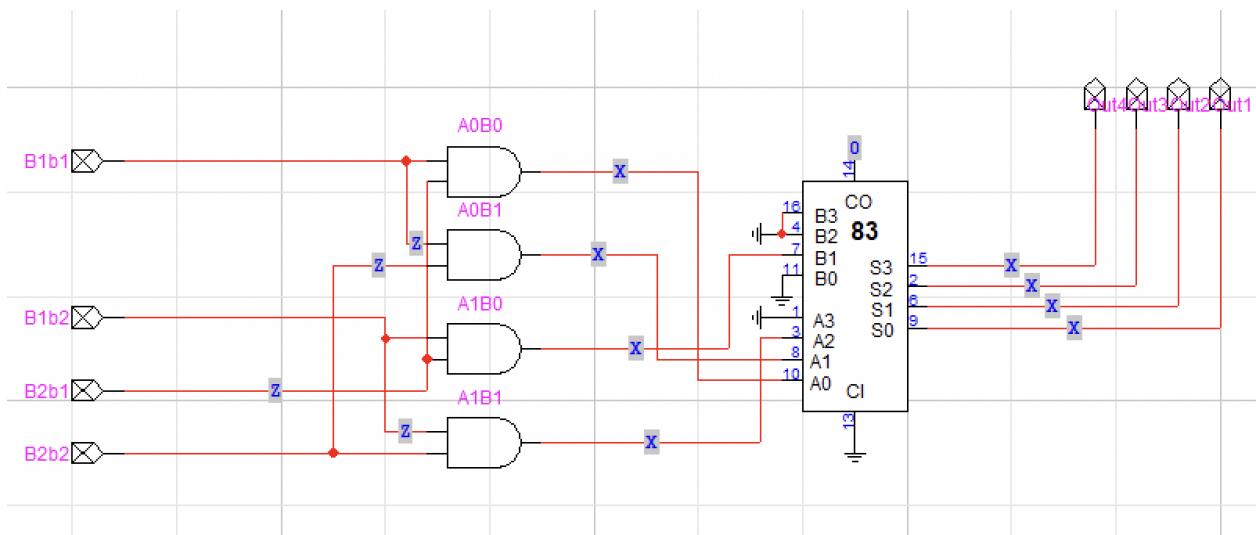
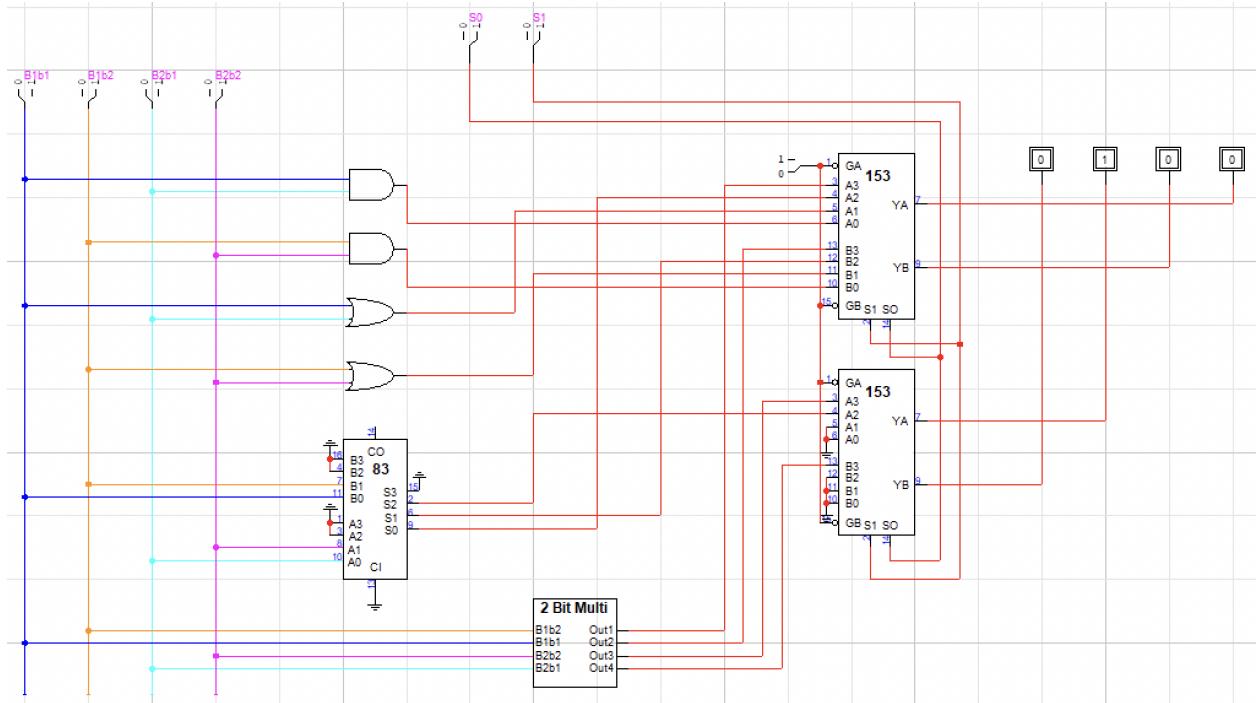


## Theory

In this lab we learned about how multiplexers work and implementations of them. In this lab we were provided with 4 4:1 multiplexers and had to use them to switch between 4 operations for 2 2 bit numbers. We basically had to implement an ALU, Arithmetic Logic Unit, that operates ANDs, ORs, Adds, and Multiplies 2 2 bit numbers. We first had to implement each individual operation into a circuit first. We then connect the outputs of each into the multiplexers. The AND and OR operations are the easiest as there are only 2 outputs so they connect directly into 2 multiplexers. A 74153 has 2 multiplexers in it so each of the output bits are connected to each with each multiplexer output representing a bit. We then move onto adding which in the edge case of  $3 + 3 = 6$  has a binary output of 3 bits, 110. We first implement it with 74283 chips and have the first and second sum bit outputs be connected to the first and second multiplexor. We then connect the third sum bit to the third multiplexer which will represent the third bit for it. This is why we have multiple multiplexores as each one will represent a bit. However we will have to ground the first 2 inputs of this multiplexer so it won't interfere with the AND and OR operations. We then have to implement a multiplication circuit which multiplies 2 2 bit numbers. We first have to implement how to multiply these numbers. Multiplying any number of bits together is just simply adding the values of each digit of one number multiplied by each digit of the other number and shifting down one place every time. For multiplying 2 2 bit numbers we would multiply each digit, and with each value from the first we shift and add a 0 to the right most place. We realistically would only be adding up the 2nd values together as the first and third values would just be adding 0. We also multiply each bit by ANDing them together. This would work with any series of numbers like a 3 bit and a 4 bit value. The ends of the addition won't be added but the 2-5 values. The edge case of multiplying 2 2 bit numbers is  $3 * 3 = 9$  which is a four bit number, 1001. The max edge case of how many bits there would be would just be adding up the number of bits being multiplied. For example 3 bit and 3 bit would give out a 6 bit number, a 3 and 4 would be 7 and 5 and 5 would be 10. Now that we have all of our operations and are connected together with the multiplexer, we still need to select through them. We have all the s0 and s1 pins connected together on all the multiplexers. We do this as all the multiplexers need to switch to that operation even if there's nothing there like the 3rd and 4th bit of the AND and OR operations. We have multiple multiplexers to have those extra bits for the Adding and Multiplication operations. If we wanted different selectors for each multiplexer, we would have to create and attach different ones to them. The 74153 chips have 2 multiplexers with one set of selector pins so if we wanted different ones we would have to use a different multiplexer so a second 74153 chip.

# Deliverables



In this lab we only worked with 2 2 bit numbers, if we wanted to scale up to 2 4 bit numbers it would conceptually be the same, we just have more bits to output. For the AND and OR operations they would be the same as the 2 2 bit numbers, we just need to add 2 more of each gate to both to handle the 4 added bits. Each bit in the first number is ANDed or ORed with each bit of the opposing number, depending on the operation, just like before but this time we have 4 bits as output. Before we set the 1st and 2nd input pins of the 3rd and 4th multiplexers to ground but this time we would connect them to the outputs of the 3rd and 4th output bits of the AND and

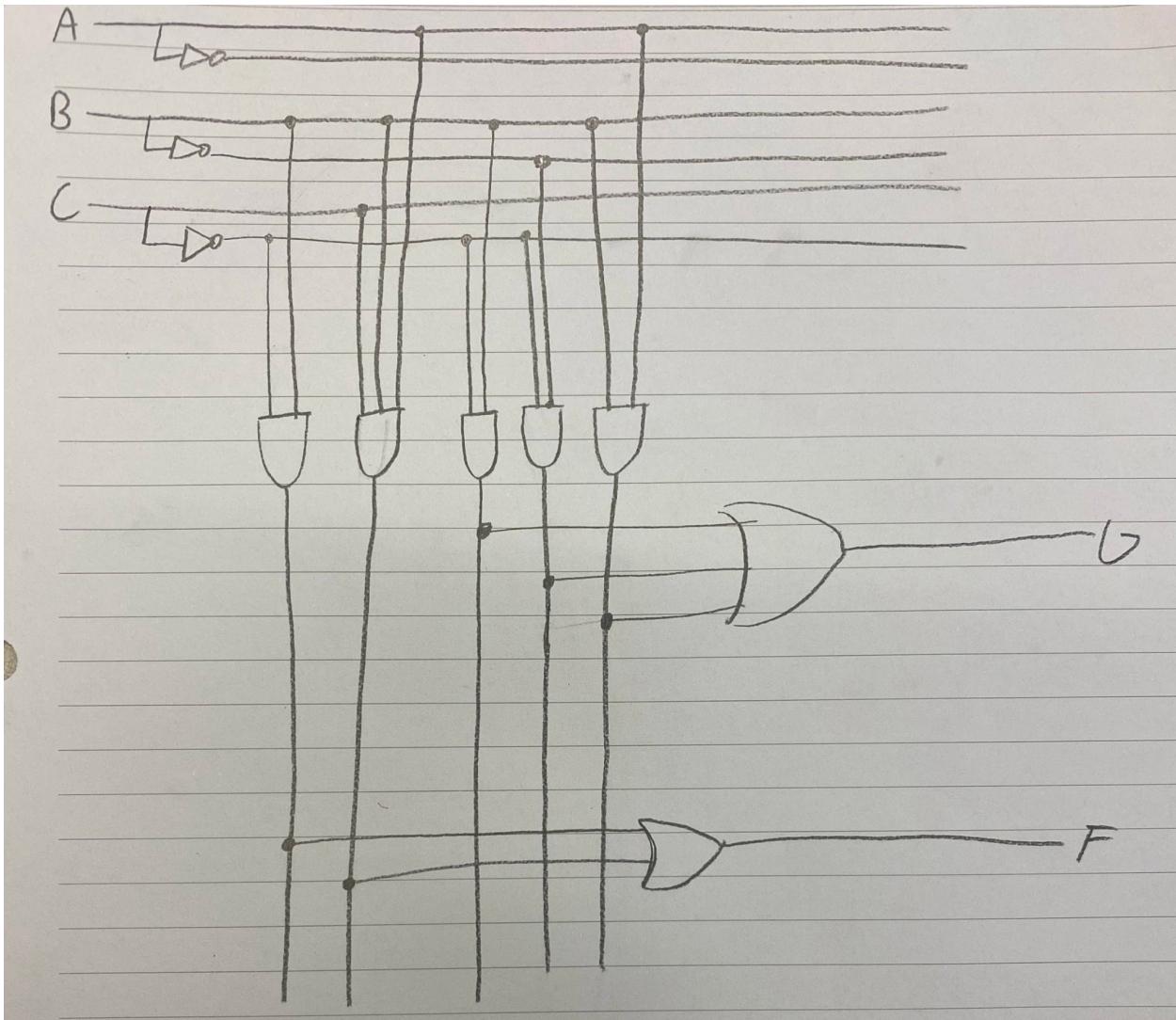
OR operations. We then move onto adding it's also the same concept and the pins in the 7483 chip that we set to ground are connected to the new input pins. We then again connect them to the multiplexers and 4th multiplexer 3rd input pin which is grounded would be used for the 4th output bit of the operation. The problem we run into is that for 2 4 inputs would have a max edge case of 5 bits as an output. We then have to use another multiplexer, which we are given, a 74157 chip which contains 4 2:1 multiplexers. We use one of the 2:1 multiplexers as our 5th bit output and have the selector pin be connected to S0 which is the deciding bit between the multiplying and adding operations. We then move onto the multiplication operation which again is the same as before. We AND each digit of one value to the other and everytime a digit is finished ANDing, we shift one the left and move onto the next then add. The output bits are again the same but now we have an edge case of it being an 8 bit number. We have half of the bits connected to our 2 74153 chips which contain 4 multiplexers and 4 outputs. We then have the remaining 4 be connected to the 74157 chip which contains 4 multiplexers totalling 4 outputs. We would have to ground the 2nd to 4th pins of the 74157 chip as they aren't being used for the addition operation only for the multiplication one.

## Discussion

In this lab we implemented an ALU circuit with AND, OR, addition and multiplication operations. I learned how useful multiplexers really are and how they operate. The analogy of it being a railroad really helped me as I didn't understand how selector pins worked but it's just used to choose between which "track". I also learned about what ALU's are and how they are used in real world applications. This lab was pretty straightforward and I actually had a lot of fun. The hardware surprisingly wasn't that bad and I actually got it working the first try without any debugging. Only thing I didn't like was the other parts of the lab which were a slight pain and on top of that, midterms this week interfering a lot. :/

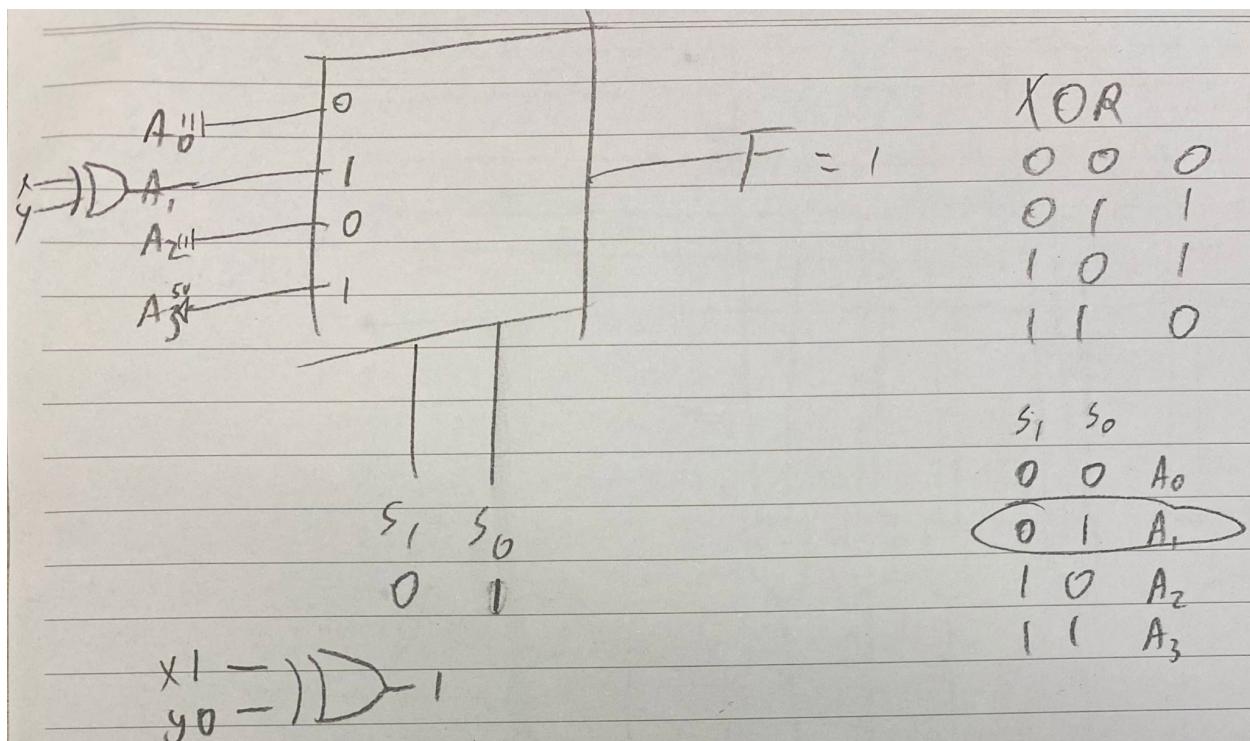
# Questions

1. Draw \*one\* PLA diagram for the following equations:



2. Imagine the following circuit: a 4-1 MUX (multiplexor) gets input from A<sub>0</sub> through A<sub>3</sub>, is controlled by S<sub>0</sub> and S<sub>1</sub> (where S<sub>0</sub> is the LSB) and produces output at F. A<sub>0</sub> and A<sub>2</sub> are connected to ground, and A<sub>3</sub> is connected to Vcc. A<sub>1</sub> is connected to an XOR gate which produces XX ⊕ YY. What is F when S<sub>0</sub> and X equal 1 and S<sub>1</sub> and Y equal 0?

$$F = 1$$



3. Multiply the following numbers together using binary multiplication. Show your work.

a) 5 (0101<sub>2</sub>) and 9 (1001<sub>2</sub>) Final answer should be 6 bits (binary) (0.3 pts).

Handwritten binary multiplication of 5 (0101) and 9 (1001). The multiplication is set up as follows:

$$\begin{array}{r} 5 \\ \times 1001 \\ \hline 0101 \\ 1001 \\ \hline 0101 \\ 0000 \\ \hline 000000 \\ + 0101000 \\ \hline 101101 \end{array}$$

The result is 101101, which is 45 in decimal.

b) -23 and 5. Express your final result as a 2's Complement number with 8 bits (0.7 pts). Don't multiply negative numbers!

Handwritten binary multiplication of -23 (101001) and 5 (00101). The multiplication is set up as follows:

$$\begin{array}{r} \text{sign } 1 \\ -23 \quad \boxed{1} 01001 \\ \times 5 \quad \boxed{0} 00101 \\ \hline 23 \quad \boxed{0} 10111 \\ 5 \quad \boxed{0} 00101 \\ \hline 10111 \\ 000000 \\ \hline 1011100 \\ \hline 1111001 \\ \boxed{1} 0001101 \end{array}$$

The result is 10001101, which is -23 in 8-bit 2's complement form.