Three out of four

Prerequisites

To do this lab assignment you should be familiar with both the operation and use of D and J-K flip-flops. Since the exercise uses truth tables, Karnaugh Maps, and State diagrams, you should be familiar with these before starting the lab work.

Theory

The theory behind this exercise relies on your understanding of how to determine whether a sequence has occurred in a string of binary bits. Many communication systems use start and stop codes to delineate the data and to be able to detect these codes is very important. The theory behind this bit counting relies on storing a state in a series of flip flops which tell the system where you are in the processing of the data. For example if you are looking to find a 010 string then a state must be set that recognizes the 01 input and then shift to either the state that is determined by a subsequent 0 or 1.

Background story

The TAs are grading a test question with 'no partial credit'. To alert them to be careful and discriminating with regards to the content of the answer we want to detect when a TA gives three consecutive 'correct' (or 1s) followed by a 0 and three consecutive 'wrong' (or 0s) followed by a 1. Note that the codes may overlap. A lamp or buzzer (to wake him/her up) is to be activated when either of the sequences occur.

Procedure

Make a sequence detector that detects '1110' and '0001' using D Flip-Flops. To do this:

- Firstly, determine how many states are required. Define them and what they mean e.g. two 1s have been received.
- Draw a state diagram indicating the input (A) and the output (B - for buzzer) at each transition. The form of the annotation at each transition should be A/B.
- Create a transition table including all states. Use D flip-flops for your implementation.
- Draw the appropriate Karnaugh Maps and minimize the D input functions.
- Build the circuit.
- Test exhaustively and check your results with the state diagram.

Note that this exercise is to show how to implement the detection not just waiting for the sequence to appear in a serially inputted register. This latter solution is not acceptable in this particular case.

Deliverables

- Draw state diagram, transition tables, and maps. Show to your TA.
- Demonstrate that your circuit works to the specifications.
- Complete a f report with diagrams, narrative, and results and submit it