SOFTWARE 5:
DIGITAL LOGIC W/ VHDL

GENERAL RUBRIC

DEMO RUBRIC

This is a "follow the instructions" lab, for the most part, but at the end, you will be required to convert the two's complement circuit from software lab 2 from on based entirely on discrete gates in one based at least partially off of VHDL modules.

Completion Requirements:

- ✓ Your FullAdder should be functional.
- ✓ You must create your own Overflow detection module with VHDL.
- ✓ Create a mock-up of software 2 using full adders and overflow detection units that you programmed. You do not have to use you full adder array in place of all four 4-bit adders – just make sure to use it at least once.

REPORT RUBRIC

This is not a formal lab report. There is no theory section or questions. You should submit your VHDL code for the adder and their overflow detection unit *WITH COMMENTS* alongside a text submission. To reiterate, the .dwv files themselves *must* be submitted. You may have a plaintext submission for the discussion part of this report.

Scoring (out of 3 points):

- ✓ **[2 points]** Deliverables:
  - [1.0] Attach your code (.dwv file) for the full adder implementation.
  - [1.0] Attach your code (.dwv file) for the overflow detector implementation.

- ✓ **[1 point]** Discussion section:
  - [0.5] Answer the opinion question at the end of the instructions: Did you prefer writing VHDL modules or connecting discrete gates?
  - [0.5] A reflection on the rest of the lab, as usual.