Benny Chen
12/04/2021
SEC 004L

CSE 2301 Lab 11
Deliverables

```
library IEEE;
use IEEE.std_logic_1164.all;


entity FullAdder is

 port(
 --Inputs and Outputs for adder
        b   : in    std_logic;
        a   : in    std_logic;
        carry   : out   std_logic;
        sum : out   std_logic;
        c   : in    std_logic
    );

end FullAdder;


architecture arch1 of FullAdder is

begin
--Sum part of FullAdder adds 2 bits together then the carried value
--and if 2 high values are inputted, returns 0
--Carry part of FullAdder checks if A B will shift onto next (third) bit and determines a carry value
  sum <= (a xor b) xor c;
  carry <= (a and b) or (c and (a xor b));

end arch1;
```

```
library IEEE;
use IEEE.std_logic_1164.all;


entity OverflowDetector is

 port(
 --Inputs and Outputs for detector
        A   : in    std_logic;
        B   : in    std_logic;
        S   : in    std_logic;
        Overflow    : out   std_logic
    );

end OverflowDetector;


architecture arch1 of OverflowDetector is

begin

--The process of how a overflow is detected
--Takes in A B whcih are the two MSB values and checks if they are both 1's then also takes in S
--which is the sum of A B to see if they shifted to a 0 which then alerts to a overflow
--It can also detect for if the two MSB are 0's by inverting A B then checking if the sum is 1
  Overflow <= (((A and B) and (not S)) or (((not A) and (not B)) and S));

end arch1;
```

Discussion

Did you prefer writing VHDL modules or connecting discrete gates?
I personally preferred connecting discrete gates over writing VHDL as writing makes it harder to imagine the design of the circuit. I also think actually connecting circuits is easier this way rather than having to write out the logic and making sure you didn't forget a parentheses or a semicolon.

In this lab I learned about a new type of method of implementing custom chips in logicworks and how VHDL code is implemented.