Homework 6 Solutions

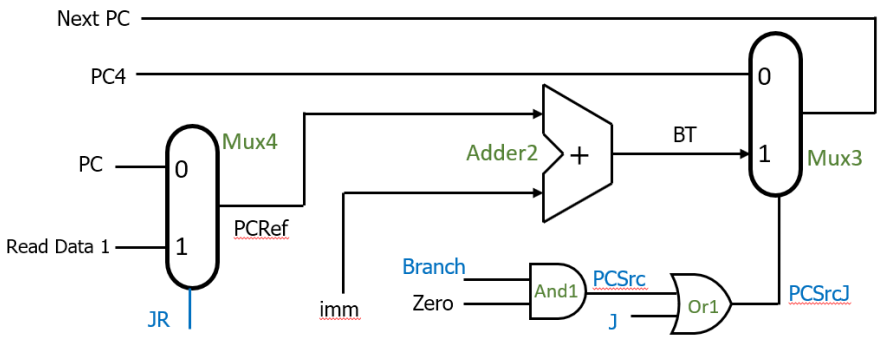
1

```
0x00400200: 0xFE542023

1111 1110 0101 0100 0010 0000 0010 0011

opcode:   0100011 (S-type)

rs1:      01000
rs2:      00101
rd:       00000
immediate:      0b111111100000  sign extended to 0xFFFFFFE0
ALUOperation:   0b0010   to calculate memory address
BranchTarget:   0x00400200 + 0xFFFFFFE0 = 0x004001E0
PCSrc:          0
NextPC:         0x00400204
```

This is a store instruction. The output of the main control for SW instruction is listed in lecture slides (and in the textbook).

2

a. Generating target address



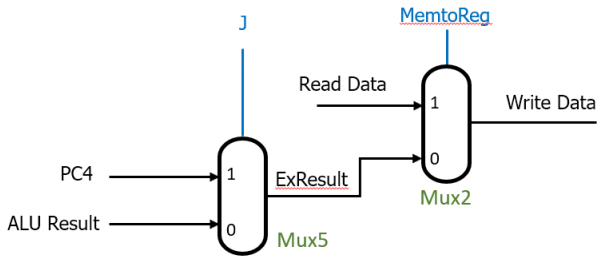
Computing target address
The target address of JAL is PC + immediate. The target address of JALR is Reg[rs1] + immediate. So we had Mux4. Mux4 selects the data going into input 1 of Adder2. Input 0 of Mux4 is PC and its input 1 is Read data 1 (from the register file). The select signal is JR.

Selecting target address
Mux3 is controlled by PCSrcJ. PCSrc is now by the following logic:

```
PCSrcJ = J | (Branch & Zero)
```

If the instruction being executed is JAL or JALR, NextPC is always BranchTarget.

b. Writing PC4 to register file.



Both JAL and JALR write PC4 to rd. We add Mux5 to select the data going into input 0 of Mux2. Input 0 of Mux5 is the output of ALU, and input 1 is PC4. The select signal of Mux4 is J so PC4 is selected if the instruction being executed is JAL or JALR.

c. Control signals

With the above changes, the control signals for JAL and JALR are as follows.

Inst.	ALU Src	Memto Reg	Reg Write	Mem Read	Mem Write	Branch	J	JR
JAL	X	0	1	0	0	0	1	0
JALR	X	0	1	0	0	0	1	1

Execution of JAL

When the processor executes the JAL instruction,

- Mux4 selects PC to Adder2.
- Adder2 calculates BranchTarget = PC + immediate.
- PCSrcJ is 1. Mux3 selects BranchTarget, which is PC + immediate, as NextPC.
- Mux5 selects PC4, the address of the instruction that follows JAL.
- Mux2 selects PC4 as Write Data, which will be written to register rd.

Execution of JALR

When the processor executes the JALR instruction,

- Mux4 sends Read data 1 to Adder2.
- Adder 2 calculates BranchTarget = Reg[rs1] + immediate.
- PCSrcJ is 1. Mux3 selects BranchTarget, which is Reg[rs1] + immediate, as NextPC.
- Mux5 selects PC4, the address of the instruction that follows JAL.
- Mux2 selects PC4 as Write Data, which will be written to register rd.