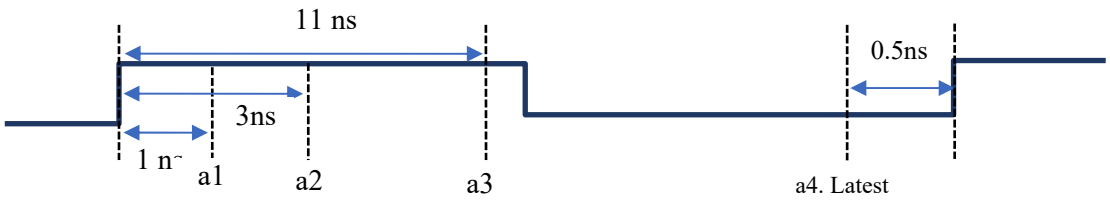
2. Timing.



Time relative to the beginning of a cycle.

a1. Reg-Ready. 1ns

a2. Control-Ready. 1 + 2 = 3ns

a3. Adder-Ready. 1 + 10 = 11ns

a4. Latest. The input to registers must be ready. This is the example in the figure.

The combinational circuit has their output ready 11 ns into a cycle. The setup time is 0.5 ns.

The minimum cycle time is: 11 + 0.5 = 11.5 ns.

The highest clock rate is: 1 / 11.5 ns = 0.08696 GHz = 87.0 MHz

If we use the same kind of registers, the max clock rate we can achieve is 1/(1ns + 0.5ns) = 0.6667 GHz = 666.7 MHz. In this case, there is no combinational circuit or no delay.

3. Multiplier.

27 * 17 = 459

```
0     0000011011    10001  0000000000
1     0000110110    01000  0000011011
2     0001101100    00100  0000011011
3     0011011000    00010  0000011011
4     0110110000    00001  0000011011
5     1101100000    00000  0111001011
```

If we consider the bits are two's complement number, 0b11011 is -5 and 0b10001 is -15. Their product is 75, which is 0b00010_01011. The lowest five bits are the same as the lowest five bits in the product register.