Homework 6 (100 points)

Due Date: By the end of Friday, 11/4/2022.

Figure 4.21 can be downloaded in HuskyCT, where Lecture 3.2 slides are posted. Note that **the figure is copyrighted**. We use it in this course for educational purposes. Do not distribute it further. The figure posted in HuskyCT also has additional signal names.

1. Assume the single-cycle RISC-V processor, as shown in Figure 4.21. Find the following signal values when the processor executes the instruction 0xFE542023 located at 0x00400200. Explain your answers.

   All signals generated by the main control.
   opcode
   rs1
   rs2
   rd
   Immediate
   ALU operation
   BranchTarget
   PCSrc
   NextPC

Continued on the next page.

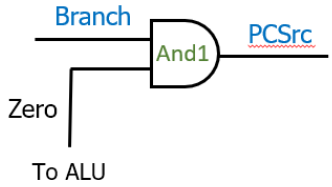
2. In this problem, we improve the processor in Figure 4.21 to support JAL and JALR instructions. Assume the following two components have already been revised.

   - The main control. It has two additional outputs J and JR. J is 1 if and only if the instruction is either JAL or JALR. JR is 1 if and only if the instruction is JALR. The two signals can be generated from the opcode.
   - ImmGen. ImmGen can generate correct immediate for all types of instructions.

   Tasks:

   a) We will start with a diagram like Figure 4.21. If you have the diagram drawn in the lecture, make sure the diagram meets the following requirements. If you draw from scratch, reading the entire question first may help you to plan the diagram.

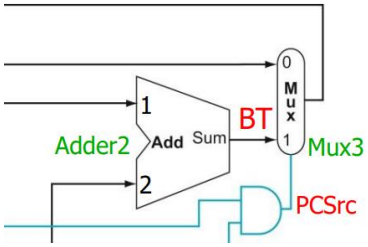
      - We do not need to include the control module. However, all control signals should be labeled. For example, Branch is labeled in the following figure, although it is not connected to the control module.



      - All wires go either horizontally or vertically, and lines are straight.
      - The input ports of Mux are labeled with 0 and 1.
      - The diagram is clean.

      The submitted diagram will have the revision we do in b) and c).

   b) We change the diagram in a) to set the correct next PC value at the output of Mux3 for JAL, JALR and branches. The part of diagram we need to change is shown in the following figure.



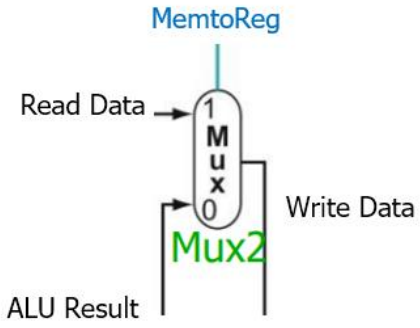
      We modify the diagram as follows.

      - Add a Mux before Adder2 so Adder2 can compute the correct target address for JAL, JALR and branches. We name the new Mux Mux4.
      - Change the logic that generates the select signal of Mux3.

In addition to changing the diagram in a), explain how the target address is computed for JAL and JALR instructions, and how the select signals of Mux4 and Mux3 are generated. Write a logic expression if necessary.

For example, the target address of branches is computed as PC + imm. Note that every signal in Figure 4.21 has a name, either indicated by the label or by the port the signal is connected to, e.g., ALU result.

c) We then change the diagram so the correct value can be saved in the destination register for JAL and JALR. The part of diagram we change is shown in the following figure. Recall that the value to be saved in the destination register is decided by Mux2, which drives Write Data.



To achieve the goal, we add another Mux, called Mux5, before Mux2.
Explain how to set the select signal of Mux5. Hint: it is controlled by a control signal from the control module. There is no need to add additional gates.

d) Specify the value of control signals for JAL and JALR. Recall that if a signal does not affect the execution of an instruction, it is a don't care signal for the instruction.

Inst.	ALU Src	Memto Reg	Reg Write	Mem Read	Mem Write	Branch	J	JR
JAL								
JALR								

Extra

Explain how JAL and JALR instructions are executed. How is the target address calculated for each instruction? How is PC4 saved? You do not need to submit your explanations.