Lab 9

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Task 1

Address	Cache index	Tag	Block offset	Hit/Miss
0x10010000	0	0x00200200	0	Miss
0x10010004	0	0x00200200	4	Hit
0x10010008	0	0x00200200	8	Hit
0x1001000C	0	0x00200200	12	Hit
0x10010010	1	0x00200200	0	Miss
0x10010014	1	0x00200200	4	Hit

The Cache index has 3 bits, the block offset again has 4 bits, and the tag has 25 bits as the complete address is 32 bits, meaning 32 bits - 3 bits - 4 bits = 25 bits. For the first 2 accesses, the tag and cache index are the same, only the block offset changes. The first operation is a miss as it puts the element in place with the next three will hit. This makes it a 75% hit rate which I predicted. There are hits 3 in a row, then a miss which repeats.

Task 2

Number of blocks	Cache size	Hit rate	Miss count
8	128 bytes	75%	3072
16	256 bytes	75%	3072
32	512 bytes	75%	3072
64	1024 bytes	99%	64
128	2048 bytes	99%	64

My prediction for this task is the same as the previous task. We can first see that when the array size is greater than the cache size, the hit rate is 75%. For

cache sizes of 1024 bytes and 2048 bytes, the hit rate is 99% as at that point, the cache size is greater than the array size. When the cache size is greater than the array size, the cache is populated with all the elements and the hit rate is close to 100%. If warray is doubled, we can still see how it would behave with how it previously behaved. Again, if the cache size is greater than the array size rather than if the array size is greater than the cache size, the hit rate would be greater. Therefore, if we double the warray size, the hit rate for 64 blocks would have a hit rate of 75% and 3072 misses.