CSE3666

Homework 8 Solutions

1

See the examples in slides and answers in HuskyCT.

2

See the examples in slides and answers in HuskyCT.

3

a)

Among 12 given bits, there are 4 tag bits and 3 index bits. The right most 5 bits are in block offset. So the block size is 32 bytes.

b)

Cache size is 32 * 8 = 256 bytes.

c)

5 misses. See the table.

Addr	Tag	Index	M/H	Highest	Lowest
0b101011100101	0b1010	0b111	0	0b101011111111	0b101011100000
0b101011100111	0b1010	0b111	1	0b101011111111	0b101011100000
0b101011111001	0b1010	0b111	1	0b101011111111	0b101011100000
0b111001010111	0b1110	0b010	0	0b111001011111	0b111001000000
0b111101001101	0b1111	0b010	0	0b111101011111	0b111101000000
0b101001010101	0b1010	0b010	0	0b101001011111	0b101001000000
0b101011100011	0b1010	0b111	1	0b101011111111	0b101011100000
0b101001011101	0b1010	0b010	1	0b101001011111	0b101001000000
0b111001001101	0b1110	0b010	0	0b111001011111	0b111001000000

4

a)

1 + 0.1 * 80 = 9

b)

1 + 0.05 * 80 = 5

c)

0.35 * 0.1 * 80 = 2.8

d)

1 * 0.05 * 80 = 4

e)

1.6 + 2.8 + 4 = 8.4

f)

8.4 / 1.6 = 5.25

5

a)

Each block can hold 16 elements. D[0] and D[15] are loaded into cache.
Note that the lower 8 bits of D[0]'s are 0. So D[0] starts a new block.

b)

Accessing D[1] through D[15] is cache hit. The first miss will be D[16].

c)

D[0] is evicted when CPU accesses a word when the cache is filled. The cache size is 64KiB. Each element in the array is 2 bytes. It takes 64 * 1024 / 2 = 32768 elements to fill up the cache. Therefore, D[0] is evicted when D[32768] is accessed.

d)

On every cache miss, a block of 32 bytes, which consists of 16 elements in the array, is loaded into cache. The 15 references after a miss will be hits. So the miss rate is 1/16 = 6.25%.

e)

Similarly, there is a miss every 32 accesses. The miss rate is 1/32.

Note that the analysis in lab 9 is similar. The difference is the cache might be able to store the entire array.