Altera Phase-Locked Loop (Altera PLL) IP Core User Guide

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The Altera PLL megafunction IP core allows you to configure the settings of PLL.

Altera PLL IP core supports the following features:

- Supports six different clock feedback modes: direct, external feedback, normal, source synchronous, zero delay buffer, and LVDS mode.
- Generates up to 18 clock output signals for the Arria® V and Stratix® V devices and nine clock output signals for the Cyclone® V device.
- Switches between two reference input clocks.
- Supports both the adjacent PLL (`adjpllin`) and the C-Counter clock source (`cclk`) inputs to connect with an upstream PLL in PLL cascading mode.
- Supports PLL output cascading.
- Generates the Memory Initialization File (**.mif**) and allows PLL dynamic reconfiguration.

Related Information

- **Introduction to Altera IP Cores**
  Provides more information about the Altera IP cores and the parameter editor.
- **Operation Modes** on page 9
- **Output Clocks** on page 9
- **Reference Clock Switchover** on page 10
- **PLL-to-PLL Cascading** on page 10
- **PLL Output Counter Cascading** on page 14

Device Family Support

The Altera PLL IP core supports the Arria V, Cyclone V, and Stratix V device families.

Altera PLL IP Core Parameters

The Altera PLL IP core parameter editor appears in the PLL category of the IP Catalog.

Altera PLL IP Core Parameters - General Tab

Table 1: Altera PLL IP Core Parameters - General Tab

Parameter	Legal Value	Description
Device Speed Grade	Stratix V: 1–4, Arria V: 3–6, Cyclone V: 6–8	Specifies the speed grade for a device. The lower the number, the faster the speed grade.
PLL Mode	Integer-N PLL or Fractional-N PLL	Specifies the mode used for the Altera PLL IP core. The default mode is **Integer-N PLL**.
Reference Clock Frequency	—	Specifies the input frequency for the input clock, `refclk`, in MHz. The default value is **100.0 MHz**. The minimum and maximum value is dependent on the selected device. The PLL reads only the numerals in the first six decimal places.

Parameter	Legal Value	Description
Operation Mode	direct, external feedback, normal, source synchronous, zero delay buffer, or lvds	Specifies the operation of the PLL. The default operation is **direct** mode. • If you select the **direct** mode, the PLL minimizes the length of the feedback path to produce the smallest possible jitter at the PLL output.The internal-clock and external-clock outputs of the PLL are phase-shifted with respect to the PLL clock input. In this mode, the PLL does not compensate for any clock networks. • If you select the **normal** mode, the PLL compensates for the delay of the internal clock network used by the clock output. If the PLL is also used to drive an external clock output pin, a corresponding phase shift of the signal on the output pin occurs. • If you select the **source synchronous** mode, the clock delay from pin to I/O input register matches the data delay from pin to I/O input register. • If you select the **external feedback** mode, you must connect the `fbclk` input port to an input pin. A board-level connection must connect both the input pin and external clock output port, `fboutclk`. The `fbclk` port is aligned with the input clock. • If you select the **zero delay buffer** mode, the PLL must feed an external clock output pin and compensate for the delay introduced by that pin. The signal observed on the pin is synchronized to the input clock. The PLL clock output connects to the `altbidir` port and drives `zdbfbclk` as an output port. If the PLL also drives the internal clock network, a corresponding phase shift of that network occurs. • If you select the **lvds** mode, the same data and clock timing relationship of the pins at the internal SERDES capture register is maintained. The mode compensates for the delays in LVDS clock network, and between the data pin and clock input pin to the SERDES capture register paths.
Enable locked output port	Turn on or Turn off	Turn on to enable the `locked` port.
Enable physical output clock parameters	Turn on or Turn off	Turn on to enter physical PLL counter parameters instead of specifying a desired output clock frequency.
Number of Clocks	Stratix V and Arria V: 1–18, Cyclone V: 1–9	Specifies the number of output clocks required for each device in the PLL design. The requested settings for output frequency, phase shift, and duty cycle are shown based on the number of clocks selected.

Parameter	Legal Value	Description
Desired Frequency [1]	—	Specifies the output clock frequency of the corresponding output clock port, `outclk[]`, in MHz. The default value is **100.0 MHz**. The minimum and maximum values depend on the device used. The PLL only reads the numerals in the first six decimal places.
Actual Frequency	—	Specifies the actual value for the output clock frequency.
Phase Shift units	ps or degrees	Specifies the phase shift unit for the corresponding output clock port, `outclk[]`, in picoseconds (ps) or degrees.
Phase Shift	—	Specifies the requested value for the phase shift. The default value is **0 ps**.
Actual Phase Shift	—	Specifies the actual value for the phase shift.
Duty Cycle	1–99	Specifies the duty cycle in percentage for the corresponding output clock port, `outclk[]`. The default value is **50%**.
Fractional carry out [2][3]	8, 16, 24, or 32	Specifies the fractional carry out (`Fcout`) for the Delta Sigma Modulator (DSM) mode for PLL. The fractional carry out determines the denominator in the equation *K*/2^`Fcout`.
DSM Order [2][3]	1st_order, 2nd_order, 3rd_order, or disable	Specifies the DSM order for shifting the fractional noise to be filtered out by the PLL to high frequencies.
Multiply Factor (M-Counter) [3]	1-512	Specifies the multiply factor of `M`-counter.
Fractional Multiply Factor (K) [2][3]	1 to (2^`Fcout`-1)	Specifies the fractional multiply factor of DSM. `Fcout` is the value of fractional carry out parameter.
Divide Factor (N-Counter) [3]	1-512	Specifies the divide factor of `N`-counter.
Make this a cascade counter [3][4]	Turn on or Turn off	Turn on to cascade this counter into the next counter output for larger division factor.
Divide Factor (C-Counter) [3]	1-512	Specifies the divide factor for the output clock (`C`-counter)

[1] This parameter is only available when **Enable physical output clock parameters** is turned off.
[2] This parameter is only available in Fractional-N PLL mode.
[3] This parameter is only available when **Enable physical output clock parameters** is turned on.
[4] This feature is only supported in Quartus® Prime version 13.1 and onwards.

Altera PLL IP Core Parameters - Clock Switchover Tab

Table 2: Altera PLL IP Core Parameters - Clock Switchover Tab

Parameter	Legal Value	Description
Create a second input clk 'refclk1'	Turn on or Turn off	Turn on to provide a backup clock attached to your PLL that can switch with your original reference clock.
Second Reference Clock Frequency	—	Selects the frequency of the second input clock signal. The default value is **100.0 MHz**. The minimum and maximum value is dependent on the device used. The PLL reads only the numerals in the first six decimal places. The PLL is automatically configured to satisfy its legality requirements for the primary reference clock only. If the second reference clock frequency is different, this may cause an illegal VCO or PFD frequency error. To avoid this error, you can turn on **Enable physical output clock parameters** and manually configure the PLL such that the frequency is legal for both `refclk` inputs.
Switchover Mode	Automatic Switchover, Manual Switchover, or Automatic Switchover with Manual Override	Specifies the switchover mode for design application. The IP supports three switchover modes: • If you select the **Automatic Switchover** mode, the PLL circuitry monitors the selected reference clock. If one clock stops, the circuit automatically switches to the backup clock in a few clock cycles and updates the status signals, `clkbad` and `activeclk`. • If you select the **Manual Switchover** mode, when the control signal, `extswitch`, changes from logic low to logic high, and stays high for at least three clock cycles, the input clock switches to the other clock. The `extswitch` can be generated from FPGA core logic or input pin. • If you select **Automatic Switchover with Manual Override** mode, when the `extswitch` signal is high, it overrides the automatic switch function. As long as `extswitch` remains high, further switchover action is blocked. To select this mode, your two clock sources must be running and the frequency of the two clocks cannot differ by more than 20%. If both clocks are not on the same frequency, but their period difference is within 20%, the clock loss detection block will detect the lost clock. The PLL most likely drops out of lock after the PLL clock input switchover and needs time to lock again.
Switchover Delay	0–7	Adds a specific amount of cycle delay to the switchover process. The default value is **0**.
Create an 'active_clk' signal to indicate the input clock in use	Turn on or Turn off	Turn on to create the `activeclk` output. The `activeclk` output indicates the input clock which is in use by the PLL. Output signal low indicates `refclk` and output signal high indicates `refclk1`.

Parameter	Legal Value	Description
Create a 'clkbad' signal for each of the input clocks	Turn on or Turn off	Turn on to creates two `clkbad` outputs, one for each input clock. Output signal low indicates the clock is working and output signal high indicates the clock is not working.

Altera PLL IP Core Parameters - Cascading Tab

Table 3: Altera PLL IP Core Parameters - Cascading Tab

Parameter	Legal Value	Description
Create a 'cascade out' signal to connect with a downstream PLL	Turn on or Turn off	Turn on to create an output port, which indicates that this PLL will be used as a source and it connects with a destination (downstream) PLL.
Specifies which outclk to be used as cascading source	Stratix V and Arria V: 1–18, Cyclone V: 1–9	Specifies the cascading source.
Create an adjpllin or cclk signal to connect with an upstream PLL	Turn on or Turn off	Turn on to create an input port, which indicates that this PLL will be used as a destination and it connects with a source (upstream) PLL.
PLL Cascading Mode	Create an adjpllin signal to connect with an upstream PLL or Create a cclk signal to connect with an upstream PLL	• If you select **Create an adjpllin signal to connect with an upstream PLL**, the `adjpllin` signal is created to connect with an upstream PLL during cascading. • If you select **Create a cclk signal to connect with an upstream PLL**, the `cclk`[5] signal is created to connect with an upstream PLL during cascading.

Altera PLL IP Core Parameters - MIF Streaming Tab

Table 4: Altera PLL IP Core Parameters - MIF Streaming Tab

Parameter	Legal Value	Description
Generate MIF file	Turn on or Turn off	Turn on to generate the `.mif` for the current PLL profile. You must turn on the **Enable dynamic reconfiguration of PLL** parameter in the **Settings** tab before selecting this function. The generated `.mif` contains a PLL profile, and a collection of physical parameters—such as `M`, `N`, `C`, `K`, bandwidth, and charge pump—that defines that PLL. You can then load this `.mif` into the Altera PLL Reconfig IP core.

[5] Not supported in Cyclone V devices.

Parameter	Legal Value	Description
Enable Dynamic Phase Shift for MIF Streaming	Turn on or Turn off	Turn on to store dynamic phase shift properties for PLL reconfiguration. You must turn on the **Enable dynamic reconfiguration of PLL** parameter in the **Settings** tab before selecting this function.
DPS Counter Selection	C0–C17, All C, or M	Selects the counter to undergo dynamic phase shift.
Number of Dynamic Phase Shifts	—	Selects the number of phase shift increments. The size of a single phase shift increment is equal to 1/8 of the VCO period. The default value is **1**.
Dynamic Phase Shift Direction	Positive or Negative	Determines the dynamic phase shift direction to store into the PLL MIF.

Altera PLL IP Core Parameters - Settings Tab

Table 5: Altera PLL IP Core Parameters - Settings Tab

Parameter	Legal Value	Description
PLL Auto Reset	On or Off	Automatically self-resets the PLL on loss of lock.
PLL Bandwidth Preset	Auto, High, Low, or Medium	Specifies the PLL bandwidth preset setting. The default setting is **Auto.**
Enable dynamic reconfiguration of PLL	Turn on or Turn off	Turn on to enable the dynamic reconfiguration of the PLL.
Enable access to dynamic phase shift ports	Turn on or Turn off	Turn on to enable the dynamic phase shift interface with the PLL.
Enable access to PLL DPA output port	Turn on or Turn off	Turn on to enable the eight bits port for the eight phases of the DPA clock.
PLL DPA output division	1, 2, or 4	Specifies the PLL DPA output division value.

Related Information

- **AN 661: Implementing Fractional PLL Reconfiguration with Altera PLL and Altera PLL Reconfig IP Cores**
  Provides more information about PLL dynamic reconfiguration and dynamic phase shift.
- **Dynamic Phase Shift Signals in Altera PLL IP Core**

Altera PLL IP Core Parameters - Advanced Parameters Tab

Table 6: Altera PLL IP Core Parameters - Advanced Parameters Tab

Parameter	Legal Value	Description
Advanced Parameters	—	Displays a table of physical PLL settings that will be implemented based on your input.

Functional Description

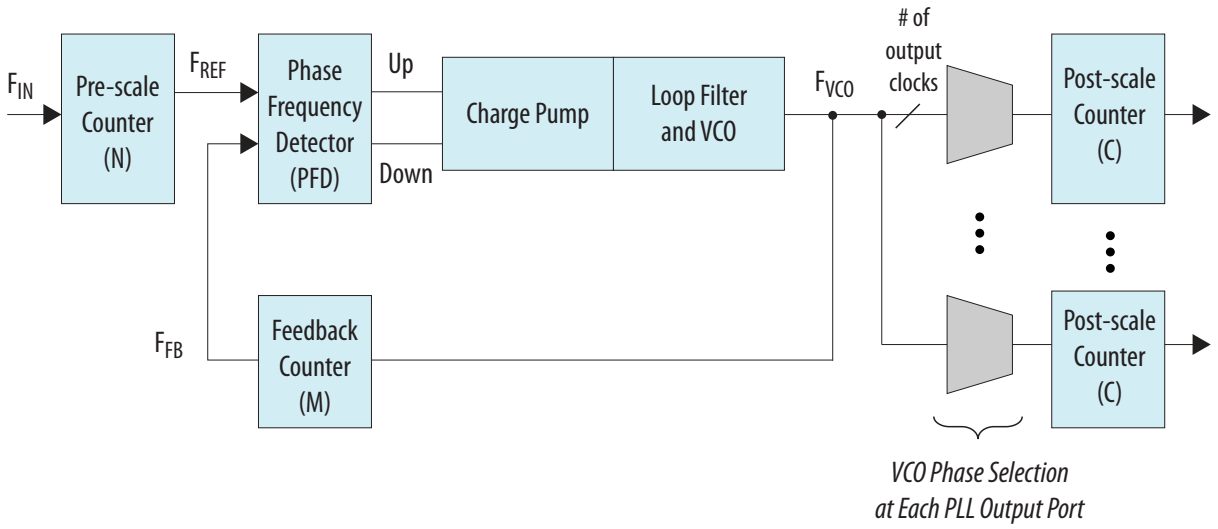
A PLL is a frequency-control system that generates an output clock by synchronizing itself to an input clock. The PLL compares the phase difference between the input signal and the output signal of a voltage-controlled oscillator (VCO). The PLL performs phase synchronization to maintain a constant phase angle (lock) on the frequency of the input or reference signal. The synchronization or negative feedback loop of the system forces the PLL to be phase-locked.

You can configure PLLs as frequency multipliers, dividers, demodulators, tracking generators, or clock recovery circuits. You can use PLLs to generate stable frequencies, recover signals from a noisy communication channel, or distribute clock signals throughout your design.

Building Blocks of a PLL

The main blocks of the PLL are the phase frequency detector (PFD), charge pump, loop filter, VCO, and counters, such as a feedback counter (`M`), a pre-scale counter (`N`), and post-scale counters (`C`). The PLL architecture depends on the device you use in your design.

Figure 1: Typical PLL Architecture



The following terms are commonly used to describe the behavior of a PLL:

- PLL lock time—also known as the PLL acquisition time. PLL lock time is the time for the PLL to attain the target frequency and phase relationship after power-up, after a programmed output frequency change, or after a PLL reset.

  Note: Simulation software does not model a realistic PLL lock time. Simulation shows an unrealistically fast lock time. For the actual lock time specification, refer to the device datasheet.
- PLL resolution—the minimum frequency increment value of a PLL VCO. The number of bits in the `M` and `N` counters determine the PLL resolution value.
- PLL sample rate—the F_{REF} sampling frequency required to perform the phase and frequency correction in the PLL. The PLL sample rate is f_{REF} /`N`.

Related Information

Phase-Locked Loop Basics, PLL page of the Intel website
Provides more information about the PLL building blocks.

PLL Lock

The PLL lock is dependent on the two input signals in the phase frequency detector. The lock signal is an asynchronous output of the PLLs.

The number of cycles required to gate the lock signal depends on the PLL input clock which clocks the gated-lock circuitry. Divide the maximum lock time of the PLL by the period of the PLL input clock to calculate the number of clock cycles required to gate the lock signal.

Operation Modes

The Altera PLL IP core supports six different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and duty-cycle programming.

The following list describes the operation modes for the Altera PLL IP core:

- Direct mode—the PLL minimizes the feedback path length to produce the smallest possible jitter at the PLL output. In this mode, the PLL does not compensate for any clock networks.
- Normal mode—the PLL feedback path source is a global or regional clock network, minimizing clock delay from the input clock pin to the core registers through global or regional clock network.
- Source-Synchronous mode—the data and clock signals arrive at the input pins at the same time. In this mode, the signals have the same phase relationship at the clock and data ports of any Input Output Enable register.
- External Feedback mode—the PLL compensates for the `fbclk` feedback input to the PLL, thus minimizing the delay between the input clock pin and the feedback clock pin.
- Zero-Delay Buffer mode—the PLL feedback path is confined to the dedicated PLL external output pin. The clock port driven off-chip is phase aligned with the clock input for a minimal delay between the clock input and the external clock output.
- LVDS mode— maintains the same data and clock timing relationship of the pins at the internal SERDES capture register. This mode compensates for the LVDS clock network delay, plus any delay difference between the data pin and clock input pin to the SERDES capture register paths. The compensation mimic path mimics the clock and data delay of the receiver side.

Related Information

- **Clock Feedback Modes, Clock Networks and PLLs in Arria V Devices chapter**
- **Clock Feedback Modes, Clock Networks and PLLs in Cyclone V Devices chapter**
- **Clock Feedback Modes, Clock Networks and PLLs in Stratix V Devices chapter**

Output Clocks

The Altera PLL IP core can generate up to 18 clock output signals for the Stratix V and Arria V devices, and nine clock output signals for the Cyclone V devices. The generated clock output signals clock the core or the external blocks outside the core.

You can use the `reset` signal to reset the output clock value to 0 and disable the PLL output clocks.

Each output clock has a set of requested settings where you can specify the value of output frequency, phase shift, and duty cycle. The requested settings are the settings that you want to implement in your design.

The actual frequency is the closest frequency setting (best approximate of the requested settings) that can be implemented in the PLL circuit.

The output frequencies are not exact when the PLL is in fractional mode. You must be cautious with appliances that require frequencies to be exact to within less than 0.5 Hz.

For applications that require more precise clock output frequencies, turn on **Enable physical output clock parameters** in the parameter editor.

Related Information

- **Arria V PLLs, Clock Networks and PLLs in Arria V Devices chapter**
- **Cyclone V PLLs, Clock Networks and PLLs in Cyclone V Devices chapter**
- **Stratix V PLLs, Clock Networks and PLLs in Stratix V Devices chapter**

Reference Clock Switchover

The reference clock switchover feature allows the PLL to switch between two reference input clocks. Use this feature for clock redundancy, or for a dual clock domain application such as in a system. The system can turn on a redundant clock if the primary clock stops running.

Using the reference clock switchover feature, you can specify the frequency for the second input clock, and select the mode and delay for the switchover.

The clock loss detection and reference clock switchover block has the following functions:

- Monitors the reference clock status. If the reference clock fails, the clock automatically switches to a backup clock input source. The clock updates the status of the `clkbad` and `activeclk` signals to alert the event.
- Switches the reference clock back and forth between two different frequencies. Use the `extswitch` signal to manually control the switch action. After a switchover occurs, the PLL may lose lock temporarily and then regain lock.

PLL-to-PLL Cascading

The Altera 28 nm devices instantiate the Altera PLL IP core to allow cascading for PLLs in normal or direct mode through the Global Clock (GCLK) network.

If you cascade PLLs in your design, the source (upstream) PLL must have a low-bandwidth setting, while the destination (downstream) PLL must have a high-bandwidth setting. During cascading, the output of source PLL serves as the reference clock (input) of the destination PLL. The bandwidth settings of cascaded PLLs must be different. If the bandwidth settings of the cascaded PLLs are the same, the cascaded PLLs may amplify phase noise at certain frequencies.

The Altera PLL IP core allows you to choose the following input clock sources to cascade with an upstream PLL:

- `adjpllin`—for inter-cascading between fracturable fractional PLLs.
- `cclk`—for intra-cascading within fracturable fractional PLLs.

The `cclk` input clock source is not supported in Cyclone V devices.

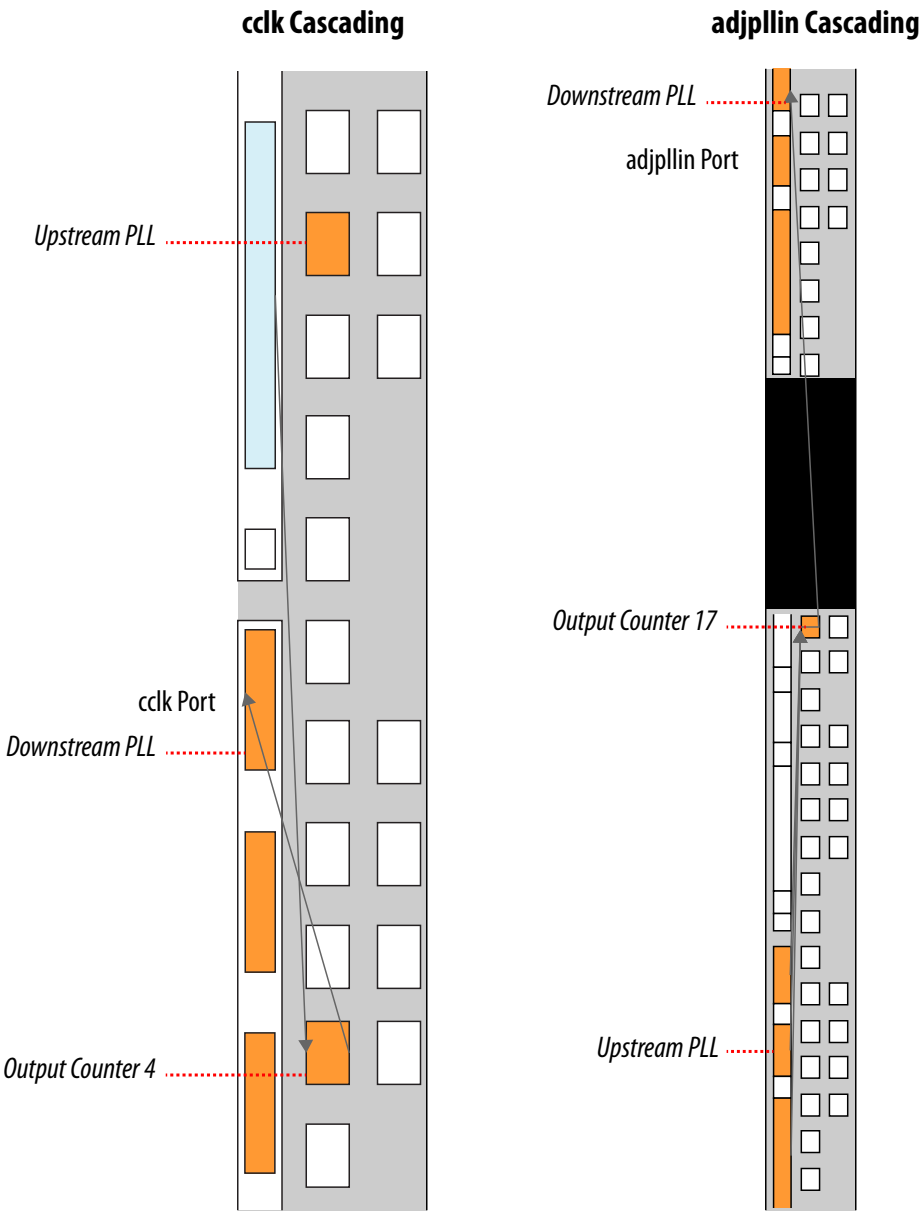
Table 7: `adjpllin` Cascading for Supported Devices

Device	adjpllin Cascading (Upstream PLL — Downstream PLL)
• Arria V GX B5 and B7 • Arria V GT D7	• FRACTIONALPLL_X0_Y96 — FRACTIONALPLL_X0_Y63 • FRACTIONALPLL_X183_Y96 — FRACTIONALPLL_X183_Y63
Arria V GZ E5 and E7	• FRACTIONAL_X0_Y31 — FRACTIONALPLL_X0_Y46 • FRACTIONALPLL_X202_Y31 — FRACTIONALPLL_X202_Y46
• Arria V SX B3 and B5 • Arria V ST D3 and D5	FRACTIONALPLL_X0_Y96 — FRACTIONALPLL_X0_Y63
• Cyclone V E A5 • Cyclone V GX C4 and C5 • Cyclone V GT D5 • Cyclone V SE A2 and A4 • Cyclone V SX C2 and C4	FRACTIONALPLL_X0_Y14 — FRACTIONALPLL_X0_Y30
• Cyclone V E A7 • Cyclone V GX C7 • Cyclone V GT D7 • Cyclone V SE A5 and A6 • Cyclone V SX C5 and C6	FRACTIONALPLL_X0_Y15 — FRACTIONALPLL_X0_Y32
• Cyclone V E A9 • Cyclone V GX C9 • Cyclone V GT C9	• FRACTIONALPLL_X0_Y22 — FRACTIONALPLL_X0_Y39 • FRACTIONALPLL_X0_Y64 — FRACTIONALPLL_X0_Y81
• Stratix V GS D5 • Stratix V GX A3 (with 36 transceivers) and A4	• FRACTIONALPLL_X0_Y31 — FRACTIONALPLL_X0_Y46 • FRACTIONALPLL_X202_Y31 — FRACTIONALPLL_X202_Y46
Stratix V GX B5 and B6	• FRACTIONALPLL_X0_Y14 — FRACTIONALPLL_X0_Y30 • FRACTIONALPLL_X0_Y76 — FRACTIONALPLL_X0_Y63 • FRACTIONALPLL_X0_Y100 — FRACTIONALPLL_X0_Y85 • FRACTIONALPLL_X197_Y14 — FRACTIONALPLL_X197_Y30 • FRACTIONALPLL_X197_Y76 — FRACTIONALPLL_X197_Y63 • FRACTIONALPLL_X197_Y100 — FRACTIONALPLL_X197_Y85
• Stratix V GT C5 and C7 • Stratix V GX A5 and A7	• FRACTIONALPLL_X0_Y29 — FRACTIONALPLL_X0_Y44 • FRACTIONALPLL_X0_Y91 — FRACTIONALPLL_X0_Y75 • FRACTIONALPLL_X210_Y29 — FRACTIONALPLL_X210_Y44 • FRACTIONALPLL_X210_Y91 — FRACTIONALPLL_X210_Y75

Device	adjpllin Cascading (Upstream PLL — Downstream PLL)
Stratix V GS D6 and D8 Devices	• FRACTIONALPLL_X0_Y41 — FRACTIONALPLL_X0_56 • FRACTIONALPLL_X0_Y103 — FRACTIONALPLL_X0_Y87 • FRACTIONALPLL_X208_Y41 — FRACTIONALPLL_X208_56 • FRACTIONALPLL_X208_Y103 — FRACTIONALPLL_X208_Y87
• Stratix V E E9 and EB • Stratix V GX A9, AB, B9, and BB	• FRACTIONALPLL_X0_Y38 — FRACTIONALPLL_X0_Y52 • FRACTIONALPLL_X0_Y99 — FRACTIONALPLL_X0_Y86 • FRACTIOANLPLL_X0_Y124 — FRACTIONALPLL_X0_Y108(6) • FRACTIONALPLL_X225_Y38 — FRACTIONALPLL_X225_Y52 • FRACTIONALPLL_X225_Y99 — FRACTIONALPLL_X225_Y86 • FRACTIOANLPLL_X225_Y124 — FRACTIONALPLL_X225_Y108(6)

(6) This PLL is not available for Stratix V E E9 and EB devices, and Stratix V GX A9 and AB devices.

Figure 2: PLL `cclk` Cascading and `adjpllin` Cascading Modes



The clock input to PLL comes from the clock input multiplexers. The clock input multiplexers provide multiple clock sources as reference clock inputs for fractional PLL.

Table 8: Reference Clock Inputs for Fractional PLL

Sources	Description
`coreclkin`	Core reference clock from clock network.
`adjpllin`	Adjacent fractional PLL clock source.

Sources	Description
refclkin[0]	Clock source from adjacent PMA triplet LVPECL buffer.
refclkin[1]	Clock source from adjacent PMA triplet LVPECL buffer.
clkin[0]	Dedicated clock input for fractional PLL from regular I/O.
clkin[1]	Dedicated clock input for fractional PLL from regular I/O.
clkin[2]	Dedicated clock input for fractional PLL from regular I/O.
clkin[3]	Dedicated clock input for fractional PLL from regular I/O.
rxiqclk	Clock source from adjacent PMA triplet rxiqclknet. For refclk and PMA/LC cascading with fractional PLL.
refiqclk	Clock source from adjacent PMA triplet rxiqclknet as refclk.
iqtxrxclk	Clock source from adjacent PMA triplet iqtxrxclk as refclk.
cclk[7]	C-Counter clock source.

PLL Output Counter Cascading

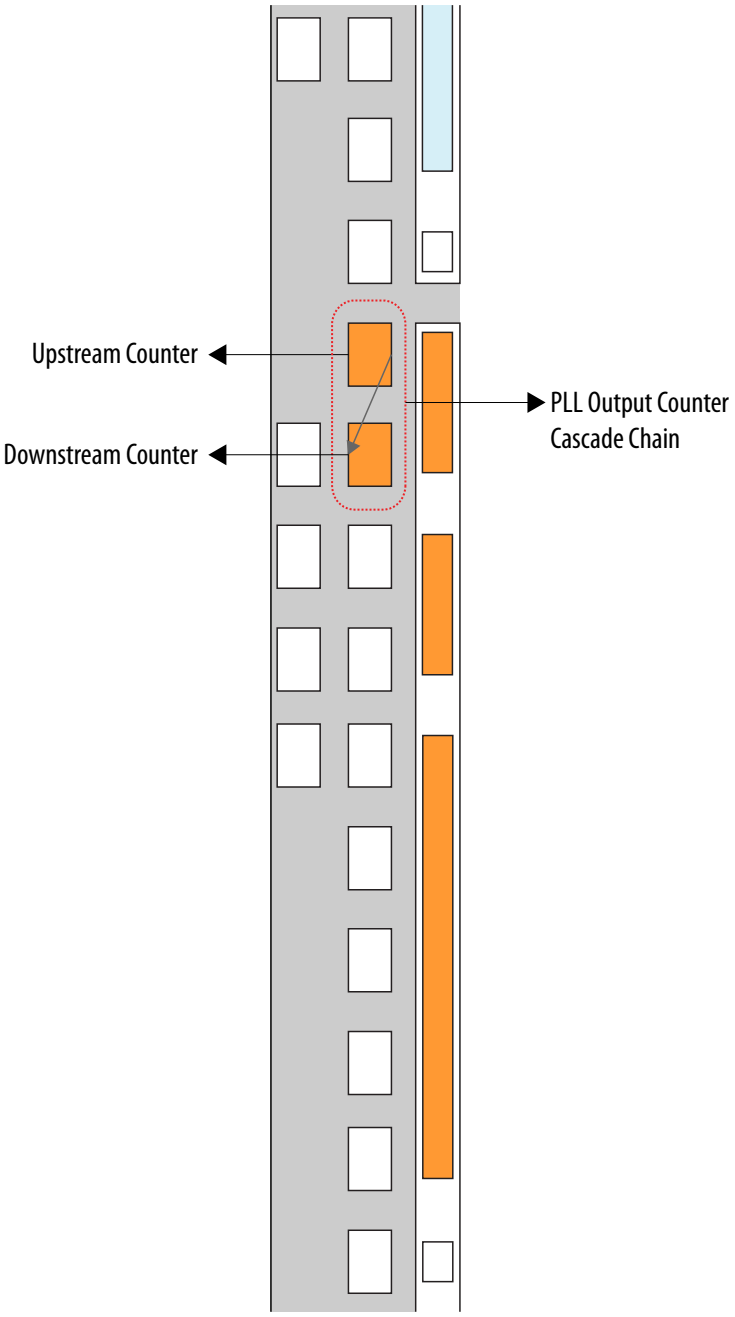
The Altera 28 nm devices instantiate the Altera PLL IP core to allow output counter cascading. PLL cascading enables PLL to synthesize a lower frequency output which is not achievable with a single counter output.

This feature is only accessible when **Enable physical output clock parameters** is turned on. Turn on **Make this a cascade counter** to select an outclk port as the upstream counter. The upstream counter serves as the reference clock to the downstream counter and not available as a PLL output.

Only the upstream counter in the PLL output counter cascade chain supports phase shifting and only the downstream counter in the cascade chain support programmable duty cycle.

[7] Not supported in Cyclone V devices.

Figure 3: PLL Output Counter Cascading Mode



Ports

Table 9: Altera PLL Ports

Port Name	Type	Condition	Description
`fbclk`	Input	Optional	The external feedback input port for the PLL. The Altera PLL IP core creates this port when the PLL is operating in external feedback mode or zero-delay buffer mode. To complete the feedback loop, a board-level connection must connect the `fbclk` port and the external clock output port of the PLL.
`fboutclk`	Output	Optional	The port that feeds the `fbclk` port through the mimic circuitry. The `fboutclk` port is available only if the PLL is in external feedback mode.
`locked`	Output	Optional	The Altera PLL IP core drives this port high when the PLL acquires lock. The port remains high as long as the PLL is locked. The PLL asserts the `locked` port when the phases and frequencies of the reference clock and feedback clock are the same or within the lock circuit tolerance. When the difference between the two clock signals exceeds the lock circuit tolerance, the PLL loses lock.
`outclk[]`	Output	Required	The clock output of the PLL. The frequency of the output clock depends on the parameter settings.
`refclk`	Input	Required	The reference clock that drives the clock network.
`reset`	Input	Required	The asynchronous reset port for the output clocks. Drive this port high to reset all output clocks to the initial value of 0.
`zdbfbclk`	Bidirectional	Optional	The bidirectional port that connects to the mimic circuitry. This port must connect to a bidirectional pin that is placed on the positive feedback dedicated output pin of the PLL. The `zdbfbclk` port is available only if the PLL is in zero-delay buffer mode.
`refclk1`	Input	Required	Second input clock signal that feeds into the PLL.

Port Name	Type	Condition	Description
extswitch	Input	Required	Assert this input signal high (1'b1) to manually switch the clock for at least 3 cycles.
activeclk	Output	Optional	Output signal to determine which input clock is in use by the PLL.
clkbad	Output	Optional	Output signal to determine which input clock is working.
cclk[8]	Input	Optional	C-Counter clock source from the fracturable fractional PLL output counter 4 or 13.
adjpllin	Input	Optional	Adjacent fractional PLL clock source.
cascade_out	Output	Optional	Output signal to feed into other fractional PLLs. This port acts as a bus port when the upstream PLL has two or more output clocks.

Document Revision History

Date	Version	Changes
June 2017	2017.06.16	• Added Cyclone V SE and SX devices in adjpllin Cascading for Supported Devices table. • Changed instances of *Quartus II* to *Quartus Prime*.

May 2015	2015.05.04	• Added Arria V and Cyclone V devices in adjpllin Cascading for Supported Devices table.
		• cclk input clock source is not supported in Cyclone V devices. Updated the information and notes in the following locations:
		  • Altera PLL IP Core Parameters - Cascading Tab table
		  • PLL-to-PLL Cascading section
		  • Reference Clock Inputs for Fractional PLL table
		  • Altera PLL Ports table

August 2014	2014.08.01	• Grouped parameters in separate tables according to parameter editor tabs. • Added parameters for the General tab and Cascading tab. • Updated parameters for the Clock Switchover tab. • Updated information on PLL-to-PLL Cascading. • Added information on PLL output counter cascading.
December 2013	1.3	Updated Table 3 on page 10 to update reset port information.

[8] Not supported in Cyclone V devices.

Date	Version	Changes
March 2013	1.2	• Added the "Reference Clock Switchover" section. • Added the "PLL to PLL Cascading" section. • Added new parameters for the following features: clock switchover, PLL cascading, MIF streaming, and PLL settings, in Table 1. • Added the following new ports: refclk1, extswitch, activeclk, clkbad, cclk, adjpilin, and cascade_out, in Table 3 and Figure 3.
January 2011	1.1	• Added two new parameters in Table 1. • Updated Figure 3: ALTERA PLL Ports.
July 2010	1.0	Initial release.