CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A070PAN01.0**
CUSTOMER APPROVED	

☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.0)**

☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.0)**

☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.0)**

☐ **CUSTOMER REMARK :**

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Product Specification

7.0 INCH COLOR TFT-LCD MODULE

Model Name : **A070PAN01.0**

Planned Lifetime:	From 2012/Aug To 2013/Jul
Phase-out Control:	From 2013/Jan To 2013/Jul
EOL Schedule:	2013/Jul

<■> Preliminary Specification
<□> Final Specification

Note: The contents of this specification are subject to change without further notice.

Record of Revision

Version	Revise Date	Page	Content
0.0	2012/Mar/28	All	First Draft

Contents

A. General Information

This product is for CE Brand Tablet application.

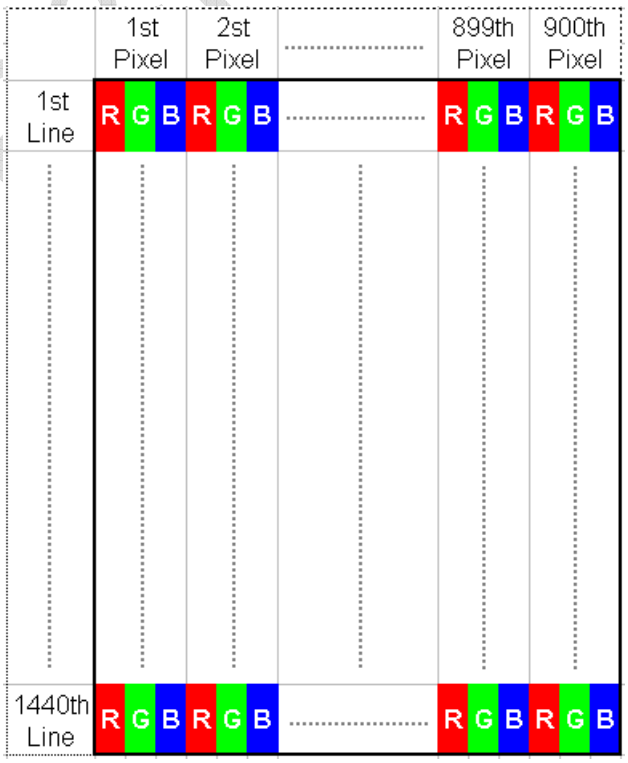
NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	7(Diagonal)	
2	Display Resolution	dot	900RGB(W)x1440(H)	
3	Overall Dimension	mm	104.65x163.7x2.14	Note 1
4	Active Area	mm	94.23(W)x150.768(H)	
5	Pixel Pitch	mm	0.1047(W)x0.1047(H)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	16.7M Colors	Note 3
8	NTSC Ratio	%	50	
9	Display Mode	--	Normally Black	
10	Panel surface Treatment	--	PET	
11	Weight	g	65	
12	Panel Power Consumption	**mW**	55	Note 4
13	Backlight Power Consumption	W	1.2	
14	Viewing direction		AHVA	

Note 1: Not include blacklight cables, FPC and PCB. Refer to the next page for further information.

Note 2: Below figure shows dot stripe arrangement.

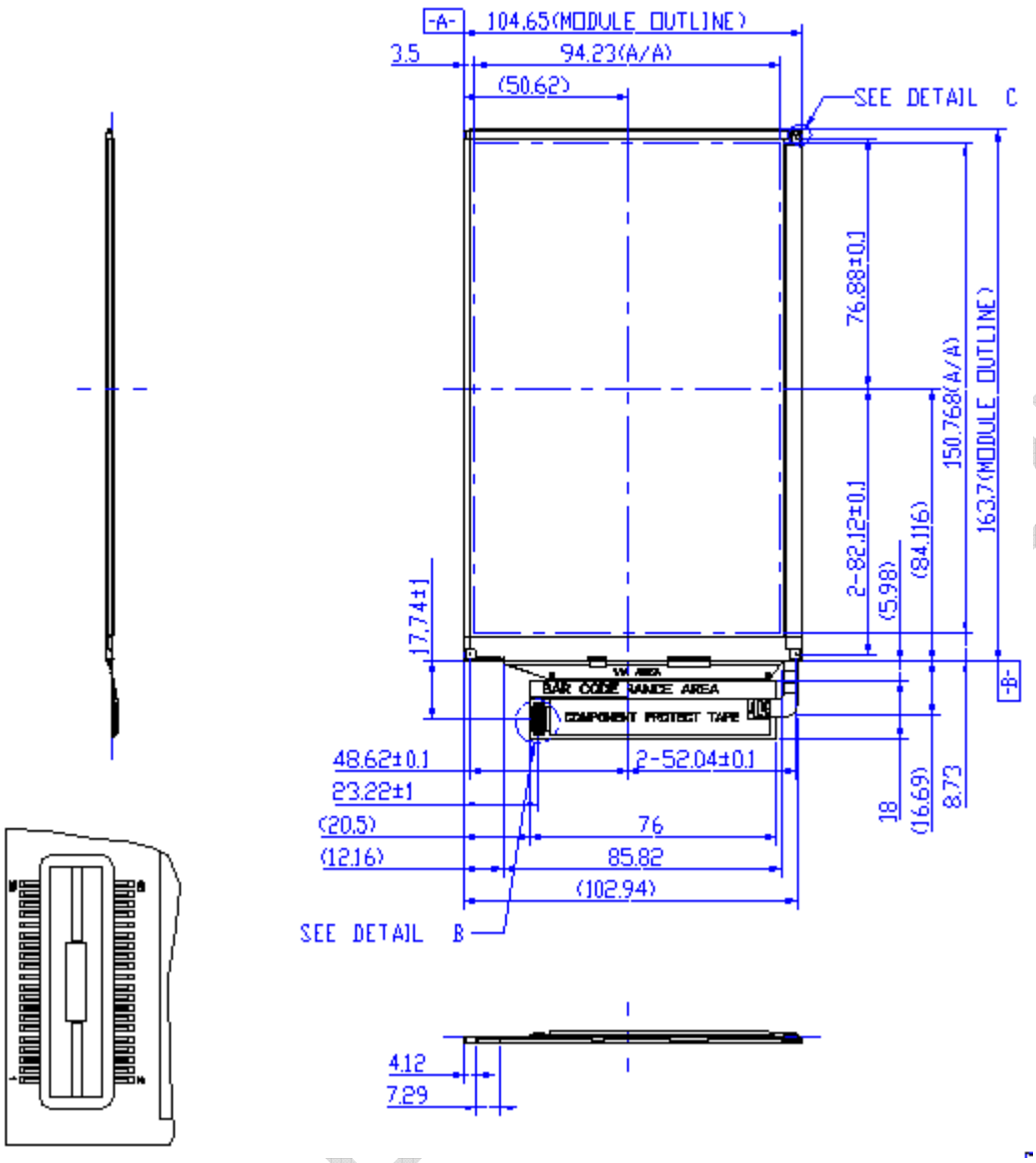
Note 3: Refer to the Electrical Characteristics chapter.at page 9

Note 4: Refer to the pattern at page 26

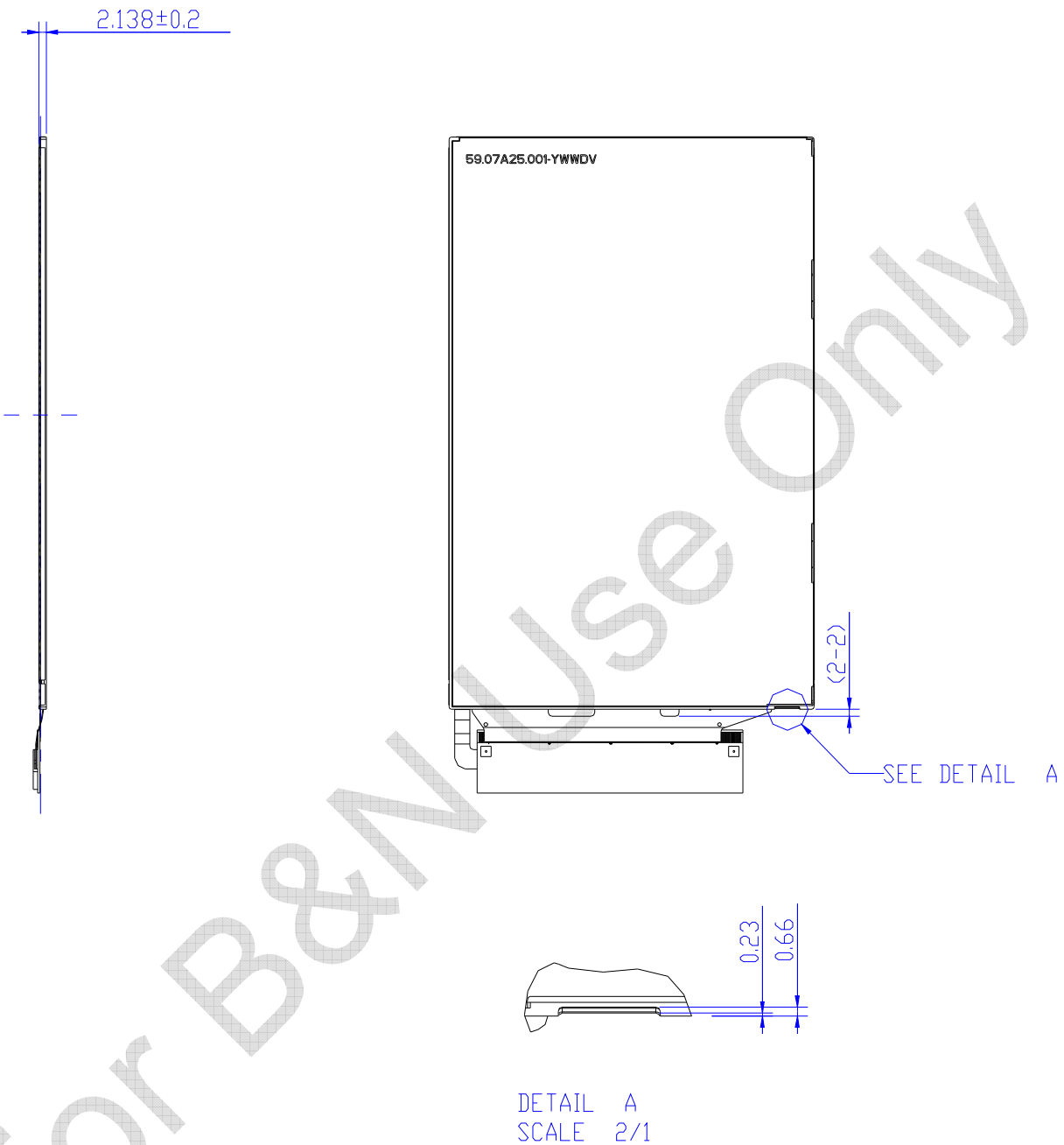


B. Outline Dimension

1. TFT-LCD Module-Front View



2. TFT-LCD Module-Rear View



UNIT	SCALE	WEIGHT	ANGLE GENERAL TOLERANCE	3rd Angle	ORIGINAL M
mm	1/2	-	±1°		A070PANC

al tolerance ±		
2	3	SELECT LEVEL
0.1	0.1	
0.1	0.1	
0.1	0.2	
0.2	0.3	-
0.3	0.5	
	0.8	

MATERIAL	-	CRITICAL DIMENSION
FINISH		MAJOR DIMENSION
APPROVED		CHECK-CODE DIMENSION
CHECKED		
DESIGNED	RJ Deng	2012/03/19

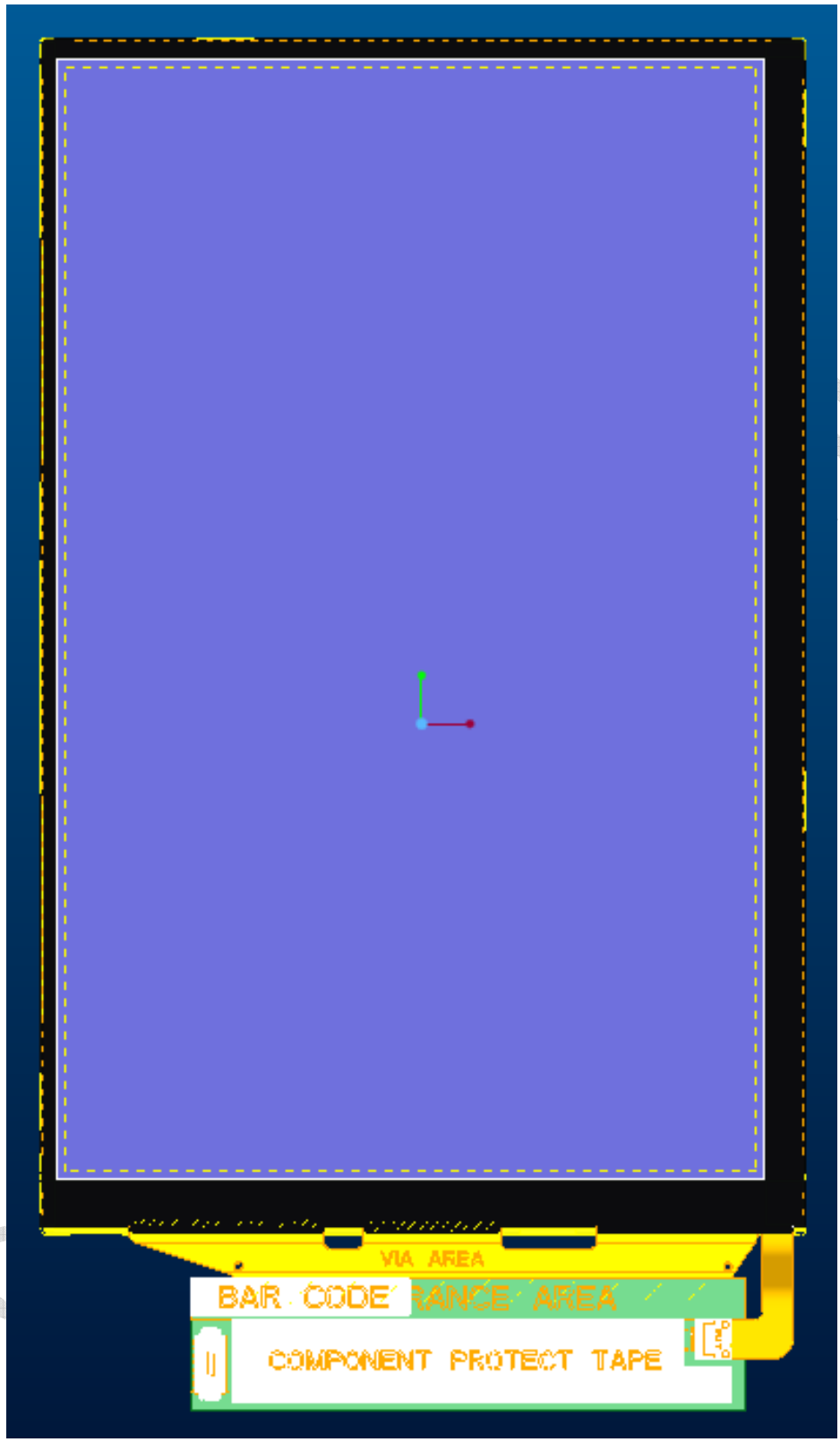
TITLE	ASSY MODULE A070PAN01.0		
DRAWING NO.(PART NO.)	97.07A25.001		
AU Optronics		SIZE A3	SHT 1/1

C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

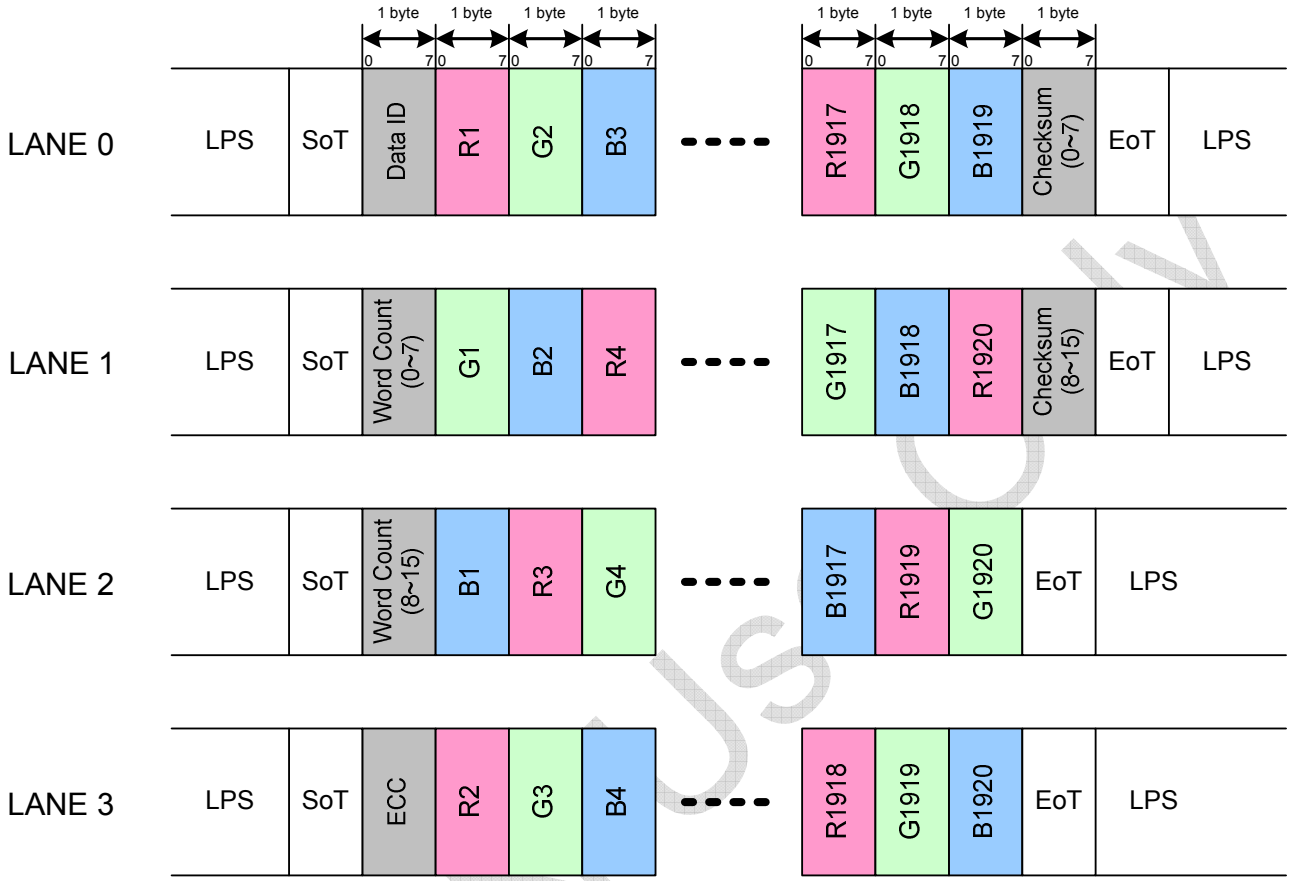
Recommended connector : JAE/WHIP040WA1

PIN	FUNCTION	Name	PIN	SYMBOL	FUNCTION
1	Ground	GND	2	VDD	Input Power (3.3V)
3	DSI Lane 0 Neg	MIPI_DO_N	4	VDD	Input Power (3.3V)
5	DSI Lane 0 Pos	MIPI_DO_P	6	VDD	Input Power (3.3V)
7	Ground	GND	8	GND	Ground
9	DSI Lane 1 Neg	MIPI_D1_N	10	GND	Ground
11	DSI Lane 1 Pos	MIPI_D1_P	12	GND	Ground
13	Ground	GND	14	CABC_EN	CABC Enable
15	DSI CLK Neg	MIPI_CLK_N	16	PWM_IN	BL PWM Input to LCM
17	DSI CLK Pos	MIPI_CLK_P	18	PWM_OUT	BL PWM Output from LCM
19	Ground	GND	20	GND	Ground
21	DSI Lane 2 Neg	MIPI_D2_N	22	AIE_EN	AIE Enable
23	DSI Lane 2 Pos	MIPI_D2_P	24	LED_A	BL LED Anode
25	Ground	GND	26	LED_A	BL LED Anode
27	DSI Lane 3 Neg	MIPI_D3_N	28	LED_A	BL LED Anode
29	DSI Lane 3 Pos	MIPI_D3_P	30	NC	NC
31	Ground	GND	32	LED_C1	BL LED Cathode String 1
33	CM Enable	CM_EN	34	LED_C2	BL LED Cathode String 2
35	Self-test	AGMODE	36	LED_C3	BL LED Cathode String 3
37	SCL	I2C Clock	38	LED_C4	BL LED Cathode String 4
39	SDA	I2C Data	40	NC	NC


VIA AREA
BAR CODE
COMPONENT PROTECT TAPE

2. The Input Data Format

Input Pixel Stream Format (1920RGB in 4 Lanes with RGB 8-8-8 format)



LPS : Low Power State
SoT : Start of Transmission
EoT : End of Transmission
ECC : Error-Correcting Code

3. Absolute Maximum Ratings

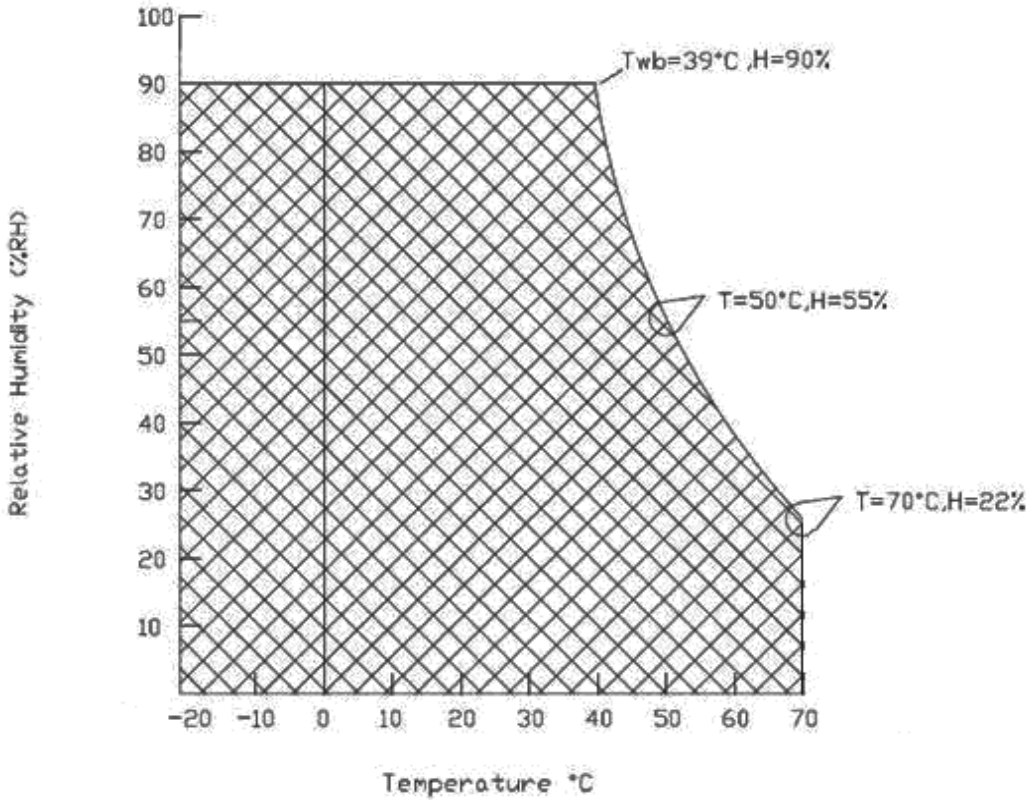
(a) Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit
Logic/LCD drive Voltage	Vin	-0.3	+4.0	[Volt]

(b) Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit
Operating Temperature	TOP	-10	+50	[°C]
Operation Humidity	HOP	5	90	[%RH]
Storage Temperature	TST	-20	+60	[°C]
Storage Humidity	HST	5	90	[%RH]

Note: Maximum Wet-Bulb should be 39 °C and no condensation.



Note 1: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

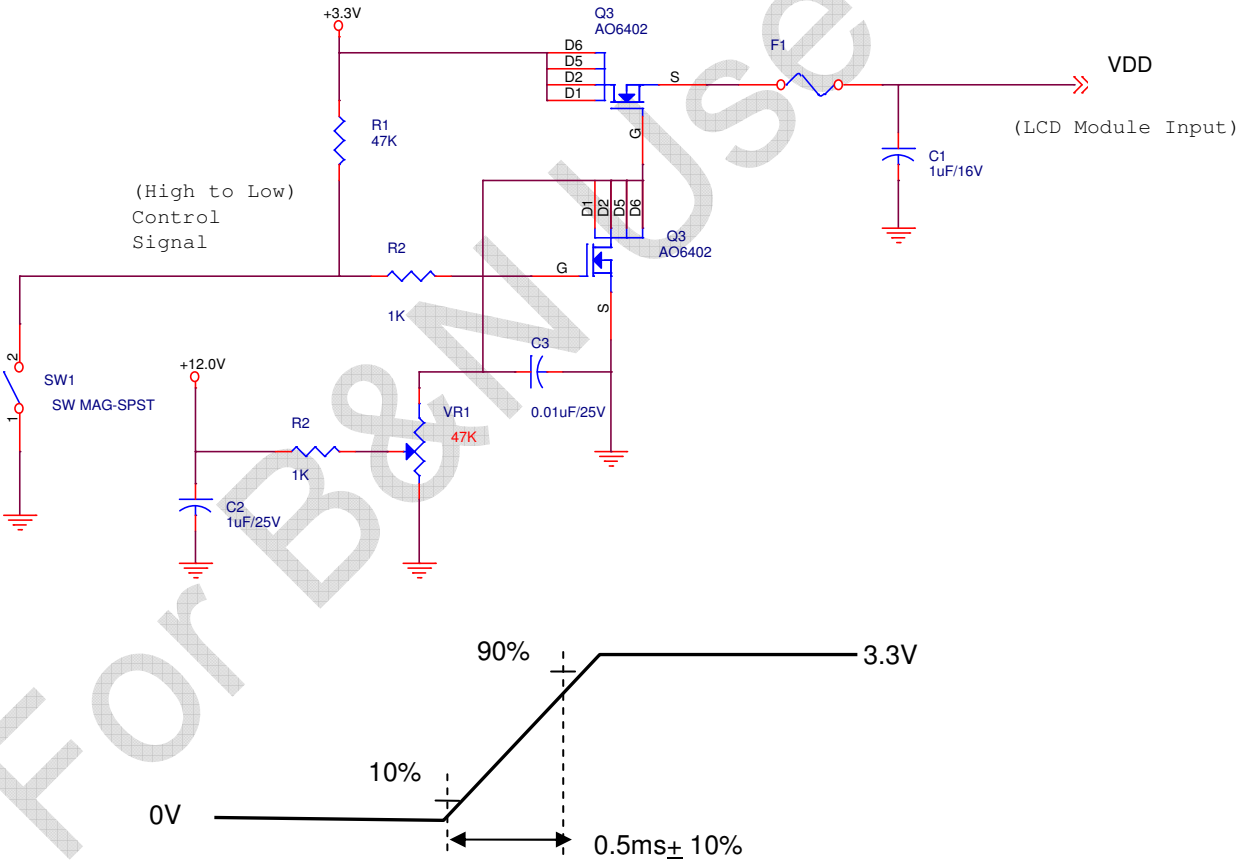
Note 2: Functional operation should be restricted under ambient temperature (25℃).

4. Electrical DC Characteristics

(a) DC Charateristics

Symbol	Parameter	Min	Typ	Max	Units	Remark
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
IDD	VDD Current	-	120	-	[mA]	10x10 Chess Pattern (VDD=3.3V, at 60Hz)
Irush	LCD Inrush Current	-	-	1.5	[A]	Note 1
PDD	VDD Power	-	0.4	-	[Watt]	10x10 Chess Pattern (VDD=3.3V, at 60Hz)
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	All white Pattern (VDD=3.3V, at 60Hz)

Note 1: Measurement condition:



VDD rising time

b. Backlight Driving Conditions

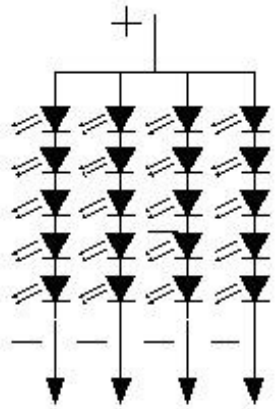
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Lightbar current	I_L	-	80	-	mA	Note 1, 2
LED Forward Voltage	Vf		15		V	
Power consumption	P		1.2	-	W	
LED Lightbar life time		TBD	-	-	Hr	Note 1, 2, 3, 4

Note 1: LED backlight is LED lightbar type(20 pcs of LED).

Note 2: Definition of “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED lightbar current= 80mA

Note 3: The value is only for reference.

Note 4: If it operates with LED lightbar voltage more than 80mA, it maybe decreases LED lifetime.



5. MIPI DC Characteristics

A. DC Characteristic

Input signals shall be low or High-impedance state when VDD is off.

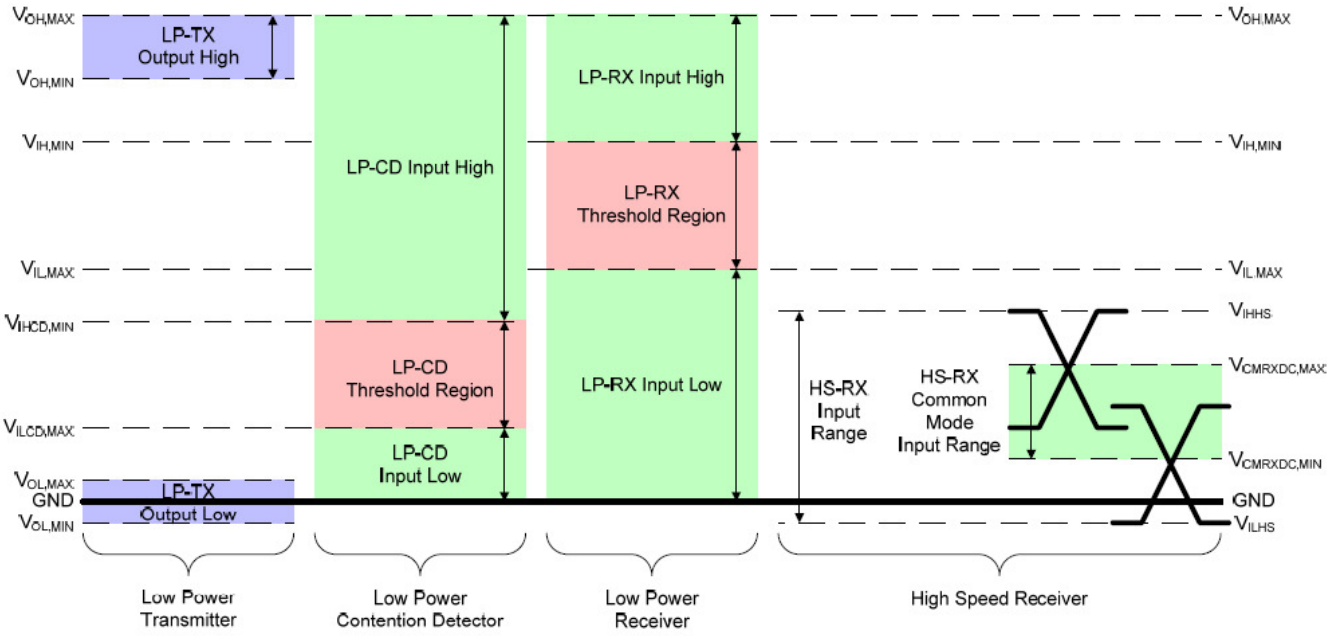
MIPI DC/AC Characteristics are as follows;

HS Receiver DC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	MIPI		2.25		3.6	V
V_{NOZ}	Supply Noise Voltage		-50	-	50	mV
$V_{CMRX(DC)}$	Differential common-mode range		70	-	330	mV
V_{IDTH}	Differential input high threshold		-	-	70	mV
V_{IDTL}	Differential Input Low Threshold		-70	-	-	mV
V_{IHHS}	Single-ended input high voltage		-	-	460	mV
V_{ILHS}	Single-ended input low voltage		-40	-	-	mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable		-	-	450	mV
Z_{ID}	Differential input impedance		80	100	125	Ω

LP Receiver DC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage		880	-	-	mV
V_{IL}	Logic 0 input voltage		-	-	550	mV
V_{HYST}	Input hysteresis		25	-	-	mV

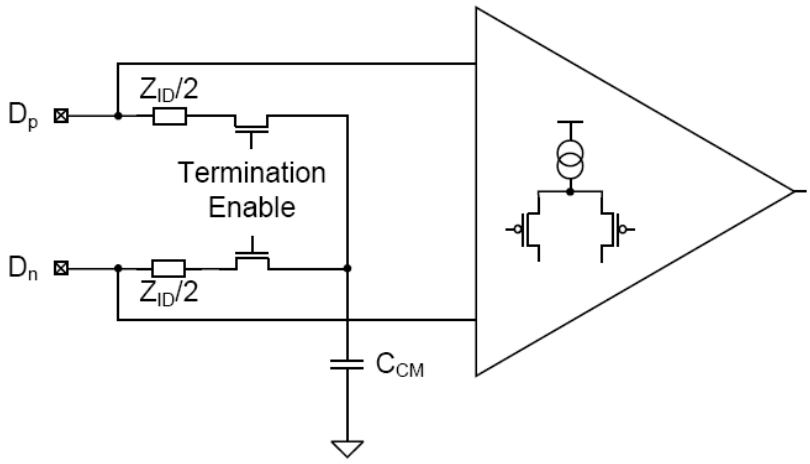
Contention Detector (LP-CD) DC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IHCD}	Logic 1 contention threshold		450	-	-	mV
V_{ILCD}	Logic 0 contention threshold		-	-	200	mV

Signaling and Contention Voltage Levels



HS Receiver AC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz		-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz ~ 450MHz		-50	-	50	mV
C_{CM}	Common-mode termination		-	-	60	pF
UI_{INST}	UI instantaneous	HF=0	2		12.5	ns
		HF=1	1		2	ns

HS RX Scheme



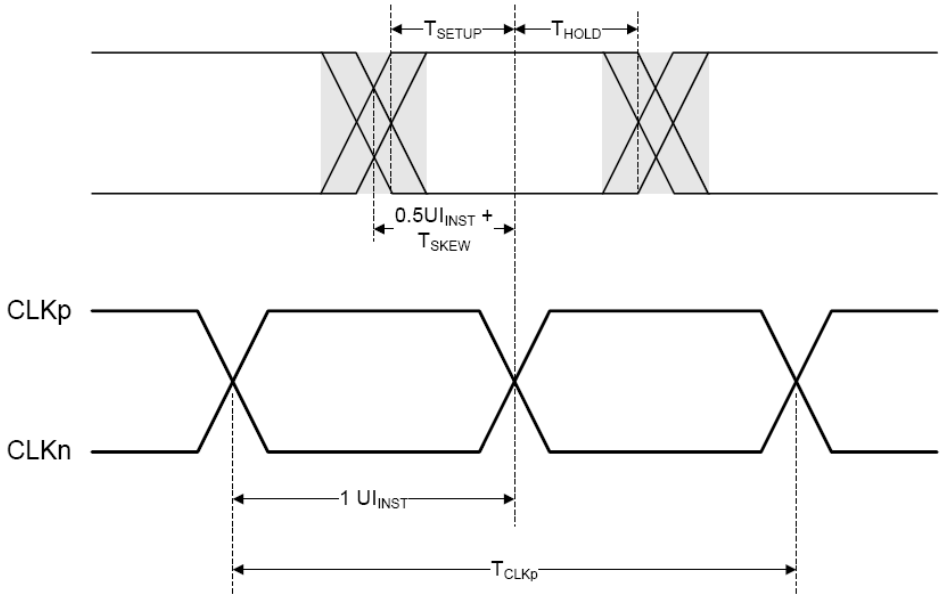
Symbol	Parameter	Min	Typ	Max	Unit	Notes
$T_{SKEW[TX]}$	Data to Clock Skew (mesured at transmitter)	-0.15		0.15	UI_{INST}	1
$T_{SETUP[RX]}$	Data to Clock Setup Time (receiver)	0.15			UI_{INST}	2
$T_{HOLD[RX]}$	Data to Clock Hold Time (receiver)	0.15			UI_{INST}	2

Note:

1. Total silicon and package delay budget of $0.3*UI_{INST}$

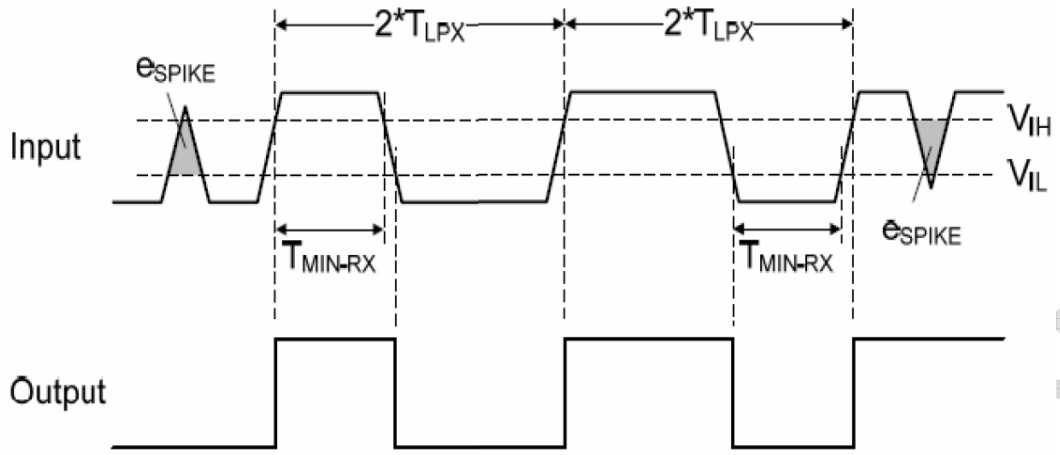
2. Total setup and hold window for receiver of $0.3*UI_{INST}$

High Speed Data Transmission: Data to Clock Timing

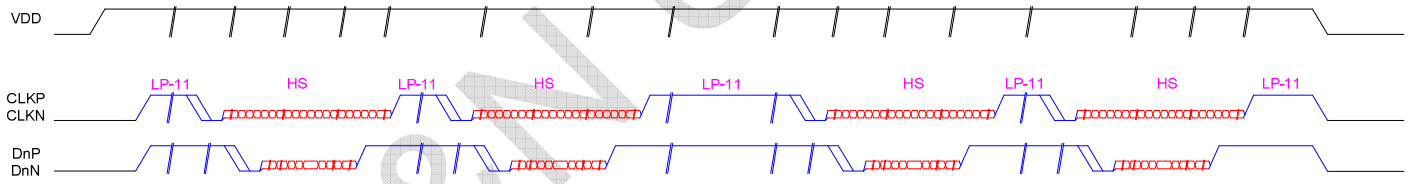


LP Receiver AC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
e_{SPIKE}	Input pulse rejection		-	-	300	V · ps
T_{MIN-RX}	Minimum pulse width response		20	-	-	ns
V_{INT}	Peak interference amplitude		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

Input Glitch Rejection of Low-Power Receivers



For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI lanes status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11 status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.



The timing definitions are listed in below,

Parameter	Description	Min	Typ	Max	Unit
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52*UI			ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns

TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			35 ns + 4*UI	ns
TEOT	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.			105 ns + 12*UI	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100			ns
THS-SYNC	HS Sync-Sequence '00011101' period		8		UI
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.	85 ns + 6*UI		145 ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns + 4*UI			ns
TLPX	Transmitted length of any Low-Power state period	50			ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	

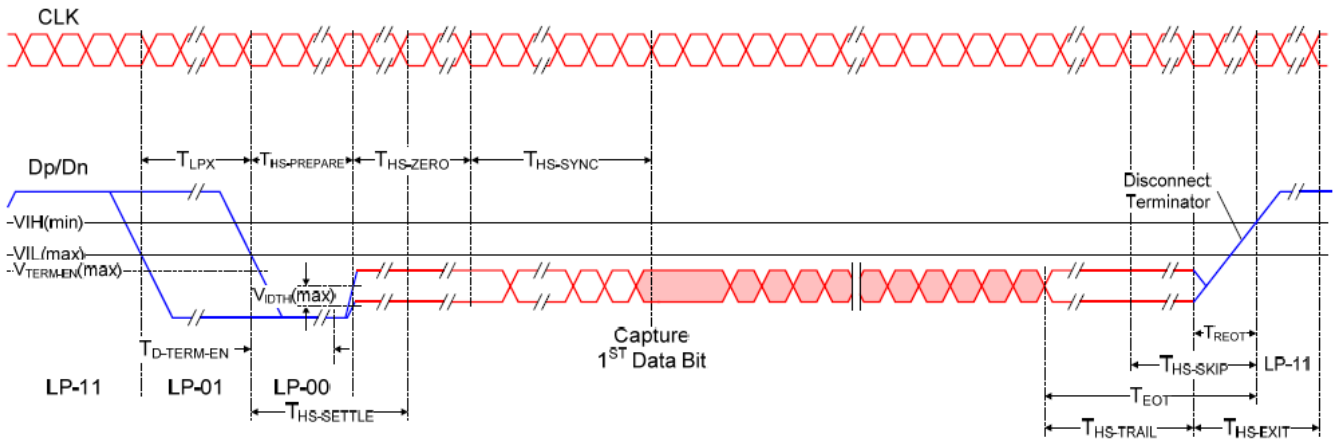
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*TLPX		ns
TTA-GO	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*TLPX		ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX		2*TLPX	ns

Note:

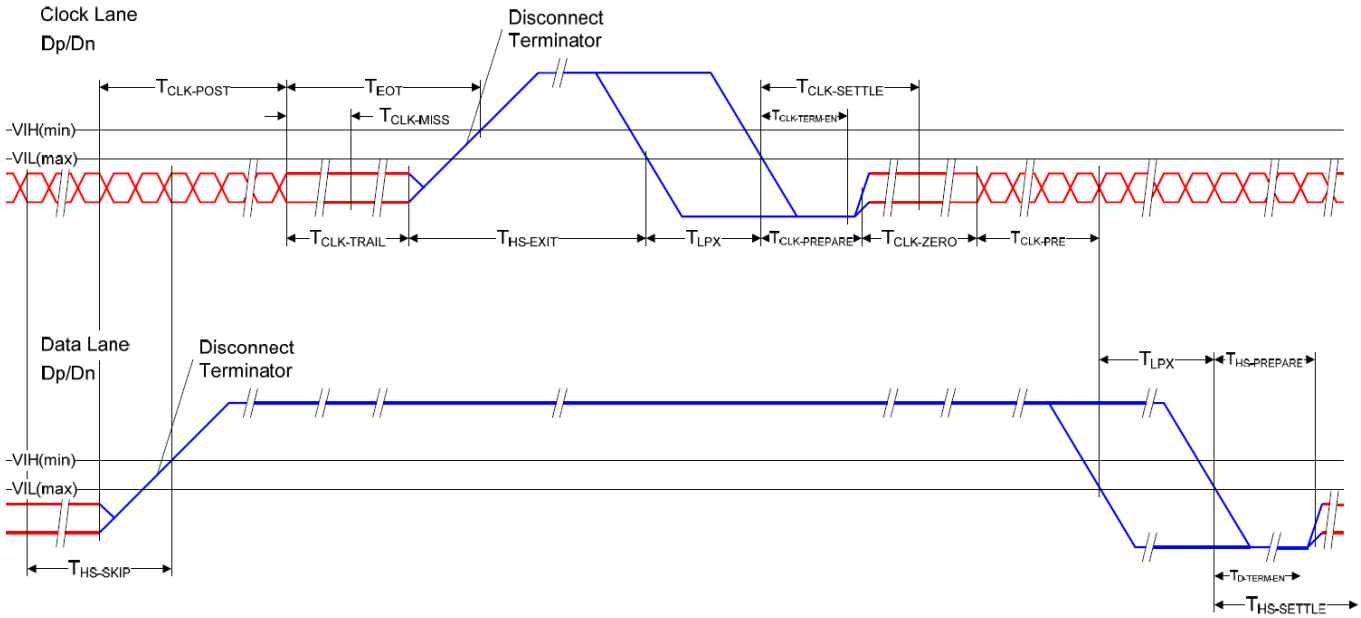
1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

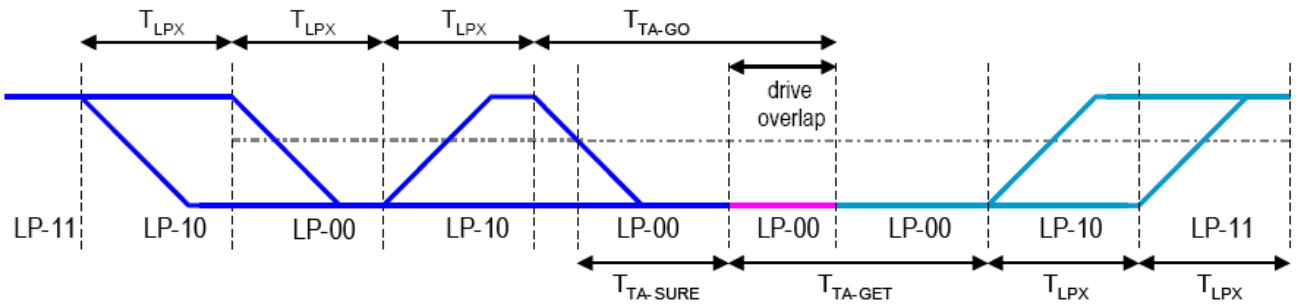
High-Speed Data Transmission in Bursts



Switching the Clock Lane between Clock Transmission and Low-Power Mode



Turnaround Procedure

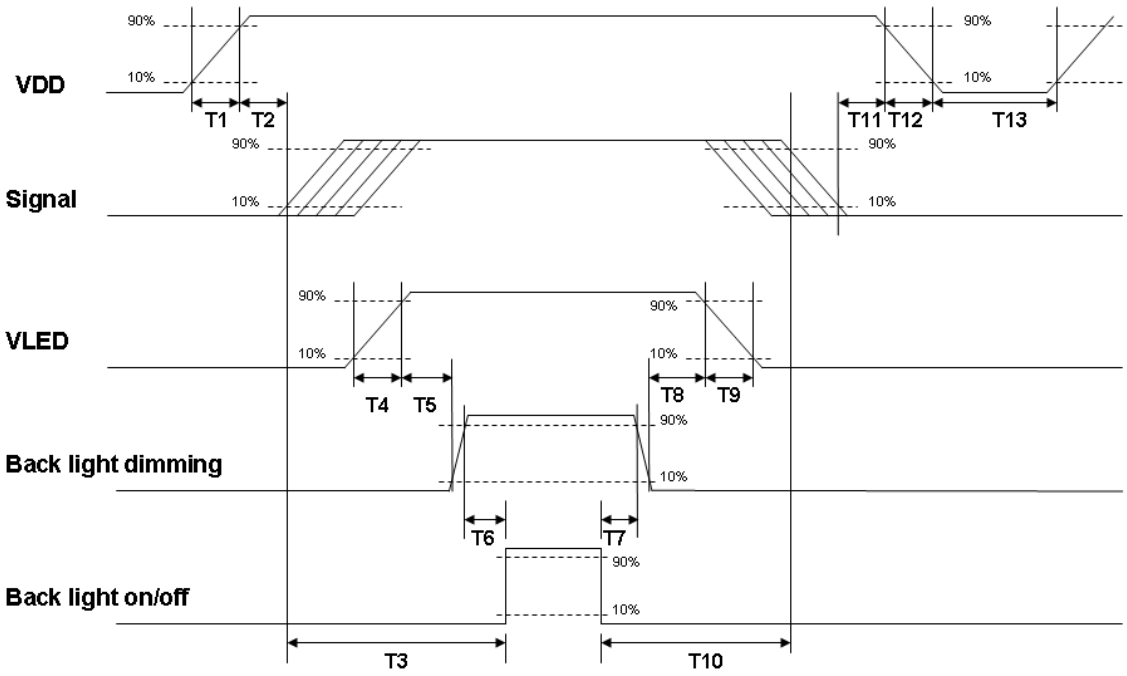


B. Input Timing Setting

Signal		Symbol	Min.	Typ.	Max.	Unit
Clock Frequency		1/ T_{Clock}	TBD	92.9	TBD	MHz
Vertical Section	Period	T_V	TBD	1460	TBD	T_{Line}
	Active	T_{VD}	--	1440	--	
	Blanking	T_{VB}	TBD	20	TBD	
Horizontal Section	Period	T_H	TBD	1060	TBD	T_{Clock}
	Active	T_{HD}	--	900	--	
	Blanking	T_{HB}	TBD	160	TBD	
Frame Rate		F	--	60	--	Hz

Note : DE mode.

c. Recommended Power On/OFF Sequence



Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	[ms]
T2	30	40	50	[ms]
T3	200	--	--	[ms]
T4	0.5	--	10	[ms]
T5	10	-	-	[ms]
T6	10	-	-	[ms]
T7	0	-	-	[ms]
T8	10	-	-	[ms]
T9	--	--	10	[ms]
T10	110	--	--	[ms]
T11	0	16	50	[ms]
T12	-	-	10	[ms]
T13	1000	-	-	[ms]

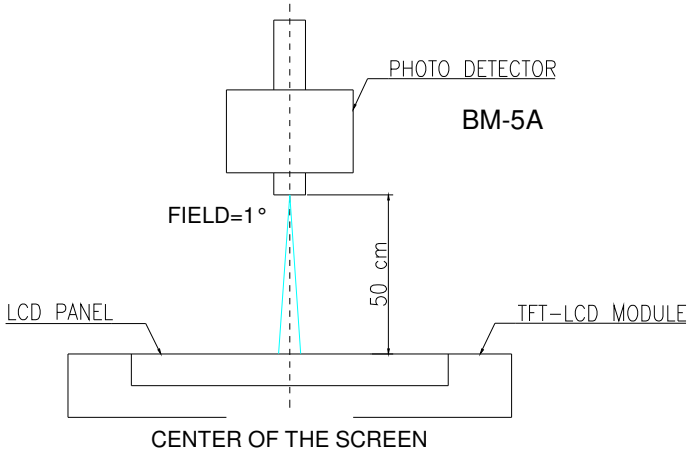
D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		Tr Tf	θ=0°	-- --	18 12	30 20	ms ms	Note 3
Contrast ratio		CR	At optimized viewing angle	--	800	--		Note 4
Viewing Angle	Top Bottom Left Right		CR≧10	70 70 70 70	85 85 85 85		deg.	Note 5
Brightness		Y_L	V_L = 12V	320	400	--	cd/m^2	Note 6
Chromaticity	White	X	θ=0°	0.273	0.313	0.353		
		Y	θ=0°	0.297	0.337	0.377		
	Red	X	θ=0°	TBD	TBD	TBD		
		Y	θ=0°	TBD	TBD	TBD		
	Green	X	θ=0°	TBD	TBD	TBD		
		Y	θ=0°	TBD	TBD	TBD		
	Blue	X	θ=0°	TBD	TBD	TBD		
		Y	θ=0°	TBD	TBD	TBD		
Uniformity 5 Points		ΔY_L	%	80	--	--	%	Note 7
Uniformity 13 Points		ΔY_L	%	70	--	--	%	Note 8

Note 1 : To be measured in the dark room temperature =25℃, and LED lightbar current I_L = 80mA.

Note 2 : To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-5A, after 15 minutes operation.

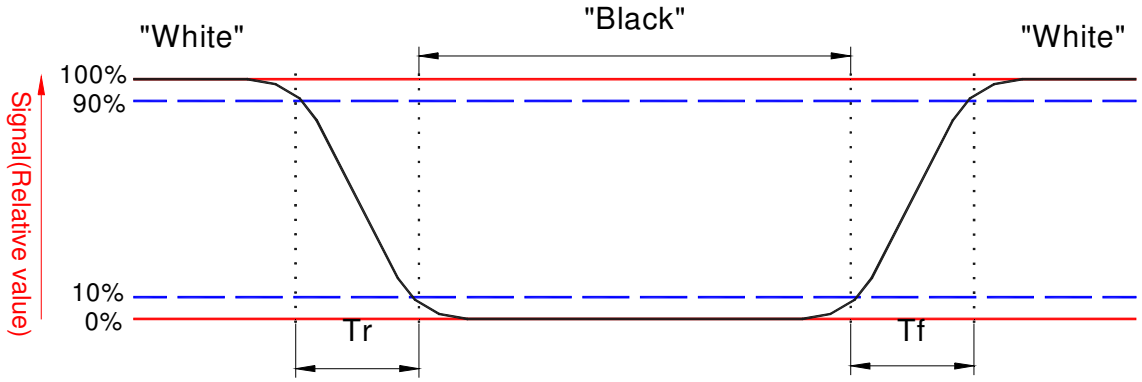


Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to

“white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

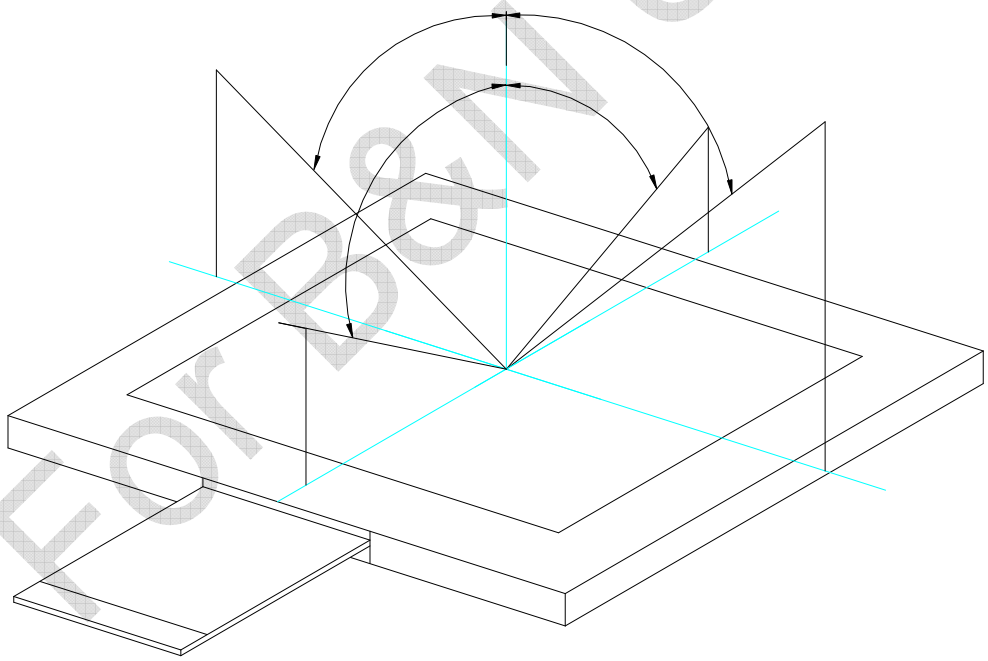


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

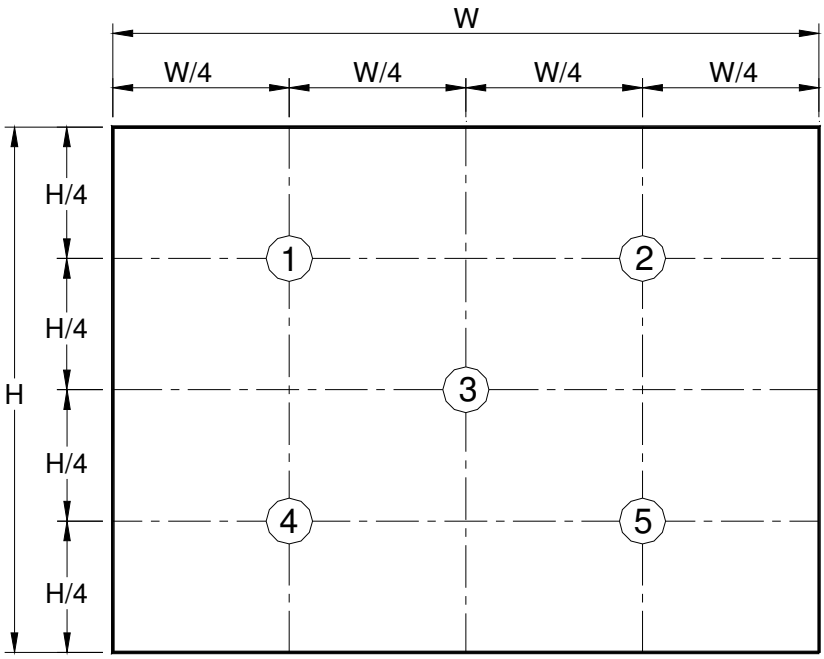
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



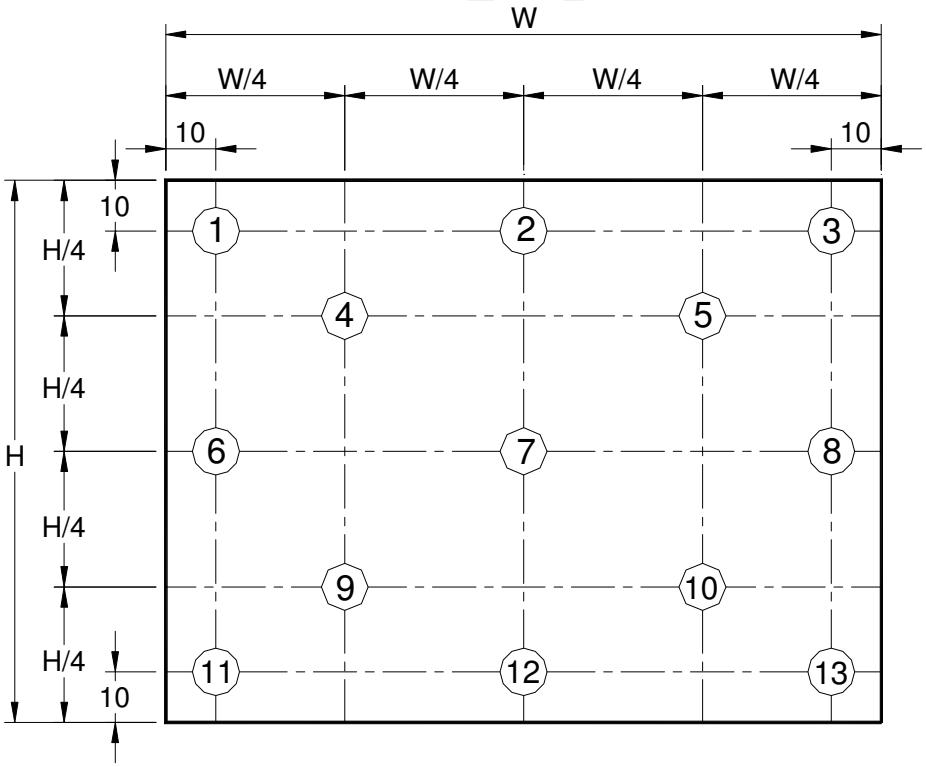
Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 5 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 5 points (1-5)}}{\text{maximum luminance in 5 points (1-5)}}$$

Note 8: Luminance Uniformity of these 13 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 13 points (1-13)}}{\text{maximum luminance in 13 points (1-13)}}$$

E. Reliability Test Items

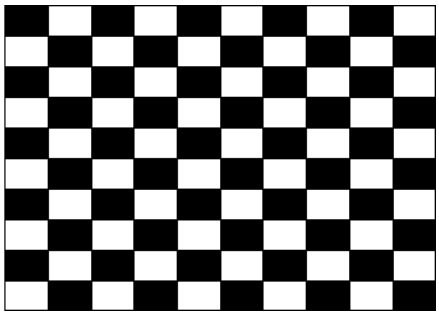
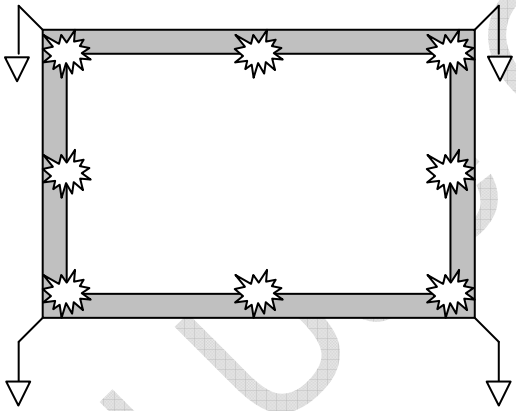
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 60℃ 240Hrs	
2	Low Temperature Storage	Ta= -20℃ 240Hrs	
3	High Ttemperature Operation	Tp= 50℃ 240Hrs	
4	Low Temperature Operation	Ta=-10℃ 240Hrs	
5	High Temperature & High Humidity	Tp= 60℃. 90% RH 240Hrs	Operation
6	Heat Shock	-20℃~70℃, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8kV, class B	Note 4
8	Image Sticking	25℃, 2hrs	Note 5
9	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10 ~ 55 ~ 10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A : 15 minutes
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

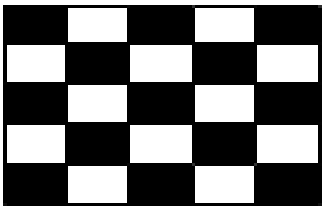
Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 3: All the cosmetic specification is judged before the reliability stress.

Note4 : All test techniques follow IEC6100-4-2 standard.

Test Condition		Note
Pattern	10x10 Chess Board 	
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 8 point, 10 times/point Air Discharge：330Ω, 150pF, 1sec, 8 point, 10 times/point 	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Gun to Panel Distance 2. No SPI command, keep default register settings.	

Note 5: Operate with 5×5 chess board pattern as figure and lasting time and temperature as the conditions. Then judge with 127 gray level after waiting 30 min, the mura is less than ND 5%.



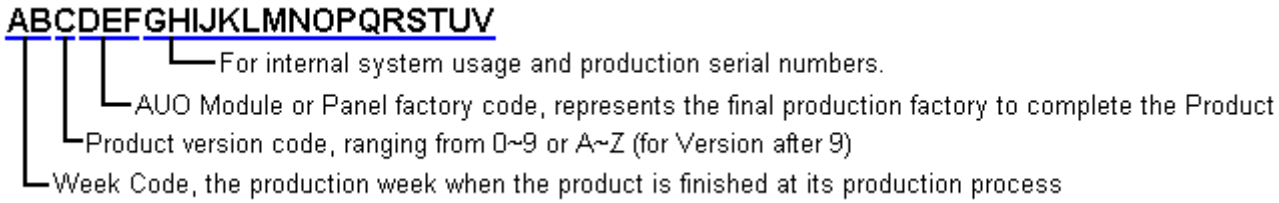
F. Packing and Marking

1. Packing Form

TBD

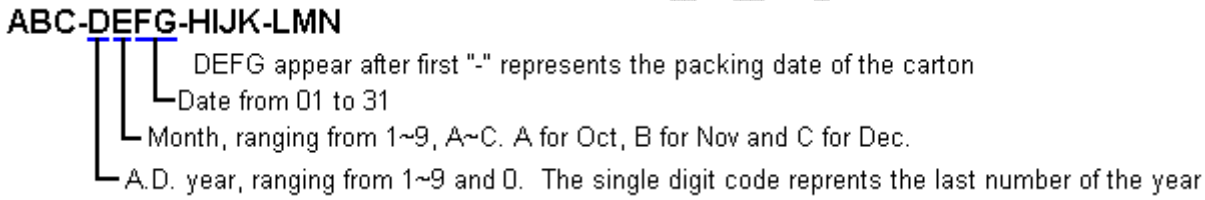
2. Module/Panel Label Information

The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:



3. Carton Label Information

The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:



Refer to the drawing of packing format for the location and size of the carton label.

G. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.