NOVATEK
聯 詠 科 技

Data Sheet

For **NT71391**

TFT-LCD Panel Timing Controller

V1.1

CONTENTS

1 Revision History

Specification Revision History			
Version	**Content**	**Editor**	**Release Date**
0.1	1. Preliminary SPEC.	Wei Yeh	2011/06/09
0.2	1. Add 60-pin information 2. Add power-on behavior 3. Modify MIPI figure	Wei Yeh	2011/07/06
0.3	1. Add 46-pin application circuit 2. Remove OE2 in 46-pin package 3. Add VDD 3.3v Info.	Wei Yeh	2011/07/21
0.4	1. Add 60-pin application circuit	Wei Yeh	2011/07/22
0.5	1. Add T_{CK-CK} in LVDS Receiver Differential Input (AC Characteristics)	Wei Yeh	2011/08/11
0.6	1. Add NT71391QG-001 information 2. Pin assignment modified in 46-pin package 3. Pin description modified in 46-pin package - pin No.2 : HSYNCO -> OE2/HSYNCO - pin No.7 : PWMI -> HSYNCO/PWMI	Wei Yeh	2011/08/18
0.7	1. Modify 60-pin pin description (POL) 2. Modify 46-pin application circuit	Wei Yeh	2011/10/28
0.8	1. Modify Figure 15(p.34) and setting table of CLKDLY(p.35) 2. Modify Input Setting Signal(p.39)	Wei Yeh	2011/11/01
1.0	1. Add MIPI power on sequence in appendix 2. Modify 60-pin application circuit (remove VMM) 3. Add MIPI Support Video Mode Interface Timing	Wei Yeh	2011/11/30
1.1	1. Add some descriptions in Non-burst mode with sync events.(p.29) 2. Add NT71391QG-001 Power-on Behavior in Appendix.	Wei Yeh	2011/12/20

2 Features

- Support input interface,
  - 4 lane 8-bit/6-bit MIPI input, up to 1Gbps/lane.
    - Support MIPI DSI interface
    - Support 1/2/3/4 data lane communication
    - Support video mode
  - 1-port/2-port (Only 60-pin QFN package) 8-bit/6-bit LVDS input, maximum clock up to 120MHz.
- Support output interface,
  - 1-port/3-pair 6/8bit mini-LVDS.
  - 1-port/6-pair 6/8bit mini-LVDS.
  - 2-port/3-pair 6/8bit mini-LVDS.
  - Maximum clock up to 350 MHz.
- Support resolution up to FHD (1920x1080) and (1920x1200).
- Support 8-bit color depth.
- Support spread spectrum clock generator (SSCG).
- Support output data skew control function.
- Support built-in self test (BIST) pattern function.
- Support free-run mode (MUTE) function.
- Support 1, 2, 1+2 line or frame inversion polarity control.
- Support DE only mode.
- Support gamma correction function.
- Support dithering function.
- Support CABC (Content Adaptive Brightness Control) function.
- Support color manager function.
- Built-in low-voltage reset function.
- Built-in internal oscillator.
- Support master I^2C interface for external EEPROM access.
- Support slave I^2C interface for CM/CABC dynamic control.
- 46-pin (4.5x6.5 mm) QFN package
- 60-pin (5.0x9.0 mm) QFN package

3 General Description

The TCON is a timing controller that embedded with 4 lane MIPI and 1-port/2-port LVDS input interface with mini-LVDS output driver interface, support resolution up to FHD (1920x1080) (1920x1200). The mini-LVDS interface embedded with reset pulse to the source driver, and the pixel rate could support up to 350 MHz.

The mini-LVDS bus in TCON transmits 6-bit/8-bit data for special resolution by customer requests. The TCON also supports an external EEPROM downloading function. This allows timing and resolution settings to be downloaded from EEPROM. The mini-LVDS interface is a low EMI and low voltage swing interface that transmits data from timing controller to the source drivers.

4 Pin Configuration

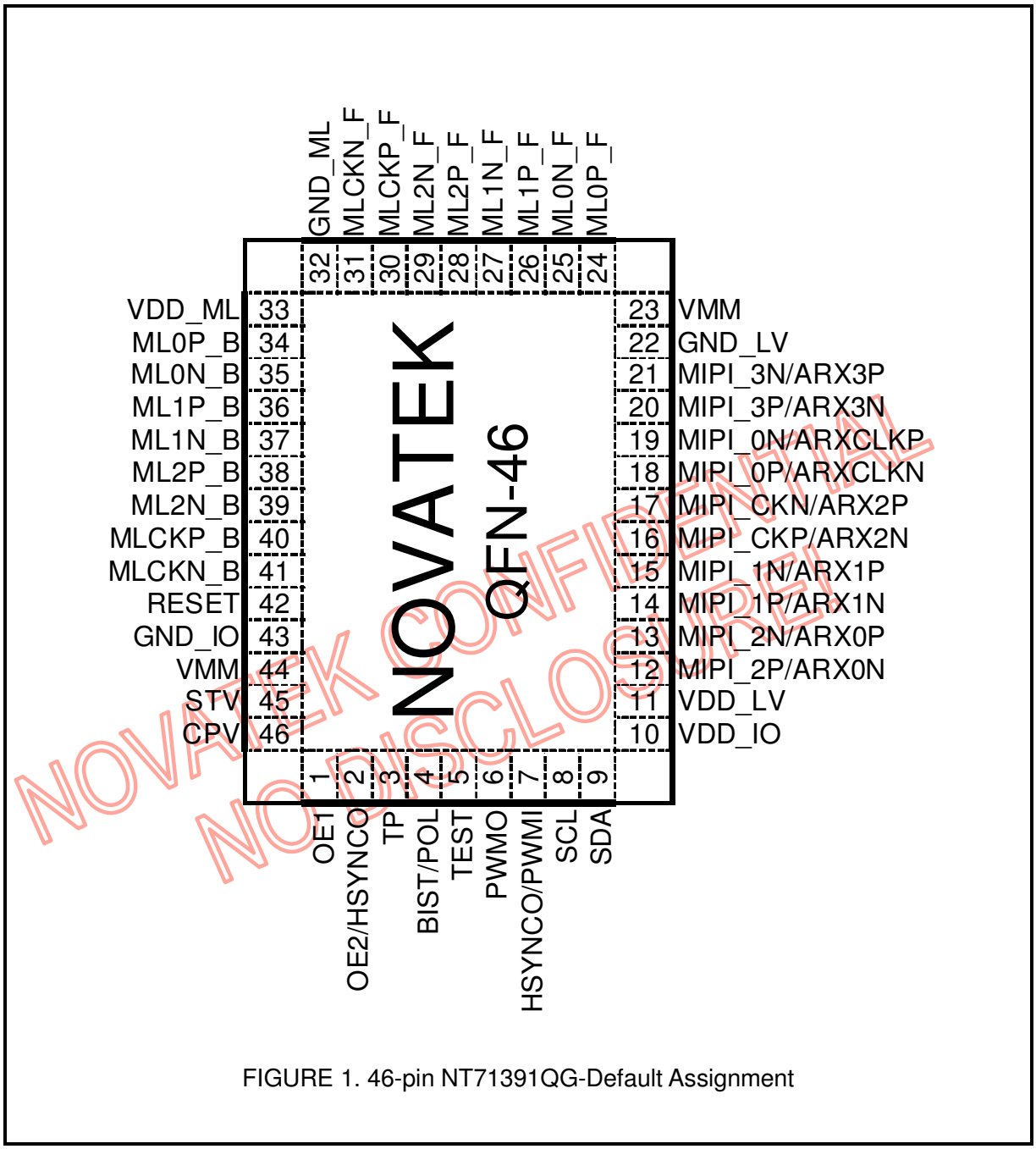


FIGURE 1. 46-pin NT71391QG-Default Assignment

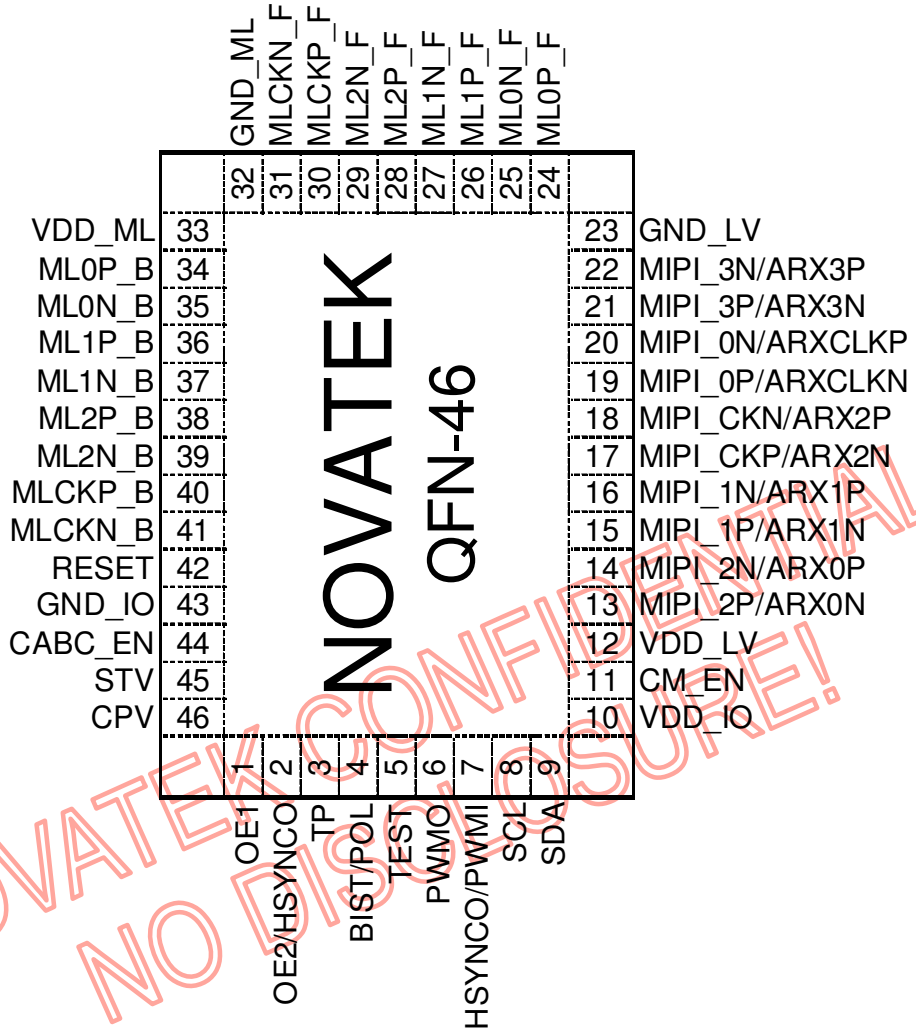


FIGURE 2. 46-Pin NT71391QG-001 Assignment

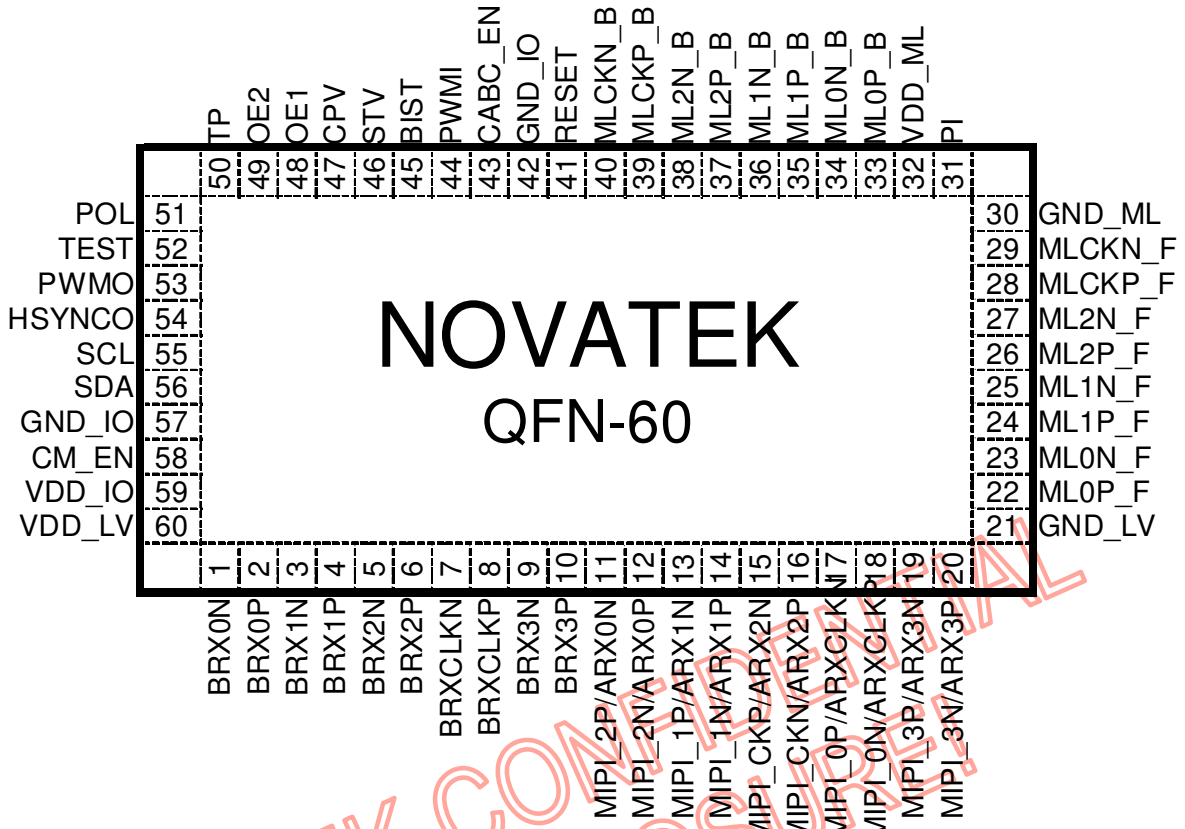


FIGURE 3. 60-Pin NT71391QG-601 Assignment

5 Block Diagram

5.1 Function Block Diagram

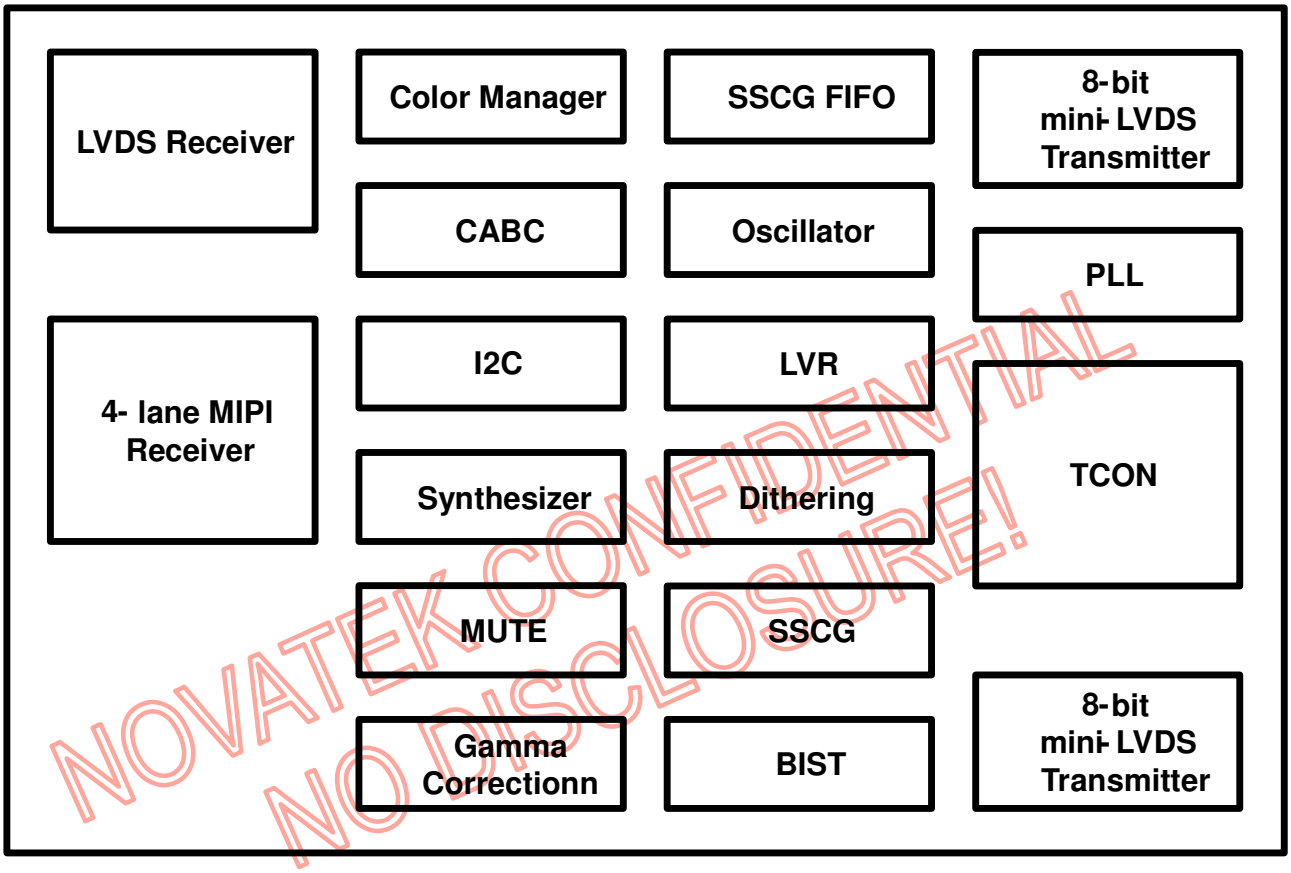


FIGURE 4. 46-pin Functional Block Diagram

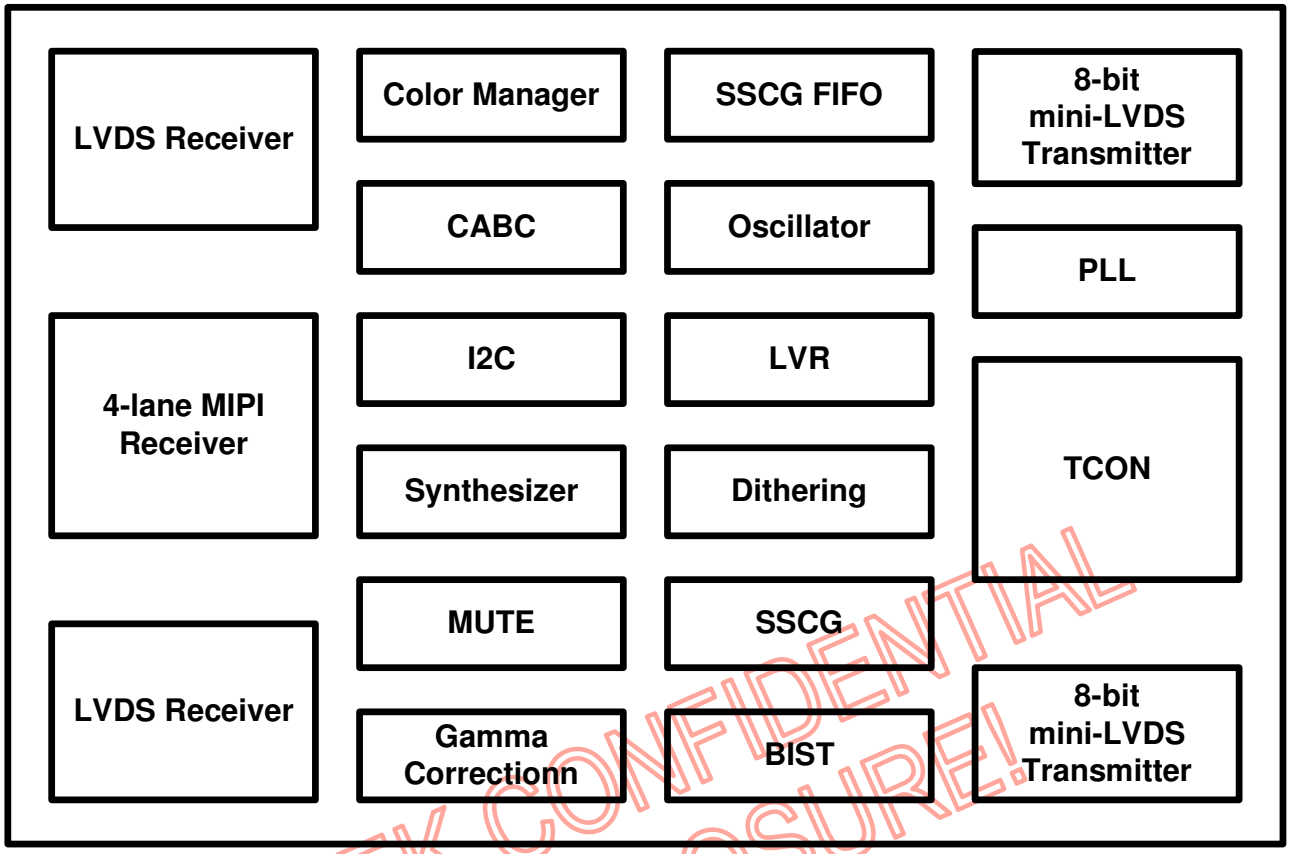


FIGURE 5. 60-pin Functional Block Diagram

5.2 System Application Diagram

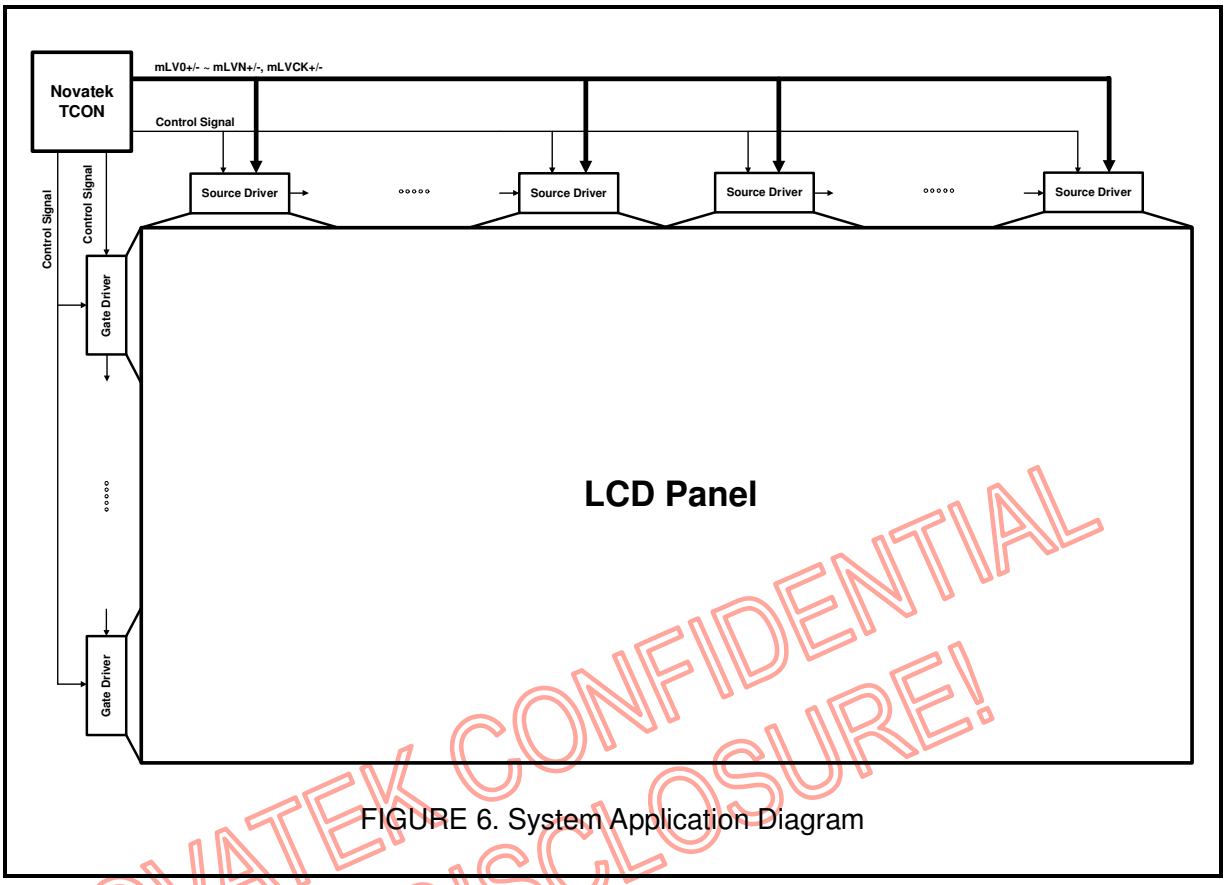


FIGURE 6. System Application Diagram

6 Pin Descriptions

NT71391QG – Default :

MIPI/LVDS PINS

No.	Name	Type	Description
12	MIPI_2P/ARX0N	I	MIPI/LVDS input data pair
13	MIPI_2N/ARX0P	I	
14	MIPI_1P/ARX1N	I	MIPI/LVDS input data pair
15	MIPI_1N/ARX1P	I	
16	MIPI_CKP/ARX2N	I	MIPI/LVDS input data pair
17	MIPI_CKN/ARX2P	I	
18	MIPI_0P/ARXCLKN	I	MIPI/LVDS input clock pair
19	MIPI_0N/ARXCLKP	I	
20	MIPI_3P/ARX3N	I	MIPI/LVDS input data pair
21	MIPI_3N/ARX3P	I	

I2C INTERFACE PINS

No.	Name	Type	Description
8	SCL	I/O	Serial clock output, open-drain
9	SDA	I/O	Serial data input/output, open-drain

OPTION PINS

No.	Name	Type	Description
4	BIST/POL	I/O	Built-in self test patterns selection @ RESET rising edge, internal pull-low L : Disable [default] H : Enable After I2C download, Source driver IC polarity control signal (Initial state = “L”) Source driver IC polarity control signal (Initial state = “L”)
5	TEST	I	Test mode function L : Disable [default] H : Enable
42	RESET	I	Reset input pin [active low] L：Reset H：Normal

mini-LVDS PINS

No.	Name	Type	Description
24	ML0P_F	O	mini-LVDS output pair
25	ML0N_F	O	
26	ML1P_F	O	mini-LVDS output pair
27	ML1N_F	O	
28	ML2P_F	O	mini-LVDS output pair
29	ML2N_F	O	
30	MLCKP_F	O	mini-LVDS output pair
31	MLCKN_F	O	
34	ML0P_B	O	mini-LVDS output pair
35	ML0N_B	O	
36	ML1P_B	O	mini-LVDS output pair
37	ML1N_B	O	
38	ML2P_B	O	mini-LVDS output pair
39	ML2N_B	O	
40	MLCKP_B	O	mini-LVDS output pair
41	MLCKN_B	O	

TCON PINS

No.	Name	Type	Description
1	OE1	O	Gate driver output enable signal (Initial state = “H”)
2	OE2/HSYNCO	O	Gate driver IC output enable signal (Initial state = “L”) or HSYNC output signal (Initial state = “L”) If pin No.7 is PWMI, pin No.2 is programmable to HSYNCO.
3	TP	O	Source IC latch control signal (Initial state = “L”)
6	PWMO	O	BLU control PWM output signal (Initial state = “L”)
7	HSYNCO/PWMI	O/I	HSYNC output signal (Initial state = “L”) BLU control PWM input signal
45	STV	O	Gate driver IC start pulse A (Initial state = “L”)
46	CPV	O	Gate driver IC shift clock (Initial state = “L”)

POWER AND GROUND PINS

No.	Name	Type	Description
10	VDD_IO	P	I/O power
11	VDD_LV	P	LVDS power
22	GND_LV	P	LVDS ground
23	VMM	P	Core power input
32	GND_ML	P	mini-LVDS ground
33	VDD_ML	P	mini-LVDS power
43	GND_IO	P	I/O ground
44	VMM	P	Core power input

NT71391QG – 001 :

MIPI/LVDS PINS

No.	Name	Type	Description
13	MIPI_2P/ARX0N	I	MIPI/LVDS input data pair
14	MIPI_2N/ARX0P	I	
15	MIPI_1P/ARX1N	I	MIPI/LVDS input data pair
16	MIPI_1N/ARX1P	I	
17	MIPI_CKP/ARX2N	I	MIPI/LVDS input data pair
18	MIPI_CKN/ARX2P	I	
19	MIPI_0P/ARXCLKN	I	MIPI/LVDS input clock pair
20	MIPI_0N/ARXCLKP	I	
21	MIPI_3P/ARX3N	I	MIPI/LVDS input data pair
22	MIPI_3N/ARX3P	I	

I2C INTERFACE PINS

No.	Name	Type	Description
8	SCL	I/O	Serial clock output, open-drain
9	SDA	I/O	Serial data input/output, open-drain

OPTION PINS

No.	Name	Type	Description
4	BIST/POL	I/O	Built-in self test patterns selection @ RESET rising edge, internal pull-low L : Disable [default] H : Enable After I2C download, Source driver IC polarity control signal (Initial state = “L”) Source driver IC polarity control signal (Initial state = “L”)
5	TEST	I	Test mode function L : Disable [default] H : Enable
11	CM_EN	I	Enable CM L : Disable [default] H : Enable
42	RESET	I	Reset input pin [active low] L：Reset H：Normal
44	CABC_EN	I	Enable CABC L : Disable [default] H : Enable

mini-LVDS PINS

No.	Name	Type	Description
24	ML0P_F	O	mini-LVDS output pair
25	ML0N_F	O	
26	ML1P_F	O	mini-LVDS output pair
27	ML1N_F	O	
28	ML2P_F	O	mini-LVDS output pair
29	ML2N_F	O	
30	MLCKP_F	O	mini-LVDS output pair
31	MLCKN_F	O	
34	ML0P_B	O	mini-LVDS output pair
35	ML0N_B	O	
36	ML1P_B	O	mini-LVDS output pair
37	ML1N_B	O	
38	ML2P_B	O	mini-LVDS output pair
39	ML2N_B	O	
40	MLCKP_B	O	mini-LVDS output pair
41	MLCKN_B	O	

TCON PINS

No.	Name	Type	Description
1	OE1	O	Gate driver output enable signal (Initial state = “H”)
2	OE2/HSYNCO	O	Gate driver IC output enable signal (Initial state = “L”) or HSYNC output signal (Initial state = “L”) If pin No.7 is PWMI, pin No.2 is programmable to HSYNCO.
3	TP	O	Source IC latch control signal (Initial state = “L”)
6	PWMO	O	BLU control PWM output signal (Initial state = “L”)
7	HSYNCO/PWMI	O/I	HSYNC output signal (Initial state = “L”) BLU control PWM input signal
45	STV	O	Gate driver IC start pulse A (Initial state = “L”)
46	CPV	O	Gate driver IC shift clock (Initial state = “L”)

POWER AND GROUND PINS

No.	Name	Type	Description
10	VDD_IO	P	I/O power
12	VDD_LV	P	LVDS power
23	GND_LV	P	LVDS ground
32	GND_ML	P	mini-LVDS ground
33	VDD_ML	P	mini-LVDS power
43	GND_IO	P	I/O ground

60-Pin Descriptions

MIPI/LVDS PINS

No.	Name	Type	Description
1	BRX0N	I	LVDS input data pair
2	BRX0P	I	
3	BRX1N	I	LVDS input data pair
4	BRX1P	I	
5	BRX1N	I	LVDS input data pair
6	BRX2P	I	
7	BRXCLKN	I	LVDS input clock pair
8	BRXCLKP	I	
9	BRX3N	I	LVDS input data pair
10	BRX3P	I	
11	MIPI_2P/ARX0N	I	MIPI/LVDS input data pair
12	MIPI_2N/ARX0P	I	
13	MIPI_1P/ARX1N	I	MIPI/LVDS input data pair
14	MIPI_1N/ARX1P	I	
15	MIPI_CKP/ARX2N	I	MIPI/LVDS input data pair
16	MIPI_CKN/ARX2P	I	
17	MIPI_0P/ARXCLKN	I	MIPI/LVDS input clock pair
18	MIPI_0N/ARXCLKP	I	
19	MIPI_3P/ARX3N	I	MIPI/LVDS input data pair
20	MIPI_3N/ARX3P	I	

I2C INTERFACE PINS

No.	Name	Type	Description
55	SCL	I/O	Serial clock output, open-drain
56	SDA	I/O	Serial data input/output, open-drain

OPTION PINS

No.	Name	Type	Description
41	RESET	I	Reset input pin [active low] L：Reset H：Normal
43	CABC_EN	I	CABC function enable L : Disable [default] H : Enable
44	PWMI	I	PWM input (Initial state = “L”)
45	BIST	I	Built-in self test patterns selection L : Disable [default] H : Enable
52	TEST	I	Test mode function L : Disable [default] H : Enable
58	CM_EN	I	Color management function L : Disable [default] H : Enable

mini-LVDS PINS

No.	Name	Type	Description
22	ML0P_F	O	mini-LVDS output pair
23	ML0N_F	O	
24	ML1P_F	O	mini-LVDS output pair
25	ML1N_F	O	
26	ML2P_F	O	mini-LVDS output pair
27	ML2N_F	O	
28	MLCKP_F	O	mini-LVDS output pair
29	MLCKN_F	O	
33	ML0P_B	O	mini-LVDS output pair
34	ML0N_B	O	
35	ML1P_B	O	mini-LVDS output pair
36	ML1N_B	O	
37	ML2P_B	O	mini-LVDS output pair
38	ML2N_B	O	
39	MLCKP_B	O	mini-LVDS output pair
40	MLCKN_B	O	
31	PI	I	External resistor input for mini-LVDS output swing control

TCON PINS

No.	Name	Type	Description
46	STV	O	Gate driver IC start pulse A (Initial state = “L”)
47	CPV	O	Gate driver IC shift clock (Initial state = “L”)
48	OE1	O	Gate driver output enable signal (Initial state = “H”)
49	OE2	O	Gate driver IC output enable signal (Initial state = “L”)
50	TP	O	Source IC latch control signal (Initial state = “L”)
51	POL	O	Source driver IC polarity control signal (Initial state = “L”)
53	PWMO	O	BLU control PWM output signal (Initial state = “L”)
54	HSYNCO	O	Hsync output signal (Initial state = “L”)

POWER AND GROUND PINS

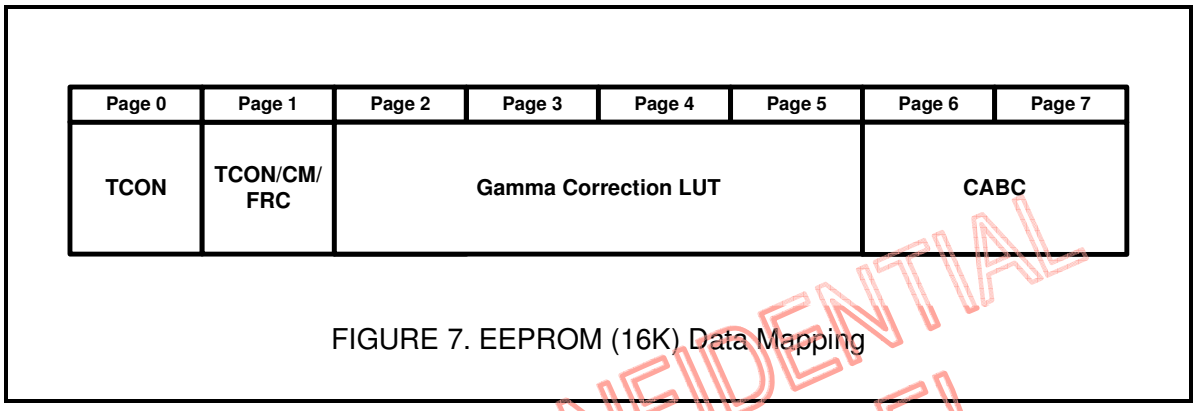
No.	Name	Type	Description
21	GND_LV	P	LVDS ground
30	GND_ML	P	mini-LVDS ground
32	VDD_ML	P	mini-LVDS power
42	GND_IO	P	I/O ground
57			
59	VDD_IO	P	I/O power
60	VDD_LV	P	LVDS power

7 Function Description

7.1 I2C Interface Function

An external EEPROM 24C16 (16K, 2048x8bits) is needed for TCON internal registers setting. When the system is powered on, TCON will start to download the EEPROM data for register initialized.

Data mapping of EEPROM is as the following diagram.

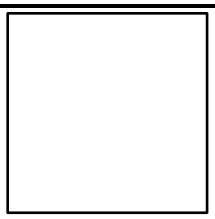
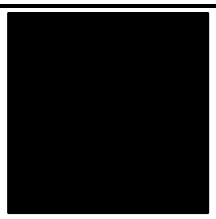
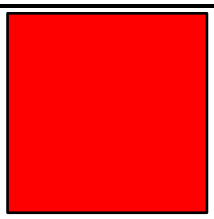
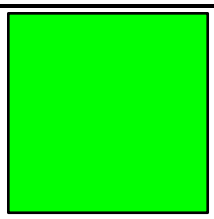
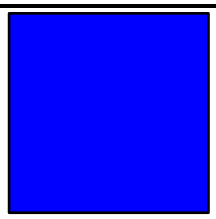


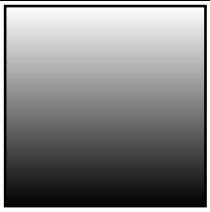
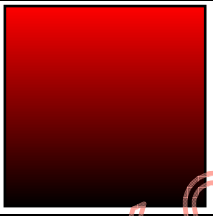
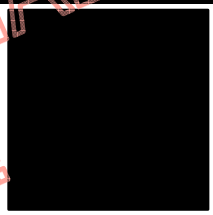
FIGUREE 7. EEPROM (16K) Data Mapping

7.2 Built-in Self Test Patterns

The TCON is built in variable test patterns. The sequence and display time of test patterns could be set by EEPROM code.

An example BIST pattern is as the following table.

PT1: White	PT2: Black	PT3: Full Red	PT4: Full Green	PT5: Full Blue
				

PT6: White Vertical Gray	PT7: Red Vertical Gray	PT8: Green Vertical Gray	PT9: Blue Vertical Gray	PT10: Black
				

7.3 Gamma Correction Function

There are three look-up (R, G, B) tables embedded in the EEPROM, and users could adjust the R, G, and B gamma curve separately by related gamma look-up tables.

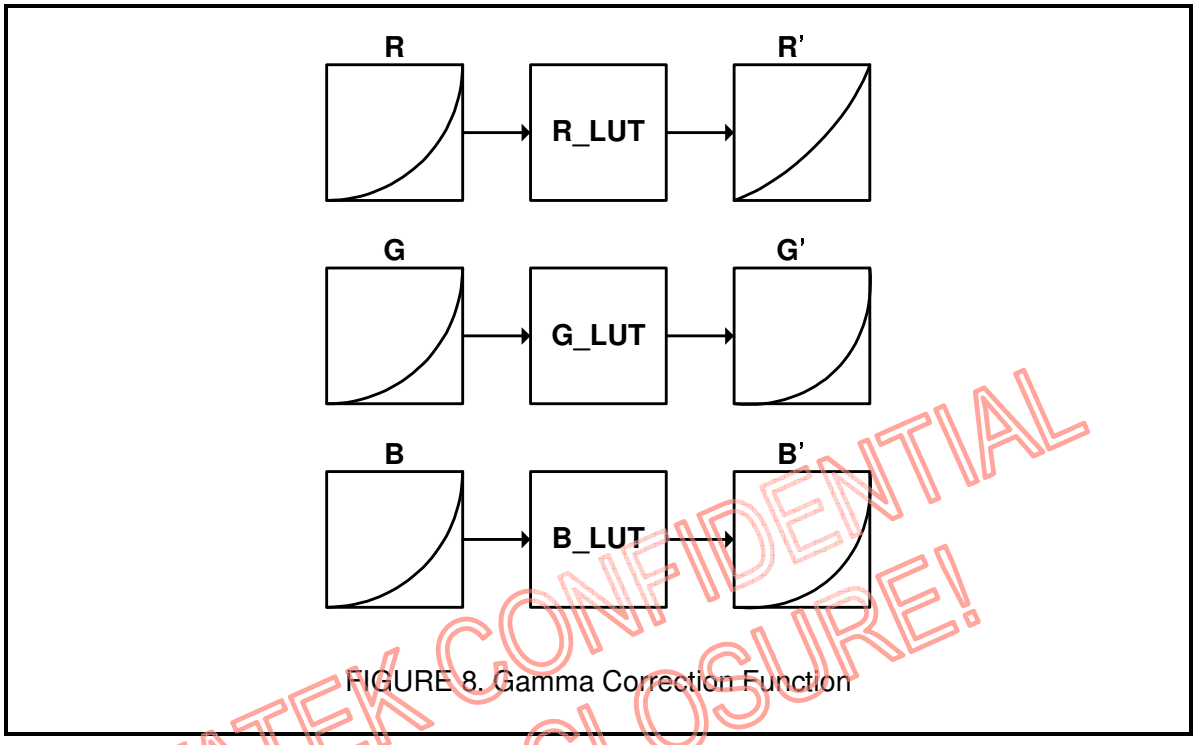


FIGURE 8. Gamma Correction Function

7.4 MIPI/LVDS Receiver

MIPI

- Support MIPI DSI interface （D-PHY：V1.0，DSI：V1.02）.
- Support 1/2/3/4data lane communication.
- Support video mode.
- Support non-continuous clock mode.
- Support RGB data type
  - 0x1E，packed pixel stream，18-bit RGB，6-6-6 format
  - 0x2E，loosely packed pixel stream，18-bit RGB，6-6-6 format
  - 0x3E，packed pixel stream，24-bit RGB，8-8-8 format
- Support video mode interface timing
  - Non-burst mode with sync pulses
  - Non-burst mode with sync events
  - Burst mode
- Lane Configuration

Clock Lane	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane1	Unidirectional ■ Forward High speed
Data Lane2	Unidirectional ■ Forward High speed
Data Lane3	Unidirectional ■ Forward High speed

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

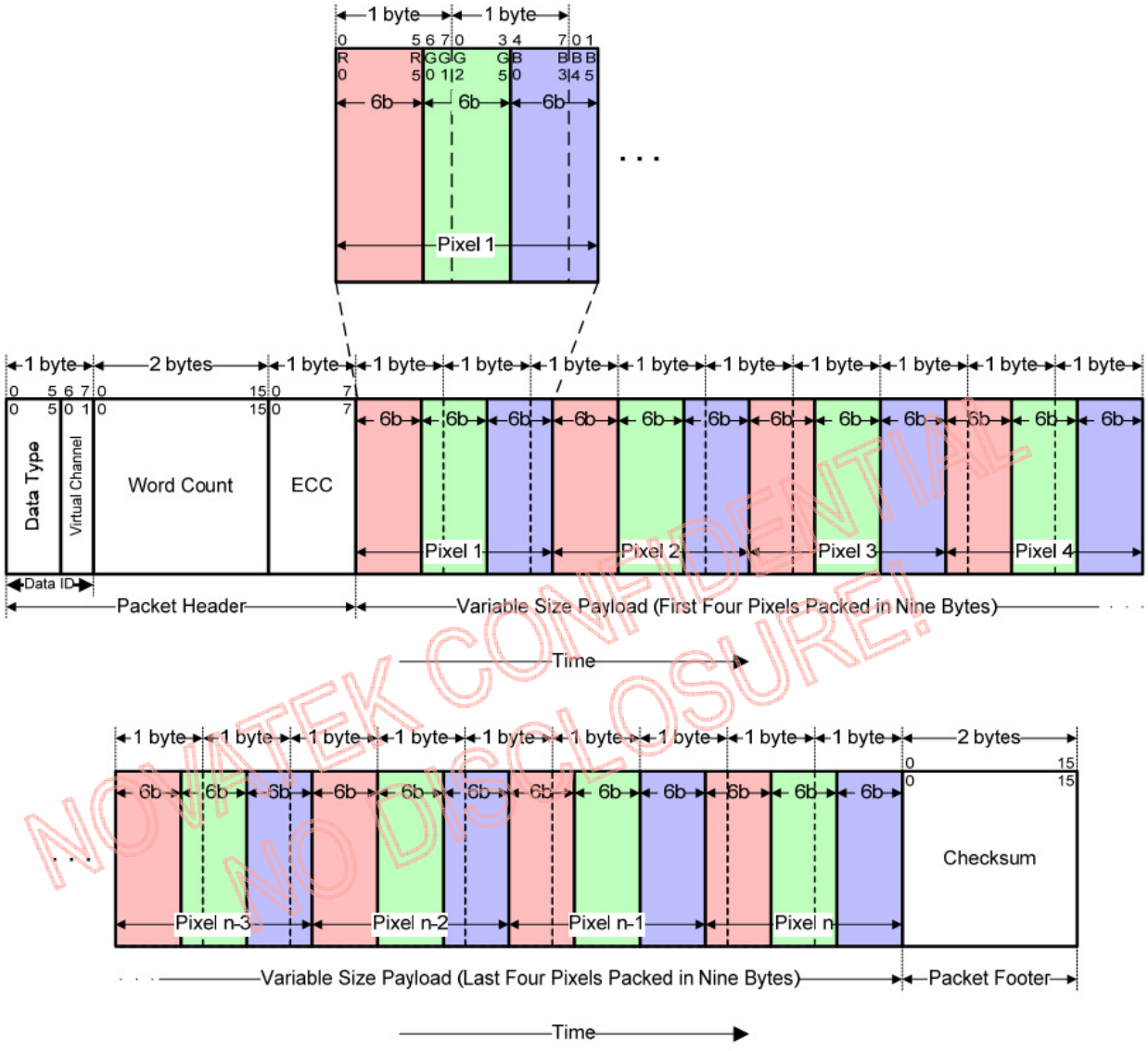
Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

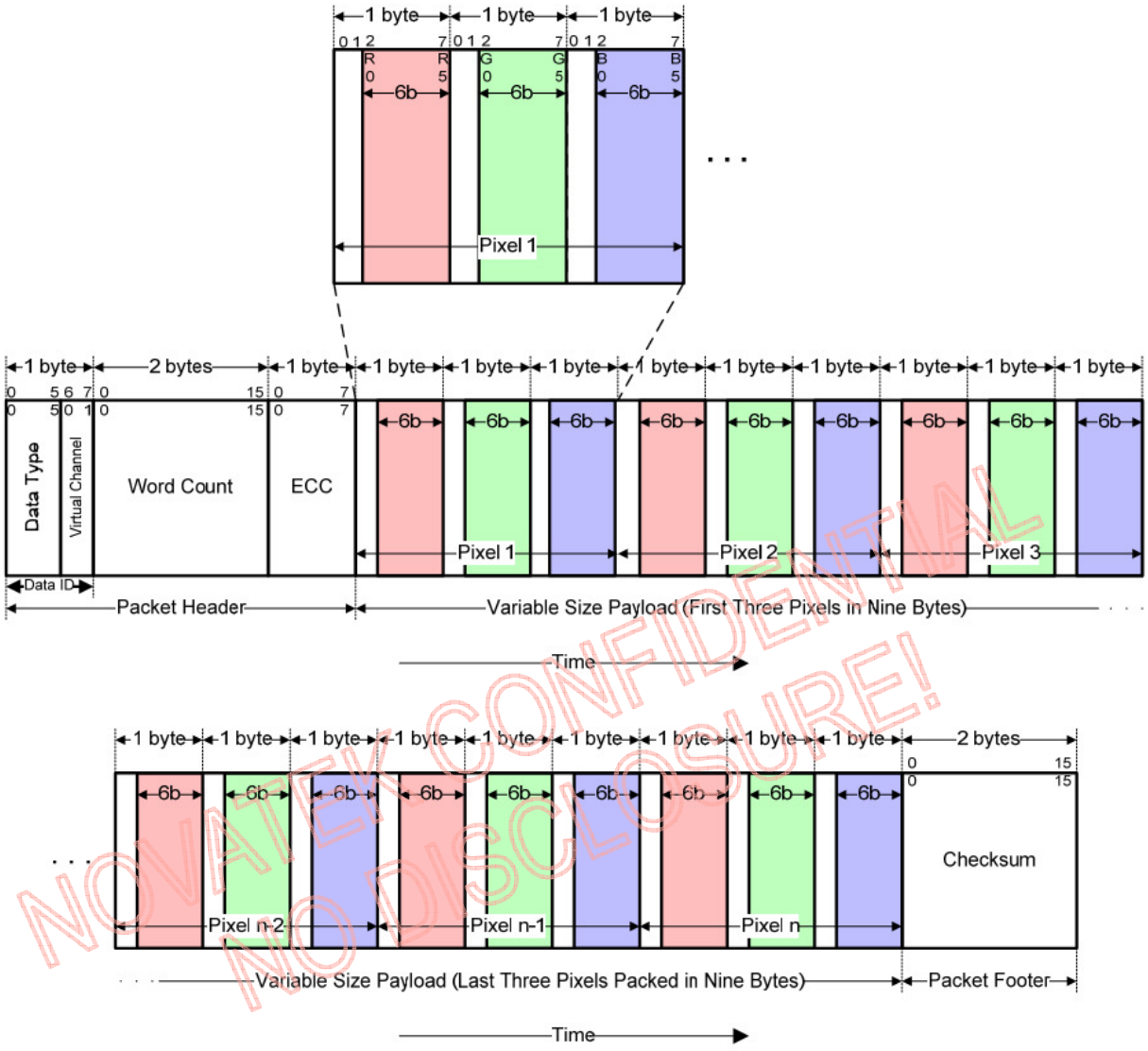
The operation and protocol of MIPI RX IP here complies with the MIPI Alliance standards and the related information such as D-PHY lower protocol, packet formatting and higher application protocol can be referred in the formal specification sheets when attempting to use this IP.

Support RGB data type:

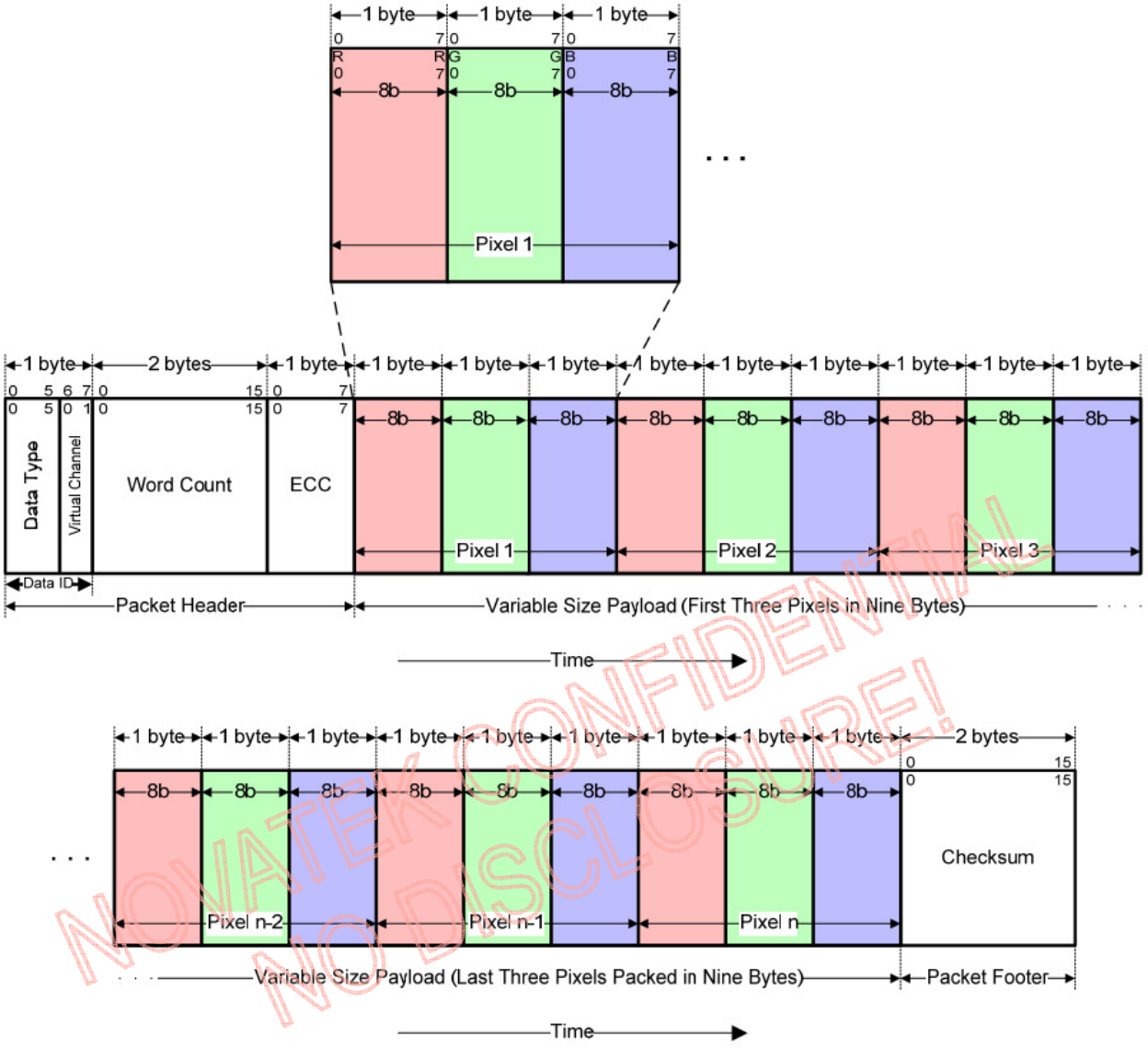
1. 0x1E，packed pixel stream，18-bit RGB，6-6-6 format



2. 0x2E，loosely packed pixel stream，18-bit RGB，6-6-6 format

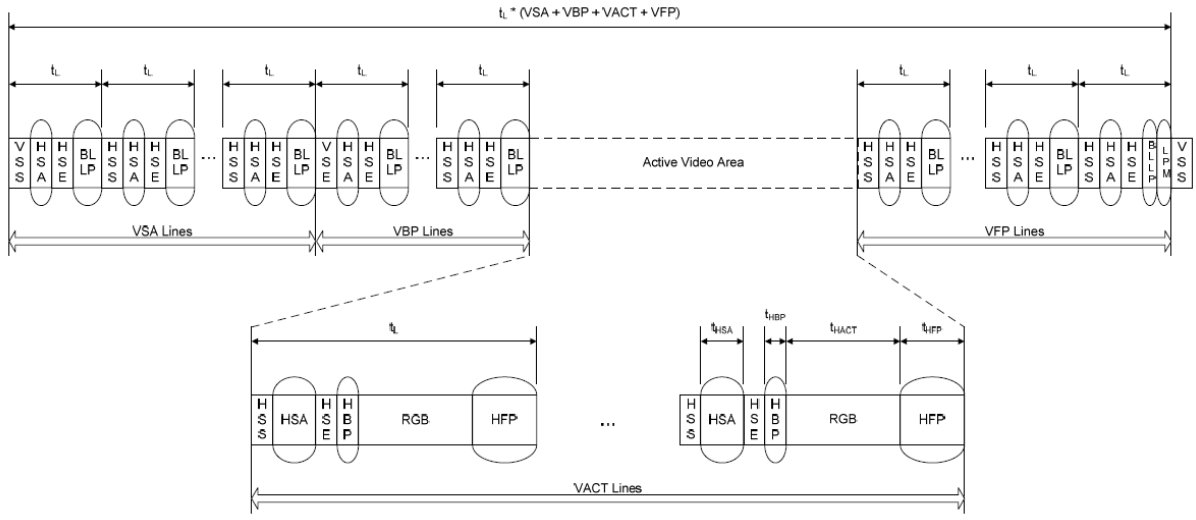


3. 0x3E，packed pixel stream，24-bit RGB，8-8-8 format

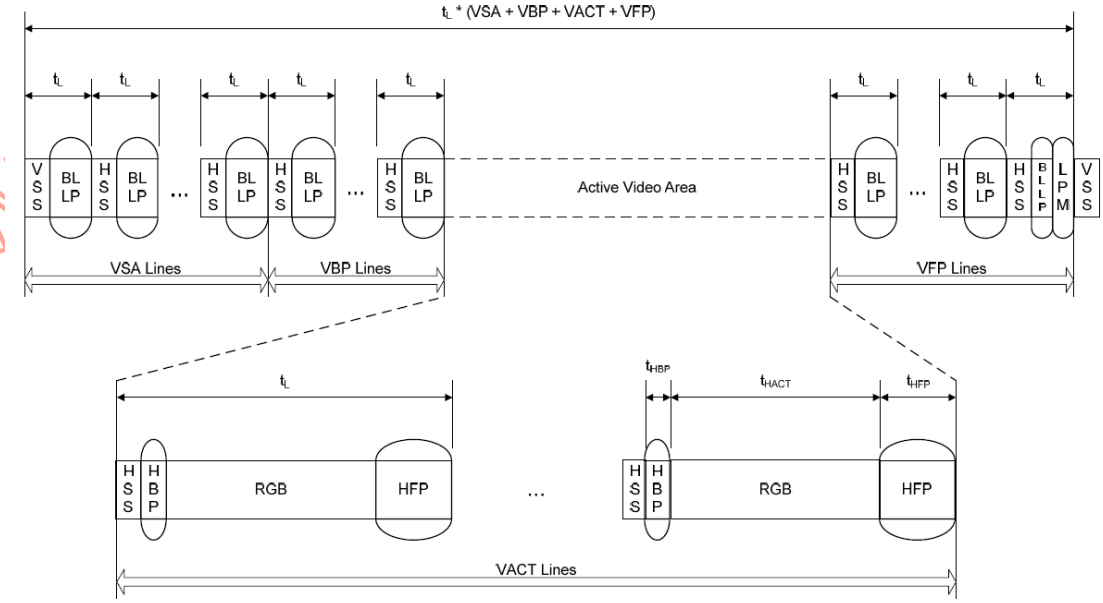


Support Video Mode Interface Timing:

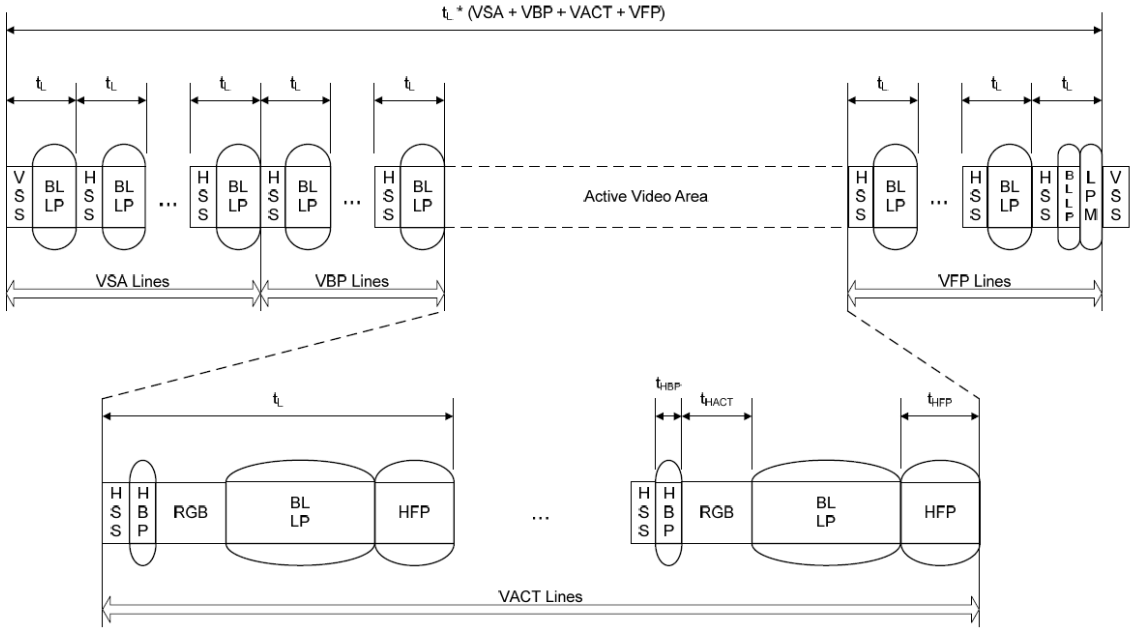
1. Non-burst mode with sync pulses: enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.



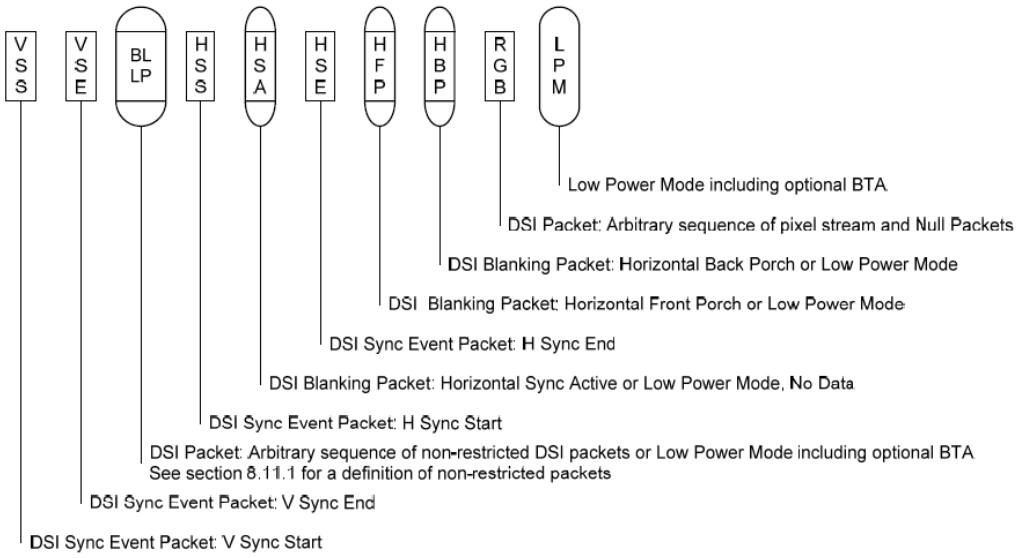
2. Non-burst mode with sync events: similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.(This mode does not need HSA.)



3. Burst transmission: RGB pixels packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.



Video Mode Interface Timing Legend:



LVDS

LVDS data mapping type could be set by internal registers, and 8-bit data sequence is shown as following table.

Channel No.	Data No.	8-bit LVDS TYPE	
		NS	JEIDA
0	Bit-0	R0	R2
	Bit-1	R1	R3
	Bit-2	R2	R4
	Bit-3	R3	R5
	Bit-4	R4	R6
	Bit-5	R5	R7
	Bit-6	G0	G2
1	Bit-0	G1	G3
	Bit-1	G2	G4
	Bit-2	G3	G5
	Bit-3	G4	G6
	Bit-4	G5	G7
	Bit-5	B0	B2
	Bit-6	B1	B3
2	Bit-0	B2	B4
	Bit-1	B3	B5
	Bit-2	B4	B6
	Bit-3	B5	B7
	Bit-4	-	-
	Bit-5	-	-
	Bit-6	DE	DE
3	Bit-0	R6	R0
	Bit-1	R7	R1
	Bit-2	G6	G0
	Bit-3	G7	G1
	Bit-4	B6	B0
	Bit-5	B7	B1
	Bit-6	-	-

8-bit LVDS input data mapping with “NS” setting is as following diagram.

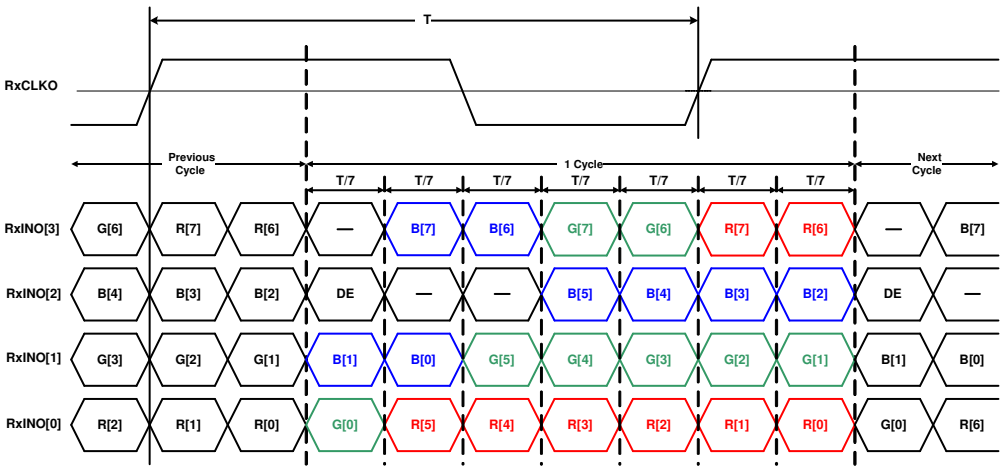


FIGURE 9. 8-bit LVDS Data Mapping (“NS” Data Format)

8-bit LVDS input data mapping with “JEIDA” setting is as following diagram.

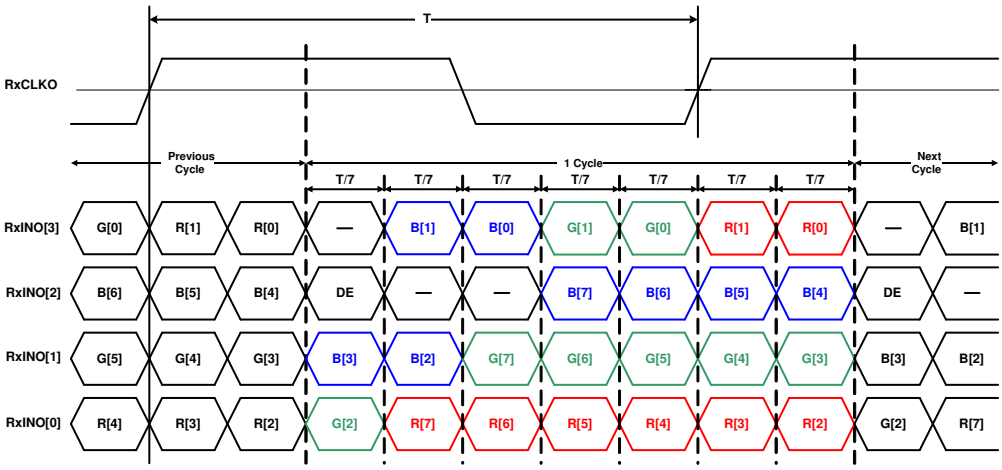


FIGURE 10. 8-bit LVDS Data Mapping (“JEITA” Data Format)

7.5 mini-LVDS Transmitter

Timing waveform between TP and mini-LVDS data is as the following diagram.

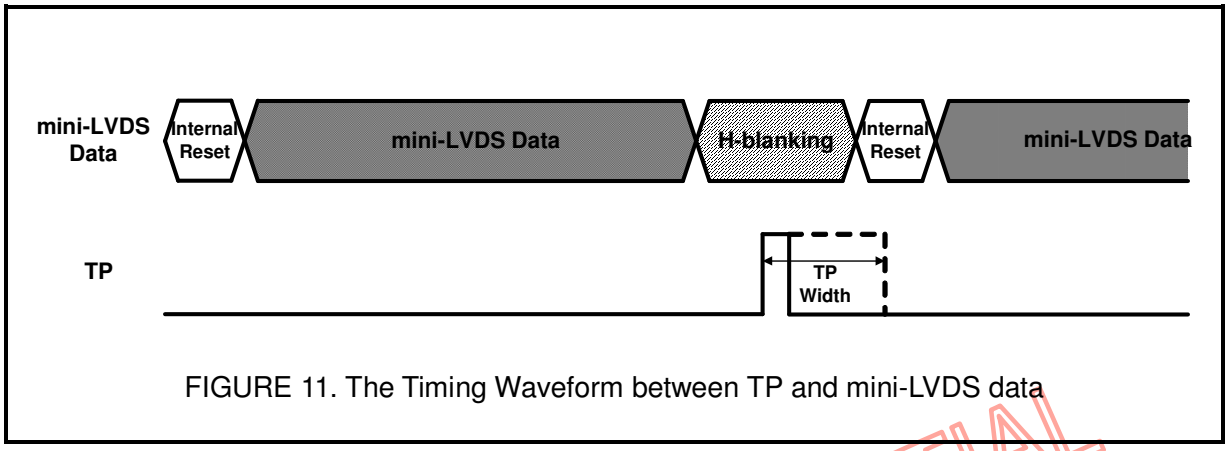


FIGURE 11. The Timing Waveform between TP and mini-LVDS data

Normal 6-bit/6-pair mini-LVDS input data mapping is as following diagram.

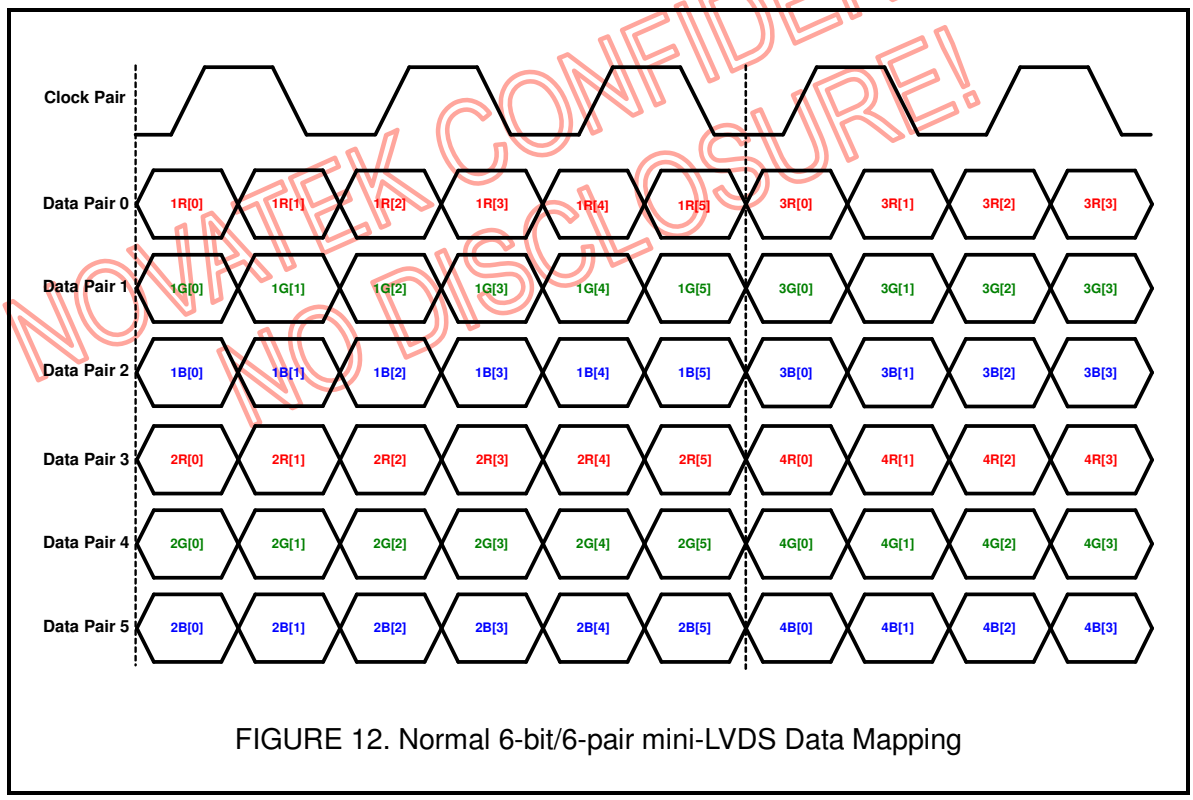


FIGURE 12. Normal 6-bit/6-pair mini-LVDS Data Mapping

Normal 6-bit/3-pair mini-LVDS input data mapping is as following diagram.

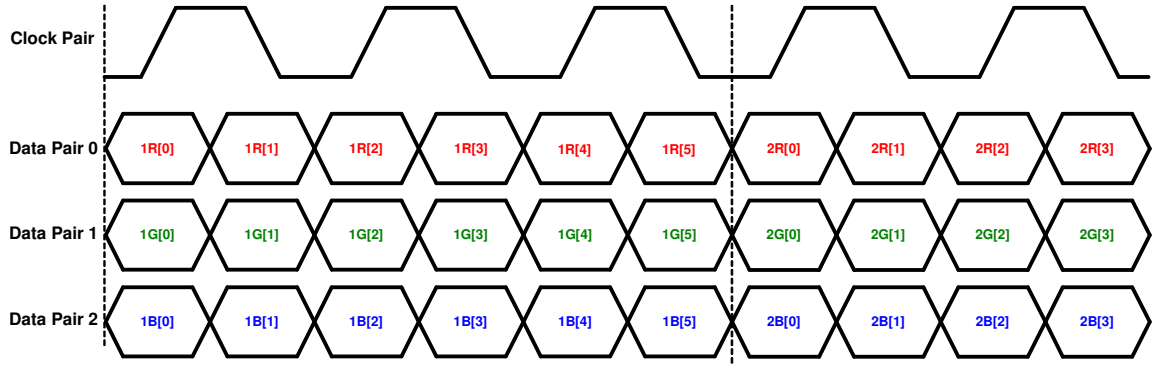


FIGURE 13. Normal 6-bit/3-pair mini-LVDS Data Mapping

Normal 8-bit/2-port/3-pair mini-LVDS input data mapping is as following diagram.

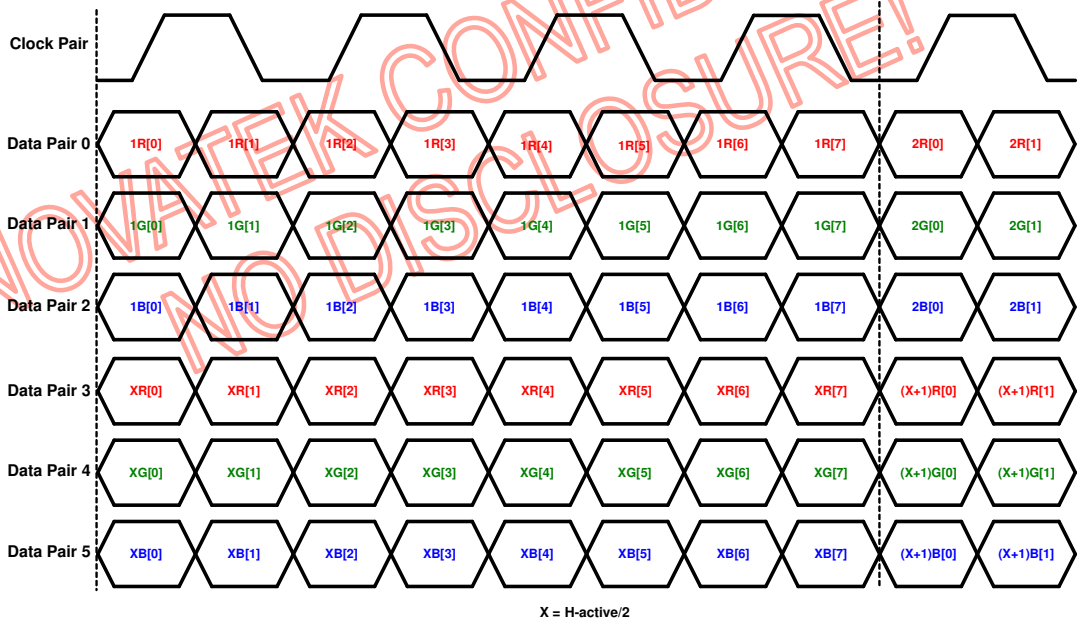


FIGURE 14. Normal 8-bit/2-port/3-pair mini-LVDS Data Mapping

Normal 8-bit/3-pair mini-LVDS input data mapping is as following diagram.

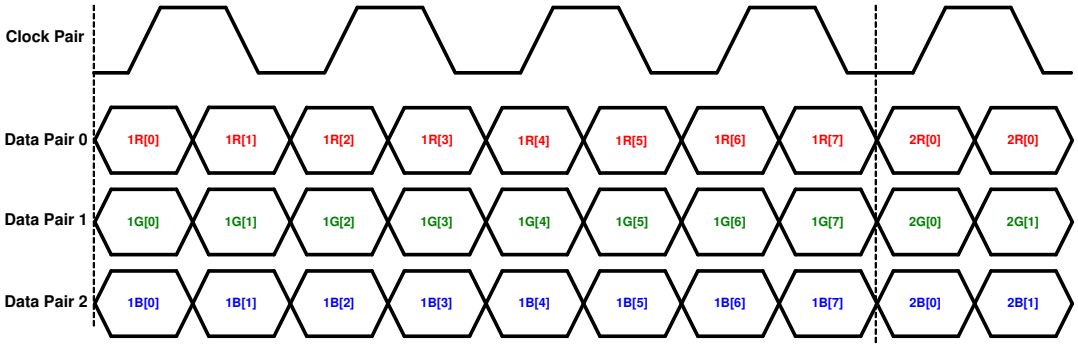


FIGURE 15. Normal 8-bit/3-pair mini-LVDS Data Mapping

The latch position between mini-LVDS CLK and data pairs could be adjusted. The phase adjusting function is as the following diagram.

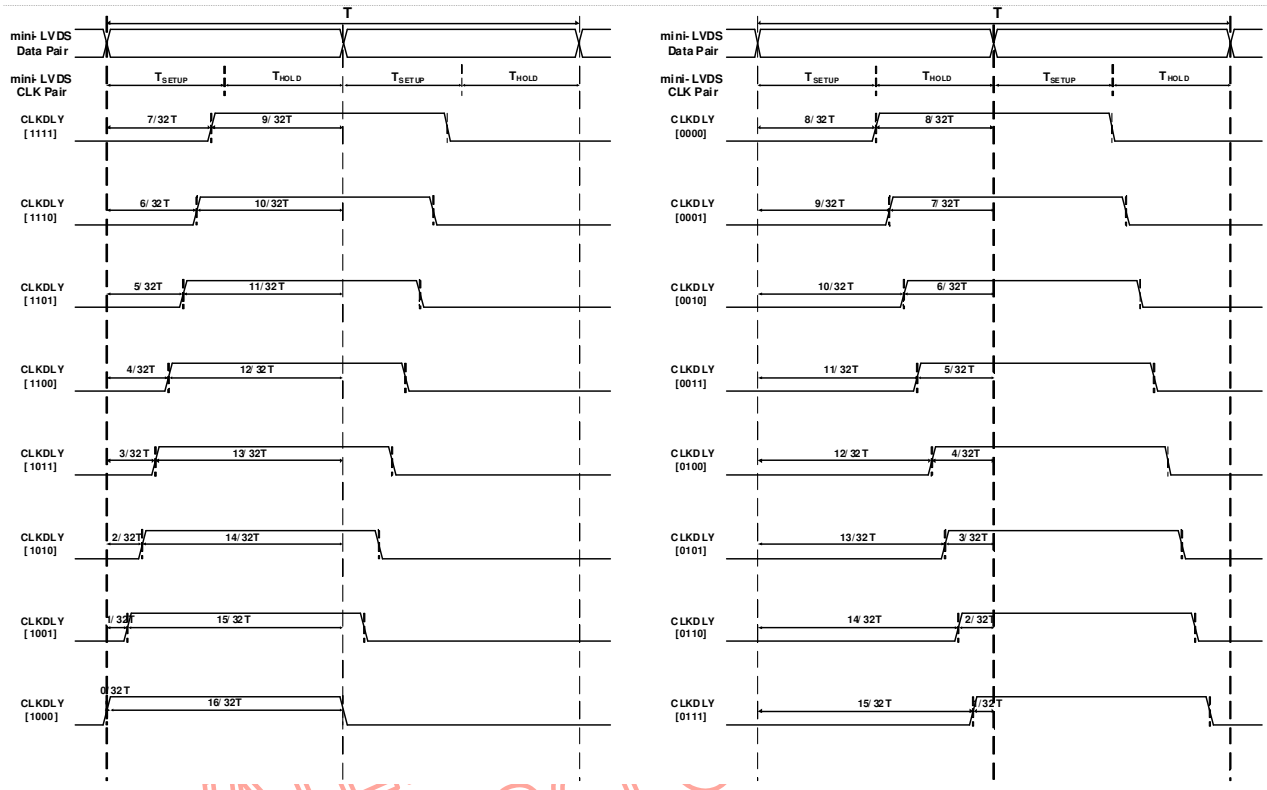


FIGURE 16. Phase Adjusting Function of mini-LVDS IP

There are registers embedded in TCON for controlling the phase delay (setup/hold time) between mini-LVDS CLK and data pairs. User could set the register value by slaver mode I2C interface.

The setting table of the register CLKDLY [3:0] is as the following table.

CLKDLY [3:0]				T_{SETUP}	T_{HOLD}	CLKDLY [3:0]				T_{SETUP}	T_{HOLD}
1	0	0	0	(0/32) T	(16/32) T	0	0	0	0	(8/32) T	(8/32) T
1	0	0	1	(1/32) T	(15/32) T	0	0	0	1	(9/32) T	(7/32) T
1	0	1	0	(2/32) T	(14/32) T	0	0	1	0	(10/32) T	(6/32) T
1	0	1	1	(3/32) T	(13/32) T	0	0	1	1	(11/32) T	(5/32) T
1	1	0	0	(4/32) T	(12/32) T	0	1	0	0	(12/32) T	(4/32) T
1	1	0	1	(5/32) T	(11/32) T	0	1	0	1	(13/32) T	(3/32) T
1	1	1	0	(6/32) T	(10/32) T	0	1	1	0	(14/32) T	(2/32) T
1	1	1	1	(7/32) T	(9/32) T	0	1	1	1	(15/32) T	(1/32) T

[NOTE] 1. T is one clock period of mini-LVDS clock.

The SSCG (Spread Spectrum Clock Generator) is used for reducing Electro Magnetic Interference (EMI). This block integrates Phase-Locked Loop (PLL) and spread spectrum modulation generator to synthesize and modulate the frequency of the input clock. The SSCG generates a phase-modulated clock output by modulating the input clock period.

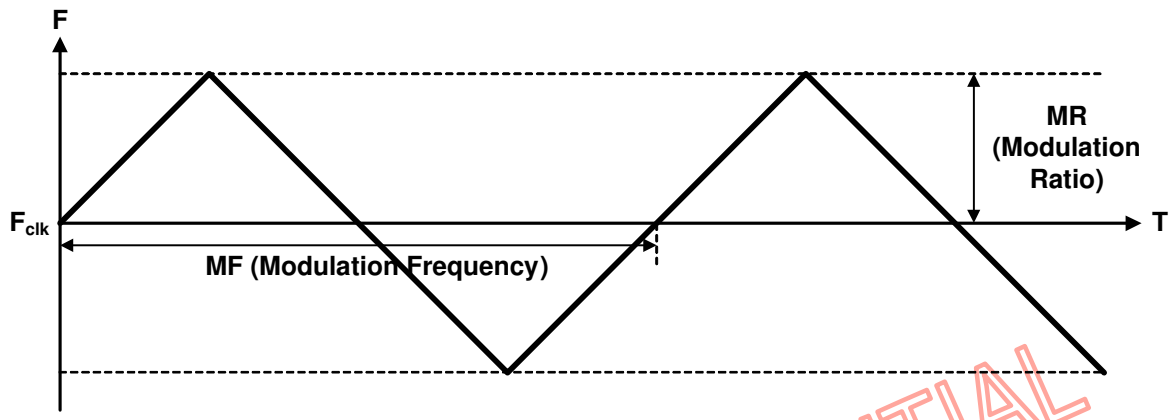


FIGURE 17. Frequency Modulation by Modulating Clock Period

8 Absolute Maximum Rating

Absolute Maximum Rating				
Symbol	Description	Ratings		Unit
		Min.	Max.	
V_{DD}	DC Supply Voltage	-0.3	4.0	V
V_{IN}	DC Input/Output Voltage	-0.3	V_{DD} + 0.3	V
T_{OPR}	Operating Temperature	-40	85	°C
T_{JUN}	Junction Temperature	0	125	°C
T_{STG}	Storage Temperature	-55	150	°C

*Comments
Stresses above what is listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above what is indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9 DC and AC Electrical Characteristics (T_A = 25°C, unless otherwise noted)

Recommended Operating Conditions						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
VDD	Supply Voltage 3.3 V	3.0	3.3	3.6	V	VDD_ML, VDD_IO, VDD_LV
	Supply Voltage 2.5 V	2.3	2.5	2.7		
VMM	Supply Voltage 1.2 V	1.1	1.2	1.3	V	VMM

Output Control Signal						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
I_{OH}	High-level output current	8	-	-	mA	@ V_{OH} = 0.7 V_{DD} STV, CPV, OE1, OE2, TP, POL, PWMO, HSYNCO
I_{OL}	Low-level output current	-	-	-8	mA	@ V_{OL} = 0.4 V STV, CPV, OE1, OE2, TP, POL, PWMO, HSYNCO, SCL, SDA,

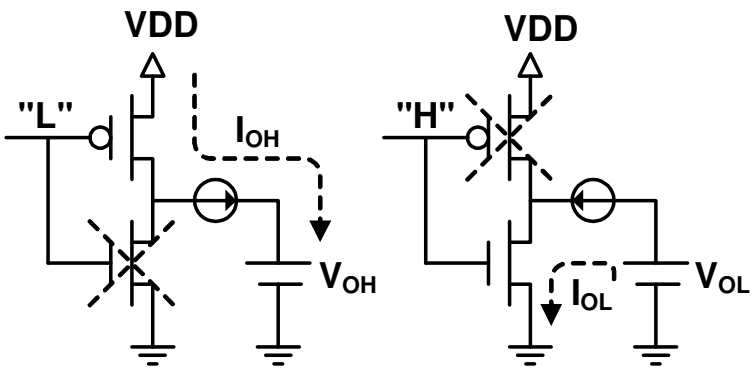


FIGURE 18. High/Low Level Output Current and High/Low Level Output Voltage

Input Setting Signal						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
V_{IH_RESET}	High-level input voltage of RESET pin	-	$0.8V_{DD}$	-	V	* Schmitt trigger input [RESET] (V_{DD} = 3.3 or 2.5 V)
V_{WIN_RESET}	Hysteresis window of Schmitt trigger input	0.4	-	-	V	* Schmitt trigger input [RESET] (V_{DD} = 3.3 V)
		0.3	-	-		* Schmitt trigger input [RESET] (V_{DD} = 2.5 V)
V_{IH_I2C}	High-level input voltage of I2C pin	0.9	1.2	1.5	V	* Schmitt trigger input [SDA,SCL] (V_{DD} = 3.3 V)
		0.7	1.0	1.3		* Schmitt trigger input [SDA,SCL] (V_{DD} = 2.5 V)
V_{WIN_I2C}	Hysteresis window of Schmitt trigger input	0.4	-	-	V	* Schmitt trigger input [SDA,SCL] (V_{DD} = 3.3 V)
		0.3	-	-		* Schmitt trigger input [SDA,SCL] (V_{DD} = 2.5 V)
V_{IH_FUN}	High-level input voltage of function pin (Only for NT71391QG-001, NT71391QG-601)	-	$0.7V_{DD}$	-	V	* Schmitt trigger input [CABC_EN, CM_EN] (V_{DD} = 3.3 or 2.5 V)
V_{WIN_FUN}	Hysteresis window of Schmitt trigger input (Only for NT71391QG-001, NT71391QG-601)	0.4	-	-	V	* Schmitt trigger input [CABC_EN, CM_EN] (V_{DD} = 3.3 V)
		0.3	-	-		* Schmitt trigger input [CABC_EN, CM_EN] (V_{DD} = 2.5 V)
V_{IH_PWMI}	High-level input voltage of PWMI pin (Only for NT71391QG-601)	-	$0.7V_{DD}$	-	V	* Schmitt trigger input [PWMI] (V_{DD} = 3.3 or 2.5 V)
V_{WIN_PWMI}	Hysteresis window of Schmitt trigger input (Only for NT71391QG-601)	0.4	-	-	V	* Schmitt trigger input [PWMI] (V_{DD} = 3.3 V)
		0.3	-	-		* Schmitt trigger input [PWMI] (V_{DD} = 2.5 V)

Input Setting Signal						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
$V_{IH\_H/P}$	High-level input voltage of HSYNCO/PWMI pin (Only for NT71391QG-default, NT71391QG-001)	-	$0.5V_{DD}$	-	V	* Schmitt trigger input [HSYNCO/PWMI] (V_{DD} = 3.3 or 2.5 V)
$V_{WIN\_H/P}$	Hysteresis window of Schmitt trigger input (Only for NT71391QG-default, NT71391QG-001)	0.4	-	-	V	* Schmitt trigger input [HSYNCO/PWMI] (V_{DD} = 3.3 V)
		0.3	-	-		* Schmitt trigger input [HSYNCO/PWMI] (V_{DD} = 2.5 V)
V_{IH_BIST}	High-level input voltage of BIST pin (Only for NT71391QG-601)	-	$0.7V_{DD}$	-	V	* Schmitt trigger input [BIST] (V_{DD} = 3.3 or 2.5 V)
V_{WIN_BIST}	Hysteresis window of Schmitt trigger input (Only for NT71391QG-601)	0.4	-	-	V	* Schmitt trigger input [BIST] (V_{DD} = 3.3)
		0.3	-	-		* Schmitt trigger input [BIST] (V_{DD} = 2.5)
$V_{IH\_B/P}$	High-level input voltage of BIST/POL pin (Only for NT71391QG-default, NT71391QG-001)	-	$0.5V_{DD}$	-	V	* Schmitt trigger input [BIST/POL] (V_{DD} = 3.3 or 2.5 V)
$V_{WIN\_B/P}$	Hysteresis window of Schmitt trigger input (Only for NT71391QG-default, NT71391QG-001)	0.4	-	-	V	* Schmitt trigger input [BIST/POL] (V_{DD} = 3.3V)
		0.3	-	-		* Schmitt trigger input [BIST/POL] (V_{DD} = 2.5V)
V_{ITH}	High-level input voltage of pure input pin	-	$V_{DD}/2$	-	V	* Pure input pin (V_{DD} = 3.3 or 2.5 V)
R_{PH}	Pull-high resistor	50	-	200	kΩ	V_I = GND
R_{PL}	Pull-low resistor	50	-	200	kΩ	V_I = V_{DD}

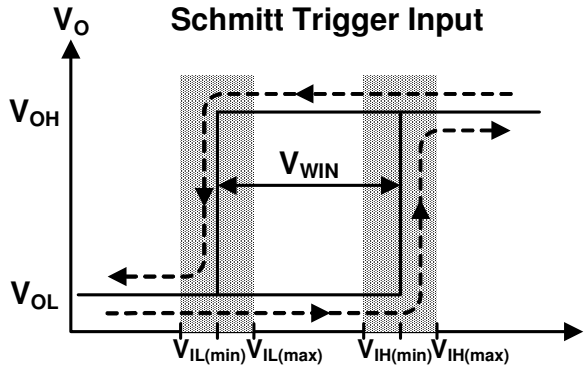


FIGURE 19. High/Low Level Input of Schmitt Trigger Input

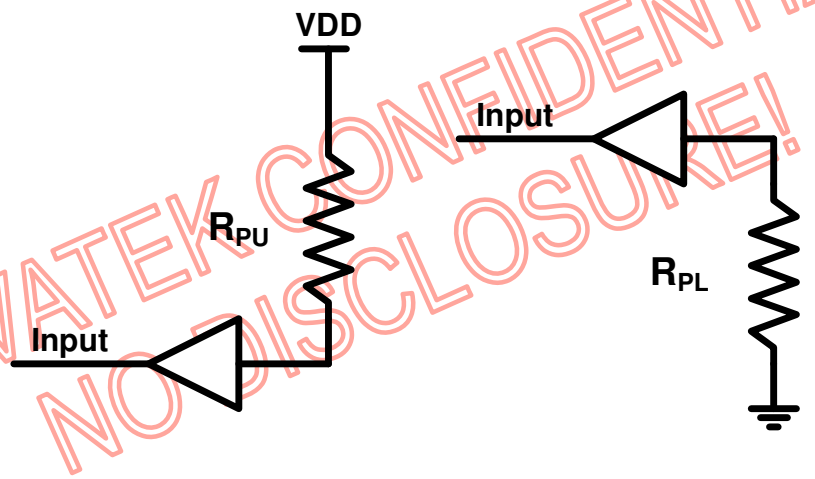


FIGURE 20. Pull-High and Pull-Low Resisters of Pure Input Pin

Low Voltage Reset						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
V_{LVRH}	High-level detect voltage of LVR	-	-	2.1	V	
V_{LVRWIN}	Hysteresis window of LVR	0.1	-	-	V	

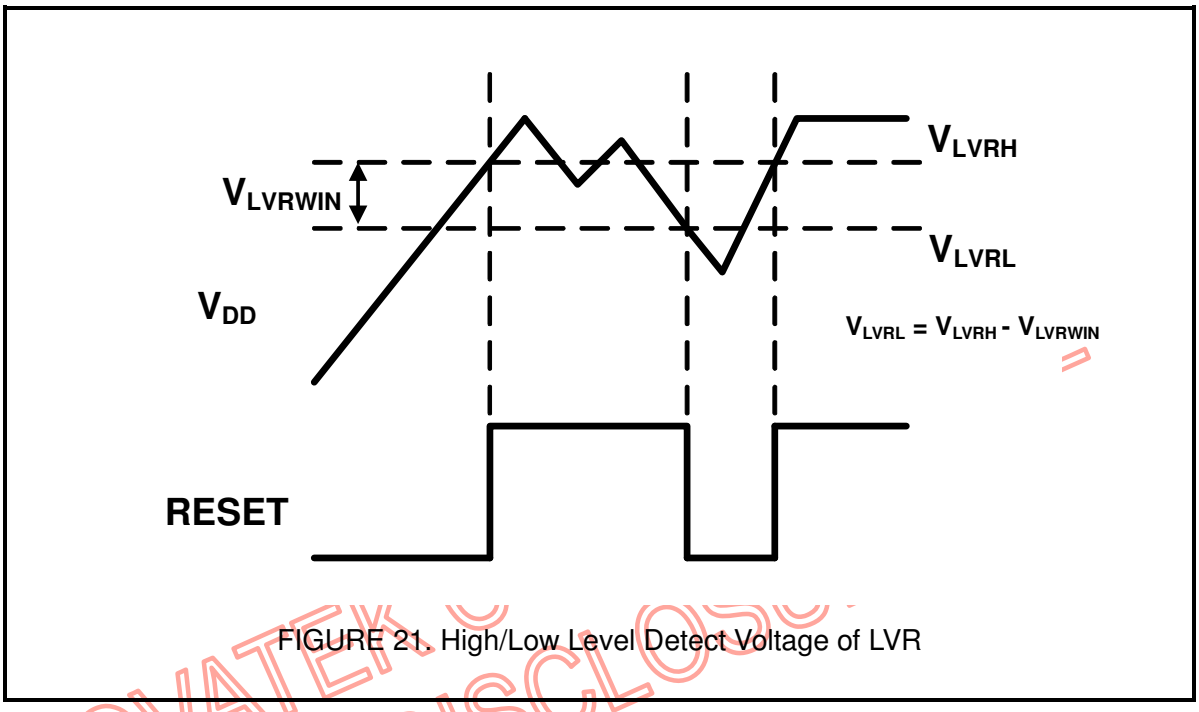


FIGURE 21. High/Low Level Detect Voltage of LVR

LVDS Receiver Differential Input (DC Characteristics)						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
R_{xVTH}	Differential input high threshold voltage	-	-	+100	mV	R_{xVCM} =1.2 V
R_{xVTL}	Differential input low threshold voltage	-100	-	-	mV	
R_{xVIN}	Input voltage range (singled-end)	0	-	2.4	V	V_{DDL} = 3.3 V
		0	-	V_{DD}-0.4		V_{DDL} = 2.5 V
R_{xVCM}	Input common mode voltage	$\|V_{ID}\|/2$	-	2.4-$\|V_{ID}\|/2$	V	V_{DDL} = 3.3 V
		$\|V_{ID}\|/2$	-	V_{DD}-0.4-$\|V_{ID}\|/2$		V_{DDL} = 2.5 V
$\|V_{ID}\|$	Differential input voltage	100	-	600	mV	-
RV_{xLIK}	Differential input leakage current	-10	-	+10	uA	-
R_{xFCLK}	Clock frequency	25	-	120	MHz	-

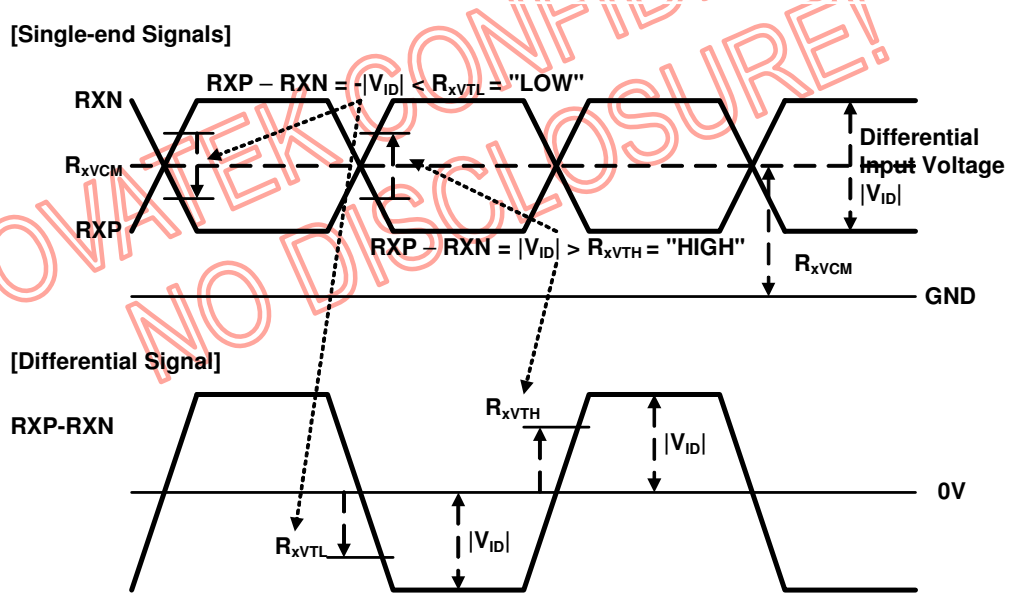


FIGURE 22. Definition of Input Threshold Voltage (R_{xVTH} / R_{xVTL}), Common Mode Voltage (R_{xVCM}), and Input Voltage Swing ($|V_{ID}|$)

LVDS Receiver Differential Input (AC Characteristics)						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
T_{RSKM}	Input data skew margin	-350	-	+350	ps	R_{xCLK} = 100 MHz $\|R_{xVTH} - R_{xVTL}\|$ = 400 mV R_{xVCM} = 1.2 V $R_{x\triangle VCM}$ = 0 mV
T_{CK-CK}	Inter-clock skew of each port (clock to clock skew margin between EVEN and ODD port)	-1/7	-	+1/7	T	-
SS_R	Input spread spectrum ratio	-	-	+/-3	%	-
F_M	Input modulation frequency	-	-	300k	Hz	-

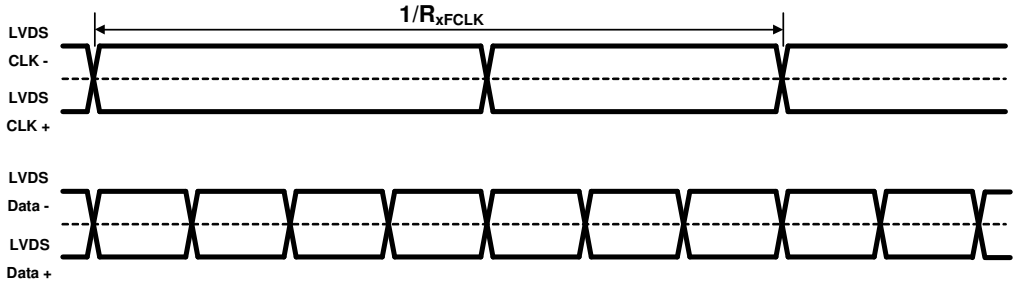


FIGURE 23. Definition of Clock Frequency (R_{xFCLK})

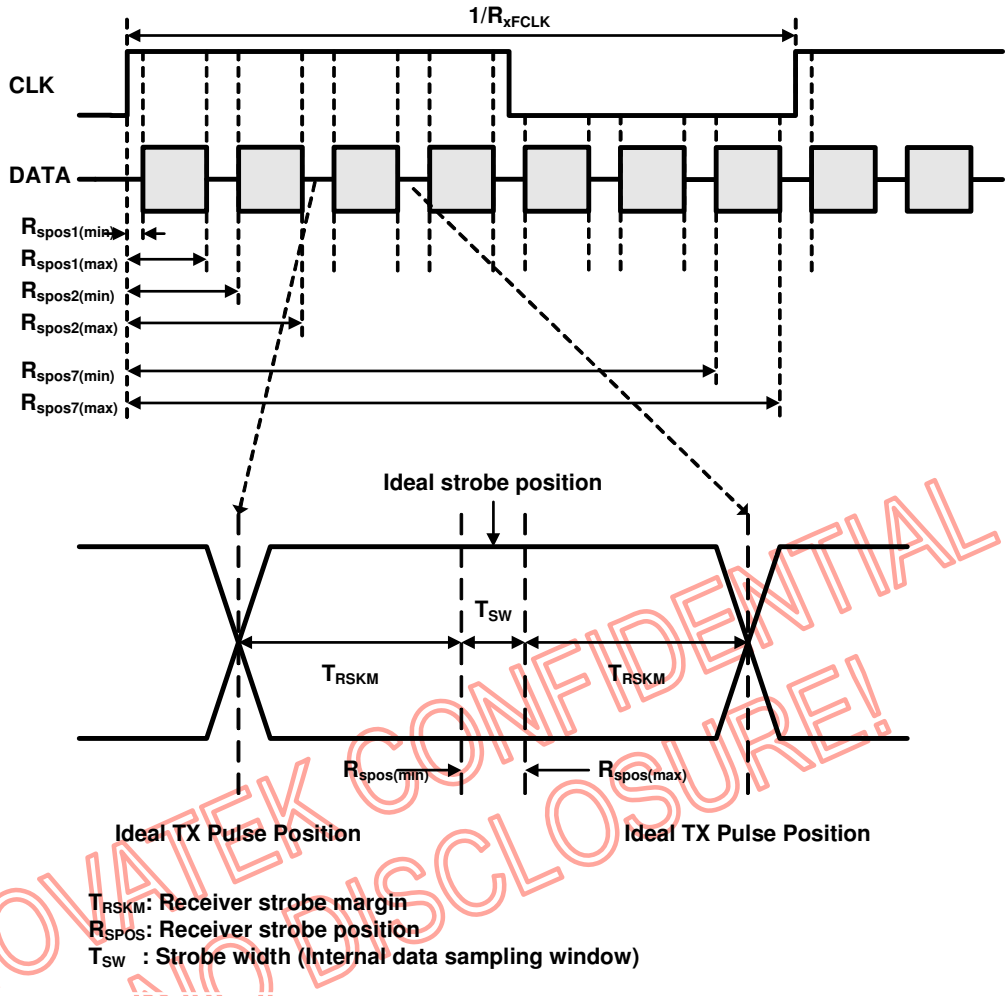


FIGURE 24. Definition of Data Skew Margin (T_{RSKM})

MIPI Receiver Differential Input (DC Characteristics)						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
BR_{MIPI}	Input data bit rate	200	-	1000	Mbps	-
V_{CMRX}	Common-mode voltage (HS Rx mode)	70	-	330	mV	
V_{IDTH}	Differential input high threshold (HS Rx mode)	-	-	70	mV	
V_{IDTL}	Differential input low threshold (HS Rx mode)	-70	-	-	mV	
$\lvert V_{IDM} \rvert$	Differential input voltage range (HS Rx mode)	70	-	500	mV	
V_{IHHS}	Single-end input high voltage (HS Rx mode)	-	-	460	mV	
V_{ILHS}	Single-end input low voltage (HS Rx mode)	-40	-	-	mV	
Z_{ID}	Differential input impedance	80	100	125	Ω	
V_{IHLP}	Logic 1 input voltage (LP Rx mode)	880	-	-	mV	
V_{ILLP}	Logic 0 input voltage (LP Rx mode)	-	-	550	mV	
V_{OH}	Output high level (LP Tx mode)	1.08	1.2	1.32	V	
V_{OL}	Output low level (LP Tx mode)	-50	-	50	mV	

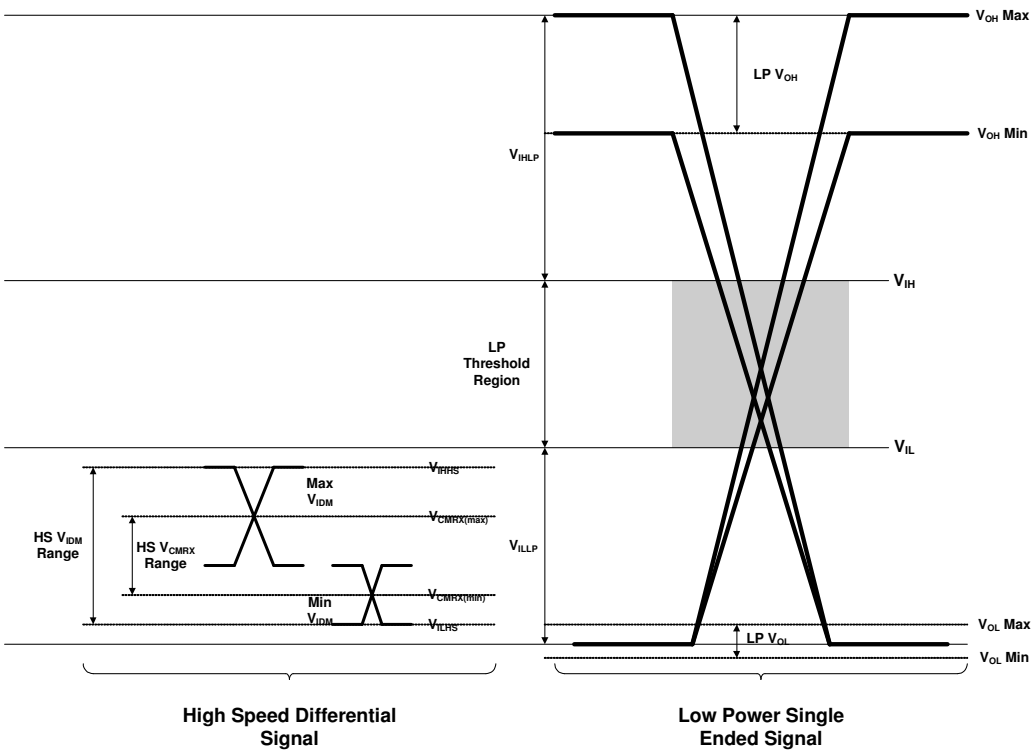


FIGURE 25. Definition of MIPI Signal Level

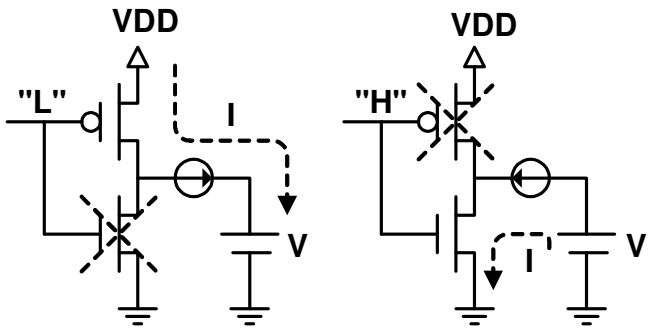


FIGURE 26. Definition of Output Impedance of LP Tx Mode

MIPI Receiver Differential Input (AC Characteristics)						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
T_{MIN-RX}	Minimum pulse width response (LP Rx mode)	50	-	-	ns	
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	50	55	58	ns	1st clock pulse after STOP state or last clock pulse before STOP state/all other pulse
T_{RLP} / T_{FLP}	15%~85% rise time and fall time (LP Tx mode)	-	-	25	ns	
T_{REOT}	30%~85% rise time and fall time of EOT (LP Tx mode)	-	-	35	ns	
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90	-	-	ns	
T_{SETUP}	Data to clock setup time	0.15	-	-	UI	
T_{HOLD}	Data to clock setup time	0.15	-	-	UI	

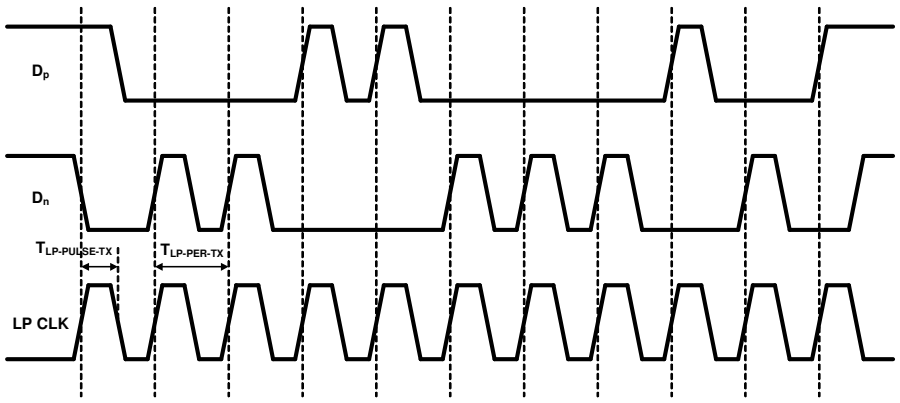


FIGURE 27. Definition of Exclusive-OR Clock in LP Mode

mini-LVDS Transmitter Differential Output (DC Characteristics)						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
$\|V_{OD}\|$	Differential output voltage	100	200	500	mV	R_L = 100 Ω Rpi = 8k Ω
V_{OS}	Offset voltage	1.0	1.2	1.4	V	
		0.6	0.8	1.0	V	

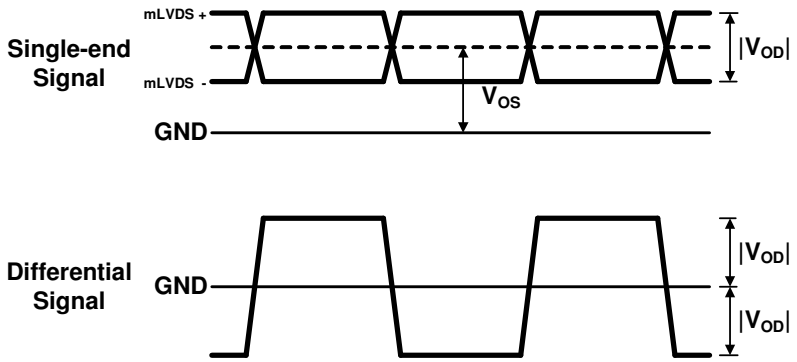


FIGURE 28. Definition of Common Mode Voltage (V_{OS}) and Differential Output Voltage ($|V_{OD}|$)

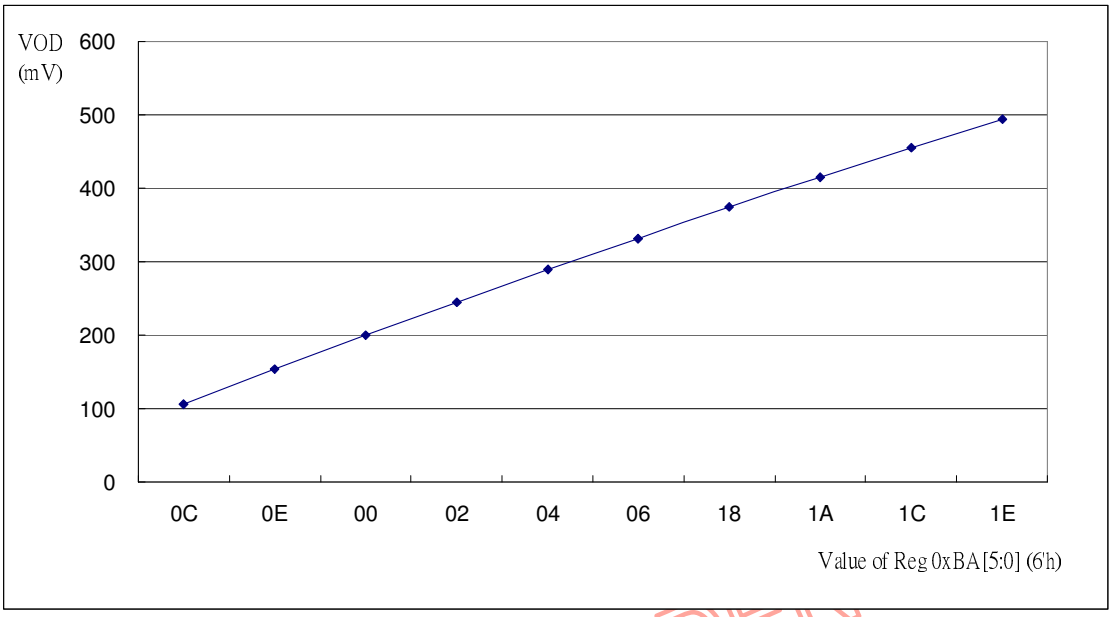


FIGURE 29. Definition of Differential Output Voltage with Different Setting

mini-LVDS Transmitter Differential Output (AC Characteristics)						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
F_{MLVCLK}	mini-LVDS clock frequency	37.5	-	350	MHz	-
T_{RISE}	Transition Rising Time	300	-	900	ps	R_L = 100 Ω, C_L = 5 pF, F_{MLVCLK} = 300 MHz
T_{FALL}	Transition Falling Time	300	-	900	ps	

FIGURE 30. Definition of transition rising time (T_{RISE}) and falling time (T_{FALL})

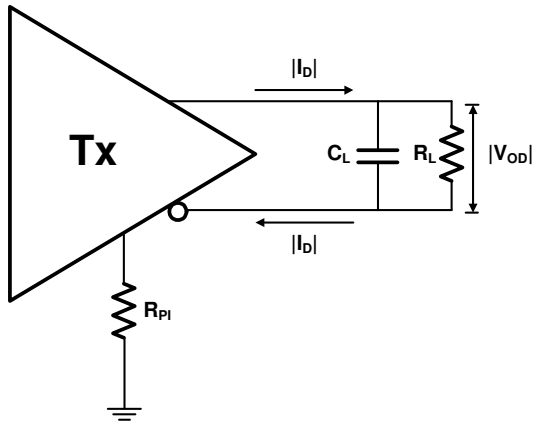


FIGURE 31. mini-LVDS loading definition

Internal Built-in Oscillator						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
f_{osc}	Internal OSC frequency	66.5	70	73.5	MHz	

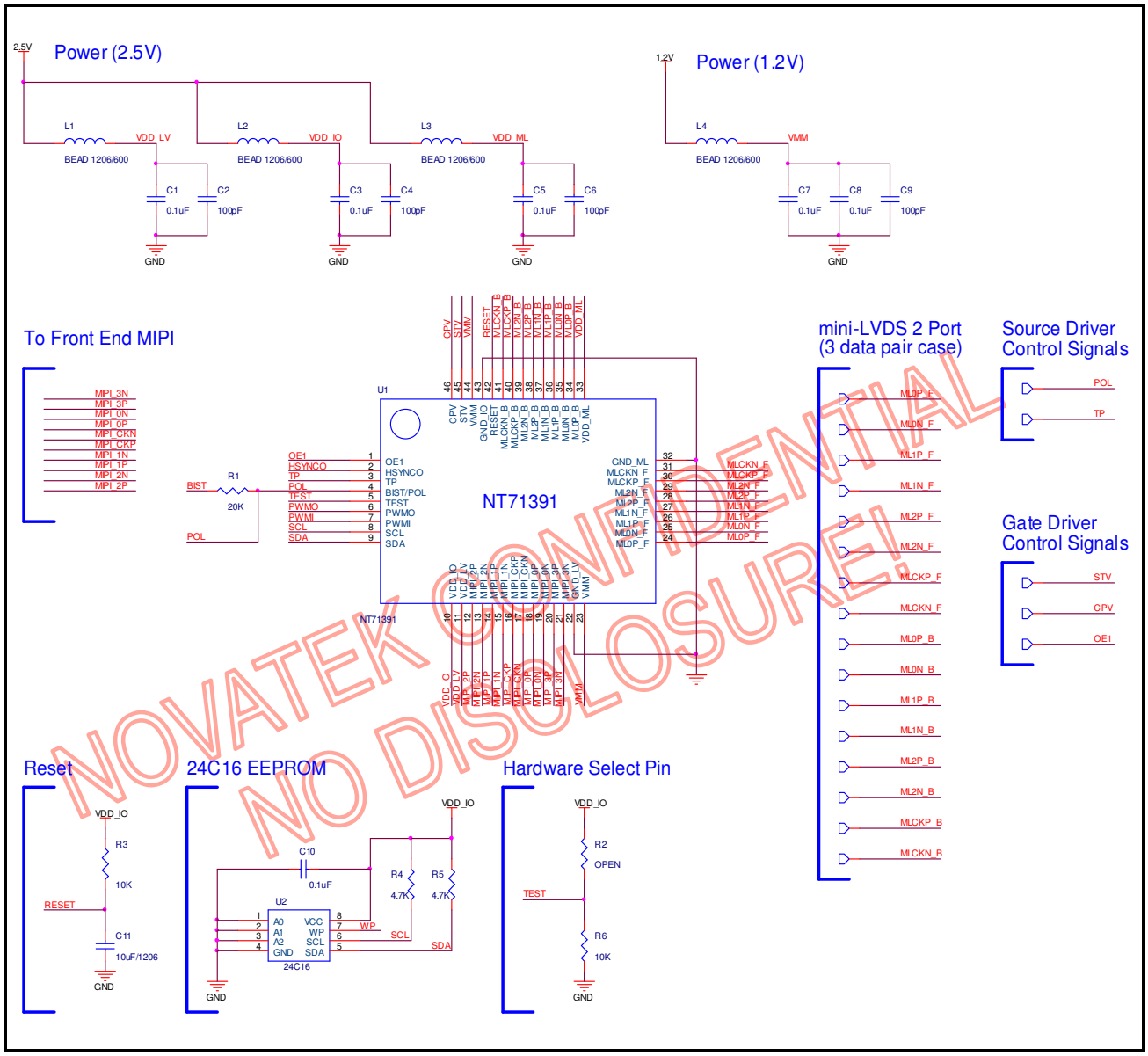
SSCG						
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
F_M	Modulation Frequency	-	50	-	kHz	
T_{dmax}	Advance/delay maximum modulation ratio	-	1.5	-	%	Mode[1:0]= 00
		-	3.0	-	%	Mode[1:0]= 01
		-	4.5	-	%	Mode[1:0]= 10
		-	6.0	-	%	Mode[1:0]= 11

10 Order Information

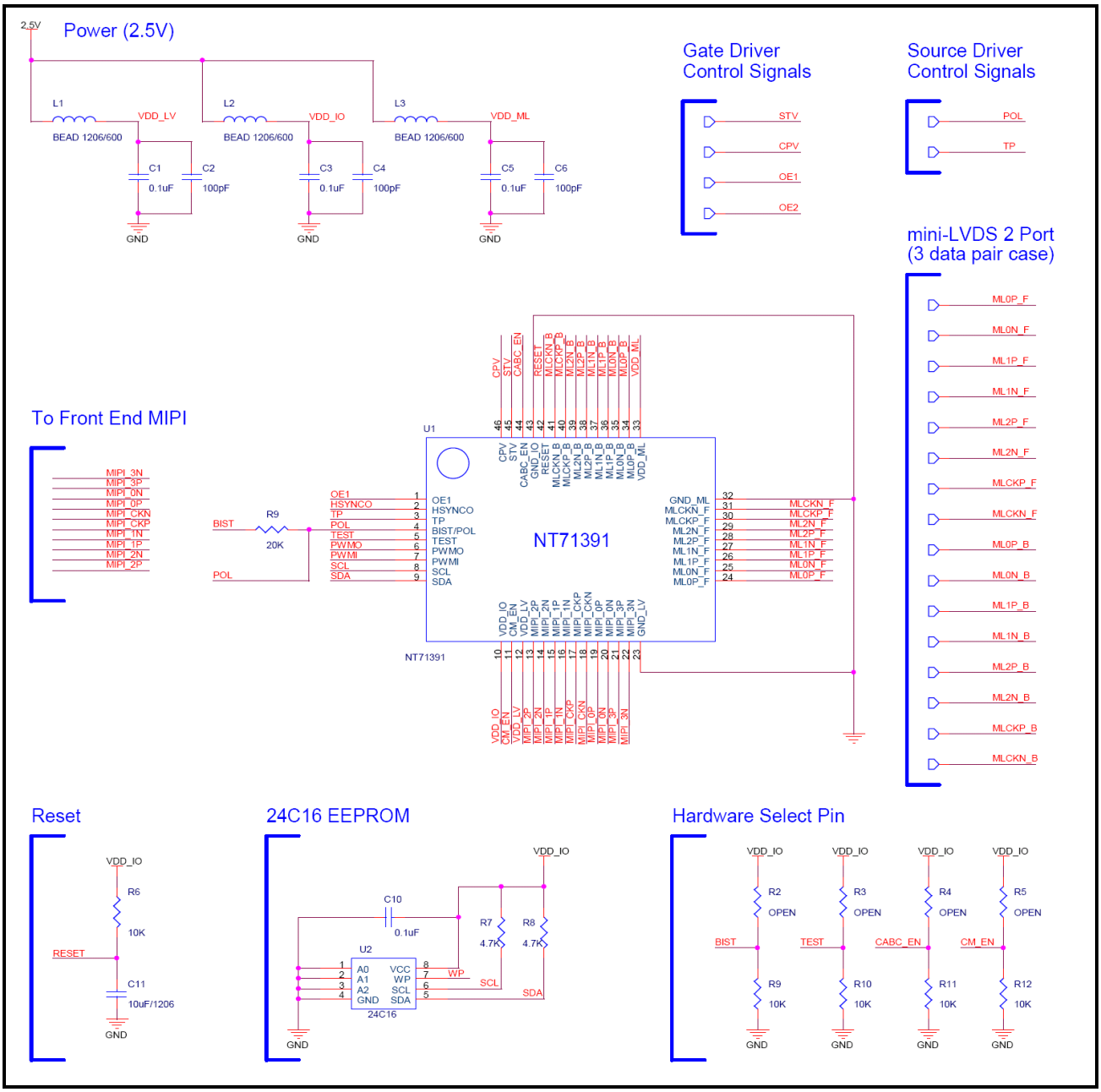
Part Name	Packages	Remark
NT71391QG	QFN 46	Pb-free
NT71391QG-001	QFN 46	Pb-free
NT71391QG-601	QFN 60	Pb-free

11 Application Circuit

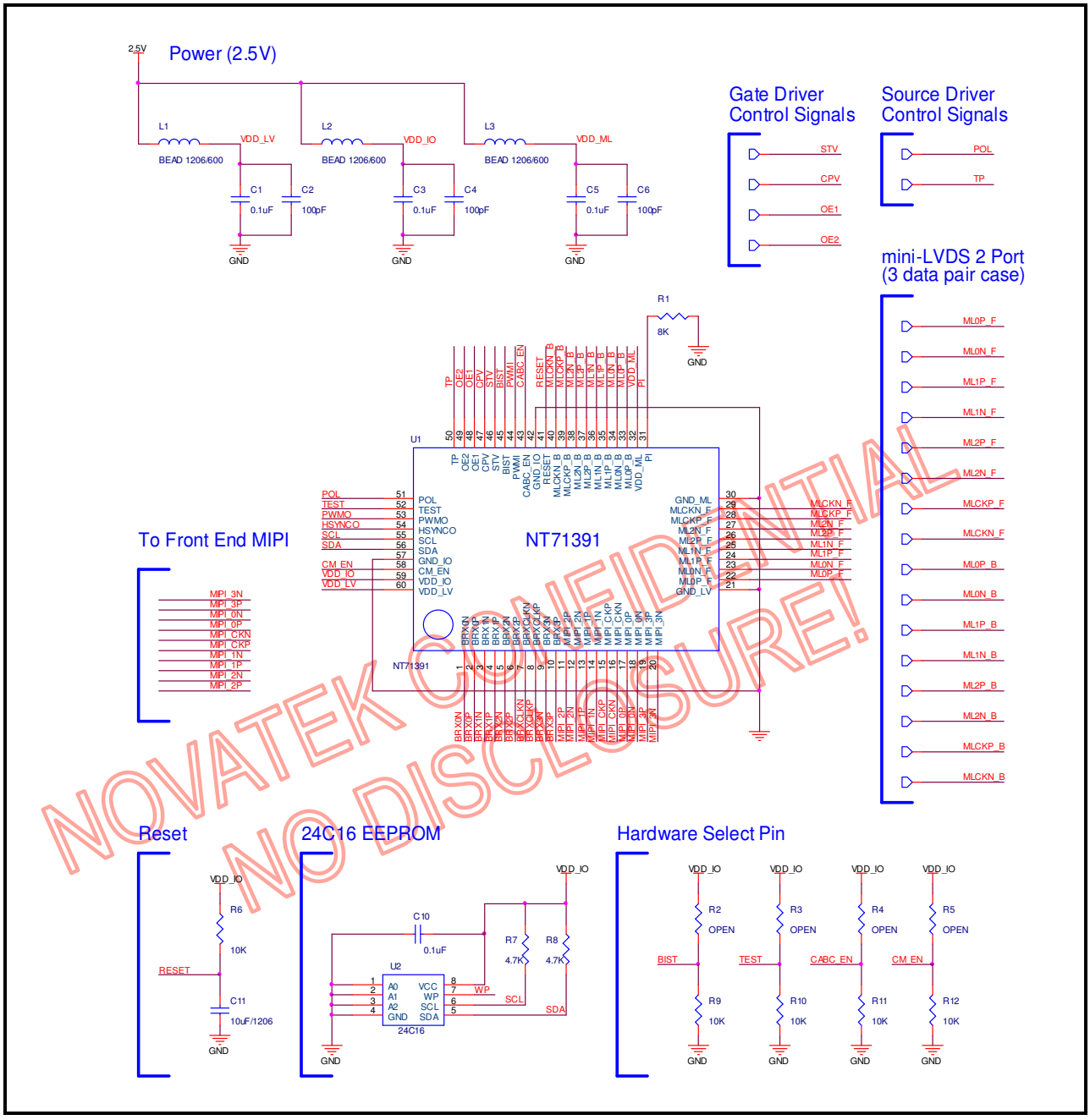
46-pin NT71391QG – Default application circuit :



46-pin NT71391QG – 001 application circuit :

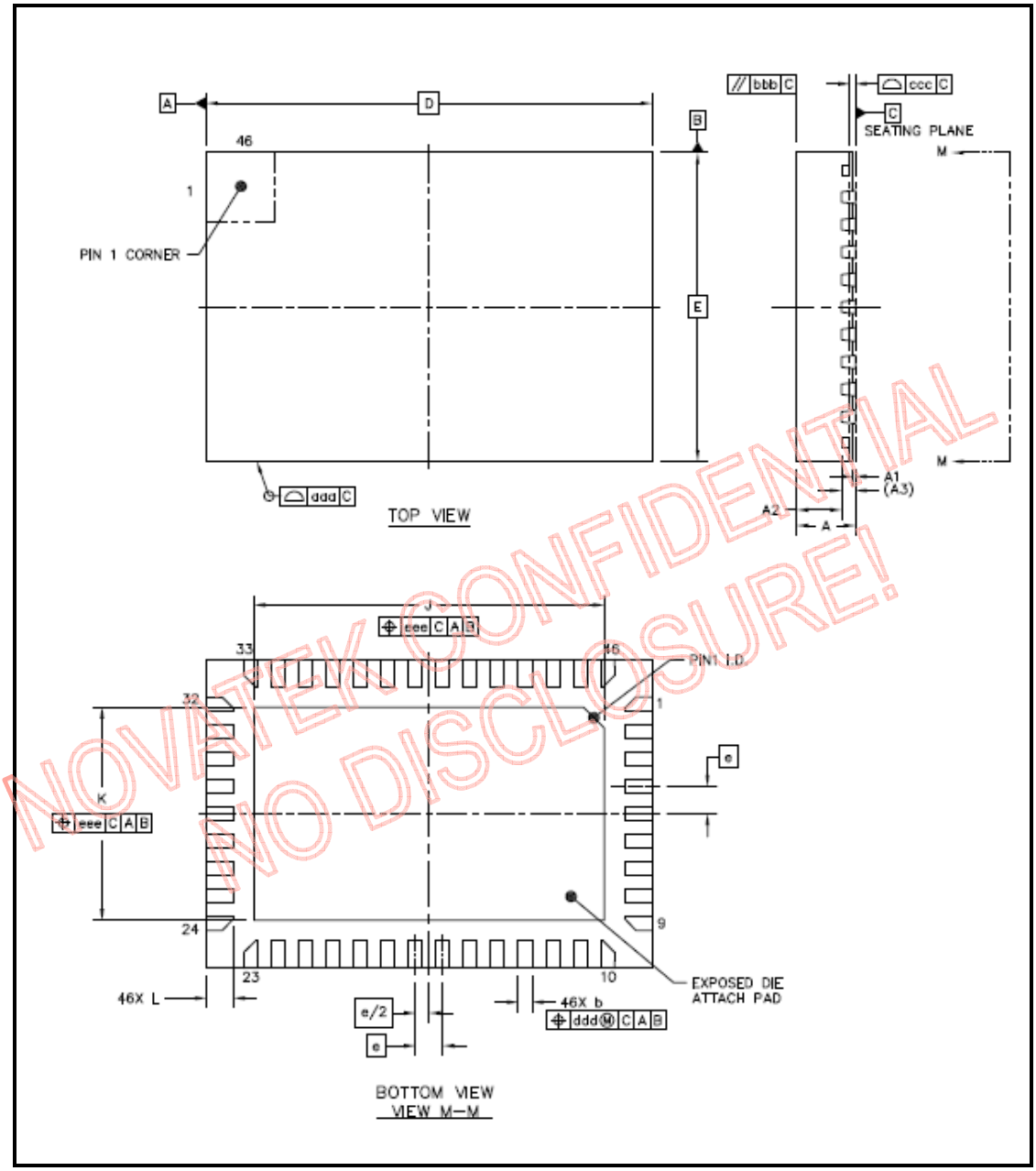


60-pin NT71391QG-601 application circuit :



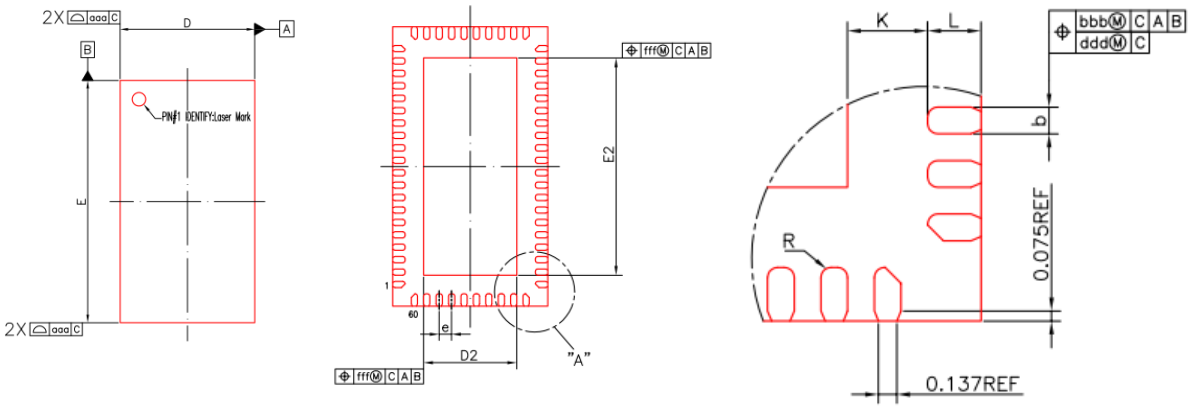
12 Package Information

46-pin Outline drawing and dimension

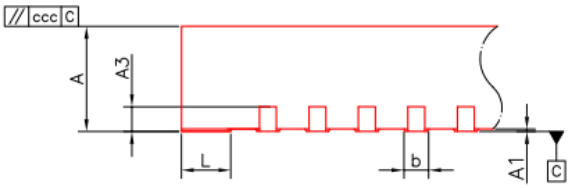


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6.5 BSC	
	Y	E		4.5 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	5	5.1	5.2
	Y	K	3	3.1	3.2
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

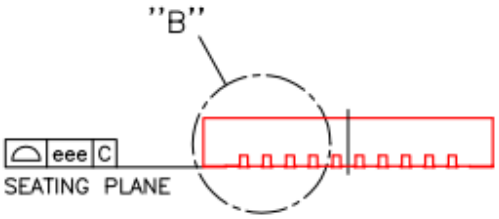
60-pin Outline drawing and dimension



DETAIL : "A"



DETAIL : "B"



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
E	8.90	9.00	9.10	0.350	0.354	0.358
D2	2.85	3.00	3.15	0.112	0.118	0.124
E2	6.85	7.00	7.15	0.270	0.276	0.281
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.075	---	---	0.003	---	---
K	0.20	---	---	0.008	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

13 Appendix

Power-on Behavior of Output Signal

The power-on behavior of TCON output signal is as the following diagram.

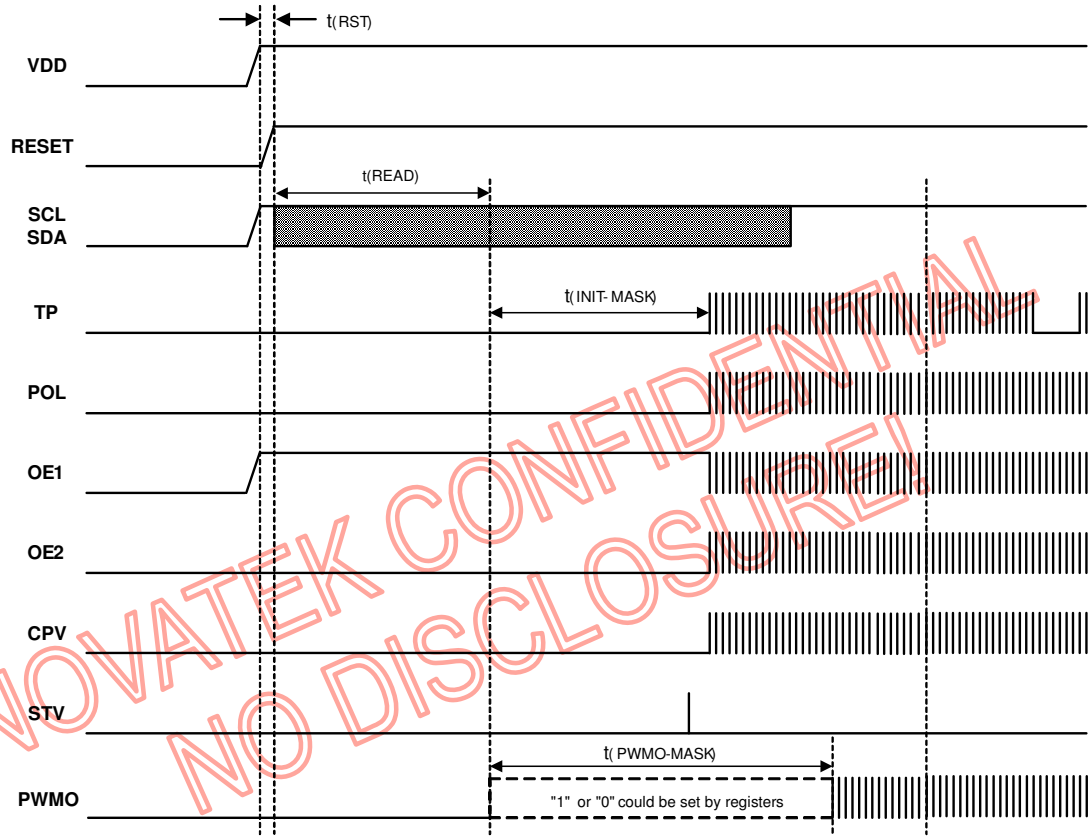
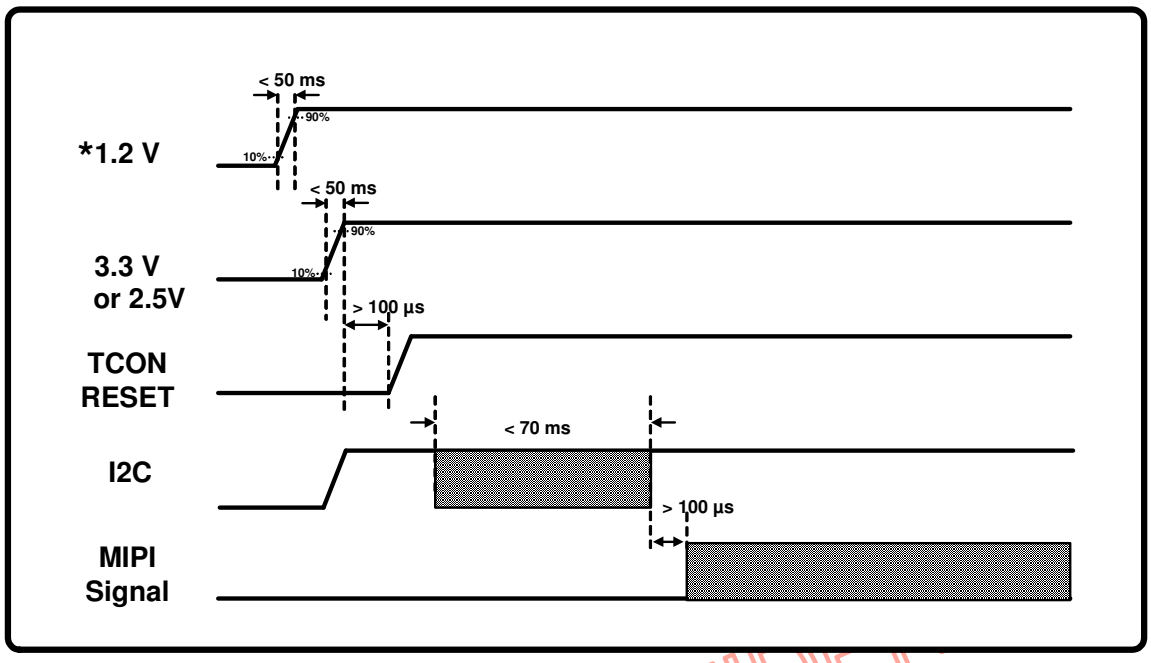


FIGURE 1. Power-on Behavior of Output Signal

$t_{(RST)}$: Reset timing of internal circuit, after V_{DD} power on.
$t_{(READ)}$: Downloading period of TCON from TCON setting page (page 0) of EEPROM.
$t_{(INIT-MASK)}$: Power-on mask period for masking initial state of TCON, and users might control it by registers setting.
$t_{(PWMO-MASK)}$: Power-on mask period for masking initial state of TCON, and users might control it by registers setting.

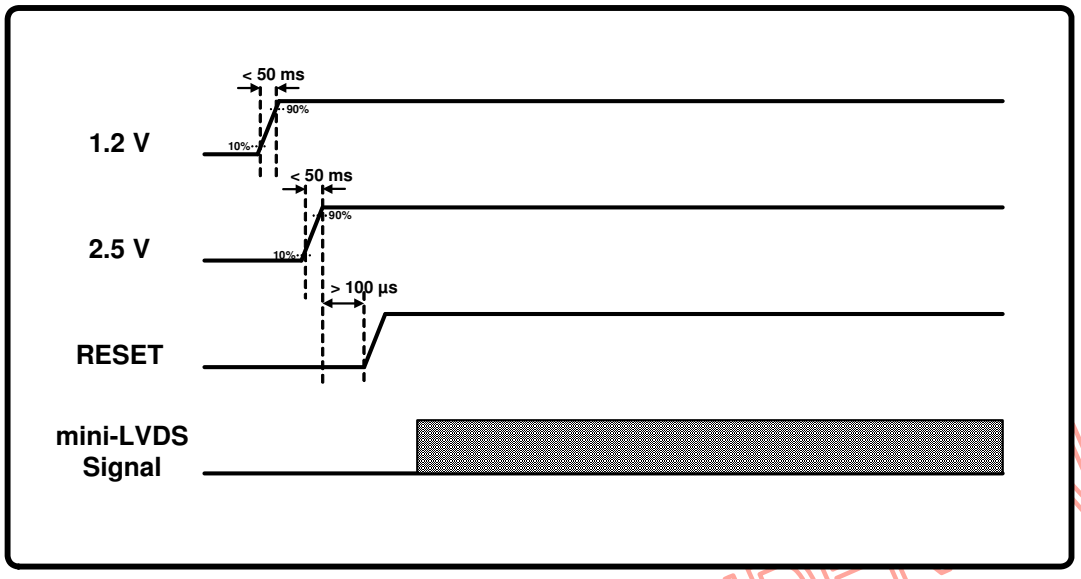
MIPI Power-on Behavior



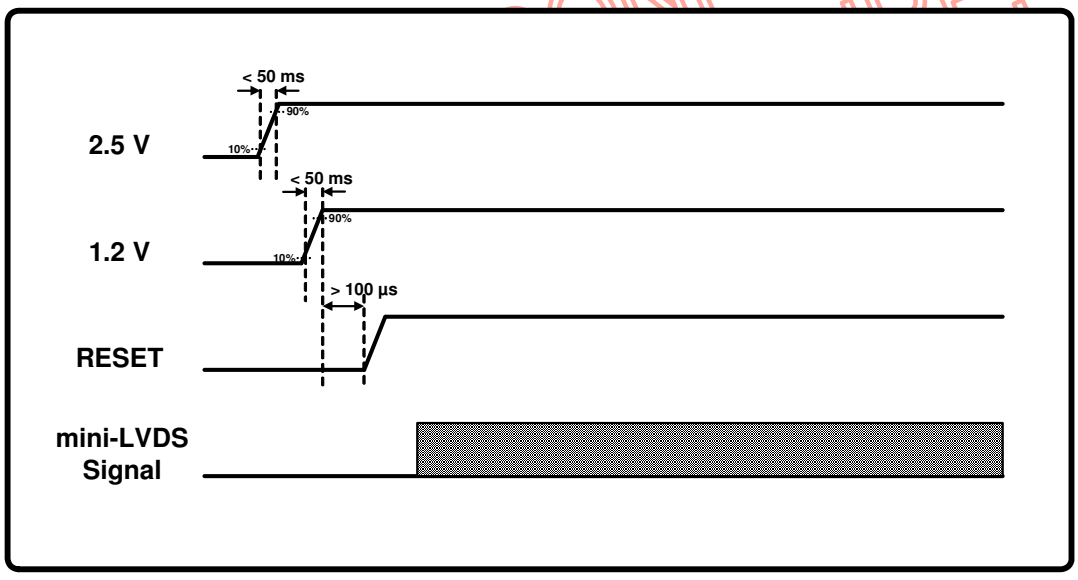
***1.2V is only for NT71391QG – Default.**

NT71391QG-001 Power-on Behavior (External VMM)

Case 1:



Case 2:



No matter 2.5V or 1.2V power on first, TCON can work well.