

Chunghwa Picture Tubes, Ltd. Product Specification

To:上海汽車 Date: 20150310

TFT LCD CLAA104EA01 XN

ACCEPTED BY : (V0.1)	
Only For customer Reference	

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REVISION STATUS

Revision Notice	Description	Page	Rev. Date
0.0	First version		2015/02/04
0.1	NC	10	2015/02/16
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1. OVERVIEW

CLAA104EA01 XN is 10.4" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs ,control circuit and LED backlight. By applying $960(H) \times 3$ (RGB) \times 1280(V) \times images are displayed on the 10.4" diagonal screen. Display 16.7M colors by R.G.B signal input.

General specification are summarized in the following table:

ITEM	SPECIFICATION			
Display Area (mm)	158.4(H) x 211.2(V)			
Number of Pixels	960(H) × 3 (RGB) × 1280(V)			
Pixel Pitch (mm)	0.165x0.165mm			
Color Pixel Arrangement	RGB vertical stripe			
Display Mode	Normally Black			
Number of Colors	16.7M (Real 8 bit)			
Brightness (cd/m^2)	650nit (min)			
Response Time (ms)	25°C : 25ms(typ) / 30ms(max)			
Response Time -20°C	Tr+ Tf: 400ms(max)			
Response Time -30°C	Tr+ Tf: 700 ms(max.)			
Contrast Ratio	800:1(Min) /1000:1(Typ)			
Viewing Angle (CR≧10)	170degree (Horizontal)			
Viewing Angle (CR = 10)	170degree (Vertical)			
Power Consumption (W)	TBD			
Interface connection	LVDS			
	173.4 x 228.7 x 9.0(W/O Heat Sink)			
Module Size (mm)	173.4 x 228.7 x 13.9 (W/ Heat Sink)			
	TOD			
Module Weight (g)	TBD			
Backlight Unit	LED			
Surface Treatment	Anti-Glare 25%, 3H			
Reflectivity	<4.5% base on SCI at 8°			

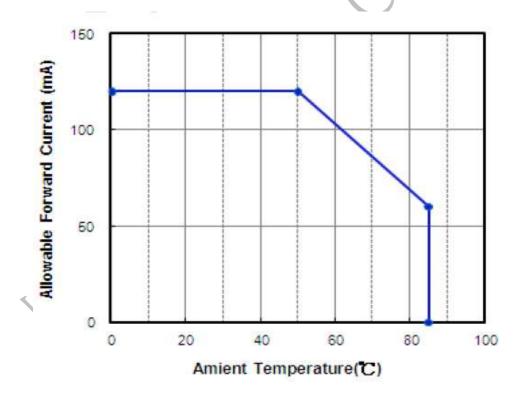
2. ABSOLUTE MAXIMUM RATINGS

The following are maximun values which, if exceeded, may cause faulty operation or damage to the unit.

Item	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	DVDD DVDD_LVDS	-0.3	3.96	V	
Analog Supply Voltage Positive	AVDDP	-0.3	6.5	V	
Analog Supply Voltage Negative	AVDDN	-6.5	0.3	V	
Gate On Voltage	VGH	-0.3	42	V	
Gate Off Voltage	VGL	-25	0.3	V	
Gate On-Gate Off Voltage	VGH-VGL	12	40	V	λ
Signal Input Voltage	NIND0 ~ NIND3 PIND0 ~ PIND3 NINC,PINC	-0.3	DVDD+0.3	V	7
Forward Current (per LED)	If	-	120	mA	
Pulse forward current (per LED)	lfp	-	240	mA	1 \ 2 \ 3
Operating temperature	Topa	-40	85	$^{\circ}\mathbb{C}$	4.5
Storage temperature	Tstg	-40	90	$\mathcal C$	4

Note:

- *1) If the product were used out of the operation and storage range, it will have quality issue.
- *2) Ifp Conditions : Pulse Width \leq 10msec , Duty \leq 1/10.
- *3) Each one of LED operation must be follow diagram of Ambient Temperature and Allowable Forward Current.



 $^{^*}$ 4) If users use the product out off the environmental operation range (temperature and humidity), it will have visual quality concerns.

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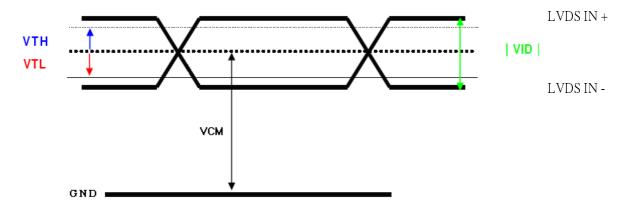
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD

Ta=25°C

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Digital Power Supply Voltage For LCD	DVDD	3	3.3	3.6	V	
	VCM	1	1.2	$1.7 - \frac{ \text{VID} }{2}$	V	Note1
Logic Input Voltage (LVDS:IN+,IN-)	VID	200	-	600	mV	Note1
(2000(1,114)	VTH	100	-	300	mV	VCM=1.2V Note1
	VTL	-300	-	-100	mV	• ()
Analog Supply Voltage Positive	AVDDP		6		V	
Analog Supply Voltage Negtive	AVDDN		-6		\	
Gate On Power Supply Voltage	VGH	17	18	19	У	
Gate Off Power Supply Voltage	VGL	-12.6	-12	-11.4	٧	
Logio logut Voltago	VIH	0.7*DVDD	-	DVDD	V	
Logic Input Voltage	VIL	GND	-	0.3*DVDD	V	

Note1: LVDS signal



[Recommend] VCOM must be optimized according to each LCM. Please adjust VR to make the flicker level be minimum for getting excellent image.

3.2 TFT-LCD Current Consumption

Item	Symbol	Condition	Min.	Тур.	Max.	Unit.	Note.
Gate on Current	IVGH	VGH =18V	-	TBD		mA	[Note1]
Gate off Current	IVGL	VGL= -12V	-	TBD		mA	[Note1]
Digital Current	IDVDD	DVDD = 3.3V	-	TBD		mA	[Note1]
Analog Current Positive	IAVDD	AVDDP = 6	-	TBD		mA	[Note1]
Analog Current Negtive	IAVDDP	AVDDN = -6	-	TBD		mA	[Note1]
Total Power Consumption	PC		-	TBD		mW	[Note1]

[Note]

Note1: Typical: Under 256 gray pattern Maximum: Under white pattern



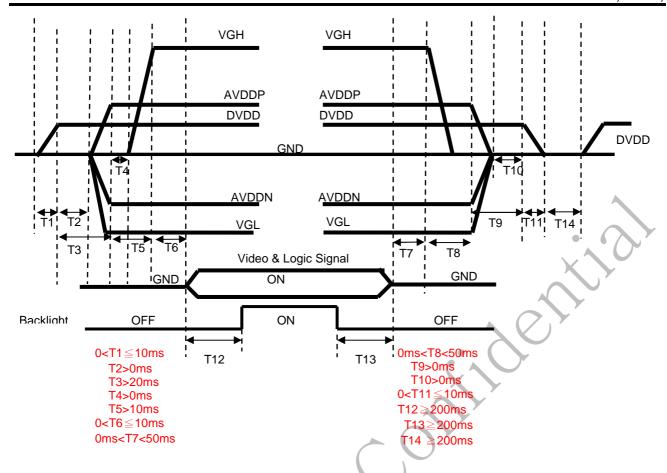
256 gray pattern



white Pattern

3.3 Power and Signal sequence

Power On: DVDD→AVDDP/AVDDN/VGL →VGH →Video &Logic Signal→Backlight Power Off: Backlight→Video &Logic Signal→ VGH→AVDDP/AVDDN/VGL→DVDD



3.4 Backlight

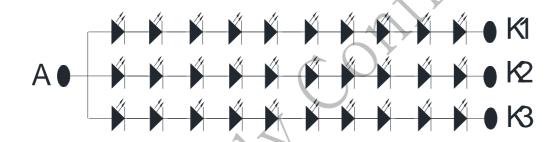
Base on 7S4P

Ta=25°C

ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
LED current	IL	Ta=25°ℂ		360		mA	LED
LLD current	ı.	(120mA/serise)		300		111/	current
LED voltage	VL	Ta=25°C		31		V	LED
LED Vollage	V L	(120mA/serise)	erise)		V		voltage
		Ta=25℃					Power
Power consumption	WL	(120mA/serise)		11.16		W	consumpt
		(1201117/361136)					ion
LED Lifetime	_	Ta=25°C	10000			Hr	LED
LLD LIIGUIIIG	_	IF=120mA	10000			111	Lifetime
LED Lifetime	_	Ta=85°C	1000			Hr	LED
LLD LIIGUIIIE	_	IF=120mA	1000				Lifetime

Remarks:

^{*1)}LED Circuit Diagram



- *2) A: Anode(+), K: Cathode(-)
- *3) Suggestion: Using the constant current control to avoid the leakage light and brightness quality issue.
- *4) Definition of Led lifetime: Luminance < Initial luminance 70%.

4. INTERFACE CONNECTION

4.1 CN1 (Input Signal)

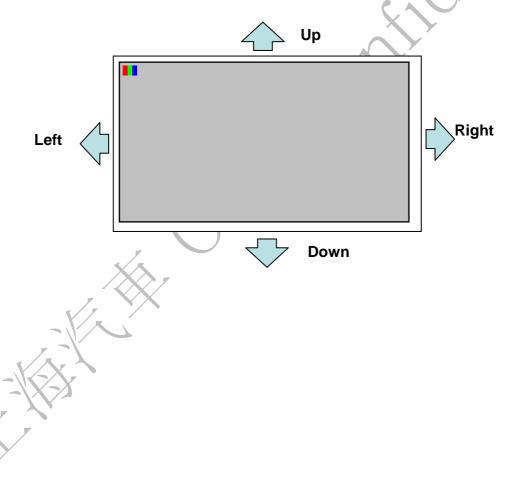
Connector: FH52-60S-0.5SH (HRS)

l	Pin NO.	Symbol	Description
ŀ	1		Not Connect
ł	2		Not Connect
	3	AGND	Analog ground
l	4		Not Connect
l	5	AVDDP	Analog power +6V(typ)
	6	AVDDP	Analog power +6V(typ)
	7		Not Connect
	8		Analog power -6V(typ)
	9		Analog power -6V(typ)
51	10		Not Connect
	11	DVDD	Digital power +3.3V(typ)
	12	DVDD	Digital power +3.3V(typ)
	13		Not Connect
	14	GND	Digital ground
	15	GND	Digital ground
	16	GND	Digital ground
l	17		Digital ground
	18	PIND3	Positive LVDS differential data input
l	19		Negative LVDS differential data input
41	20		Digital ground
Ш	21		Positive LVDS differential clock input
	22		Negative LVDS differential clock input
	23	GND	Digital ground
	24	PIND2	Positive LVDS differential data input
Ī	25	NIND2	Negative LVDS differential data input
	26	GND	Digital ground
	27	PIND1	Positive LVDS differential data input
	28	NIND1	Negative LVDS differential data input
[29	GND	Digital ground
31	30	PIND0	Positive LVDS differential data input
	31	NIND0	Negative LVDS differential data input
	32	GND	Digital ground
	33	GND	Digital ground
			Global reset pin. Active low to enter reset state.
	34	GRB	Suggest to connecting with an RC reset circuit for stability.
			Normally pull high. (R=47K Ω , C=0.1 μ F)
			Standby mode, normally pull high
	35	STBYB	STBYB="1", normal operation
		V/AX	STBYB="0",timing control, source driver will turn off, all output are high-Z
	36	RL	Left or right display control
	37	DVDD	Digital power +3.3V(typ)
	38	TB	Up / down display control
21	39	NC NC	For Test, Please Keep it floating
21	40	NC	For Test, Please Keep it floating
	41/	NC A CNID	For Test, Please Keep it floating
	42		Analog ground
- 1	43		Not Connect
-	44		Analog power +6V(typ)
- 1	45		Analog power +6V(typ)
}	46 47		Not Connect
-			Analog power -6V(typ)
ŀ	48		Analog power -6V(typ)
11	49		Not Connect
	50		Digital ground
	51	GND	Digital ground

52	GND	Digital ground
53	NC	Not Connect
54	DVDD	Digital power +3.3V(typ)
55	NC	Not Connect
56	VGH	Positive power for TFT +18V(typ)
57	NC	Not Connect
58	VGL	Negative power for TFT -12V(typ)
59	NC	Not Connect
60	GND	Digital ground

Note 1: RL and TB control function

RL	ТВ	Data shifting
DVDD	GND	Left→Right , Up→Down(default)
GND	GND	Right→Left [,] Up→Down
DVDD	DVDD	Left→Right [,] Down→Up
GND	DVDD	Right→Left [,] Down→Up



4.2 CN2 (LED backlight)

Modify by the first version SPEC and NTC: Murata (NCP18XH103F0SRB)

Pin No.	Symbol	Function
1	A	Anode
2	Α	Anode
3	Α	Anode
4	Dummy	NC
5	K1	Cathode 1
6	K2	Cathode 2
7	K3	Cathode 3
8	Dummy	NC
9	NTC_A	NTC_Anode
10	NTC_K	NTC_Cathode

Note-1: Inverter side connector: FH52-10S-0.5SH (HRS)

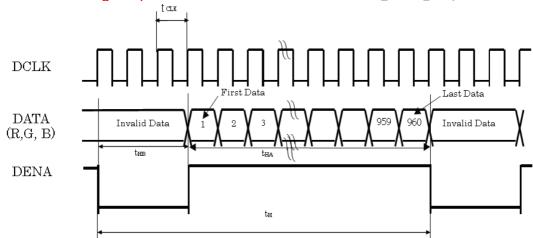
5. INPUT SIGNAL(DE ONLY MODE)

5.1 Timing Specification

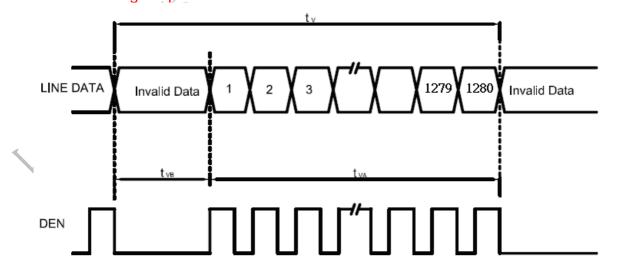
		Symbol	Min.	Тур.	Max.	Unit		
LVDS input signal sequence		CLK Fre	equency	tclk	(70.4)	78.4	(83.2)	MHz
			(984)	990	(1004)	990	1004	tCLK
		Horizontal	Horizontal effective Time	t _{HA}		960		tCLK
LCD input signal sequence	DENIA		Horizontal Blank Time	t _{HB}	(24)	30	(44)	tCLK
(Input LVDS	DENA		Vertical total Time	t_V	(1300)	1320	(1380)	t _H
Transmitter)		Vertical	Vertical effective Time	t_{VA}		1280	• (ŧн
			Vertical Blank Time	t_{VB}	(20)	40	(100)	t _H

5.2 Timing sequence(Timing chart)

5.2.1 Horizontal Timing Sequence

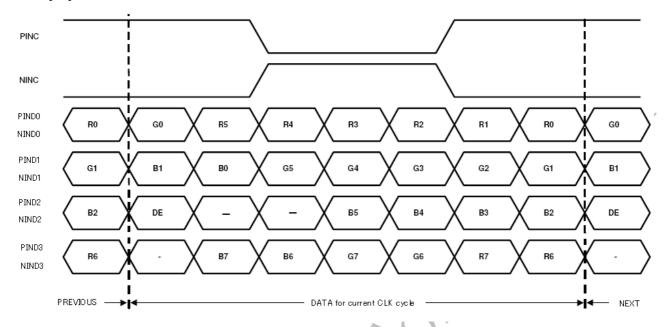


5.2.2 Vertical Timing Sequence



5.2.3 LVDS Input Data mapping

8 Bit LVDS input Modify by the first version SPEC



5.2.4 Color Data Reference Modify by the first version SPEC

Widaii	by the mat	VEIS	ersion SPEC																						
					R D	_			1		ı			ATA		1			1	1	B D				
COLOR	INPUT DATA	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	В7	B6	B5	B4	ВЗ	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BASIC	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
COLOR	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1/	1
	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	r 0	0	0	0
RED																	_			•					
																			X						
	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	_1	0	0	0	0	0	0	0	0	0
GREEN												1													
	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1,	∢1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	BLUE(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
BLUE																									
	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
-	. ,	_		1		7																			

(Note)

1) Gray level:

Color(n): n is level order; higher n means brighter level.

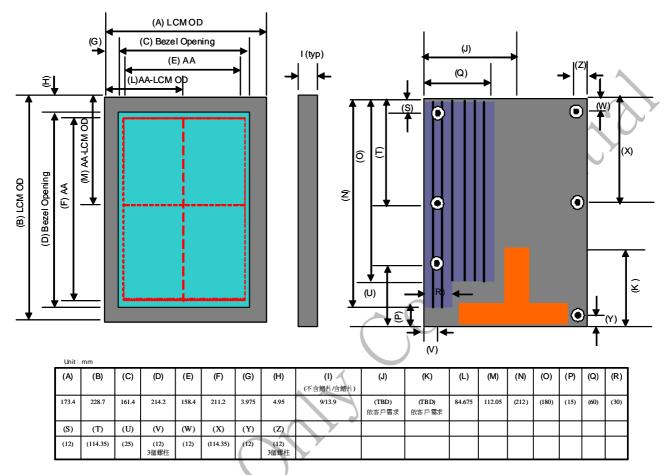
2) DATA:

1: high , 0: low

6. MECHANICAL DIMENSION

6.1 Front Side

Modify by the first version SPEC



NOTE: General tolerance=±0.3mm

NOTE: General tolerance=±0.3mm

6.2 Rear Side

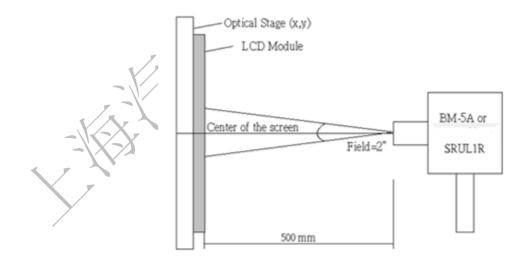
(Unit: mm)

7. OPTICAL CHARACTERISTICS

Ta = 25℃, VCC=3.3V

I	ГЕМ	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Consti	rast Ratio	CR	Point-5	800	1000			1, 2, 3
Lumina	nce(CEN)	Lw	Point-5	650	1		cd/m ²	1, 3
Luminand	e Uniformity	ΔL		80	-		%	1, 3
	nse Time e - Black)	Tr +Tf	Point-5	-	25	30	ms	1, 3, 5
N	TSC	-	Point-5		70	1	%	1, 4
	Vertical	Upper(θ)		75	85		•	
Viewing	vertical	$Down(\theta)$	CR≧10	75	85			1, 4
Angle	Horizontal	Left(ψ)	Point-5	75	85		0	1, 4
	Honzoniai	Right(ψ)		75	85			1, 4
	White	Wx Wy		(0.2873) (0.2987)	(0.3173) (0.3197)	(0.3473) (0.3497)		
Color	Red	Rx Ry	Point-5	(TBD) (TBD)	(TBD) (TBD)	(TBD) (TBD)		1, 3
Coordinate	Green	Gx Gy		(TBD) (TBD)	(TBD) (TBD)	(TBD) (TBD)		·
	Blue	Bx By		(TBD) (TBD)	(TBD) (TBD)	(TBD) (TBD)		

Note1: Measure condition: 25°C±2°C → 60±10%RH → under 1 Lux in the dark room color coordinate and color gamut are measured by SRUL1R,and all the other items are measured by BM-5A (TOPCON) → viewing angle2° → IL=320mA (Backlight current) → measurement after lighting on 10 mins



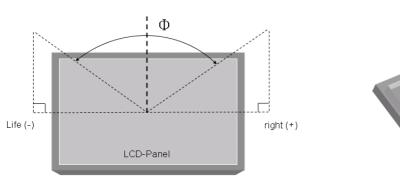
Note2: Definition of contrast ratio :

Contrast Ratio (CR)= (White) Luminance of ON ÷ (Black) Luminance of OFF

Note3: Definition of luminance : Measure white luminance on the point 5 as figure.7-1 Definition of Luminance Uniformity: Measure white luminance on the point1~9 as figure.7-1 $\Delta L = [L(MIN)/L(MAX)] \times 100$

Fig.7-1 Measuring point

Note 4: Definition of Viewing Angle(θ , ψ),refer to Fig.7-2 as below :



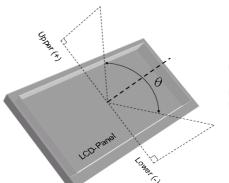


Fig.7-2 Definition of Viewing Angle

Note5: Definition of Response Time.(White-Black)

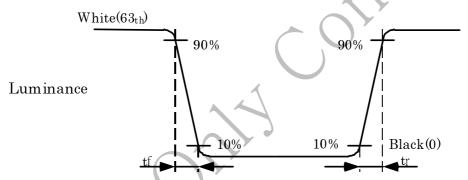


Fig.7-3 Definition of Response Time(White-Black)

8. RELIABILITY TEST

8.1. Temperature and humidity

TEST ITEMS	CONDITIONS	NOTE
High Temperature Operation	85° C ;504hrs	
High Temperature Storage	90° C ;504hrs	
High Temperature High Humidity Operation	60°C; 90%; 504hrs	No condensation
Low Temperature Operation	-40° C ; 504hrs	Function only
Low Temperature Storage	-40° C ; 504hrs	
Thermal Shock	–40°C (0.5hr) ~ 85°C (0.5hr) ;	
Thermal Shock	300 Cycles	
Image Sticking	25 $^{\circ}$ C ± 2 $^{\circ}$ C; 2hrs	Note 1

Note 1.:

Condition of Image Sticking test : 25 $^{\circ}$ C ± 2 $^{\circ}$ C

Operation with test pattern sustained for 2 hrs, then change to gray pattern immediately.

After 5 mins, the mura must be disappeared completely.

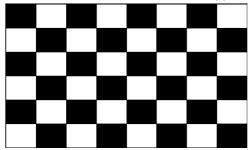


Image Sticking -pattern

Mid-Gray pattern

8.2. Shock and Vibration

TEST ITEMS	CONDITIONS							
Shock (Non-operation)	 Shock level: 980m/s2(equal to 100G). Waveform: half sinusoidal wave,6ms. Number of shocks: +X,+Y,+Z each axis 3 times 							
	● Frequency range: 8~33.3Hz							
√x	Stoke: 1.3 mm							
Vibration	Vibration: sinusoidal wave, perpendicular axis							
(Non-operation)	● (both x, z axis:2Hrs, y axis 4Hrs).							
1/7	 Sweep: 2.9G, 33.3 Hz -400 Hz 							
	Cycle: 15 min							

8.3 Electrostatic Discharge

TEST ITEM	CONDITIONS	Note
ESD (Power On)	330pF \ 2KΩ \ 10 polarity / point / 3s Contact discharge : ±4Kv (Class B) ±8Kv (Class B) ±15Kv (Class C) 330pF \ 2KΩ \ 10 polarity / point / 3s	1
	Air discharge : ±6Kv (Class B) ±15Kv (Class C)	1
ESD (Power Off)	330pF · 2KΩ · Air discharge · ±25Kv	1

Note: Measure

1: LCD glass and metal bezel

8.4. Judgment standard

The judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect.

Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defects.

9. WARRANTY

- 9.1 The period is within 12 months since the date of shipping out under normal using and storage conditions.
- 9.2 The warranty will be avoided in case of defect induced by customer