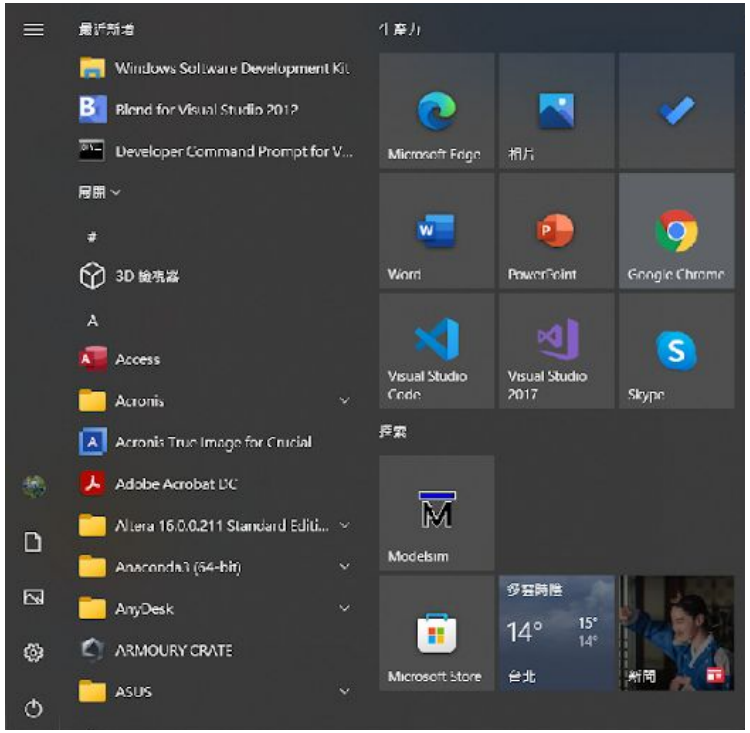
National Cheng Kung University

DIC LAB

製作 : 蔣有為

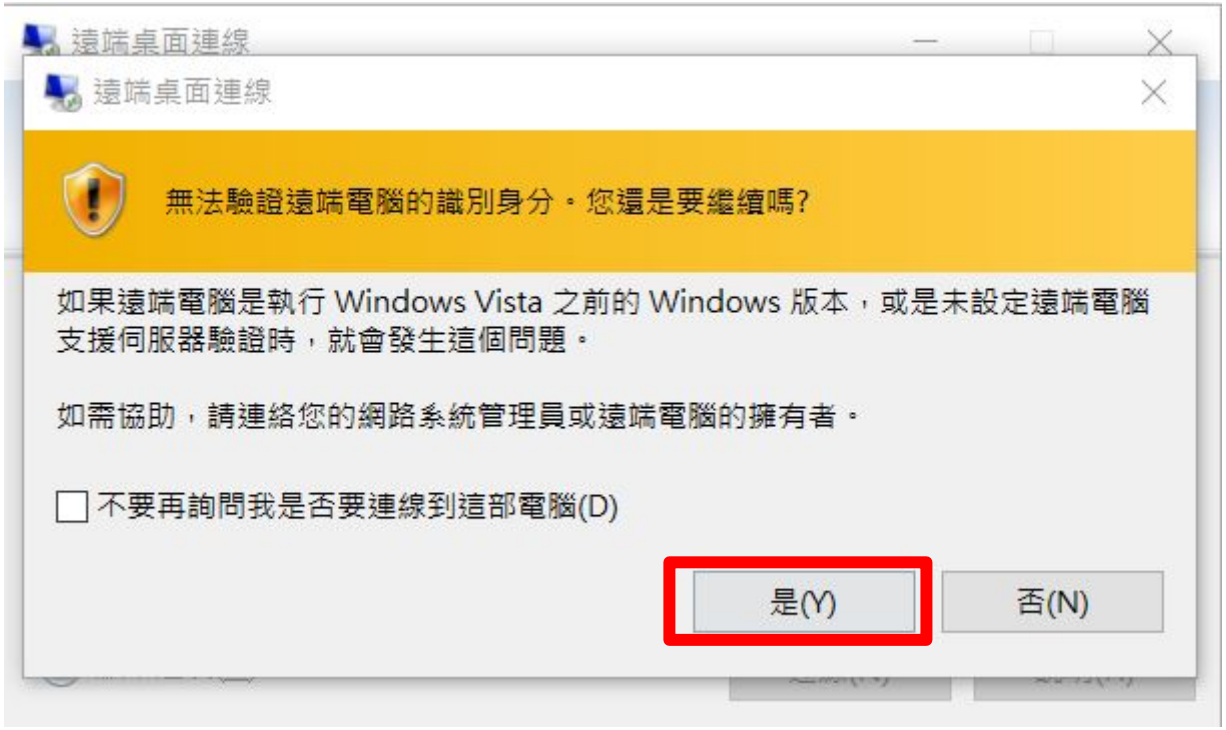
NCKU College of Engineering

STEP 1 .

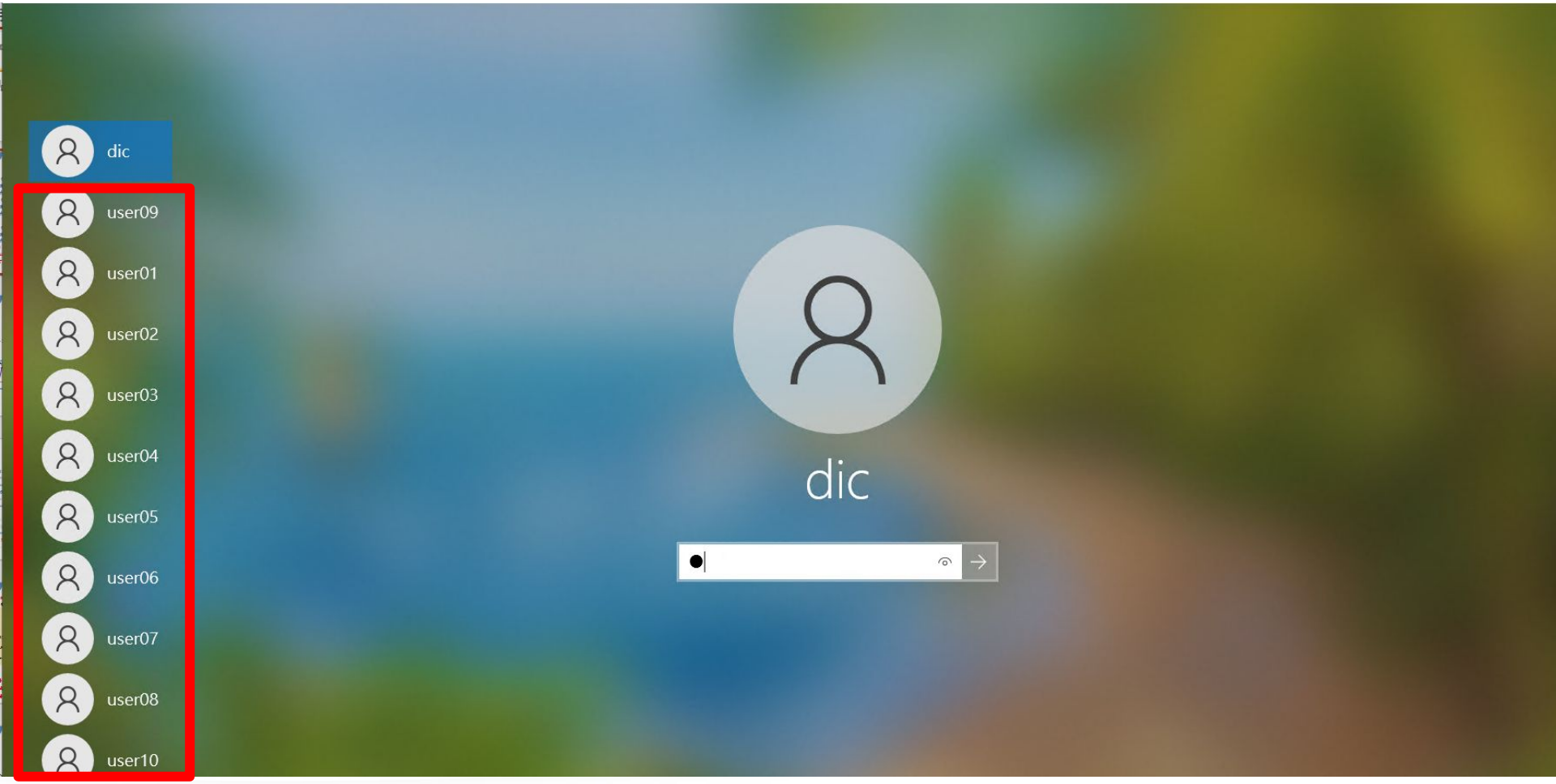


輸入 IP :
140.116.245.82

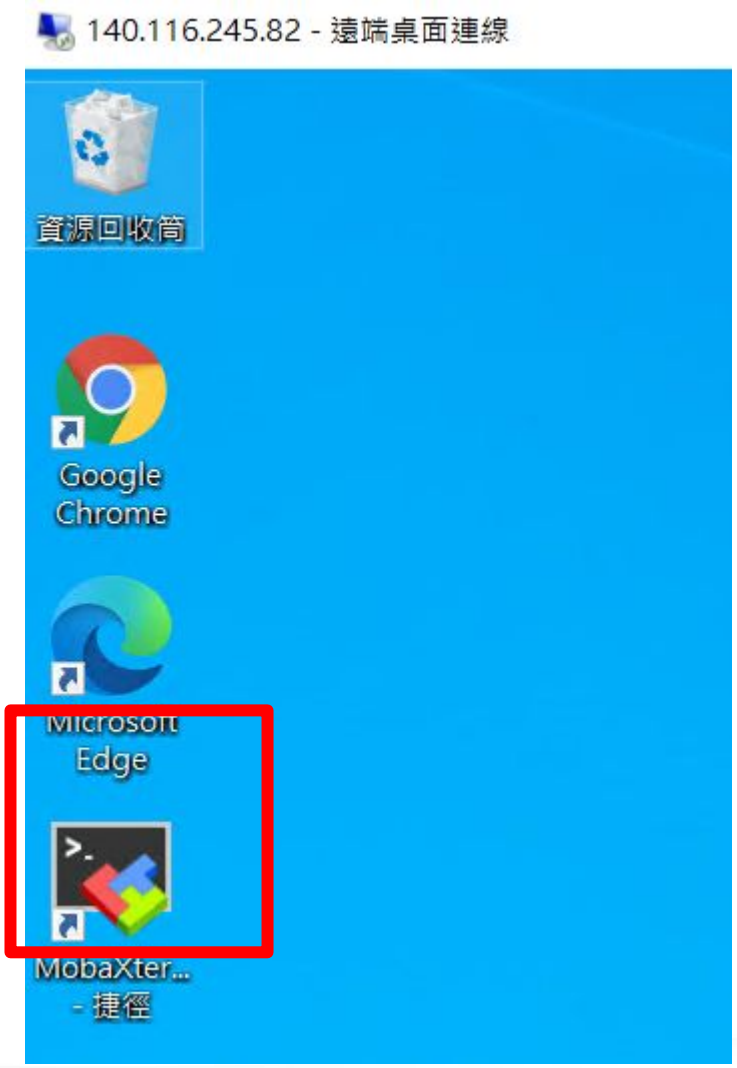
STEP 2 .


遠端桌面連線
遠端桌面連線
無法驗證遠端電腦的識別身分。您還是要繼續嗎?
如果遠端電腦是執行 Windows Vista 之前的 Windows 版本，或是未設定遠端電腦支援伺服器驗證時，就會發生這個問題。
如需協助，請連絡您的網路系統管理員或遠端電腦的擁有者。
不要再詢問我是否要連線到這部電腦(D)
是(Y)
否(N)

STEP 3 . dic 禁止連線, 其餘皆可, 盡量不要跟其他人重複使用

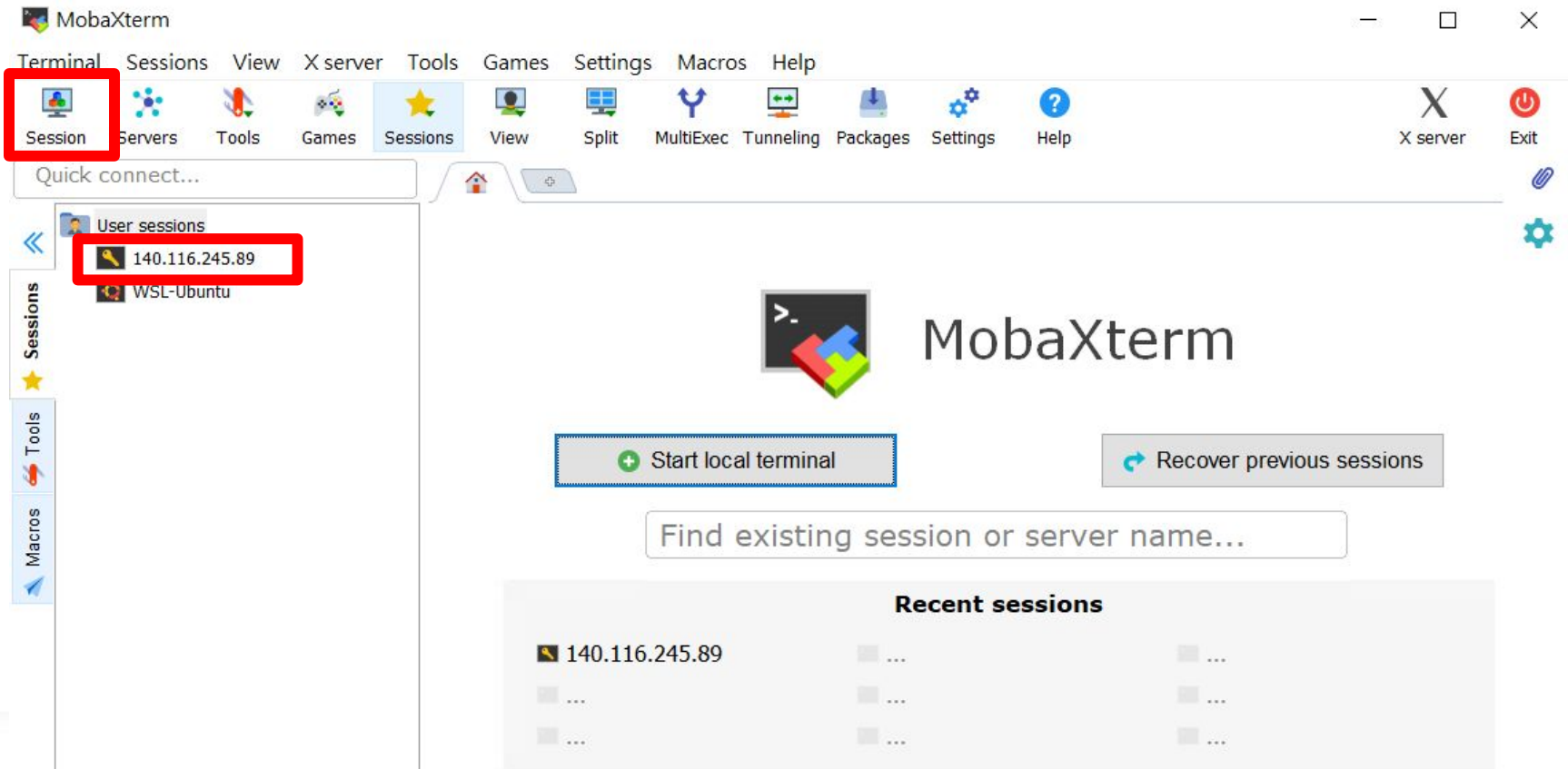


STEP 4 . 打開MobaXterm



STEP 5 . 連線至工作站

Server IP: 140.116.245.89
帳號:ic_contest
密碼:dicicd



IC競賽-Design Compilier 教學

數位晶片設計實驗室(DIC LAB)

ncverilog guide

- **Functional Simulation:**
  - ncverilog tb.v top.v +define+tb1 +notimingcheck
- **Gate-level Simulation:**
  - ncverilog tb.v top_syn.v –v tsmc13_neg.v +define+tb1 +define+SDF

What is design compiler?

- **Design Compiler為Synopsys所開發的電路合成工具**
  - 將register transfer level HDL code轉成gate-level HDL code

- **Design Setup基本流程**
  - 1. mkdir xxx : 建立自己的資料夾
  - 2. cd xxx : 進入自己的資料夾
  - 3. csh : 進入shell
  - 4. menu，選擇 1) Design Compiler
  - 5. dv (open the design vision)

```
ic_contest@CSH: >menu
        Please select the CAD tools you want:

-----Synopsys
1) Design Compiler
2) IC Compiler
3) PrimeTime
4) Formality
5) TetraMax
6) Star-rcxt
7) Spyglass


-----Cadence
i) Incisive

-----Spring Soft
v) Verdi

-----Mentor
m) ModelSim

q) exit

Please select the TOOL you want:1
Platform = amd64
```

合成基本流程(for IC contest)

- **Synthesis基本流程**
  1) dv (open the design vision)
  2) source .synopsys_dc.setup
  3) read_file top_module.v
  4) source top_module_DC.sdc
  5) compile
  6) output the necessary files
     - write -format verilog -hierarchy -output top_module_syn.v
     - write -format ddc -hierarchy -output top_module_syn.ddc
     - write_sdf -version 2.1 top_module_syn.sdf
  7) Report
     report_timing
     report_area

設定 synopsys_dc.setup

- **Search path : 填寫合成所需要用library所在路徑**
  - TSMC130nm:
    /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/
- **target_library: 電路合成時所會使用的standard cell library**
  - fast.db
- **link_library: HDL裡面所有reference到的standard cell library 以及IP**
  - fast.db memory.db
- **Symbol library: 用來產生schematic圖型所使用的library**
  - generic.sdb
- **Synthetic library: DesginWare library to be used**
  - dw_foundation.sldb

設定 synopsys_dc.setup

```
set company "CIC"
set designer "Student"
set search_path      "../lib   $search_path"
set target_library   "slow.db"
set link_library     "* $target_library dw_foundation.sldb"
set symbol_library   "tsmc13.sdb generic.sdb"
set synthetic_library "dw_foundation.sldb"

set hdlin_translate_off_skip_text "TRUE"
set edifout_netlist_only "TRUE"
set verilogout_no_tri true

set hdlin_enable_presto_for_vhdl "TRUE"
set sh_enable_line_editing true
set sh_line_editing_mode emacs
history keep 100
alias h history

set bus_inference_style {%s[%d]}
set bus_naming_style {%s[%d]}
set hdlout_internal_busses true
define_name_rules name_rule -allowed {a-z A-Z 0-9 _} -max_length 255 -type cell
define_name_rules name_rule -allowed {a-z A-Z 0-9 _[]} -max_length 255 -type net
define_name_rules name_rule -map {{"\\*cell\\*" "cell"}}
```

DC.sdc

```
# operating conditions and boundary conditions #
set cycle  10

### === Set Clocks Timing Contrants === ###
create_clock -name CLK -period $cycle [get_ports  clk]
set_dont_touch_network      [get_clocks CLK]
set_clock_uncertainty  1    [get_clocks CLK]
set_clock_latency      1    [get_clocks CLK]
set_fix_hold                [get_clocks CLK]
set_ideal_network           [get_ports clk]

### === Set Driving Strength & delay paramete === ###

set_input_delay -clock CLK  -max -rise 4.5 [remove_from_collection [all_inputs] [get_clocks ]]
set_input_delay -clock CLK  -max -fall 4.5 [remove_from_collection [all_inputs] [get_clocks ]]

set_output_delay -clock CLK -max -rise 4.5  [all_outputs]
set_output_delay -clock CLK -max -fall 4.5  [all_outputs]

set_load -pin_load 1  [all_outputs]
set_drive          1  [all_inputs]

set_operating_conditions -min_library fast -min fast -max_library slow -max slow
set_wire_load_model -name tsmc13_wl10 -library slow
```

告訴Tool合成目標的clock width

Output files

- **Verilog File**
  - Command: write –format verilog –hierarchy –output FAS_syn.v
- **DDC File(Synopsys Internal Database format)**
  - Command: write –format ddc –output FAS_syn.ddc
- **SDF(Standard Delay Format)**
  - Command: write_sdf –version 2.1 –context verilog –load_delay net FAS_syn.sdf

Example

- 範例程式碼在FTP內有(/example)
- 在Server裡也有放