2022 Digital IC Design Homework 3

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NAME
                          洪緯宸
Student ID
                         E14086020
                                                              Simulation Result
Functiona
                                                                            Gate-level
                              Pass
                                                     Pass
                                                                                                          Pass (encoder)
                                                                                                                                         Pass (decoder)
                                                 (decoder)
                                                                            simulation
                         (encoder)
simulation
              (your pre-sim result)
                                                                                (your post-sim result) encoder/decoder
                  encoder/decoder
                                                                       cycle 04309, expect((i,i,8)), get((i,i,8)) >> Fass
                                                                       cycle 043ec, expect(7,7,8) , get(7,7,8) >> Pass cycle 043ff, expect(7,7,8) , get(7,7,8) >> Pass
pycle 043II, expect(/,/,0), get(/,1,0) >> rass
pycle 044I2, expect(7,7,8), get(7,7,8) >> Pass
pycle 04425, expect(7,7,8), get(7,7,8) >> Pass
pycle 04438, expect(7,7,8), get(7,7,8) >> Pass
                                                                       cycle 04412, expect(7,7,8) , get(7,7,8) >> Pass
                                                                       cycle 04425, expect(7,7,8) , get(7,7,8) >> Pass
zycle 0444b, expect(7,7,8) , get(7,7,8) >> Pass
zycle 0445e, expect(7,7,8) , get(7,7,8) >> Pass
zycle 0447l expect(7,7,8) , get(7,7,8) >> Pass
zycle 0449c, expect(7,6,6) , get(7,7,8) >> Pass
                                                                       cycle 04438, expect(7,7,8) , get(7,7,8) >> Pass
                                                                       cycle 0444b, expect(7,7,8) , get(7,7,8) >> Pass
                                                                       cycle 0445e, expect(7,7,8) , get(7,7,8) >> Pass
                                                                       cycle 04471, expect(7,7,8) , get(7,7,8) >> Pass
----- Encoding finished, ALL PASS ------
                                                                       cycle 0449c, expect(7,6,$) , get(7,6,$) >> Pass
** Note: $finish : tb_Encoder.sv(250)
_ Time: 526950 ns _Iteration:_1 Instance
                                                                        ----- Encoding finished, ALL PASS -----
    = Decoding string "080808"
ycle 007ff, expect 0, get 0 >> Pass
                                                                       ** Note: $finish : C:/Users/bob90/verilog/IC_de
                                                                           Time: 526950 ns Iteration: 1 Instance: /testi
ycle 00800, expect 8, get 8 >> Pass
                                                                      1
pycle 007fe, expect 8, get 8 >> Pass
== Decoding string "000008"
pycle 007ff, expect 0, get 0 >> Pass
pycle 00000, expect 8, get 8 >> Pass
pycle 00800, expect 9, get 0 >> Pass
pycle 00802, expect 9, get 8 >> Pass
pycle 00803, expect 0, get 0 >> Pass
pycle 00803, expect 0, get 0 >> Pass
pycle 00804, expect 8, get 8 >> Pass
ycle 00801, expect 0, get 0 >> Pass
ycle 00802, expect 8, get 8 >> Pass
ycle 00803, expect 0, get 0 >> Pass
ycle 00804, expect 8, get 8 >> Pass
----- Decoding finished, ALL PASS -----
                                                                        ----- Decoding finished, ALL PASS -----
* Note: $finish
                            : C:/Users/bob90/verilog/IC
   Time: 61590 ns Iteration: 1 Instance: /tes
                                                                       ** Note: $finish : C:/Users/bob90/verilog/IC_design_Homework/HW3/gatelevel Time: 61590 ns | Iteration: 1 | Instance: /testfixture_decoder
              (your pre-sim result)
                                                                                (your post-sim result) encoder/decoder
                  encoder/decoder
                                                                                                               Img1
                            Img1
                                                                       i cycle 0441b, expect(5,1,4) , get(5,1,4) >> Pass
i cycle 0442a, expect(5,1,8) , get(5,1,8) >> Pass
i cycle 04439, expect(3,2,f) , get(3,2,f) >> Pass
i cycle 04447, expect(0,0,6) , get(0,0,6) >> Pass
i cycle 04453, expect(0,0,6) , get(0,0,5) >> Pass
 cycle 04400, expect(3,2,e) , get(3,2,e) >> Pass
 cycle 0440e, expect(0,0,d) , get(0,0,d) >> Pass
 cycle 0441b, \mathsf{expect}(5,1,4) , \mathsf{get}(5,1,4) >> Pass
 cycle 0442a, expect(5,1,8) , get(5,1,8) >> Pass
                                                                       ----- Encoding finished, ALL PASS -----
 cycle 04439, expect(3,2,f) , get(3,2,f) \gg Pass
                                                                           Note: $finish : C:/Users/bob90/verilog/IC_design_Homework/HW3/gatelev
Time: 524760 ns | Iteration: 1 | Instance: /testfixture_encoder
 cycle 04447, expect(0,0,6) , get(0,0,6) >> Pass
 cycle 04453, expect(0,0,$) , get(0,0,$) >> Pass
                                                                       Break in Module testfixture_encoder at C:/Users/bob90/verilog/IC_design_Hom
  ----- Encoding finished, ALL PASS -----
                                                                              == Decoding string "f4f"
                                                                          == Decoding string "f4"
cycle 00801, expect f, get f >> Pass
cycle 00802, expect 4, get 4 >> Pass
cycle 00803, expect f, get f >> Pass
e= Decoding string "6"
cycle 00804, expect 6, get 6 >> Pass
 ** Note: $finish : tb Encoder.sv(250)
    Time: 524760 ns Iteration: 1 Instance: /test
----- Decoding finished, ALL PASS -----
                                                                         | ** Note: Sfinish : C:/Users/bob90/verilog/IC_design_Homework/HW3/gatelevel
| ** Instance: /testfixture_decoder
cycle 00804, expect 6, get 6 >> Pass
  ----- Decoding finished, ALL PASS -----
                                                                         Break in Module testfixture decoder at C:/Users/bob90/verilog/IC design Homew
Break in Module testfixture_decoder at tb_Decoder.sv line
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(your pre-sim result)
                                                                (your post-sim result) encoder/decoder
              encoder/decoder
                                                          cycle 0272d, expect(7,7,7) , get(7,7,7) >> Fass cycle 02740, expect(7,7,7) >, get(7,7,7) >> Fass cycle 02767, expect(7,5,6) , get(7,5,6) >> Fass cycle 02781, expect(1,7,6) , get(1,7,6) >> Fass
                      Img2
                                                          cycle 027a8, expect(7,5,7) , get(7,5,7) >> Pass
t cycle 02767, expect(7,5,6) , get(7,5,6) >> Pass
t cycle 02781, expect(1,7,6) , get(1,7,6) >> Pass
                                                          cycle 027d2, expect(1,3,6) , get(1,3,6) >> Pass
                                                          cycle 027eb, expect(5,5,7) , get(5,5,7) >> Pass cycle 027ff, expect(5,7,6) , get(5,7,6) >> Pass cycle 02812, expect(7,7,7) , get(7,7,7) >> Pass
 cycle 027a8, expect(7,5,7) , get(7,5,7) >> Pass
 cycle 027b9, expect(7,7,7) , get(7,7,7) >> Pass
 cycle 027d2, expect(1,3,6) , get(1,3,6) >> Pass
                                                          cycle 0283d, expect(7,6,$) , get(7,6,$) >> Pass
 cycle 027eb, expect(5,5,7) , get(5,5,7) \gg Pass
 cycle 027ff, expect(5,7,6) , get(5,7,6) >> Pass cycle 02812, expect(7,7,7) , get(7,7,7) >> Pass
                                                          ----- Encoding finished, ALL PASS -----
                                                            Note: $finish : C:/Users/bob90/verilog/IC_design_Homework/HW3/gateleverime: 309060 ns | Iteration: 1 | Instance: /testfixture_encoder
 cycle 0283d, expect(7,6,$) , get(7,6,$) >> Pass
 ----- Encoding finished, ALL PASS -----
                                                          Break in Module testfixture_encoder at C:/Users/bob90/verilog/IC_design_Hom
                      : tb Encoder.sv(250)
                                                         Decoding string "d7d7d7"
    Time: 309060 ns Iteration: 1 Instance: /test
                                                         e 007ff, expect d, get d >> Pass
                                                         e 00800, expect 7, get 7 >> Pass
cycle 00800, expect 7, get 7 >> Pass cycle 00801, expect d, get d >> Pass
                                                         e 00801, expect d, get d >> Pass
                                                        .e 00802, expect 7, get 7 >> Pass
cycle 00802, expect 7, get 7 >> Pass
                                                         e 00803, expect d, get d >> Pass
cycle 00803, expect d, get d >> Pass
cycle 00804, expect 7, get 7 >> Pass
                                                         .e 00804, expect 7, get 7 >> Pass
 ----- Decoding finished, ALL PASS -----
                                                         ---- Decoding finished, ALL PASS -----
** Note: $finish : tb_Decoder.sv(228)
Time: 61590 ns Iteration: 1 Instance: /testfixtu
                                                         ote: $finish
                                                                              : C:/Users/bob90/verilog/IC design Hom
                                                         ime: 61590 ns Iteration: 1 Instance: /testfixture_de
Break in Module testfixture_decoder at tb_Decoder.sv
             Synthesis Result
                                                                     encoder
                                                                                                          Decoder
Total logic elements
                                                         21202
                                                                                                 81
Total memory bit
                                                         0
                                                                                                 0
Embedded multiplier 9-bit element
                                                                                                 0
                                                         0
Simulation time img0
                                                         526950
                                                                                                 61590
Simulation time img1
                                                         524760
                                                                                                 61620
Simulation time img2
                                                         309060
                                                                                                 61590
(your flow summary) encoder
                                                         (your flow summary) decoder
                                 LZ77 Encoder
                                                                                           LZ77 Decoder
Revision Name
                                                         Revision Name
Top-level Entity Name
                                 LZ77_Encoder
                                                        Top-level Entity Name
                                                                                          LZ77_Decoder
Family
                                 Cyclone II
                                                        Family
                                                                                          Cyclone II
                                 EP2C70F896C8
                                                                                          EP2C70F896C8
Device
                                                         Device
Timina Models
                                 Final
                                                         Timing Models
                                                                                          Final
                                21,202 / 68,416 ( 31 % ) Total logic elements
Total logic elements
                                                                                          81 / 68.416 ( < 1 % )
  Total combinational functions 20,945 / 68,416 ( 31 % )
                                                           Total combinational functions 52 / 68,416 ( < 1 % )
                                                           Dedicated logic registers
  Dedicated logic registers 16,519 / 68,416 ( 24 % )
                                                                                          75 / 68,416 ( < 1 % )
                                 16519
Total registers
                                                         Total registers
                                                                                           75
                                 28 / 622 (5%)
                                                                                          27 / 622 (4%)
Total pins
                                                        Total pins
Total virtual pins
                                                        Total virtual pins
Total memory bits
                                0 / 1,152,000 (0 %)
                                                        Total memory bits
                                                                                          0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements
                                0/300(0%)
                                                         Embedded Multiplier 9-bit elements 0 / 300 (0 %)
Total PLLs
                                 0/4(0%)
                                                        Total PLLs
                                                                                           0/4(0%)
```

Description of your design

Encoder 在 read state 先把值全部存到 reg 裡,在進行解析,我在前面多加了 8 個 element 用來給一開始的 search pointer,避免他指到負的,再來美輸出一個就把 string_buffer 往後移 len+1 個直到結束

Decoder 則是在每一個 clock 都把 buffer 往後移一位,buff[0] 則是根據 cnt 是否 等於 code_len 來判斷是 chardata 還是 buff[code_pos],一直下去就會直到正確答案。

 $Scoring = (Total\ logic\ elements + total\ memory\ bit + 9*embedded\ multiplier\ 9-bit\ element)$