2022 Digital IC Design Homework 3

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Simulation Result

Functional simulation	Pass (encoder)	Pass (decoder)	Gate-level simulation	Pass (encoder)	Pass (decoder)

(your pre-sim result) encoder/decoder img0

```
cycle 04412, expect(7,7,8) , get(7,7,8) >> Pass
cycle 04425, expect(7,7,8) , get(7,7,8) >> Pass
cycle 04438, expect(7,7,8) , get(7,7,8) >> Pass
cycle 0444b, expect(7,7,8) , get(7,7,8) >> Pass
cycle 0445e, expect(7,7,8) , get(7,7,8) >> Pass
cycle 04471, expect(7,7,8) , get(7,7,8) >> Pass
cycle 0449c, expect(7,6,$) , get(7,6,$) >> Pass
---------------------------------------------
--------- Encoding finished, ALL PASS ---------
---------------------------------------------
** Note: $finish    : tb_Encoder.sv(250)
  == Decoding string "080808"
cycle 007ff, expect 0, get 0 >> Pass
cycle 00800, expect 8, get 8 >> Pass
cycle 00801, expect 0, get 0 >> Pass
cycle 00802, expect 8, get 8 >> Pass
cycle 00803, expect 0, get 0 >> Pass
cycle 00804, expect 8, get 8 >> Pass
---------------------------------------------
--------- Decoding finished, ALL PASS ---------
---------------------------------------------
** Note: $finish    : C:/Users/bob90/verilog/IC
   Time: 61590 ns  Iteration: 1  Instance: /tes
```

(your post-sim result) encoder/decoder img0

```
cycle 043ec, expect(7,7,8) , get(7,7,8) >> Pass
cycle 043ff, expect(7,7,8) , get(7,7,8) >> Pass
cycle 04412, expect(7,7,8) , get(7,7,8) >> Pass
cycle 04425, expect(7,7,8) , get(7,7,8) >> Pass
cycle 04438, expect(7,7,8) , get(7,7,8) >> Pass
cycle 0444b, expect(7,7,8) , get(7,7,8) >> Pass
cycle 0445e, expect(7,7,8) , get(7,7,8) >> Pass
cycle 04471, expect(7,7,8) , get(7,7,8) >> Pass
cycle 0449c, expect(7,6,$) , get(7,6,$) >> Pass
---------------------------------------------
--------- Encoding finished, ALL PASS ---------
---------------------------------------------
** Note: $finish    : C:/Users/bob90/verilog/IC_de
   Time: 526950 ns  Iteration: 1  Instance: /testi
cycle 007fe, expect 8, get 8 >> Pass
  == Decoding string "080808"
cycle 007ff, expect 0, get 0 >> Pass
cycle 00800, expect 8, get 8 >> Pass
cycle 00801, expect 0, get 0 >> Pass
cycle 00802, expect 8, get 8 >> Pass
cycle 00803, expect 0, get 0 >> Pass
cycle 00804, expect 8, get 8 >> Pass
---------------------------------------------
--------- Decoding finished, ALL PASS ---------
---------------------------------------------
** Note: $finish    : C:/Users/bob90/verilog/IC_design_Homework/HW3/gatelevel
   Time: 61590 ns  Iteration: 1  Instance: /testfixture_decoder
```

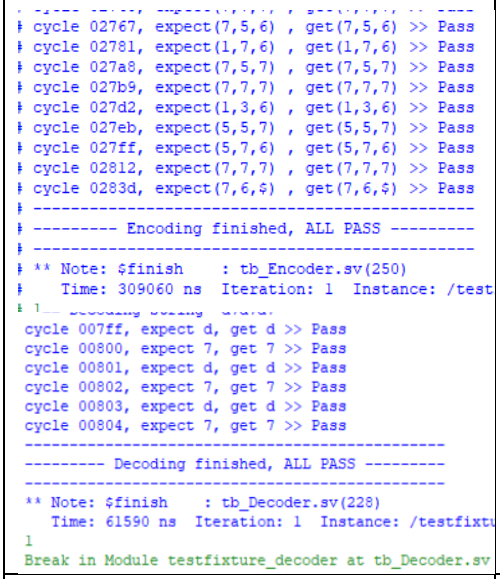
(your pre-sim result) encoder/decoder Img1

```
cycle 04400, expect(3,2,e) , get(3,2,e) >> Pass
cycle 0440e, expect(0,0,d) , get(0,0,d) >> Pass
cycle 0441b, expect(5,1,4) , get(5,1,4) >> Pass
cycle 0442a, expect(5,1,8) , get(5,1,8) >> Pass
cycle 04439, expect(3,2,f) , get(3,2,f) >> Pass
cycle 04447, expect(0,0,6) , get(0,0,6) >> Pass
cycle 04453, expect(0,0,$) , get(0,0,$) >> Pass
---------------------------------------------
--------- Encoding finished, ALL PASS ---------
---------------------------------------------
** Note: $finish    : tb_Encoder.sv(250)
   Time: 524760 ns  Iteration: 1  Instance: /test
1
cycle 00801, expect f, get f >> Pass
cycle 00802, expect 4, get 4 >> Pass
cycle 00803, expect f, get f >> Pass
  == Decoding string "6"
cycle 00804, expect 6, get 6 >> Pass
---------------------------------------------
--------- Decoding finished, ALL PASS ---------
---------------------------------------------
** Note: $finish    : tb_Decoder.sv(228)
   Time: 61620 ns  Iteration: 1  Instance: /testfixture_de
1
Break in Module testfixture_decoder at tb_Decoder.sv line
```

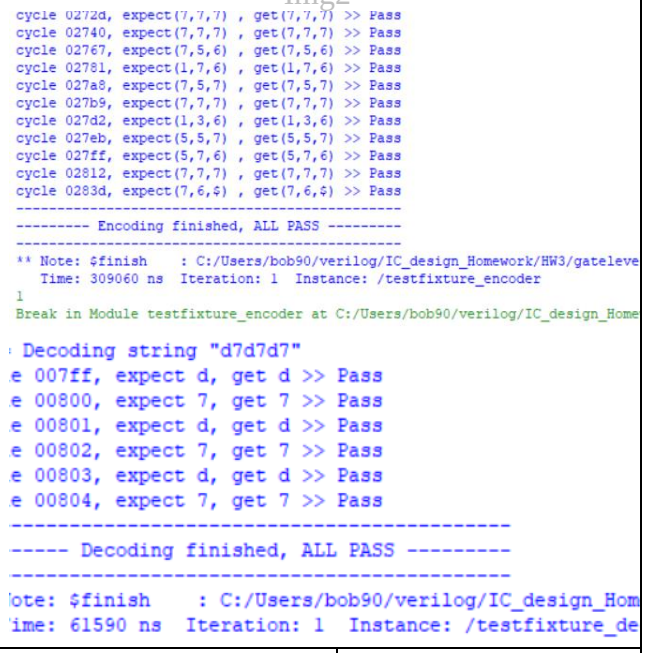
(your post-sim result) encoder/decoder Img1

```
cycle 0441b, expect(5,1,4) , get(5,1,4) >> Pass
cycle 0442a, expect(5,1,8) , get(5,1,8) >> Pass
cycle 04439, expect(3,2,f) , get(3,2,f) >> Pass
cycle 04447, expect(0,0,6) , get(0,0,6) >> Pass
cycle 04453, expect(0,0,$) , get(0,0,$) >> Pass
---------------------------------------------
--------- Encoding finished, ALL PASS ---------
---------------------------------------------
** Note: $finish    : C:/Users/bob90/verilog/IC_design_Homework/HW3/gateleve
   Time: 524760 ns  Iteration: 1  Instance: /testfixture_encoder
1
Break in Module testfixture_encoder at C:/Users/bob90/verilog/IC_design_Home
  == Decoding string "f4f"
cycle 00801, expect f, get f >> Pass
cycle 00802, expect 4, get 4 >> Pass
cycle 00803, expect f, get f >> Pass
  == Decoding string "6"
cycle 00804, expect 6, get 6 >> Pass
---------------------------------------------
--------- Decoding finished, ALL PASS ---------
---------------------------------------------
** Note: $finish    : C:/Users/bob90/verilog/IC_design_Homework/HW3/gatelevel
   Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder
1
Break in Module testfixture_decoder at C:/Users/bob90/verilog/IC_design_Homew
```

(your pre-sim result)
encoder/decoder
Img2



(your post-sim result) encoder/decoder
Img2



Synthesis Result	encoder	Decoder
Total logic elements	21202	81
Total memory bit	0	0
Embedded multiplier 9-bit element	0	0
Simulation time img0	526950	61590
Simulation time img1	524760	61620
Simulation time img2	309060	61590

(your flow summary) encoder

Revision Name	LZ77_Encoder
Top-level Entity Name	LZ77_Encoder
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	21,202 / 68,416 (31 %)
Total combinational functions	20,945 / 68,416 (31 %)
Dedicated logic registers	16,519 / 68,416 (24 %)
Total registers	16519
Total pins	28 / 622 (5 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

(your flow summary) decoder

Revision Name	LZ77_Decoder
Top-level Entity Name	LZ77_Decoder
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	81 / 68,416 (< 1 %)
Total combinational functions	52 / 68,416 (< 1 %)
Dedicated logic registers	75 / 68,416 (< 1 %)
Total registers	75
Total pins	27 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

Encoder 在 read state 先把值全部存到 reg 裡，在進行解析，我在前面多加了 8 個 element 用來給一開始的 search pointer，避免他指到負的，再來美輸出一個就把 string_buffer 往後移 len+1 個直到結束

Decoder 則是在每一個 clock 都把 buffer 往後移一位，buff[0] 則是根據 cnt 是否等於 code_len 來判斷是 chardata 還是 buff[code_pos]，一直下去就會直到正確答案。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element)*