2022 Digital IC Design Homework 2

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| NAME | | 洪緯宸 | | | | |
| Student ID | | E14086020 | | | | |
| **Functional Simulation Result** | | | | | | |
| Stage 1 | Pass | | Stage 2 | Pass | Stage 3 | Pass |
| **Stage 1** | | | | | | |
|  | | | | | | |
| **Stage 2** | | | | | | |
|  | | | | | | |
| **Stage 3** | | | | | | |
|  | | | | | | |
| **Description of our design** | | | | | | |
| 首先，我設了兩個reg state 跟 next\_state，控制state register是循序電路，next state 是組合電路，next state 根據state, counter, SET, Jump, Stop, reset來決定next\_state 是什麼state，再來是counter計算也是根據state stop reset jump來決定counter是否歸零還是+1<，在set == 1 && pose clk時， 把GYR值存進來放在reg，最後在使用組合電路根據現在的state給出正確的output。 | | | | | | |