Documentation for project DocumentationExample

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Revision

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Design Units

This project has 6 design units.

- Entity work.clock_generator
- Architecture work.clock_generator(BEH)
- Entity work.dut
- Architecture work.dut(RTL)
- Entity work.testbench
- Architecture work.testbench(STR)

Entity work.clock_generator

This design unit is implemented in file: `clock_generator.vhd`

This file has no special dependencies

Description

Generate a clock signal. Duty cycle is 50%. Frequency = 1/(2*PERIOD)

Architectures

- work.clock_generator(BEH)

Ports and Generics

Generics

Name	Type	Default Value
PERIOD	time	25 ns

Ports

Name	Direction	Type
clock	Out	std_logic

Architecture work.clock_generator(BEH)

This design unit is implemented in file: `clock_generator.vhd`

This architecture implements entity work.clock_generator

This file has no special dependencies

Description

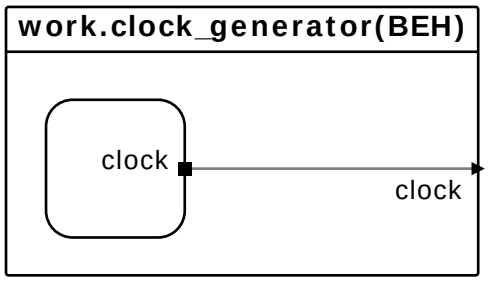
Test implementation of a clock generator

Signals and constants

Instantiations

No instantiations

Block Diagram



Entity work.dut

This design unit is implemented in file: `dut.vhd`

This file has no special dependencies

Description

Design Under Test

Architectures

- work.dut(RTL)

Ports and Generics

Generics

Name	Type	Default Value
test	integer	

Ports

Name	Direction	Type
data_out	Out	std_logic_vector(7 downto 0)
	test comment	
data_in	In	std_logic_vector(7 downto 0)
	test2 comment	
valid	Out	std_logic
start	In	std_logic
	More info about this at http://www.sigasi.com	
clock	In	std_logic
reset	In	std_logic

Architecture work.dut(RTL)

This design unit is implemented in file: `dut.vhd`

This architecture implements entity work.dut

This file has no special dependencies

Description

Register Transfer Level architecture of the Device Under Test

Signals and constants

Signals

Name	Type
count	integer range 0 to MAX_COUNT
	counter

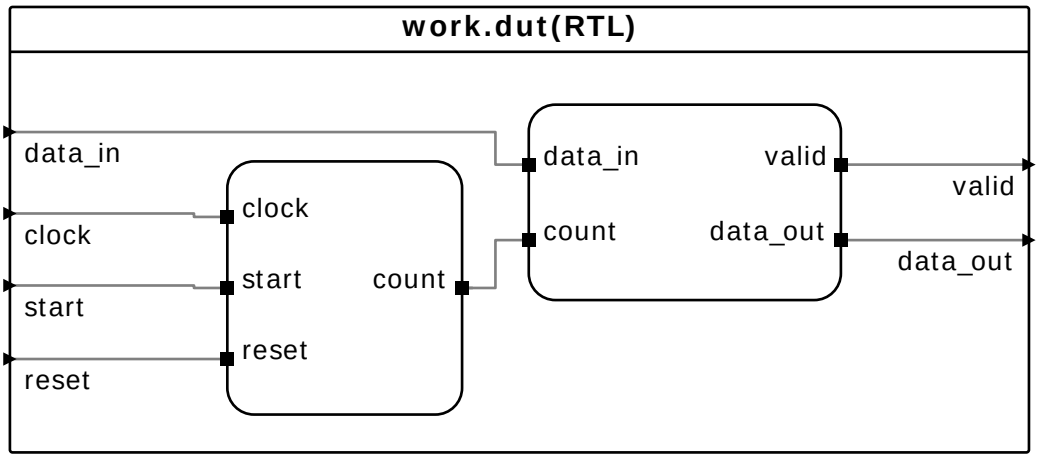
Constants

Name	Type	Value
MIN_COUNT	integer	0
	Unused constant? TODO review	
MAX_COUNT	integer	5
	Maximum value of the counter	

Instantiations

No instantiations

Block Diagram



Entity work.testbench

This design unit is implemented in file: `testbench.vhd`

This file depends on: `clock_generator.vhd`, `dut.vhd`

Description

Test bench for Sigasi Tutorial Project.

Architectures

- work.testbench(STR)

Ports and Generics

Architecture work.testbench(STR)

This design unit is implemented in file: `testbench.vhd`

This architecture implements entity work.testbench

This file depends on: `clock_generator.vhd`, `dut.vhd`

Description

No Description

Signals and constants

Signals

Name	Type
data_out	std_logic_vector(7 downto 0)
	data_out blabla
data_in	std_logic_vector(7 downto 0)
valid	std_logic
start	std_logic
clock	std_logic
reset	std_logic

Constants

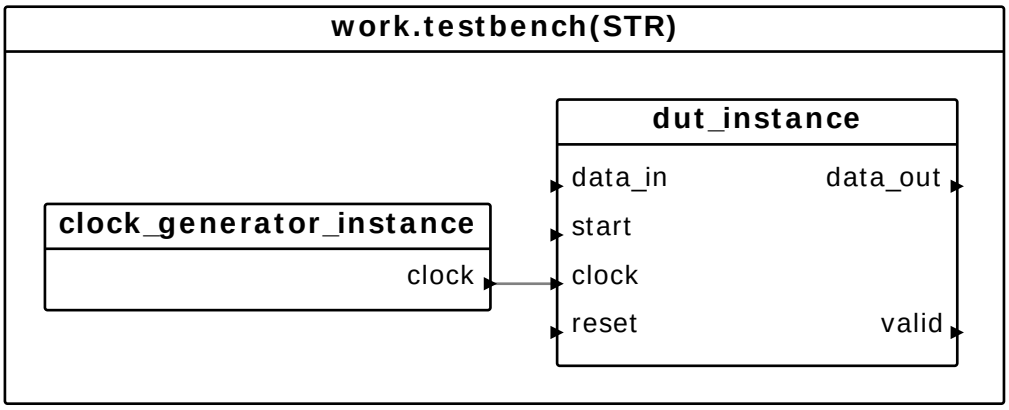
Name	Type	Value
PERIOD	time	50 ns

Name	Type	Value
	Half the clock period. The frequency will be 1/(2*PERIOD) = 100 MHz	

Instantiations

- clock_generator_instance : work.clock_generator
  - # Generic Map
    - # PERIOD : PERIOD
  - # Port Map
    - # clock : clock
- dut_instance : work.dut
  - # Generic Map
    - # test : 0
  - # Port Map
    - # data_out : data_out -- test comment
    - # data_in : data_in -- test2 comment
    - # valid : valid
    - # start : start -- More info about this at http://www.sigasi.com
    - # clock : clock
    - # reset : reset

Block Diagram



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[1] http://www.sigasi.com/app/docgen