```
//Verilog behavioural code for Half Adder

module HalfAdd(A,B,SUM,C_OUT);
input   A,B;
output  SUM, C_OUT;
reg SUM, C_OUT;
always@(A,B)
    if ((A == 1'b0) && (B == 1'b0))
        begin
        SUM <= 0;
        C_OUT <= 0;
        end

    else if ((A == 1'b1) && (B == 1'b1))
        begin
        SUM <= 0;
        C_OUT <= 1;
        end

    else
        begin
        SUM <= 1;
        C_OUT <= 0;
        end
endmodule
```