

```
1  //Verilog behavioural code for Half Adder
2
3  module HalfAdd(A,B,SUM,C_OUT);
4  input  A,B;
5  output SUM, C_OUT;
6  reg SUM, C_OUT;
7  always@(A,B)
8      if ((A == 1'b0) && (B == 1'b0))
9          begin
10             SUM <= 0;
11             C_OUT <= 0;
12             end
13
14         else if ((A == 1'b1) && (B == 1'b1))
15             begin
16                 SUM <= 0;
17                 C_OUT <= 1;
18             end
19
20         else
21             begin
22                 SUM <= 1;
23                 C_OUT <= 0;
24             end
25 endmodule
```