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/*****************************************************
Verilog code and test banch for carry select adder
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module carry_sel_adder_tb();

reg [7:0]   Atest,Btest;
reg     Cintest;
wire    [7:0]   Sumtest;
wire        Couttest;

carry_sel_adder c1 (Sumtest,Couttest,Atest,Btest,Cintest);
initial
    begin
    Atest = 8'h00;
    Btest = 8'h00;
    Cintest = 1'b0;

    #150;
    Atest = 8'h02;
    Btest = 8'h02;

    #150;
    Atest = 8'h30;
    Btest = 8'h30;

    #150;
    Atest = 8'h5f;
    Btest = 8'hf0;

    #150;
    Atest = 8'h0f;
    Btest = 8'h02;

    #150;
    Atest = 8'h50;
    Btest = 8'ha0;

    #150;
    Atest = 8'h08;
    Btest = 8'h0a;
    end
endmodule
module carry_sel_adder(sum,cout,a,b,cin);
input   [7:0]   a,b;
output  [7:0]   sum;
input       cin;
output      cout;
//reg       sum;
//reg       cout;
wire    [3:0]   W1,W2,sum3to0;
wire        carry2,carry3;
wire        carrystage;
wire        muxsel;
assign  muxsel = carrystage;
cla4    (sum3to0,carrystage,a[3:0],b[3:0],cin);
cla4    (W1,carry2,a[7:4],b[7:4],1'b1);
cla4    (W2,carry3,a[7:4],b[7:4],1'b0);

//case(muxsel)
//1'b1: begin
    assign  sum = carrystage ? {W1,sum3to0}:{W2,sum3to0};
    assign  cout = carrystage ? carry2:carry3;
    //end

//1'b0: begin
    //assign    sum = {W2,sum3to0};
//  assign  cout = carry3;
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70  //  end
71  //endcase
72  endmodule
73  module cla4(sum,cout,a,b,cin);
74  input   [3:0]   a,b;
75  input       cin;
76  output  [3:0]   sum;
77  output      cout;
78
79  wire    [3:0]   Pi,Gi;
80  wire    [4:0]   Ci;
81
82  assign Ci[0] = cin;
83  assign Ci[1] = (Gi[0] + (Pi[0] & Ci[0]));
84  assign Ci[2] = (Gi[1] + (Pi[1] & Ci[1]));
85  assign Ci[3] = (Gi[2] + (Pi[2] & Ci[2]));
86  assign Ci[4] = (Gi[3] + (Pi[3] & Ci[3]));
87
88  assign  Pi = a + b;
89  assign  Gi = a & b;
90  assign sum = (a ^ b ^ Ci[3:0]);
91  assign cout = Ci[4];
92  endmodule
```