```verilog
// Verilog code for digital counter/decrementer
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module dig_counter(RESETL,PRESETL,LOAD_ENA,UP,DATA_IN,CLK,COUNT);

input   [3:0]   DATA_IN;
input           RESETL,PRESETL,LOAD_ENA,UP,CLK;
output  [3:0]   COUNT;
reg     [3:0]   COUNT;

always @(RESETL or PRESETL or posedge CLK)
begin
    if (~RESETL)            COUNT <= 4'b0000;

    else if (~PRESETL)      COUNT <= 4'b1111;

    else if (UP) begin
        if (COUNT == 15) begin
                COUNT  <= 0;
                COUNT <= (COUNT + 1);
            end
        else COUNT <= (COUNT + 1);
        end

    else if (~UP) begin
        if (COUNT == 0) begin
                COUNT  <= 15;
                COUNT <= (COUNT - 1);
            end
        else COUNT <= (COUNT - 1);
        end
    else if (LOAD_ENA)  COUNT <= DATA_IN;
end
endmodule
```