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2
3   //Verilog code for Carry Look Ahead Adder
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6
7
8   module cla4(sum,cout,a,b,cin);
9   input   [3:0]   a,b;
10  input           cin;
11  output  [3:0]   sum;
12  output          cout;
13
14  wire    [3:0]   Pi,Gi;
15  wire    [4:0]   Ci;
16
17  assign Ci[0] = cin;
18  assign Ci[1] = (Gi[0] + (Pi[0] & Ci[0]));
19  assign Ci[2] = (Gi[1] + (Pi[1] & Ci[1]));
20  assign Ci[3] = (Gi[2] + (Pi[2] & Ci[2]));
21  assign Ci[4] = (Gi[3] + (Pi[3] & Ci[3]));
22
23  assign  Pi = (a ^ b);
24  assign  Gi = (a & b);
25  assign sum = (a ^ b ^ Ci[3:0]);
26  assign cout = Ci[4];
27  endmodule
28
```