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REVISION HISTORY:

Rev	Date	Notes
X100	2015/05/22	INITIAL RELEASE OF TURBOT DESIGN
X200	2015/07/30	FIXES BASED ON ALPHA QUALIFICATION
X201	2015/08/17	SWAP IN NEW LOW-Vth FET FOR Q16, DNI U33 (SPD EEPROM)
X202	2015/08/27	STUFF R354, REPLACE U32 (USB POWER SWITCH) WITH PART FROM X100 RELEASE
X203	2015/09/23	ADD LABELS TO BOM FOR PILOT PRODUCTION RELEASE
X204	2015/10/13	BOM FIX D5, D6, D10 TO PART WITH CORRECT FOOTPRINT
X205	2015/08/27	NO STUFF R53, R54, R55, R56 TO MATCH VALIDATED PROTOTYPES

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Minnowboard Turbot design derived from Minnowboard MAX as designed by CircuitCo LLC.

All derivative works are to be attributed to ADI Engineering and $\mbox{CircuitCo\ LLC}$.

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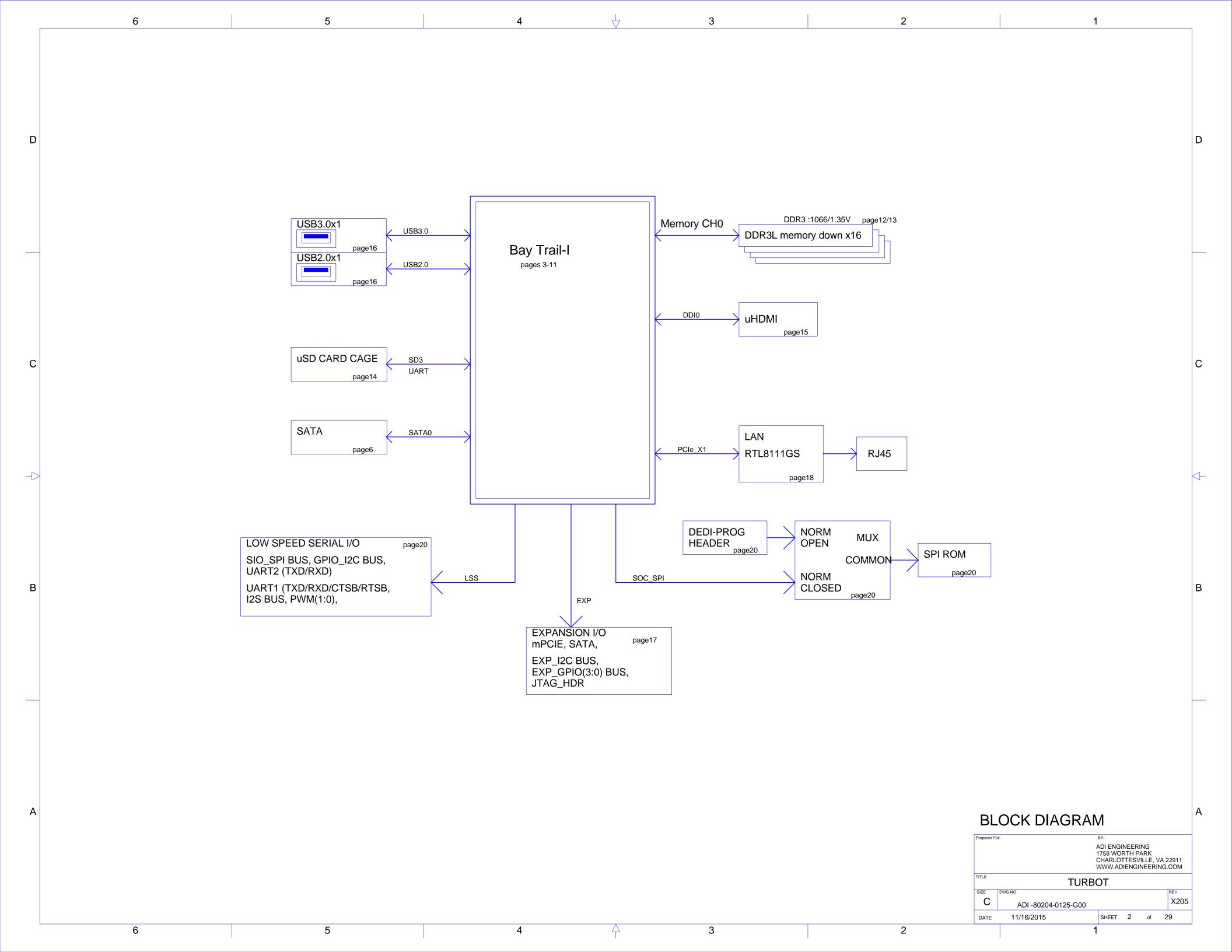
For all design files, including bill of materials and gerber files, please visit www.minnowboard.org

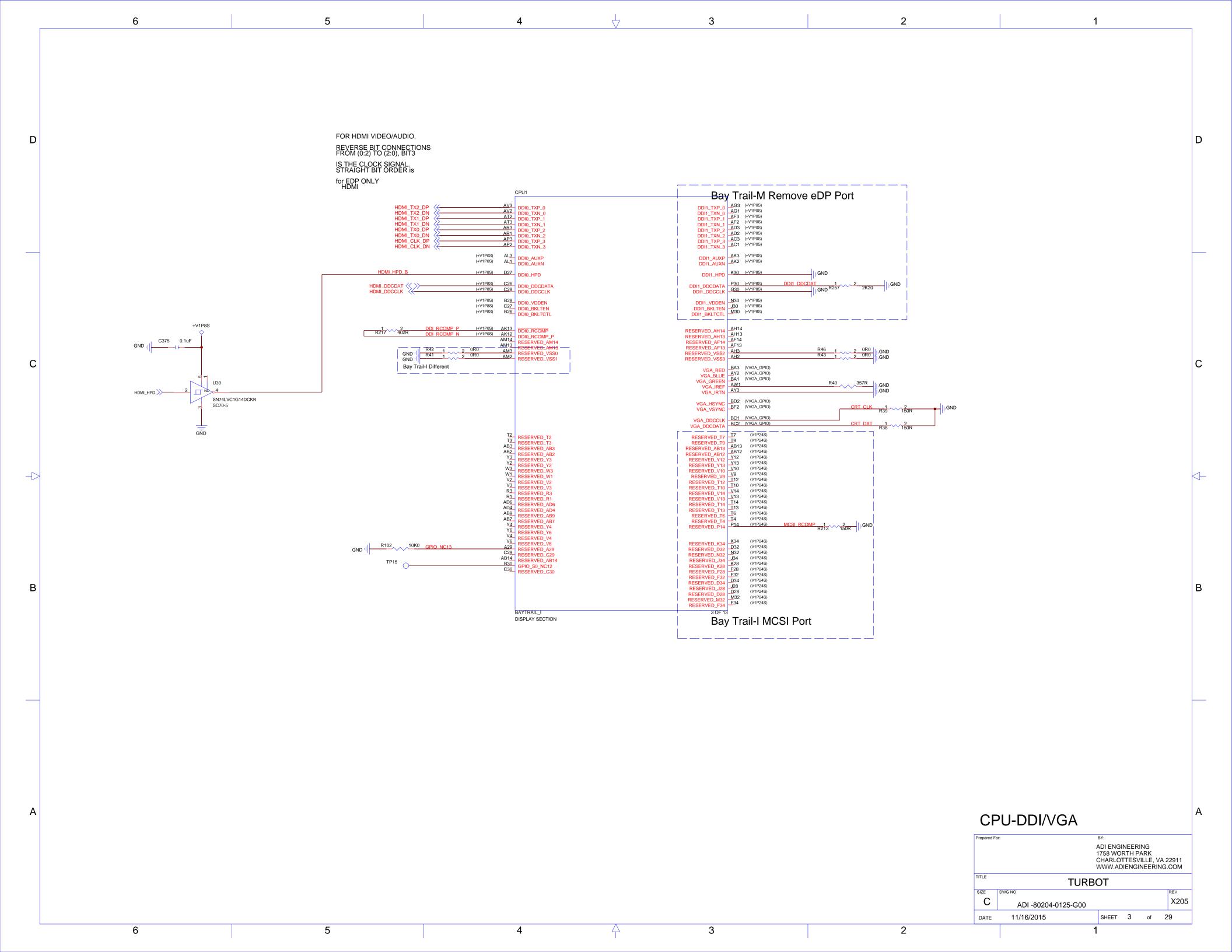
ADI ENGINEERING 1758 WORTH PARK CHARLOTTESVILLE, VA 22911 WWW.ADIENGINEERING.COM TURBOT SIZE С X205 ADI -80204-0125-G00 11/16/2015 SHEET 1 of 29

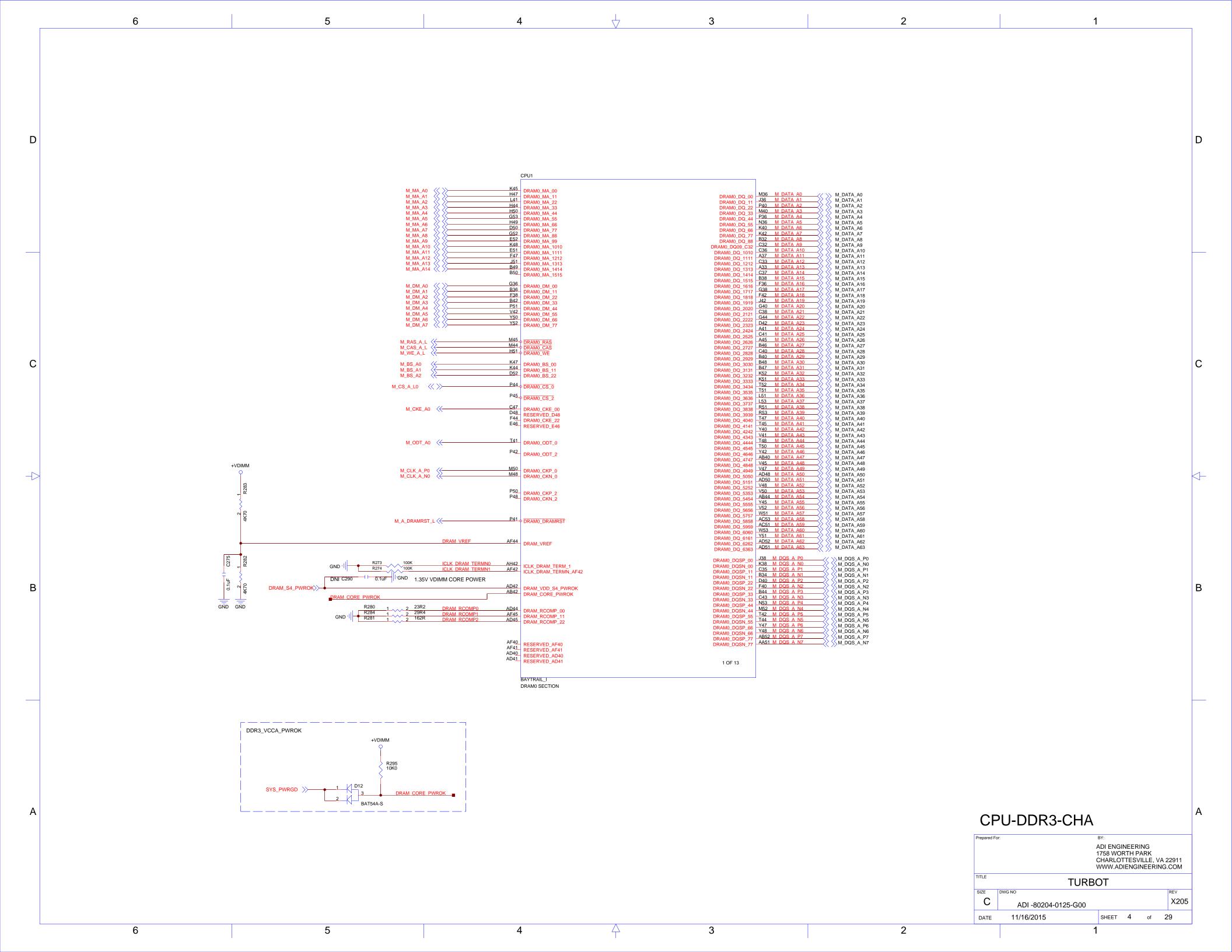
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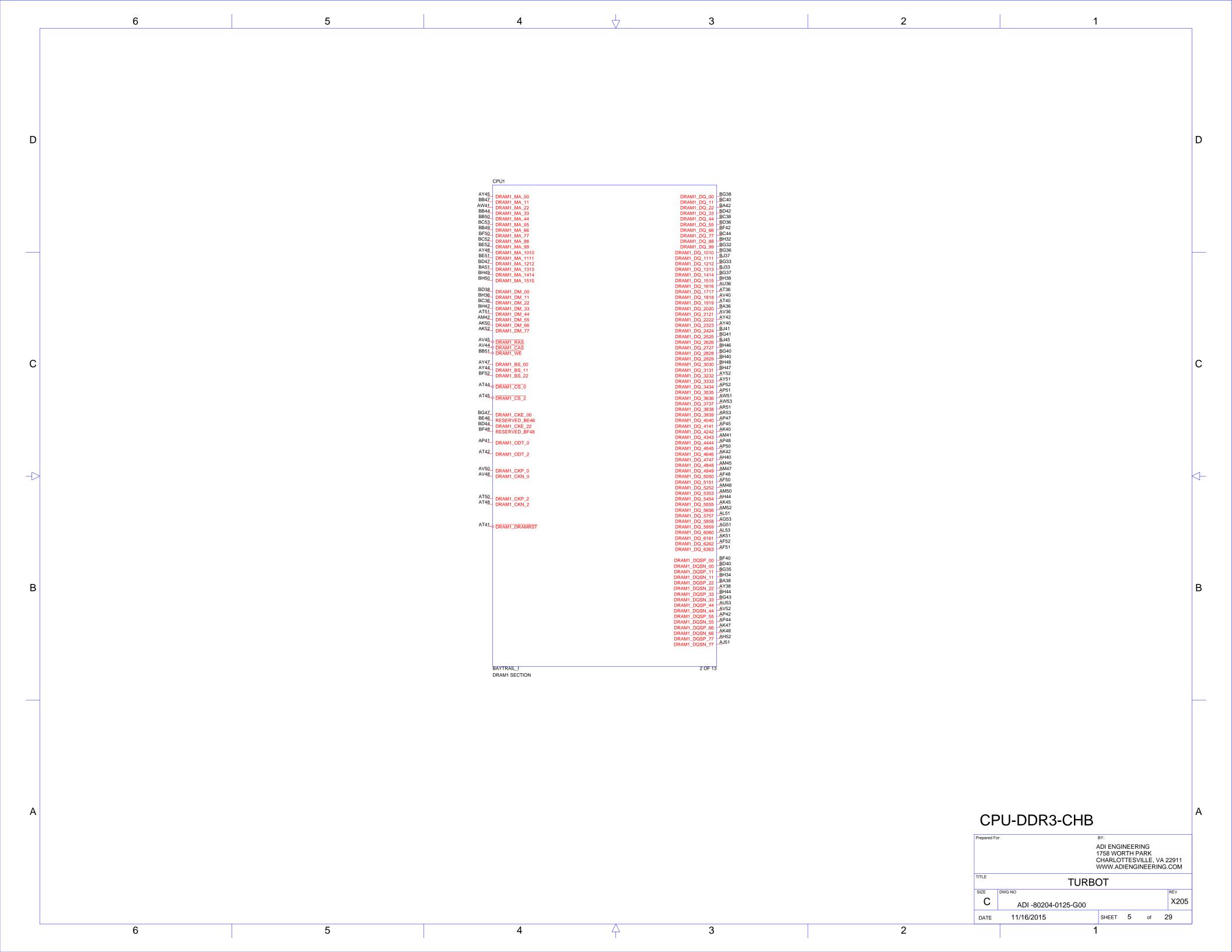
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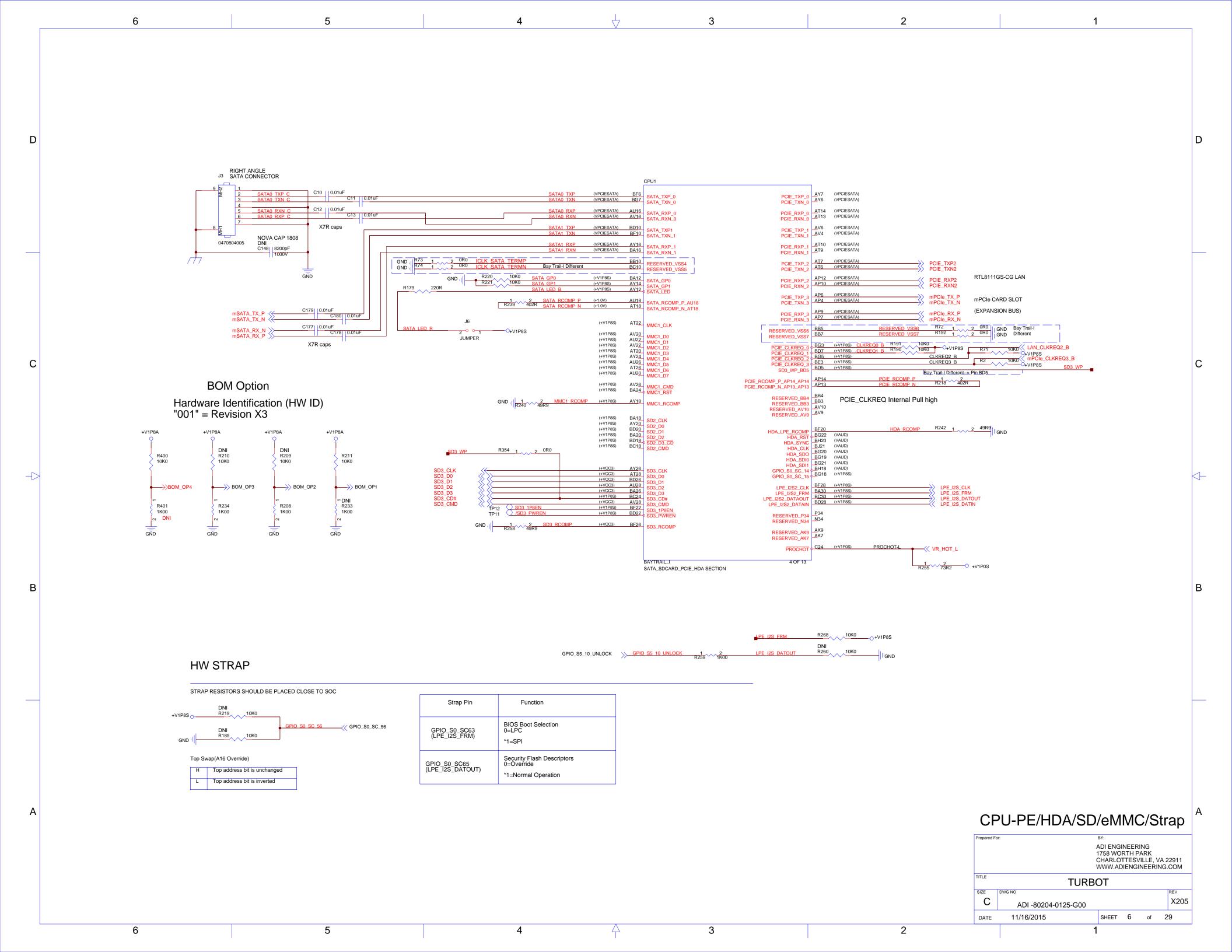
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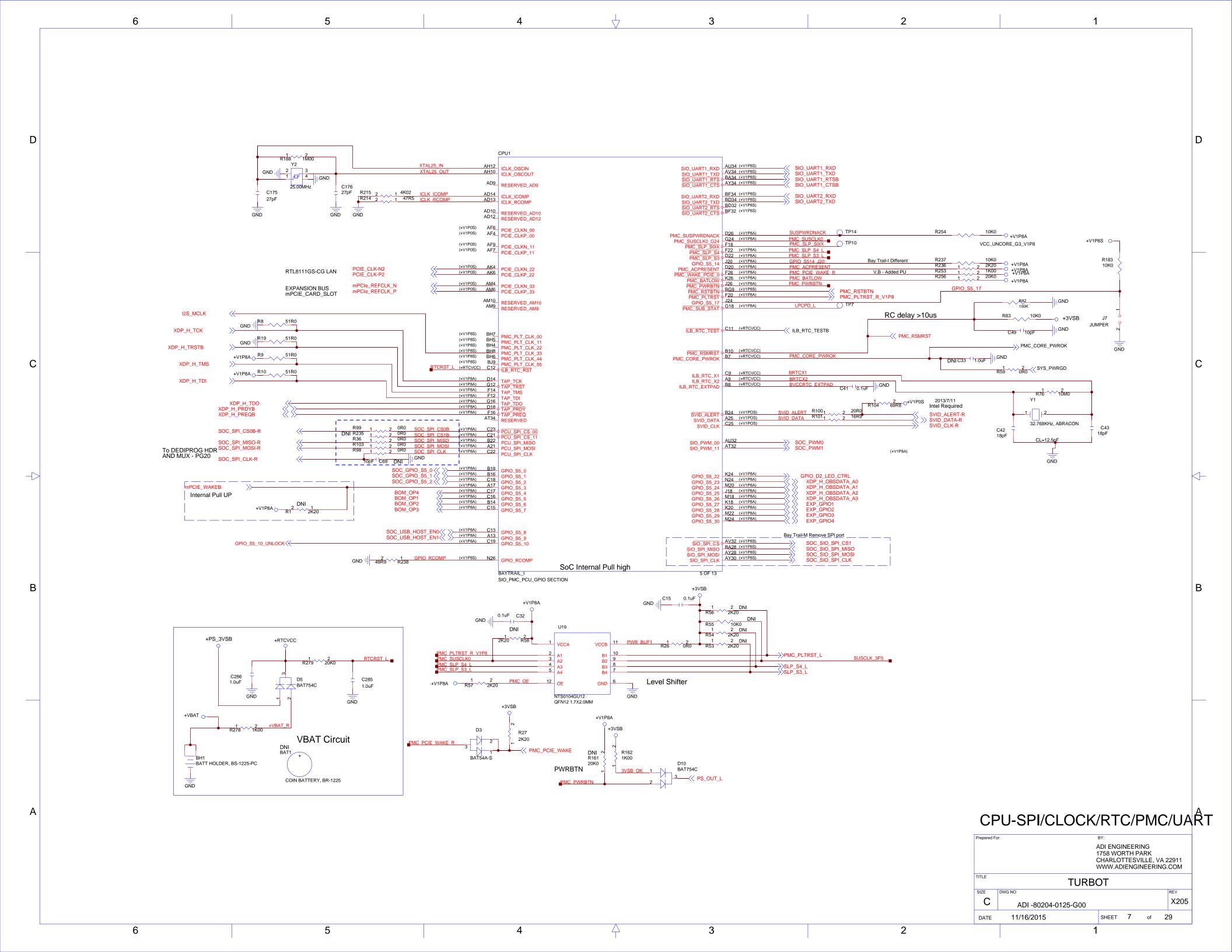


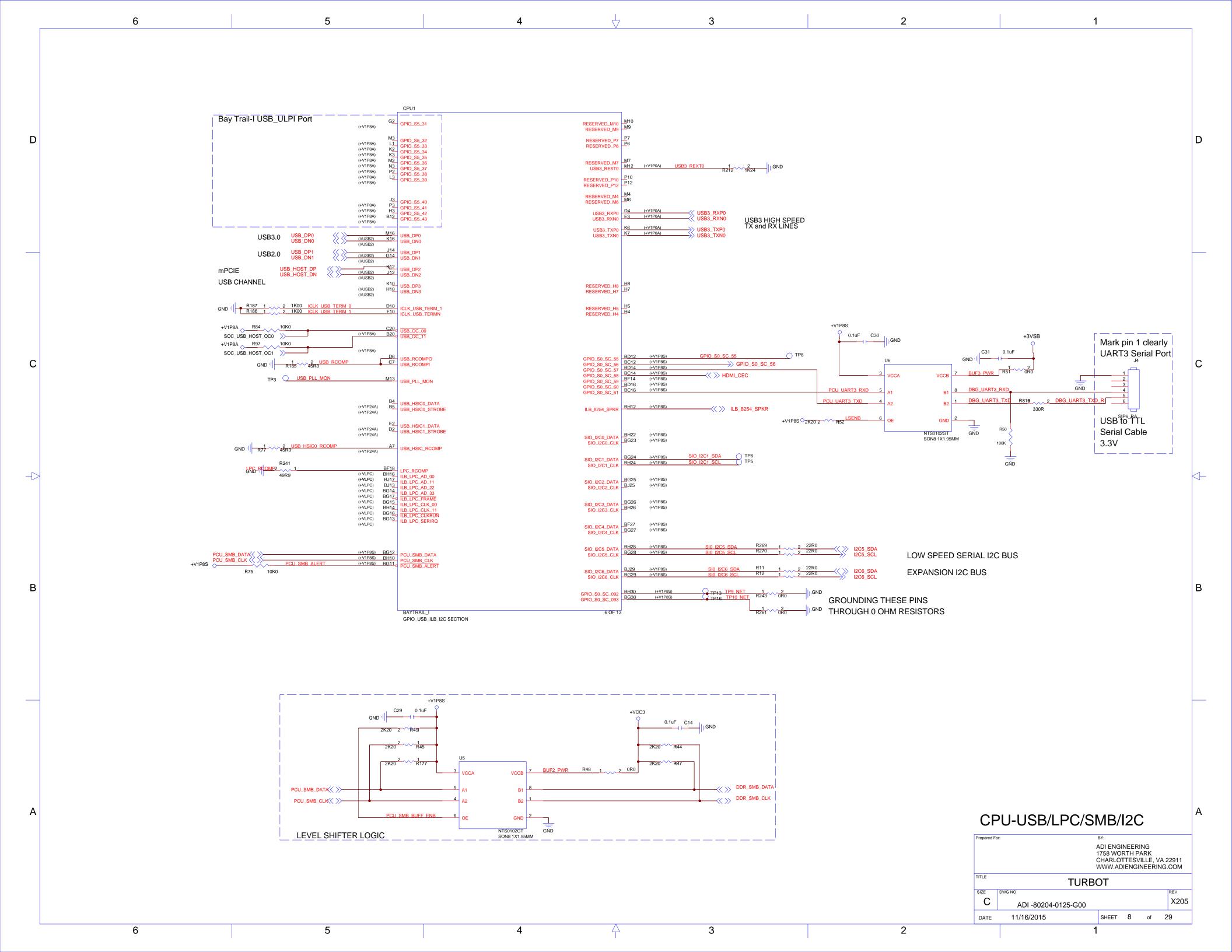


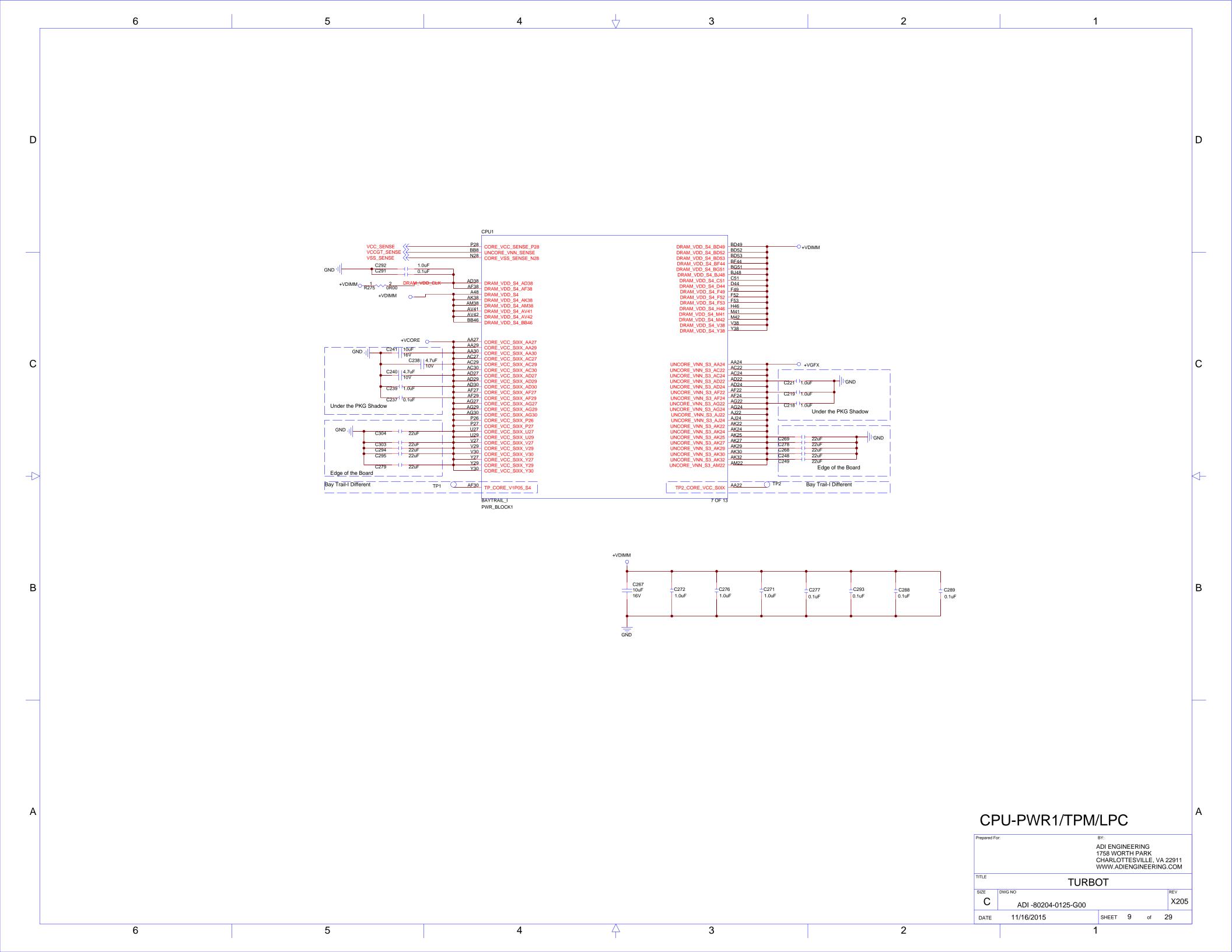


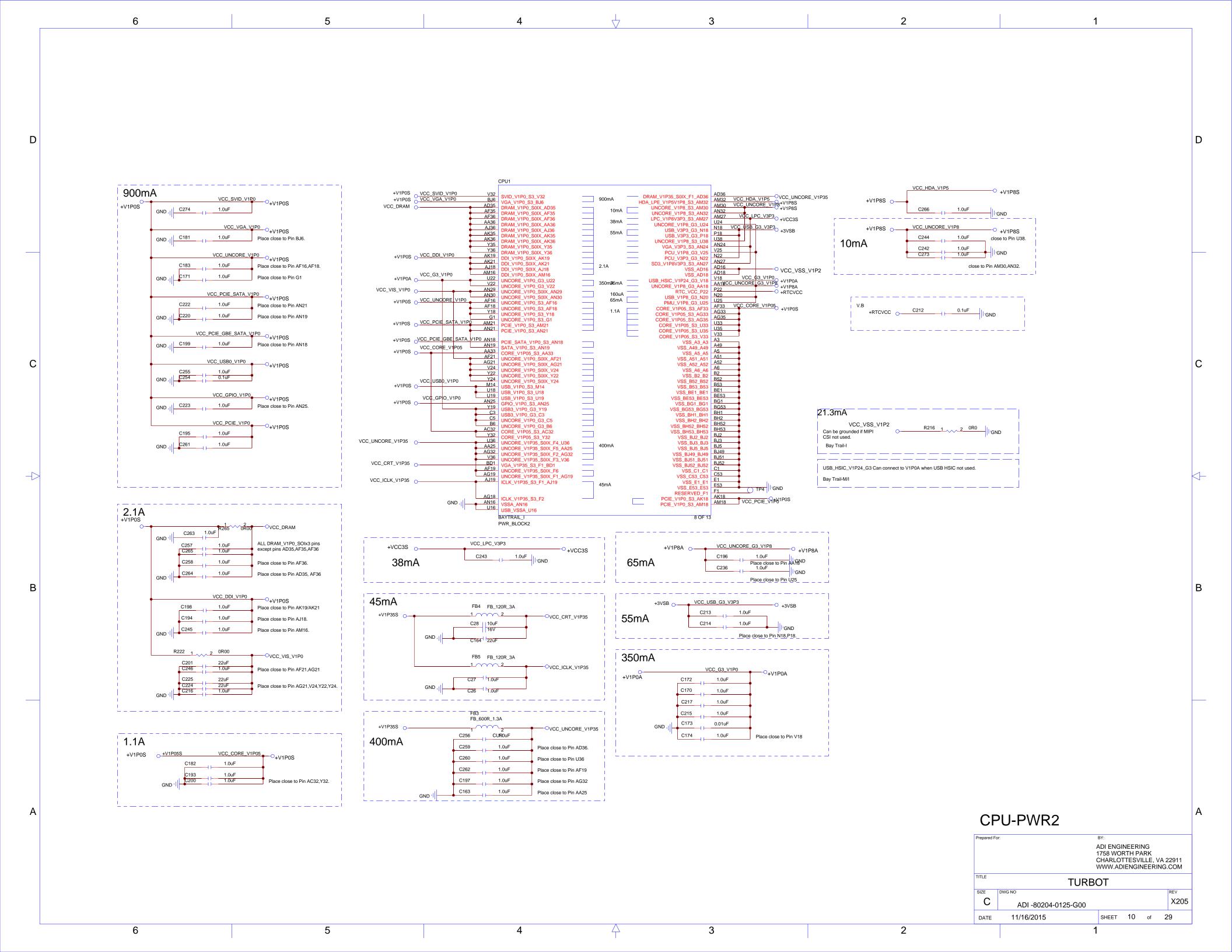


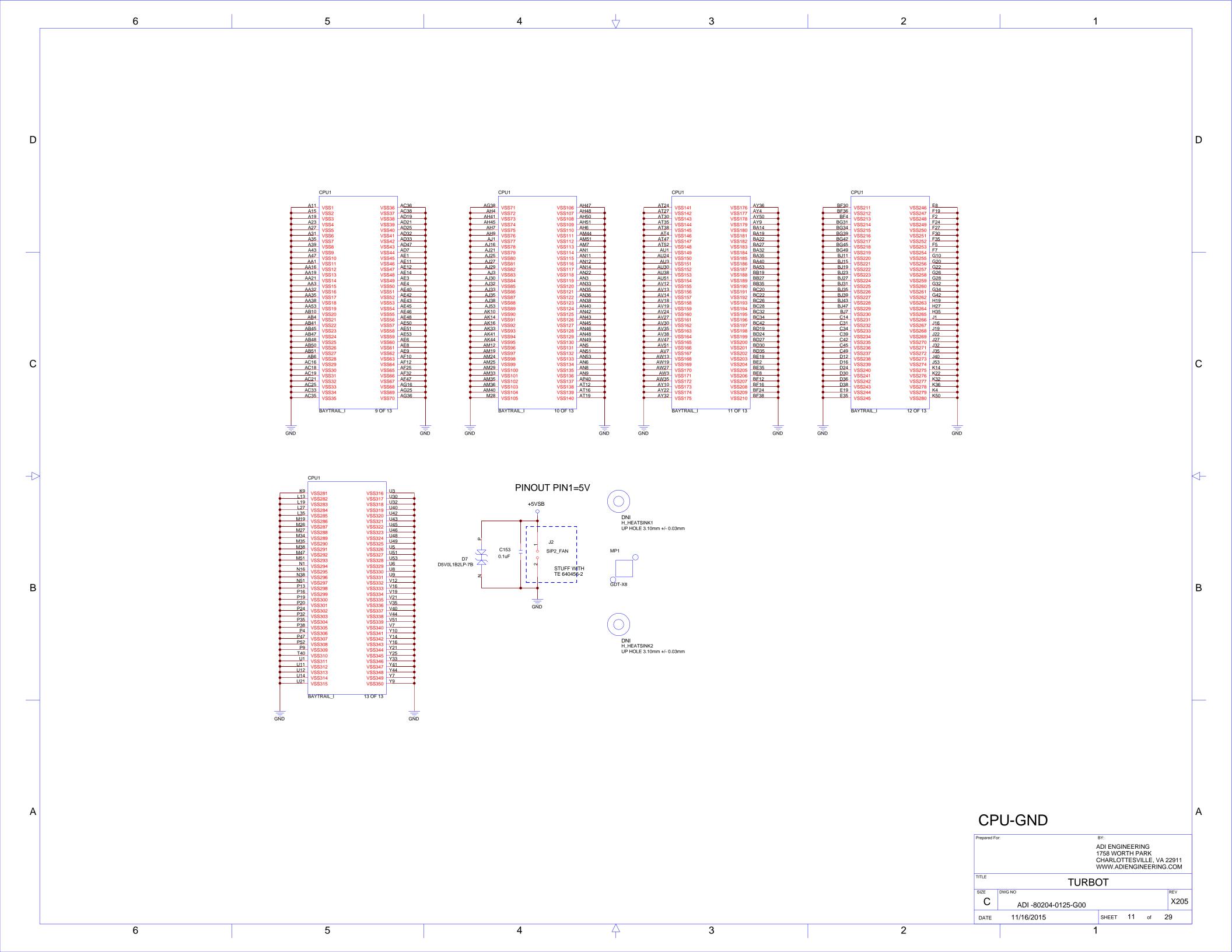


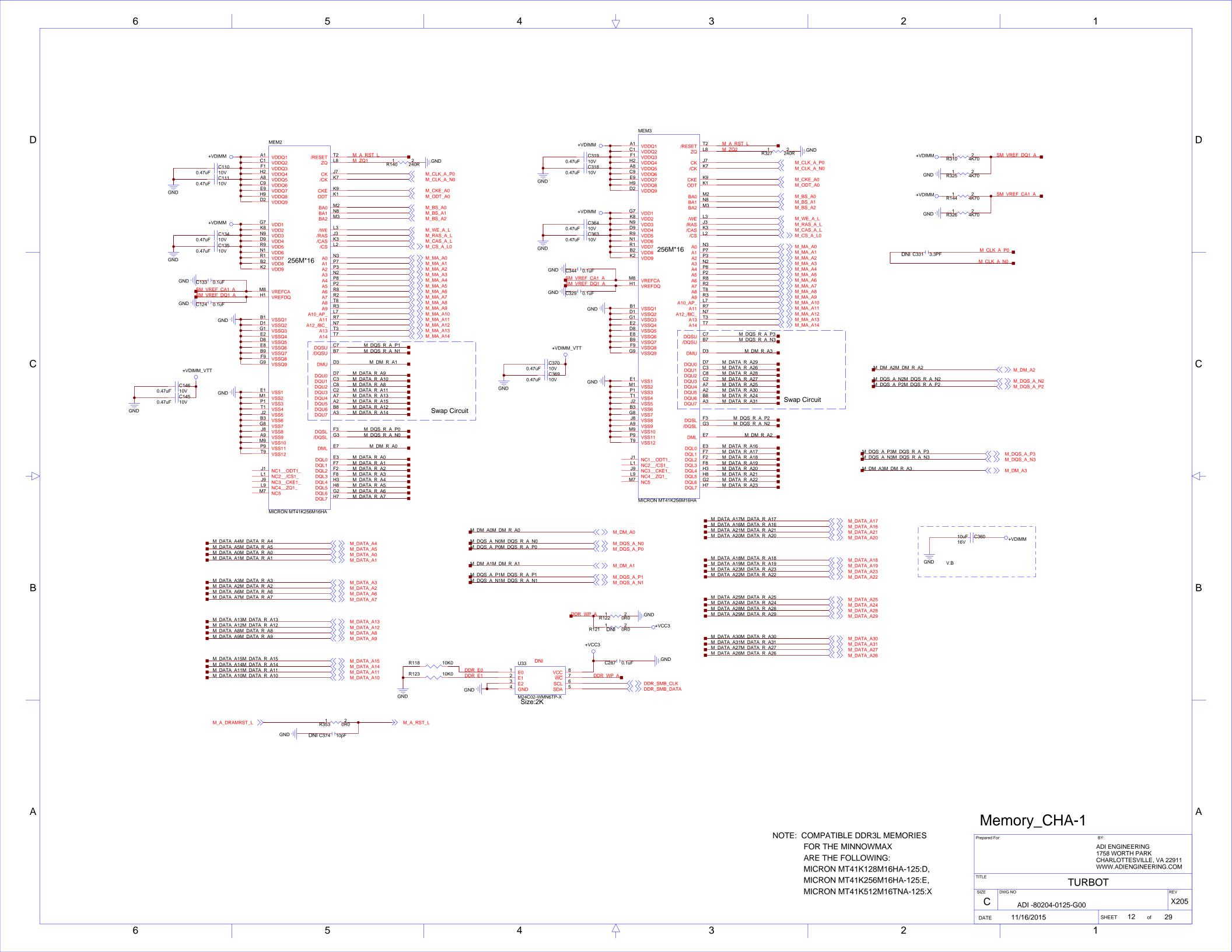


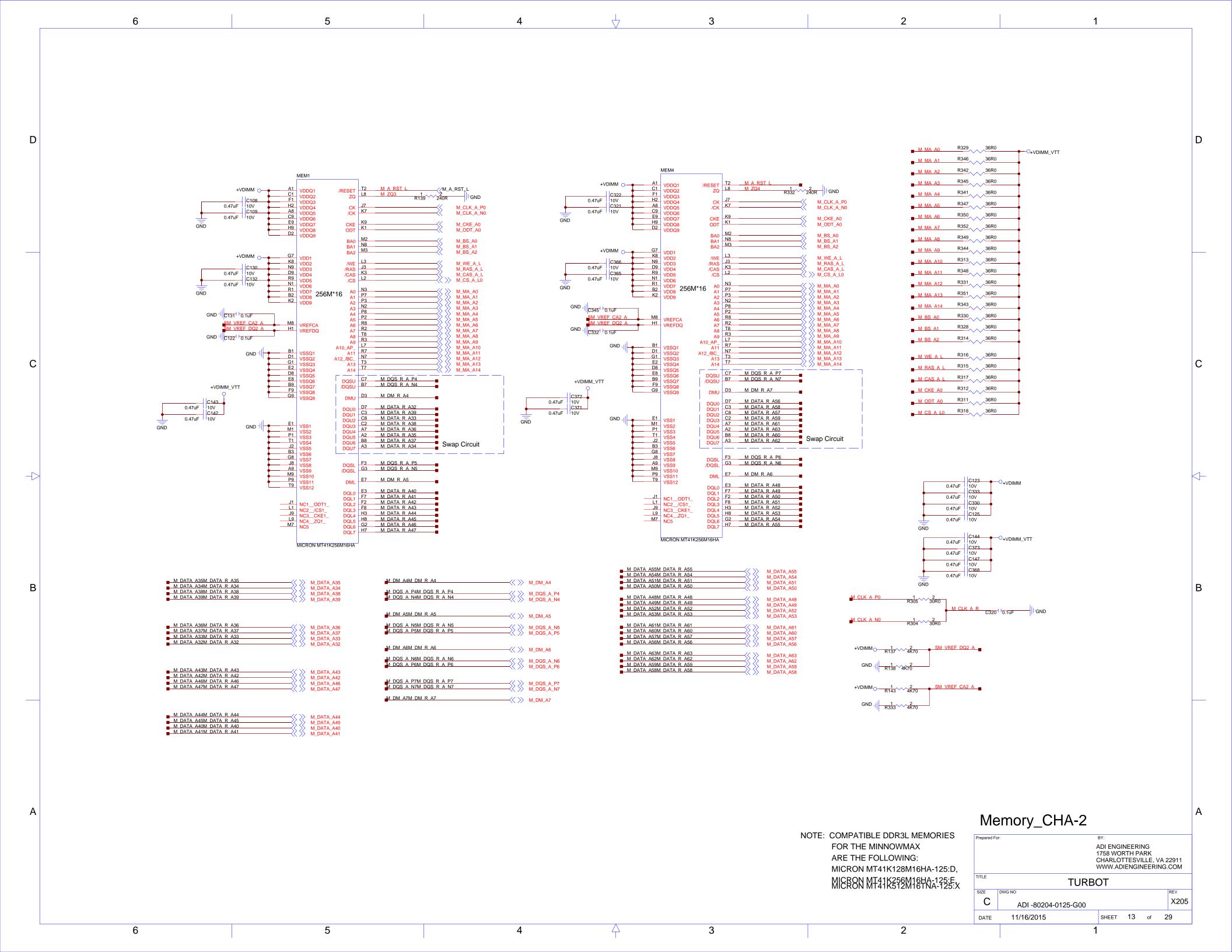


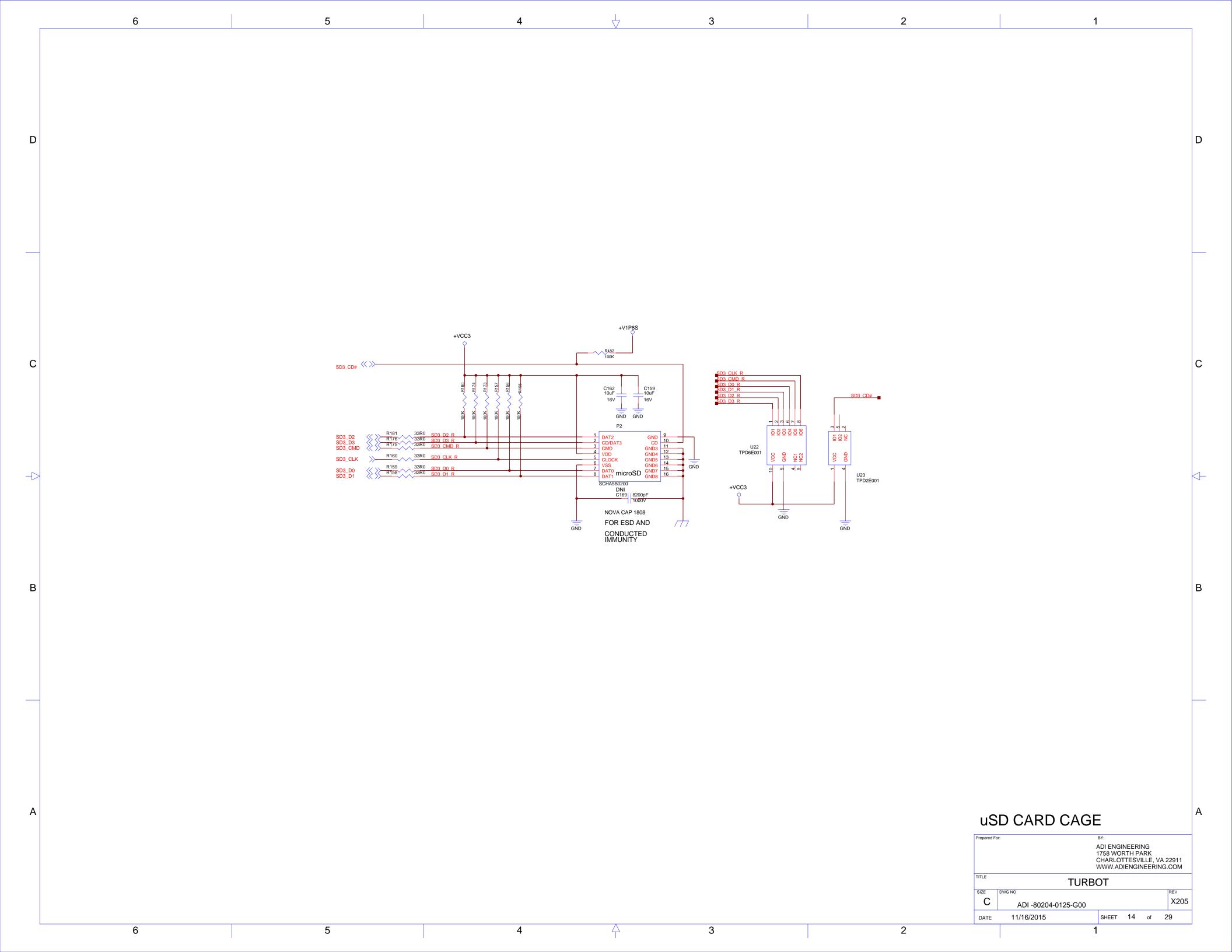


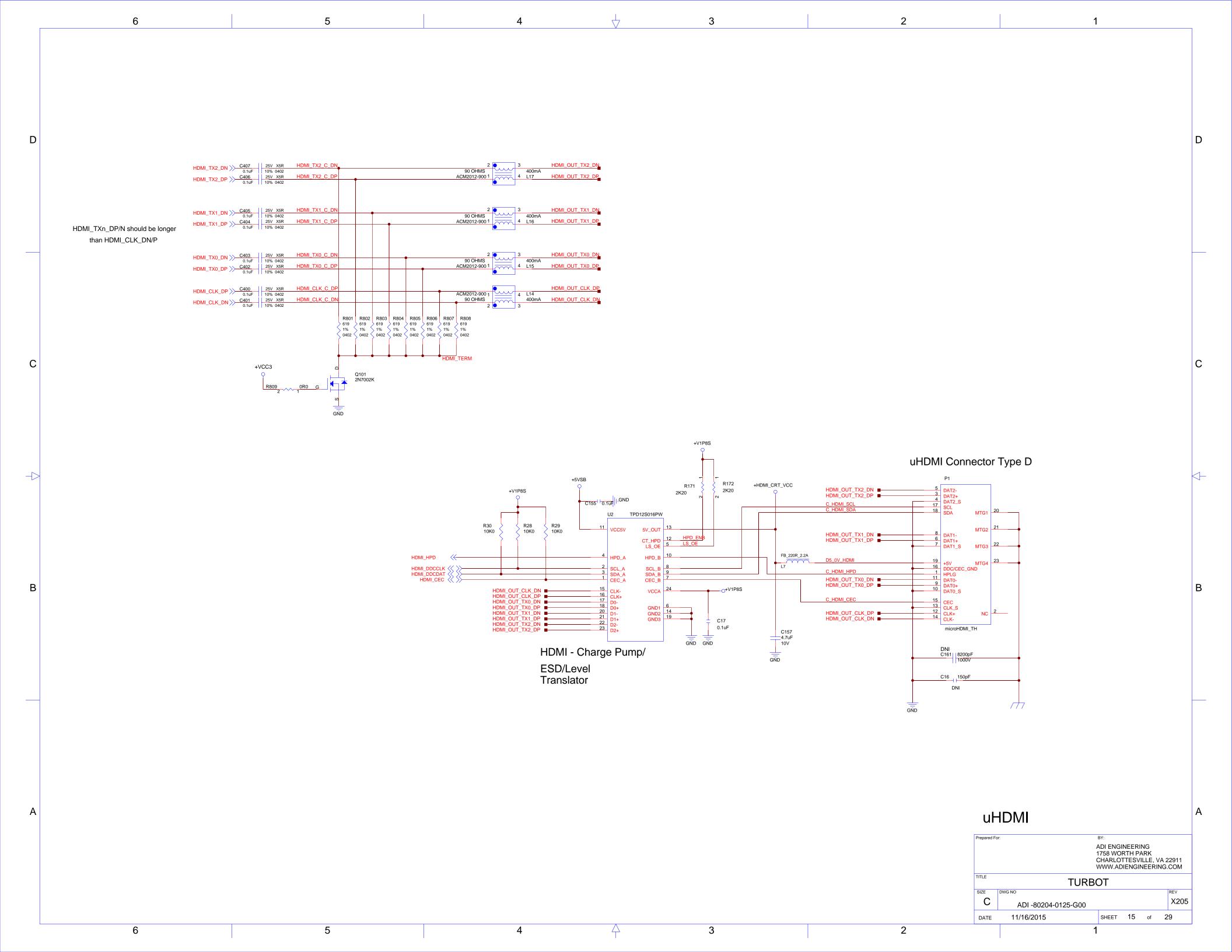


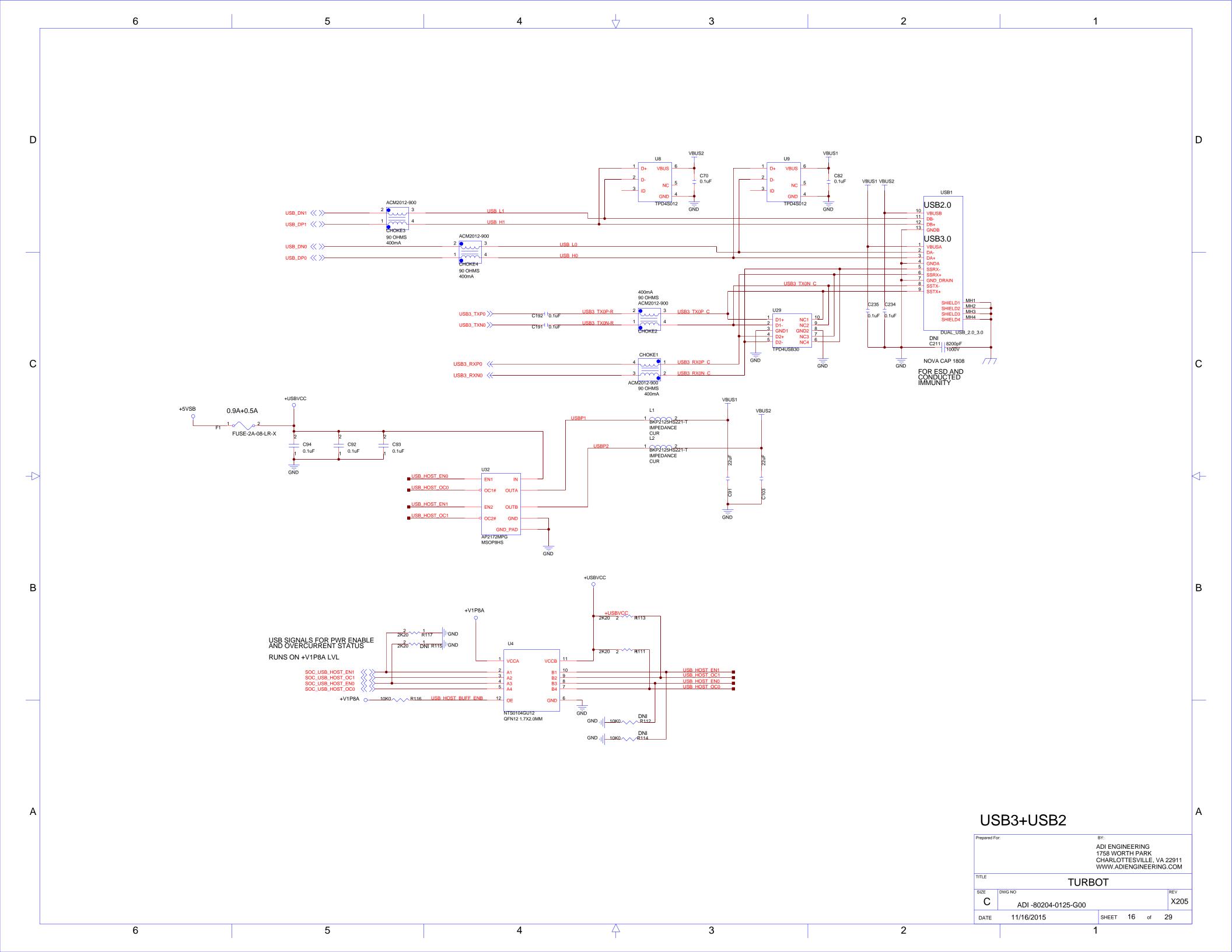


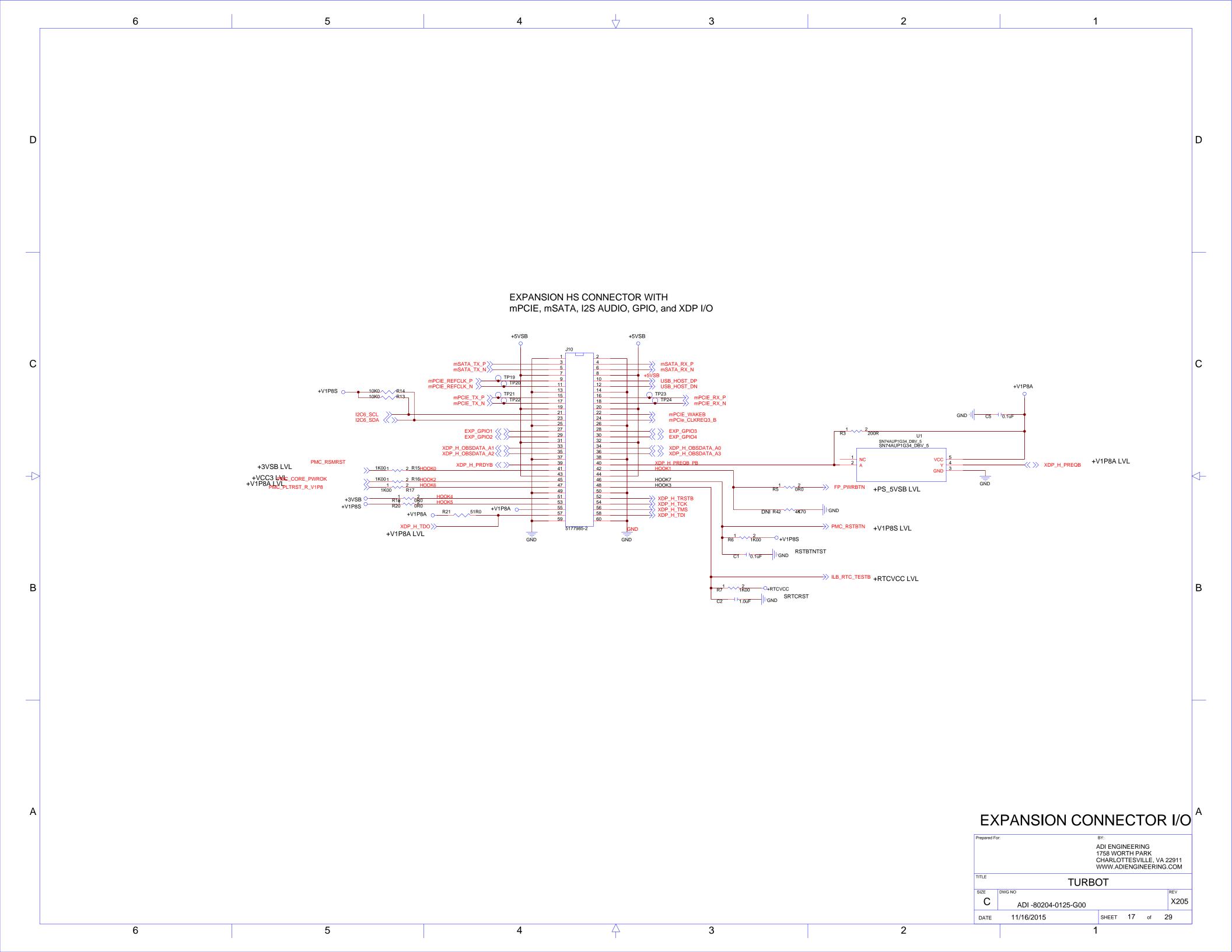


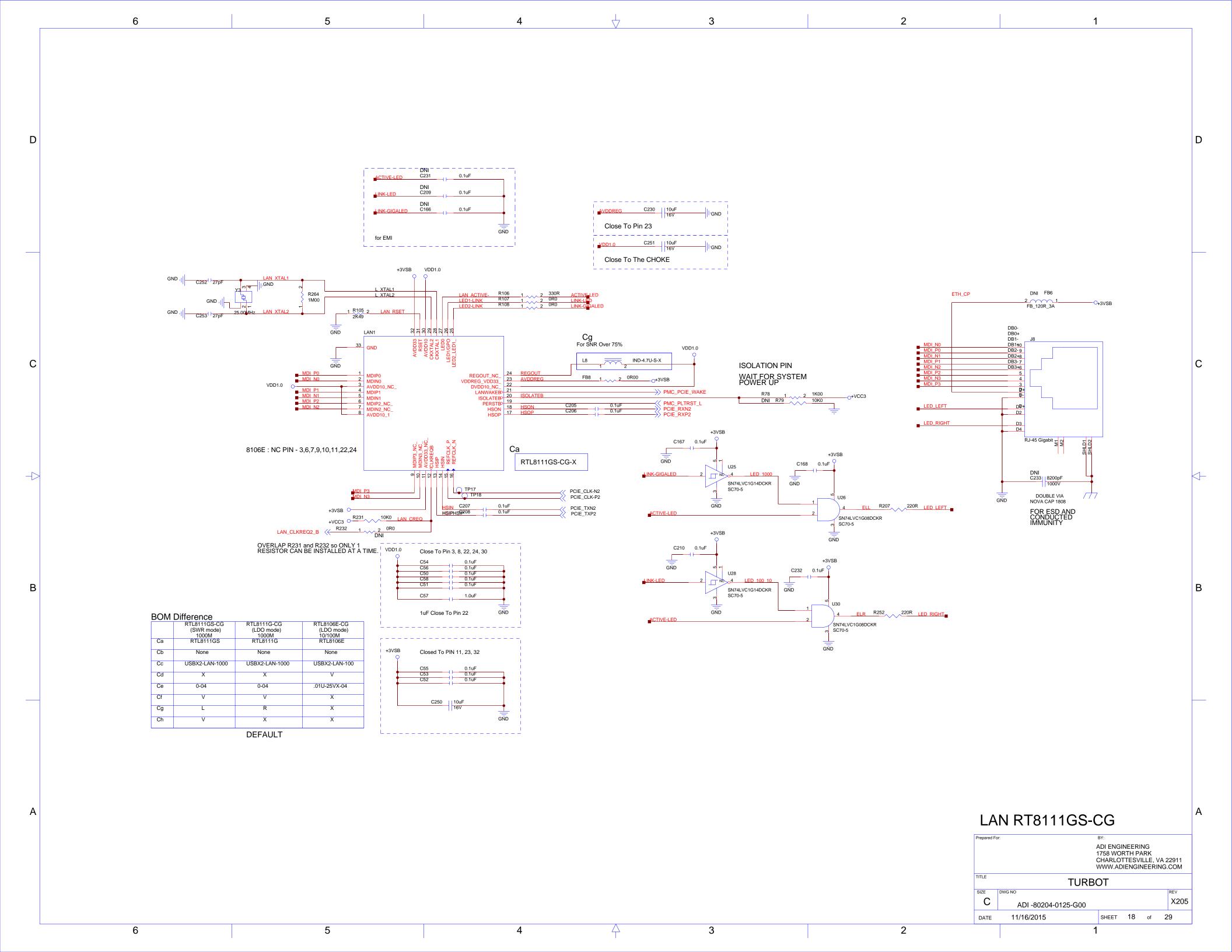




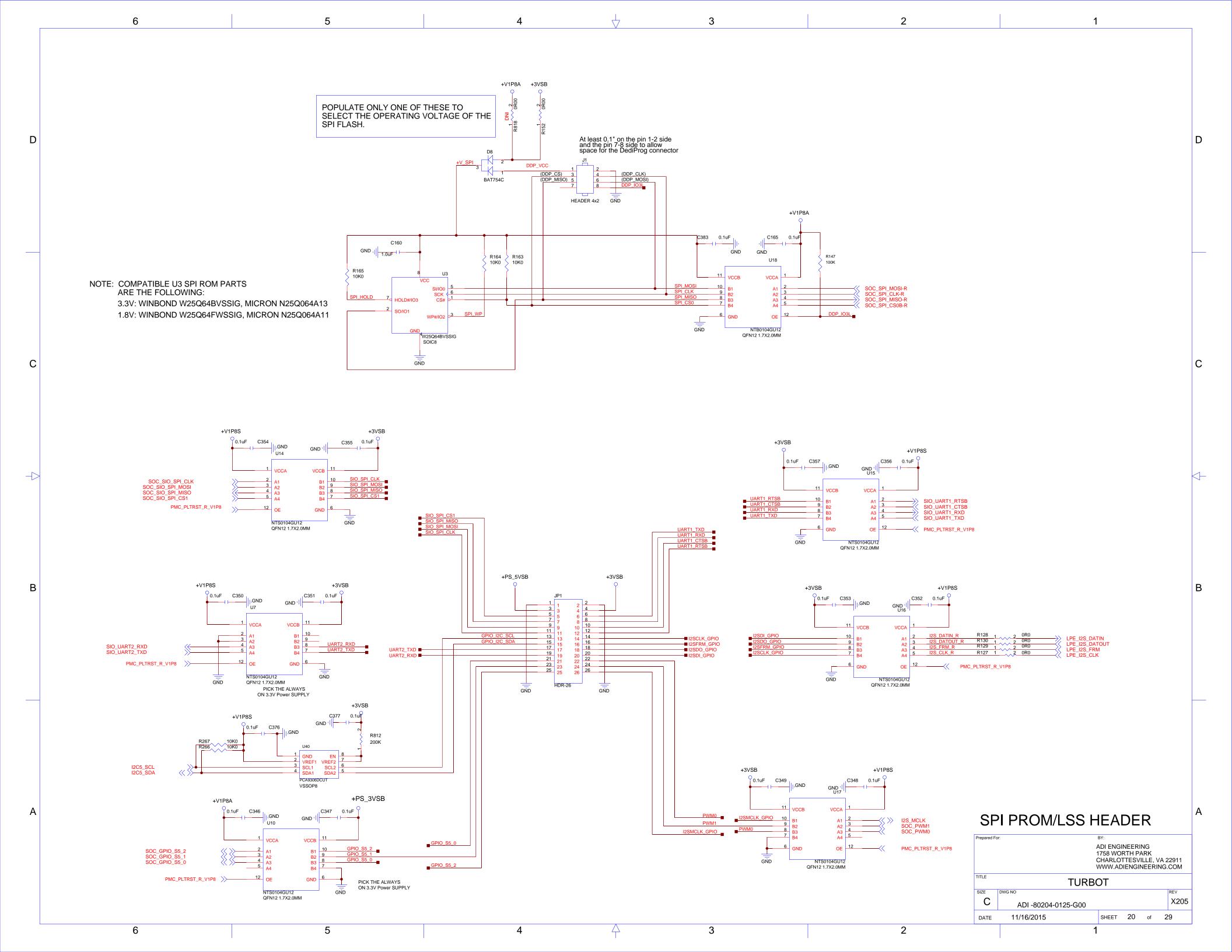


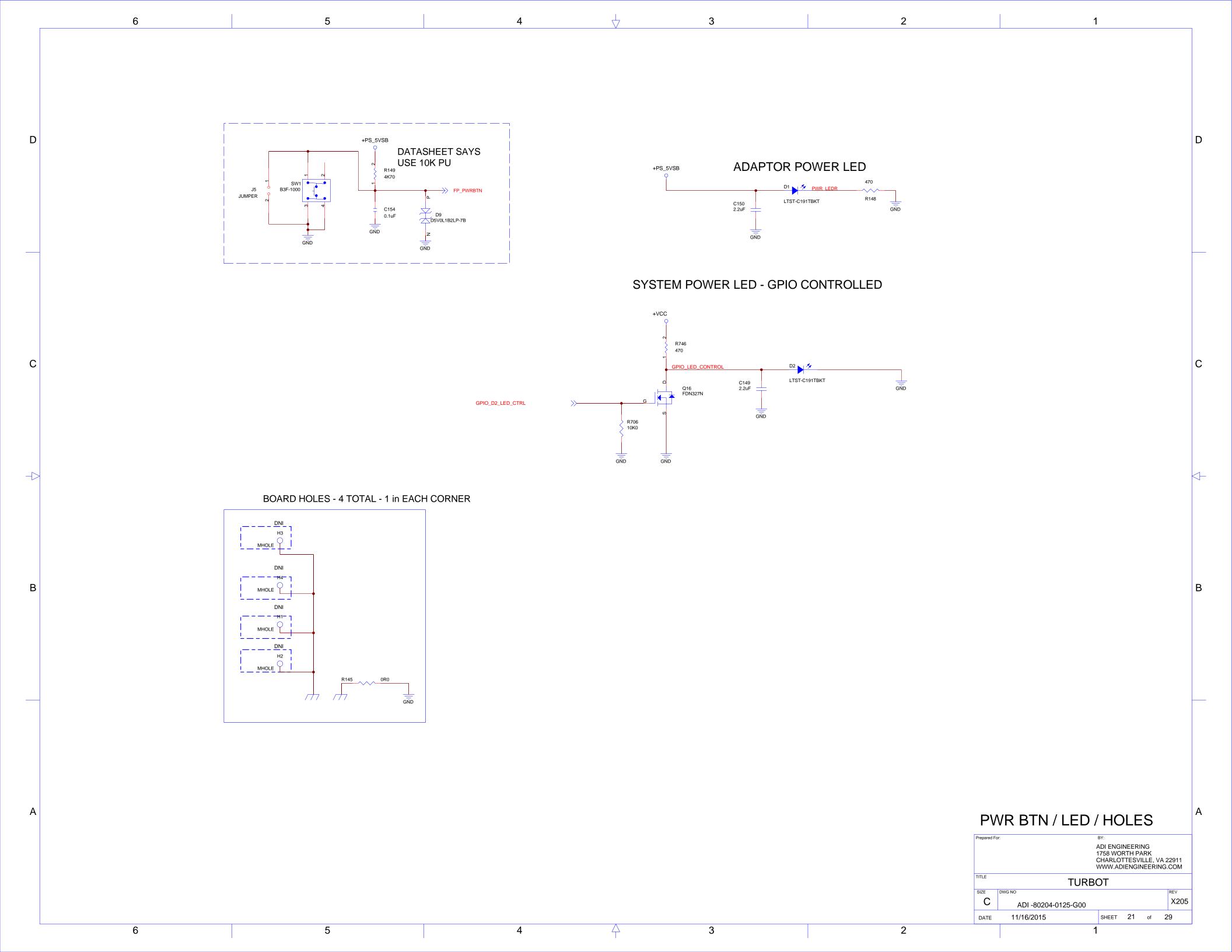


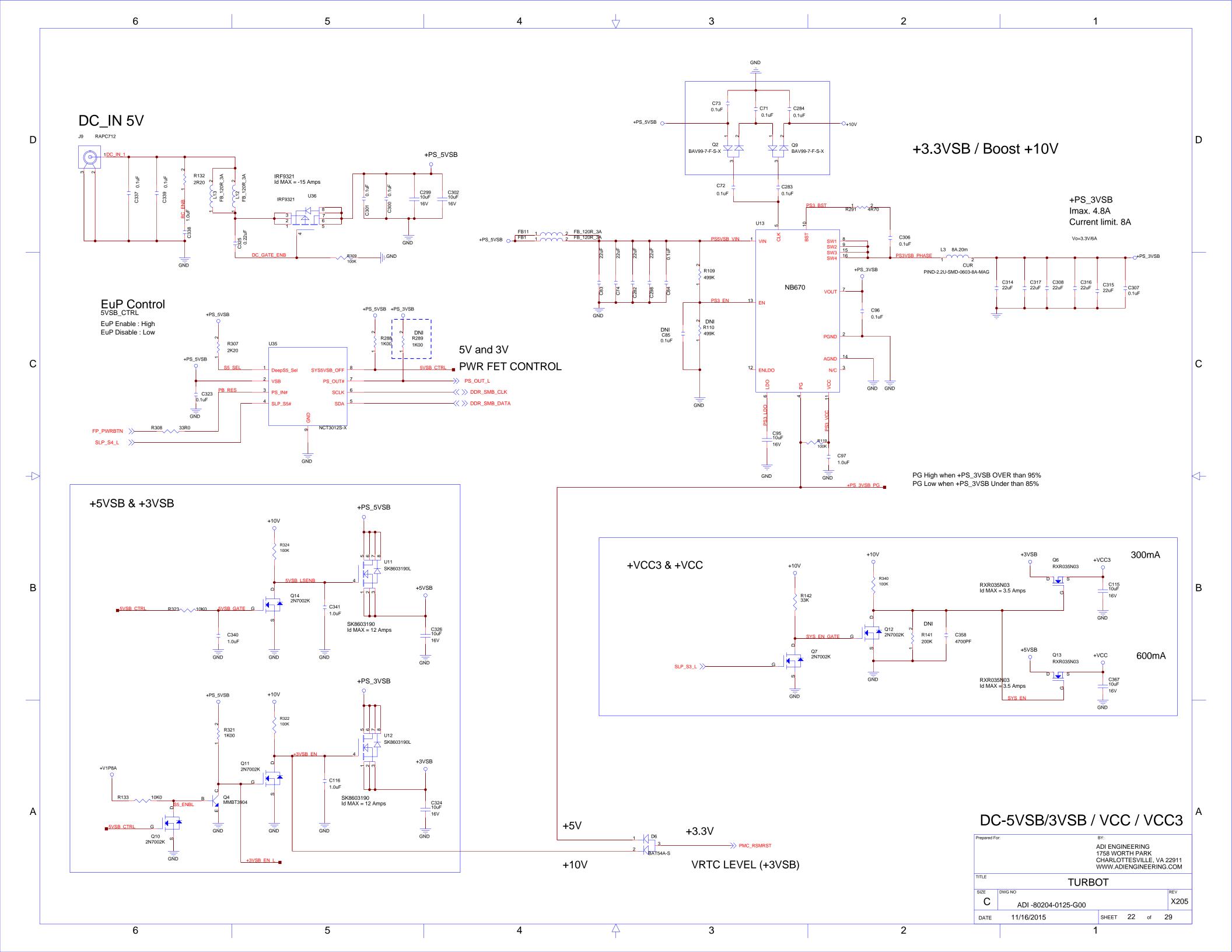


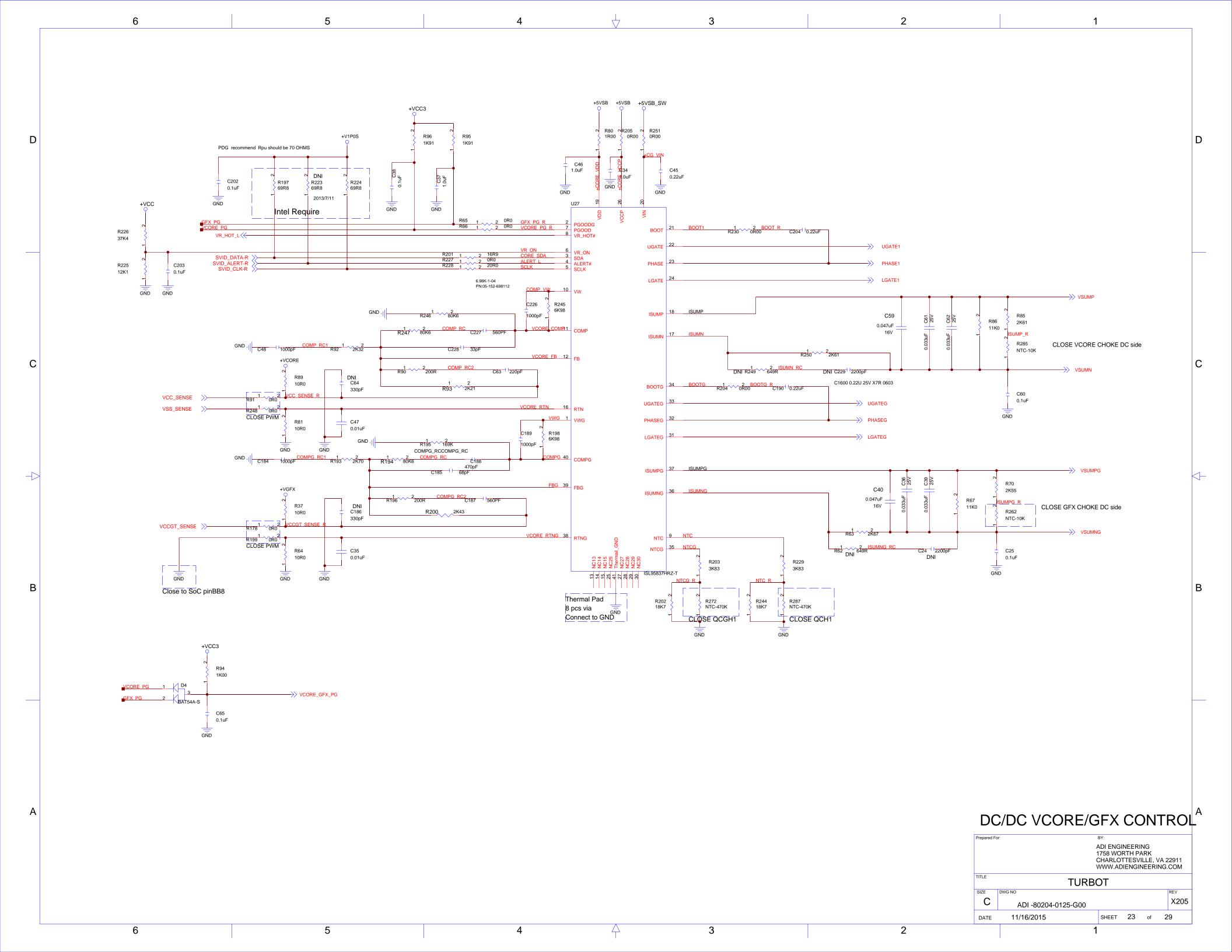


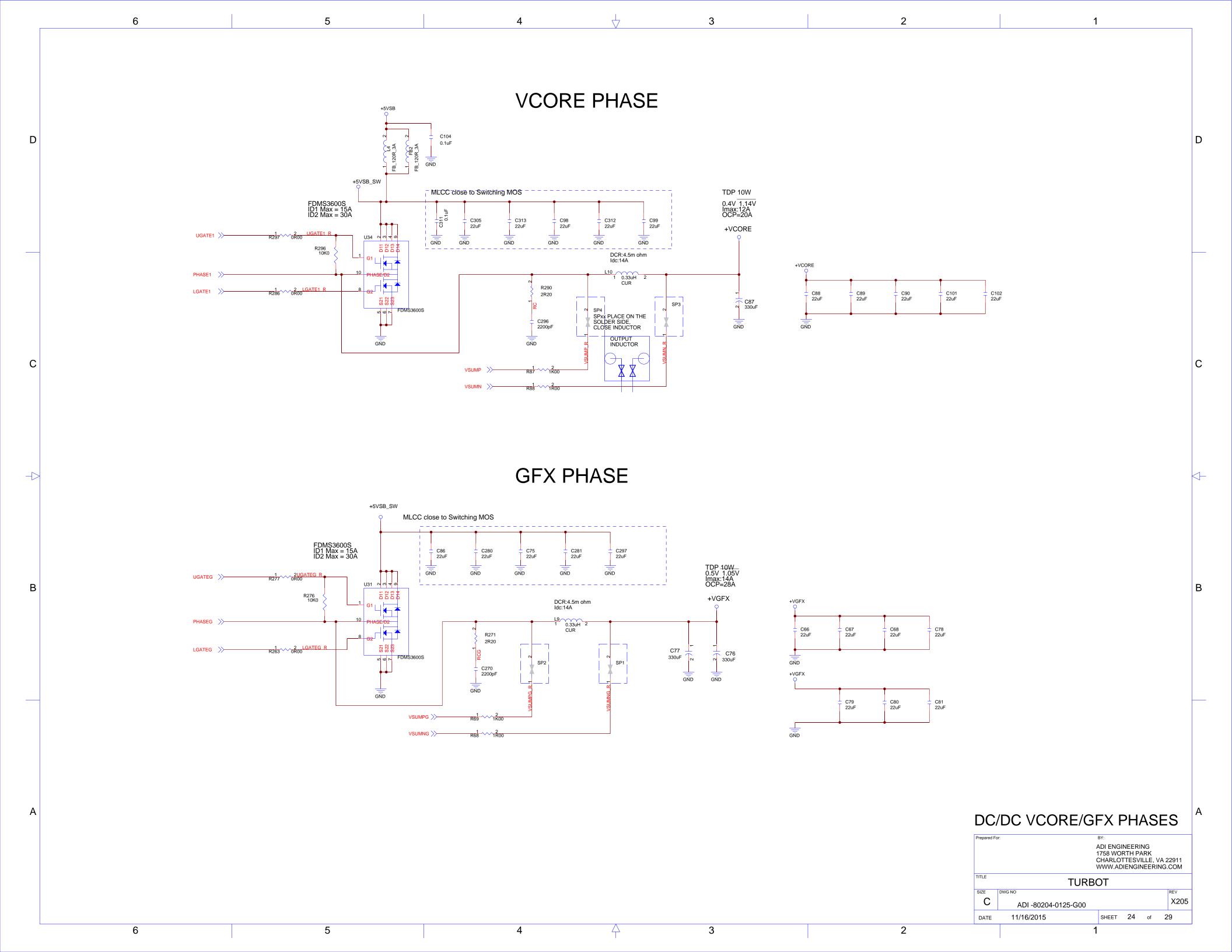


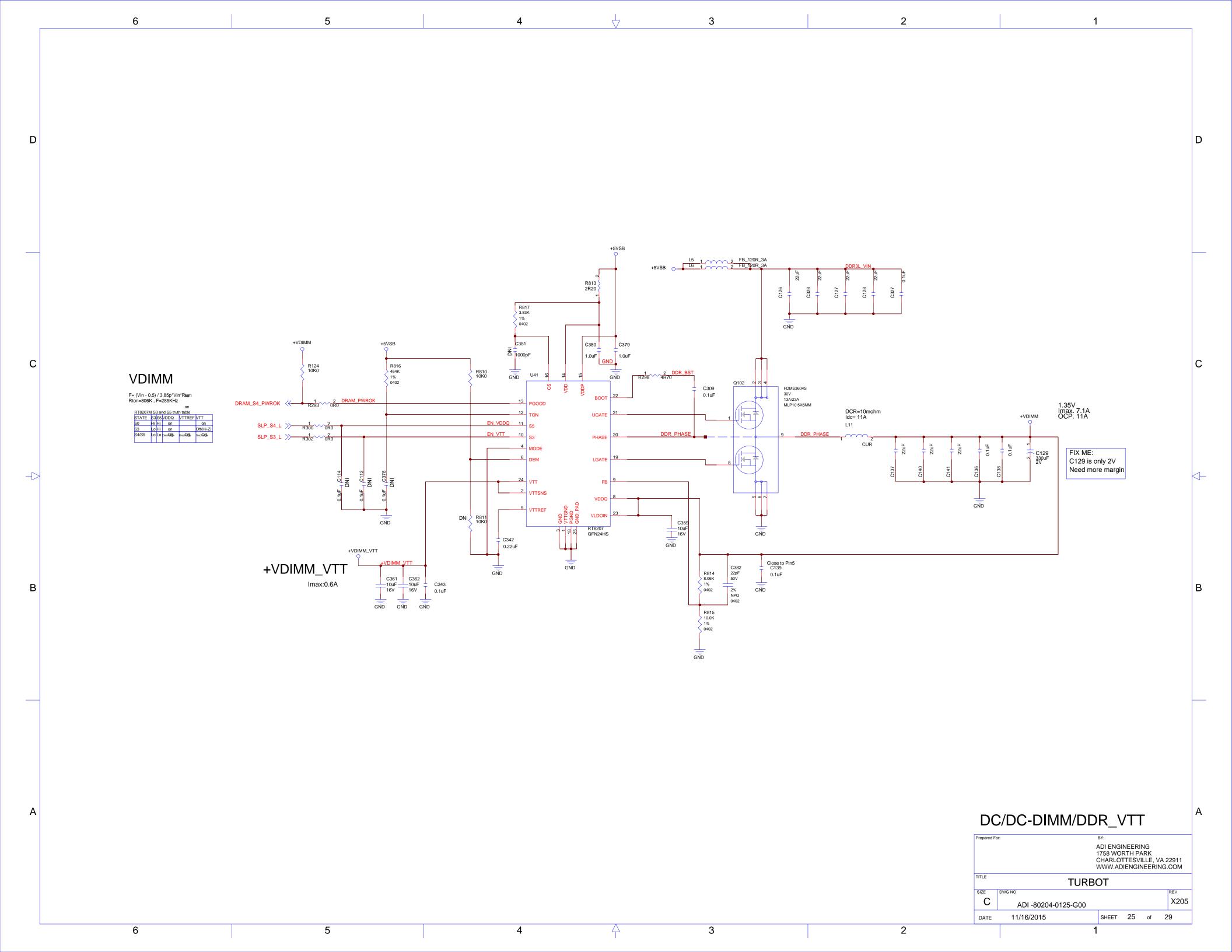


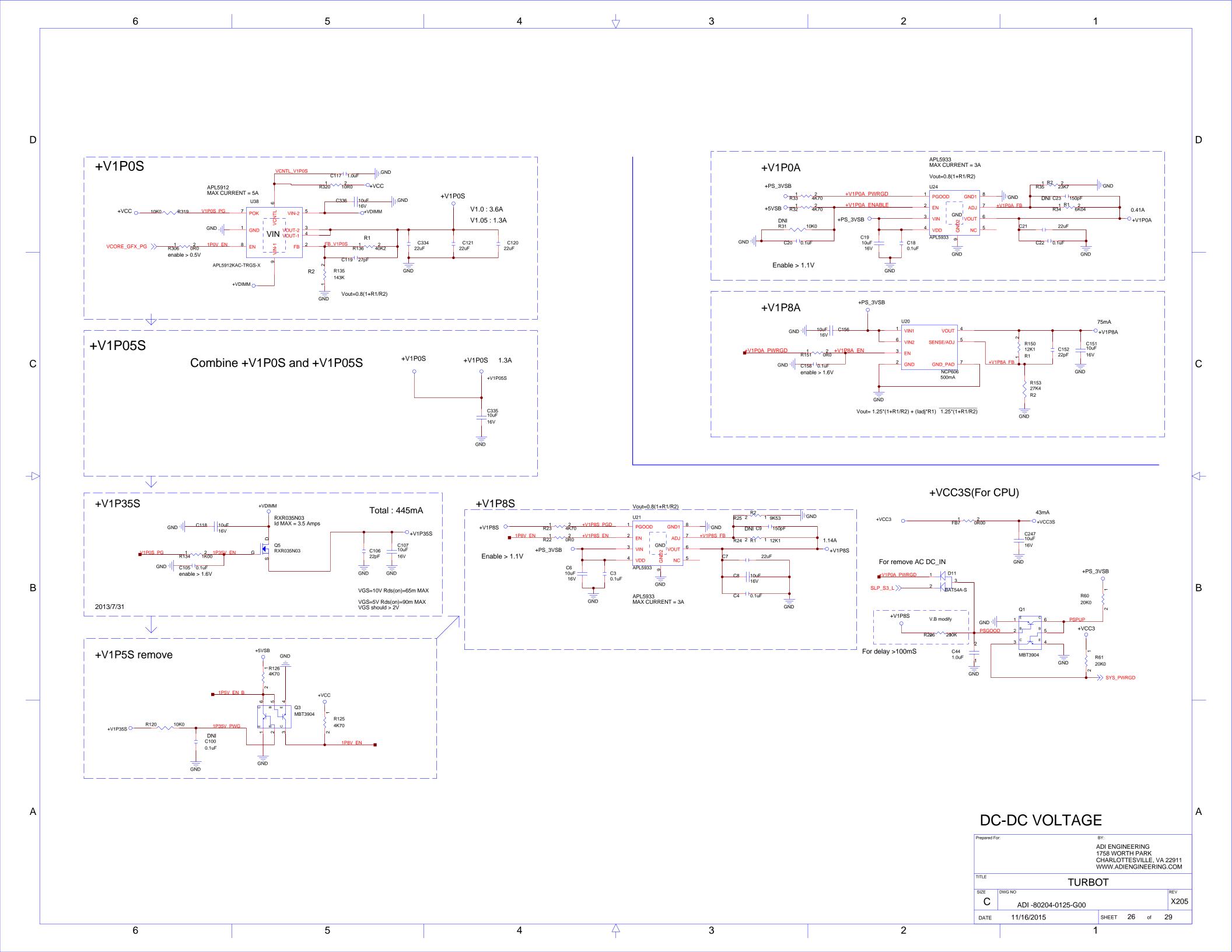












6 3 PCH-GPIO function Interrupt mapping INT# port PCIe*1 port Pin Name Power Well Usage Boot Set Function Device GPIO_S5[00] 1P8VSB, 20k,H SOC_GPIO_S5_0 (LSS CONN) GPO LAN INTC# RTL8111GS-CG port 2 GPIO_S5[01] 1P8VSB, 20k,H SOC_GPIO_S5_1 (LSS CONN) GPO GPIO_S5[02] 1P8VSB, 20k,H SOC_GPIO_S5_2 (LSS CONN) GPO mPCIE_WAKEB GPI GPIO_S5[03] 1P8VSB, 20k,H GPO OPEN GPIO_S5[04] 1P8VSB, 20k,L BOM OPTION GPI GPIO_S5[05] 1P8VSB, 20k,L BOM OPTION GPI GPIO_S5[06] 1P8VSB, 20k,L GPIO_S5[07] 1P8VSB, 20k,L BOM OPTION GPI GPO GPIO_S5[08] 1P8VSB, 20k,H HDMI_DC_DC ENABLE GPO 1P8VSB, 20k,H HDMI LD SWITCH ENABLE GPIO_S5[09] GPO GPIO_S5[10] 1P8VSB, 20k,H TXE UNLOCK control OPEN GPIO_S0_SC[022] 1P8V, 20k,H GPO GPIO_S0_SC[023] 1P8V, 20k,H XDP_H_OBSDATA_A0 GPO XDP_H_OBSDATA_A1 GPIO_S0_SC[024] 1P8V, 20k,H GPO XDP_H_OBSDATA_A2 GPO GPIO_S0_SC[025] 1P8V, 20k,H XDP_H_OBSDATA_A3 GPO GPIO_S0_SC[026] 1P8V, 20k,H GPIO_S0_SC[027] 1P8V, 20k,H EXPANSION_BUS GPIO1 GPO GPIO_S0_SC[028] GPO 1P8V, 20k,H EXPANSION_BUS GPIO2 GPO GPIO_S0_SC[029] 1P8V, 20k,H EXPANSION_BUS GPIO3 EXPANSION_BUS GPIO4 GPIO_S0_SC[030] GPO 1P8V, 20k,H GPIO reserved GPO GPIO_S0_SC[058] 1P8V, 20k,L GPIO_S0_SC[059] 1P8V, 20k,L GPIO reserved GPO GPO 1P8V, 20k,L GPIO reserved GPIO_S0_SC[060] GPIO_S0_SC[057] Debug Port UART3 TXD 1P8V, 20k,H UART GPIO_S0_SC[061] Debug Port UART3 RXD UART 1P8V, 20k,H

GPIO/HW MAPPING

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