ADQ7WB Datasheet

ADQ7WB is a high-end 12b data acquisition board, designed to meet the most challenging wide-band measurements. ADQ7WB is optimized for general wide-band radio applications as RF / IF and IQ receivers. ADQ7WB features:

- *2 channels operations*
- *5 GSPS per channel*
- *7 GByte/s sustained data transfer rate*
- *6.5 GHz analog bandwidth*
- *2.5 GHz instantaneous bandwidth*
- *Open FPGA for real-time DSP*
- *Digital Down-Converter firmware option*

ADQ7WB Datasheet

Features

- 2 analog channels
- 5 GSPS sample rate per channel
- 12 bits vertical resolution
- AC-coupled 6.5 GHz analog BW
- 2.5 GHz instantaneous bandwidth
- Internal and external clock reference
- Internal and external clock
- Clock reference output
- Internal and external trigger
- Multi-unit synchronization
- Time-stamp for real-time operation
- 4 GBytes data memory
- 5 GBytes/s sustained data streaming to PC
- 7 GBytes/s peer-to-peer streaming to GPU
- Data interfaces PCIe and PXIe

ADQ7 Development Kit

- Open FPGA for custom applications
- Real-time signal processing

Applications

- RADAR
- LIDAR
- Wireless communication
- L-band direct sampling
- High-speed RF data recording
- Scientific instruments
- Particle physics
- Semiconductor test
- ATE
- Test and measurement
- Quantum technology

Advantages

- PC interface options for optimized systems partitioning.
- Advanced analog front-end and high sample rate for meeting system requirements.
- Real-time custom processing for partitioning of advanced systems. This optimizes cost of ownership.
- SP Devices' design services are available for fast integration to lower time-to-market.

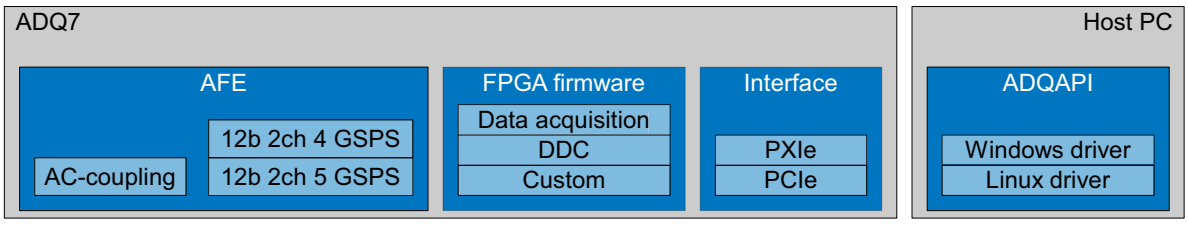
Digitizer solution for radio applications.

The AC-coupled front-end of ADQ7WB is optimized for high linearity for wide-band IF/IQ/RF radio applications.

Due to the vast amounts of data produced the signal processing support is key. Therefore ADQ7WB includes several layers of high-speed signal processing; the open FPGA and application-specific firmware enables integration of real-time algorithms and very compact system design; the software development kit for application integration is available both for Windows and Linux.

The high-speed PXIe and PCIe Gen3 x8 enable efficient communication between the firmware and the software. The form factor (host PC interfaces) options allow the ADQ7WB to be integrated into either a powerful PC or a modular instrument for a wide range of system architectures.

The PCIe interface also includes support for peer-to-peer streaming directly to a GPU.



1 Selection guide

There are several options for ADQ7WB. This guide will help you to select the right options. Follow the procedure listed to find the best product for your application. Each of the items in the list are described further in this document. The table below to shows which combinations that are available.

1. Select form factor; –PCIE or –PXIE.
2. Select one or several of the firmware packages; –FWDAQ, or/and –FW4DDC.
3. Add ADQ7 Development Kit if custom real-time signal processing in the FPGA is required; –DEV7DAQ.

		ADQ7WB
Key parameters (Factory installed)		
Number of channels		2
Sample rate / channel with internal clock	[GSPS]	5
Sample rate / channel with external clock	[GSPS]	4 and 5
Mechanical form factor (select one, factory installed)		
PXIe Gen3 x8	–PXIE	✓
PCIe Gen3 x8	–PCIE	✓
Firmware (in-field upgrade possible)		
Data Acquisition (included)	–FWDAQ	✓
Radio Systems	–FW4DDC	✓
ADQ7 Development Kit for –FWDAQ	–DEV7DAQ	✓

Note: The firmware option –FW4DDC is a replacement (not an add-on) of the standard –FWDAQ firmware. This means that some of the functions in examples and in documentation for –FWDAQ may not be available. Only the API functions and examples especially designed for the specific firmware option will work when that firmware option is loaded. Please note that with each device you are always entitled to load the standard –FWDAQ onto the device and use the device with the standard firmware acquisition modes.

Note: Changing firmware consists of uploading new contents to the on-board flash memory and restarting the digitizer. The restart requires a cold reboot as the PCIe link has to be re-enumerated by the BIOS of the host system.

2 Technical data

All values are typical unless otherwise noted.

Table 1: General parameters

		ADQ7WB
Key parameters		
Channels		2
Sample rate / channel with internal clock	[GSPS]	5
Sample rate / channel with external clock	[GSPS]	4, 5
Resolution	[bits]	12
Analog bandwidth	[Hz]	300 k to 6.5 G
Data memory[1]	[GByte]	4
Power		
Power supply	[V]	12
Power dissipation	[W]	60

1. The data memory is shared between data (2 bytes per sample) and record headers. The memory is shared between all activated channels.

Table 2: Analog input

		ADQ7WB
Analog inputs		
Coupling		AC
Input Impedance AC	[Ω]	50
Input Impedance DC	[Ω]	10k
Input range	[V_{pp}]	0.9
Over-voltage protection		See **Table 12**
Bandwidth lower –3 dB	[kHz]	300
Bandwidth upper –1 dB	[GHz]	4
Bandwidth upper –3 dB	[GHz]	>6
Connector		SMA

Table 3: Dynamic performance

		ADQ7WB
Analog performance up to 1 GHz for –1dBFS		
SNR	[dBFS]	55
SNDR	[dBFS]	55
SFDR	[dBFS]	60
ENOB	[bits]	8.8
Noise power spectral density	[dBFS/Hz]	–153
Analog performance up to 4 GHz for –1dBFS		
SNR	[dBFS]	49
SNDR	[dBFS]	49
SFDR	[dBFS]	60
ENOB	[bits]	7.8
Noise power spectral density	[dBFS/Hz]	–153
Inter modulation 2 tones at –7dBFS up to 3 GHz		
IMD3	[dBFS]	–62
Sampling time		
Jitter[1]	[fs]	125

1. Using internal clock reference. Measured indirect from SNR of a –1 dBFS sine wave signal.

Table 4: Clock

		ADQ7WB
Internal Clock Reference		
Frequency	[MHz]	10
Accuracy	[ppm]	± 3 ± 1/year
Front panel connector used as clock reference input		
Frequency	[MHz]	10/100 MHz ± 5 ppm
Signal level (min – max)	[Vpp]	0.5 – 3.3
Impedance AC	[Ω]	50
Impedance AC (high[1])	[Ω]	200
Impedance DC	[Ω]	10 k
Connector		SMA
PXIe clock reference (–PXIE option only)		
PXIe clk	[MHz]	100
PCIe sync	[MHz]	10
Front panel connector used as clock reference output		
Frequency	[MHz]	10
Signal level into 50 Ω load	[Vpp]	1.2
Output impedance AC	[Ω]	50
Output impedance DC	[Ω]	10 k
Duty cycle		50% ± 5%
Connector		SMA
Front panel connector use as external clock input[2]		
Frequency	[GHz]	2, 2.5

1. Software-controlled high-impedance setting for large fan-out distribution using bussed connection.
2. Sample rate is 2 x external clock frequency.

Table 5: Trigger/GPIO front panel connector

		ADQ7WB
Connector		
Connector shared between input and output		SMA
External trigger used as input		
PRF (max)	[MHz]	78.125
Impedance DC	[Ω]	50
Impedance DC (high[1])	[Ω]	500
Signal level (min – max)	[V]	–0.5 to 3.3
Adjustable trigger threshold	[V]	0 to 3
Sensitivity	[mVpp]	200
Time resolution	[ps]	25
Excess jtter[2]	[ps]	25
Max GPI data rate	[Mbit/s]	156.25
External trigger used as output		
PRF (max)	[MHz]	156.25
Low level output voltage max	[V]	0.1
High level output voltage min	[V]	2.2 (into 50 Ω load)
Impedance DC	[Ω]	50
Max GPO data rate	[Mbit/s]	156.25

1. Software-controlled high-impedance setting for large fan-out distribution using bussed connection.
2. The excess jitter is jitter added to the trigger signal in addition to the jitter caused by the finite timing resolution.

Table 6: Sync/GPIO front panel connector

		ADQ7WB
Connector		
Connector shared between input and output		SMA
External sync used as input		
PRF (max)	[MHz]	78.125
Impedance DC	[Ω]	50
Impedance DC (high[1])	[Ω]	500
Signal level (min – max)	[V]	–0.5 to 3.3
Adjustable trigger threshold	[V]	0 to 3
Sensitivity	[mVpp]	200
Max GPI data rate	[Mbit/s]	156.25
External sync used as output		
PRF (max)	[MHz]	156.25
Low level output voltage max	[V]	0.1
High level output voltage min	[V]	2.2 (into 50 Ω load)
Output impedance DC	[Ω]	50
Max GPO data rate	[Mbit/s]	156.25

1. Software-controlled high-impedance setting for large fan-out distribution using bussed connection.

Table 7: GPIO connector

		ADQ7WB
GPIO single ended		
Number of I/O		12
Data rate per pin	[Mbit/s]	156.25
Low level input voltage max	[V]	0.8
High level input voltage min	[V]	2
Low level output voltage max	[V]	0.1
High level output voltage min	[V]	2.2 (no load)
GPIO differential LVDS		
Input		2
Clock input		2
Output		3
Data rate per pin	[Mbit/s]	156.25

Table 8: General specifications

PARAMETERS		INTERFACE OPTION –PXIE	INTERFACE OPTION –PCIE
Data rate			
Interface to host PC		PCIe	PCIe
Standard		Gen3 by 8 lanes	Gen3 by 8 lanes
Data rate sustained peer-to-peer to GPU[1] [2]	[GBytes/s]	–	7
Data rate sustained to host PC[2]	[GBytes/s]	5	5
Mechanical			
Mechanical bus width [3]	[lanes]	–	16
Weight	[g]	700	700
Board width [4]	[slot]	2	2
Board length		–	full length
Board height		3U	–
Electrical			
Power supply		From chassis	6-pin ATX power
Bus width electrical (PCIe Gen3 x8)	[lanes]	8	8
Temperature range			
Operation	[°C]	0 to 45	0 to 45
Compliances			
CE		✓	✓
RoHS2		✓	✓
FCC		Exclusion according to CFR 47, part 15, paragraph 15.103(c)	

1. Firmware option –FWDAQ only.
2. This is the sustained data rate supported by ADQ7WB, i.e. the transfer rate of data (excluding headers etc.) maintained on average for a long time. The system performance is depends on the capacity of the complete system, including the host computer, accessories and the user's application.
3. The wide connector is required to support the weight of the board.
4. 2nd slot is left of the connector. See **Section 19.3** and **Section 19.4** respectively.

Table 9: Firmware option feature list

	FIRMWARE OPTION	
	–FWDAQ	–FW4DDC
Signal enhancement IP		
DBS (Digital Baseline stabilizer)	✓	–
ADX (Time interleaving correction)	✓	✓
Trigger modes		
Software trigger	✓	✓
External trigger	✓	✓
Common level trigger [1]	✓	–
PXIe backplane trigger [2]	✓	✓
Internal trigger	✓	✓
Trigger output		
Internal trigger	✓	✓
Trigger event	✓	✓
Clock		
Internal clock reference	✓	✓
External clock reference	✓	✓
Sample skip	✓	✓ [3]
External clock	✓	✓
Clock reference output	✓	✓
Data acquisition modes		
Continuous streaming	✓	✓
Triggered streaming with header	✓	✓
Triggered streaming w/o header	✓	✓
ADQ Development Kit		
Custom FW development Kit	✓	–

1. Both channels trigger simultaneously at an event on one selected channel.
2. Requires system timing module.
3. Sample skip on –FW4DDC is implemented by decimation including filtering in power of 2.

Table 10: Data acquisition parameters –FWDAQ

		FIRMWARE OPTION	
		–FWDAQ	–FW4DDC
Triggered streaming			
Re-arm time	[ns]	20	20
Pre-trigger length	[samples]	16 ki	16 ki
Pre-trigger length resolution	[samples]	8	8
Trigger delay	[samples]	$2^{32} - 1$	$2^{32} - 1$
Trigger delay length resolution	[samples]	16	16
Record length max	[samples]	2 Gi	2 Gi
Record length min	[samples]	40	40
Record length resolution	[samples]	16	16
Continuous streaming			
Data rate		PC link speed limit, see **Table 8**	PC link speed limit, see **Table 8**

Table 11: Software support

	FIRMWARE OPTION	
	–FWDAQ	–FW4DDC
Operating systems[1]		
Windows 7, 32-bit and 64-bit	✓	✓
Windows 8 / 8.1, 32-bit and 64-bit	✓	✓
Windows 10, 32-bit and 64-bit	✓	✓
Linux	✓	✓
Application		
ADCaptureLab GUI[2]	✓	–
MATLAB API and examples [3]	✓	–
C/C++ API and examples	✓	✓
.Net (C#, Visual Basic) API and examples	✓	–
Python examples	✓	✓
LabVIEW low level functions and examples [4]	✓	–

1. See “15-1494 Operating System Support” for supported distributions.
2. Windows only and firmware option –FWDAQ only. Intended for basic measurements, acquisition and analysis. Limited function support.
3. Windows only and firmware option –FWDAQ only.
4. Windows only and firmware option –FWDAQ only.

3 Absolute maximum ratings

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device. The analog inputs are protected from over-voltage but the values in **Table 12** must never be exceeded.

The ADQ7WB–PCIE has a built-in fan to cool the device. ADQ7WB–PXIE is cooled from the chassis fan. If there is a high fan setting on the chassis it should be used. The built-in temperature monitoring unit will protect the ADQ7WB from overheating by temporarily shutting down parts of the device if an overheat situation would occur.

The SMA connectors have an expected life time of 100 operations. For frequent connecting and disconnecting of cables, connector savers are therefore required. Note that the SMA connectors are sensitive to torque and bend. Always use a torque wrench with 4 to 5 in-lb. Use a flexible cable to avoid bending of the connector. Rigid components attached to the connector has to be supported by a mechanical structure to avoid bending the SMA connector.

Table 12: Absolute Maximum Ratings

		ADQ7WB
Analog input		
AC	[V]	± 2
DC max	[V]	–2
DC min	[V]	+2
External clock reference		
Signal level AC and DC combined	[V]	± 5
External trigger input		
Signal level to GND min	[V]	–2
Signal level to GND max 50-ohm mode	[V]	4.5
Signal level to GND max high impedance mode	[V]	5.5
External sync input		
Signal level to GND min	[V]	–2
Signal level to GND max 50-ohm mode	[V]	4.5
Signal level to GND max high impedance mode	[V]	5.5
Power supply		
Voltage to GND (min)	[V]	–0.4
Voltage to GND (max)	[V]	14
Temperature		
Operating (min)	[^{o}C]	0
Operating (max)	[^{o}C]	45

4 Frequency response

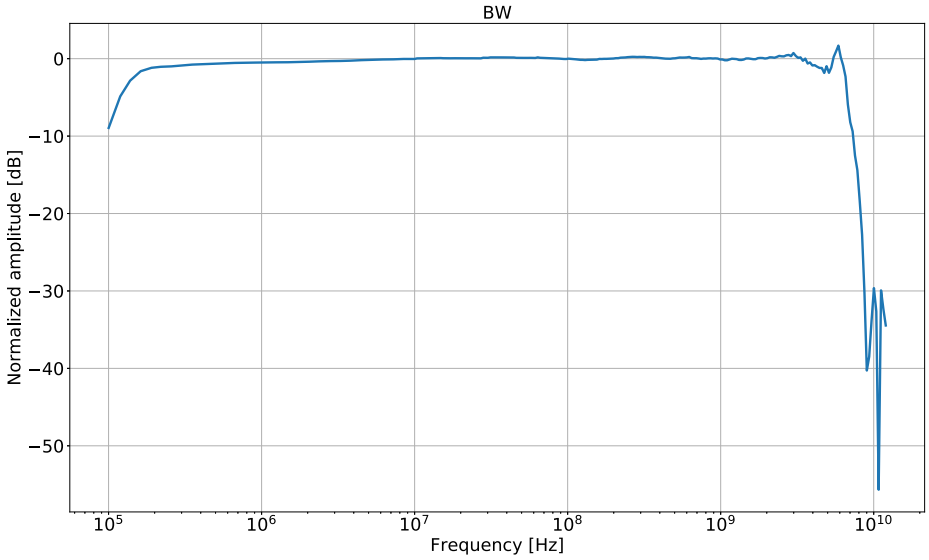


Figure 1: Frequency response on logarithmic frequency scale.

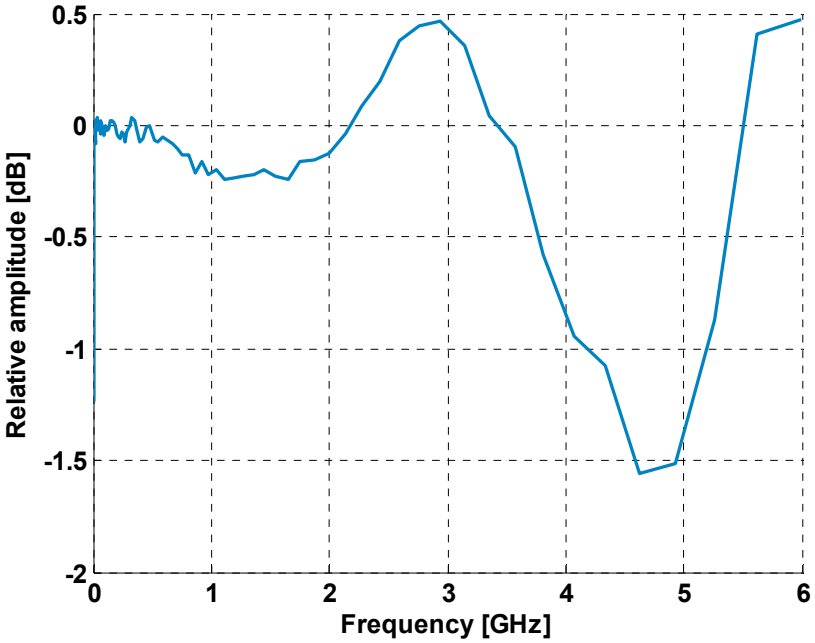


Figure 2: Frequency response channel A on linear frequency scale up to 6 GHz.

5 Frequency domain

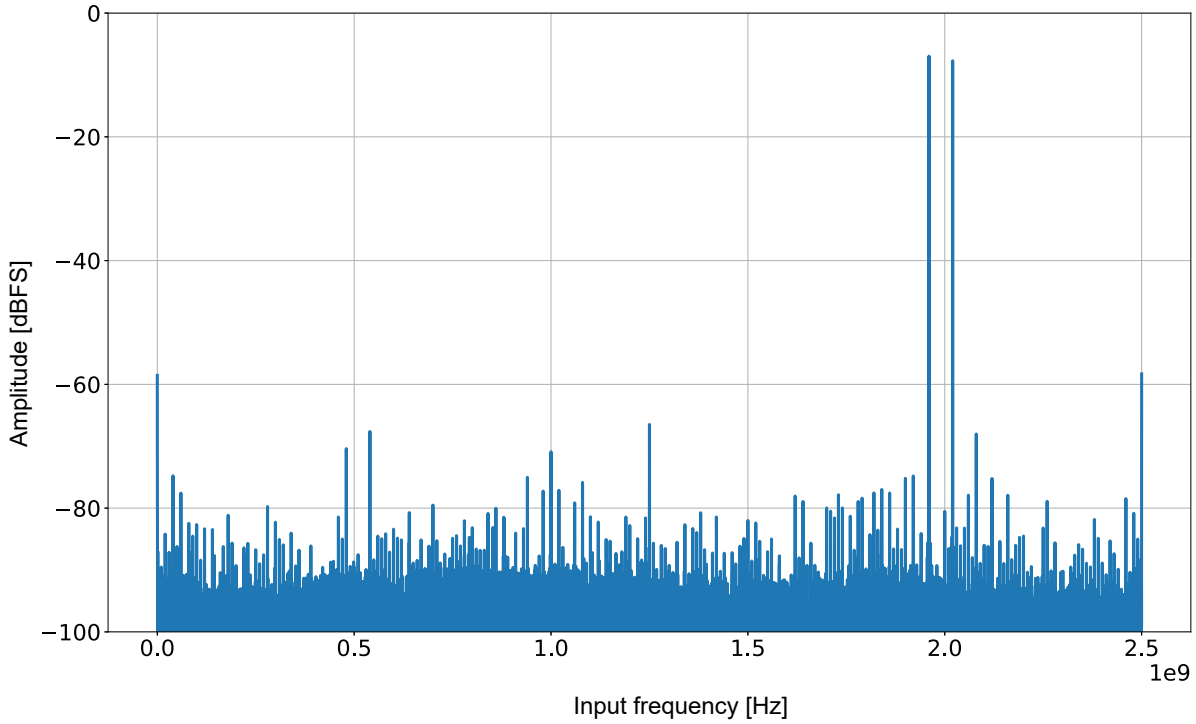


Figure 3: 2-tone measurement at 2 GHz.

6 Dynamic range

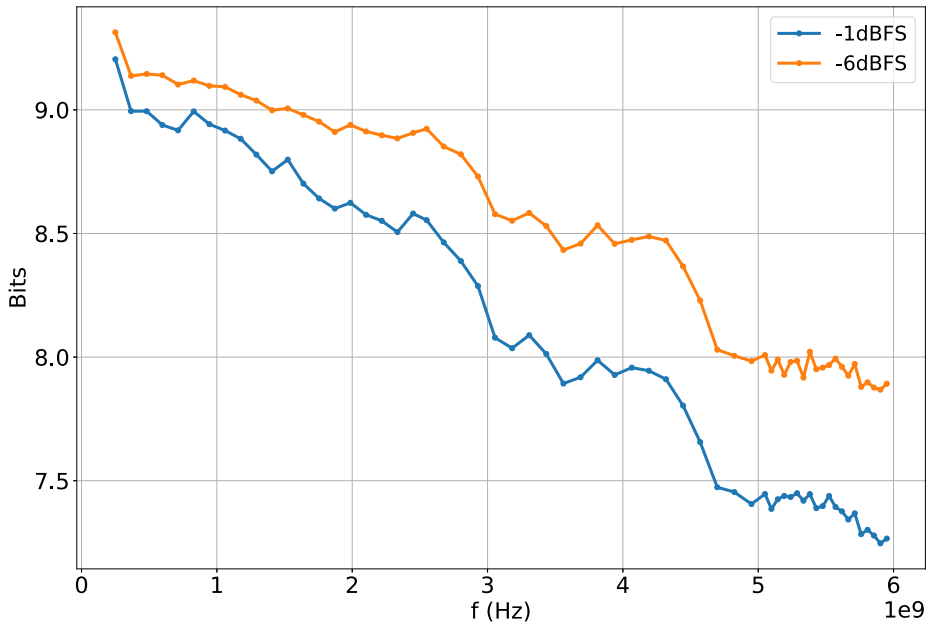


Figure 4: ENOB with respect to full scale for swept input signal frequency.

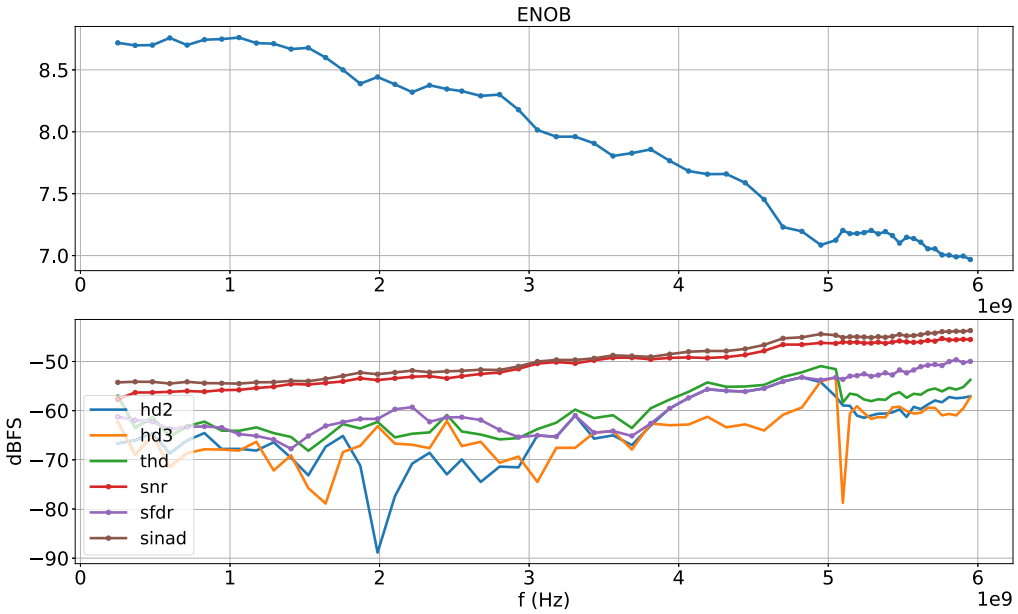


Figure 5: Parameters with respect to full scale for swept input signal frequency. Measured at –1dBFS.

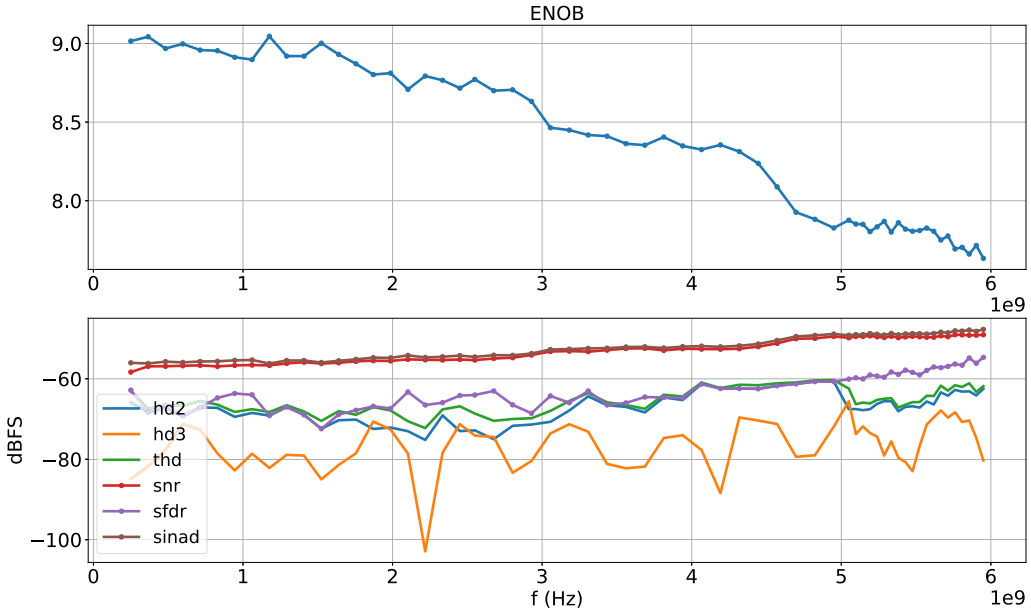


Figure 6: Parameters with respect to full scale for swept input signal frequency. Measured at –6dBFS.

7 Integrating the ADQ7WB

Figure 7 illustrates how ADQ7WB supports the key parts of the system integration.

7.1 Detecting the analog signal

The analog front-end (AFE) combines high dynamic range with high bandwidth to support the most advanced detectors. The AC-coupled front-end has high sensitivity to simplify the interfacing of various radio frequency systems.

7.2 Timing and synchronization

The clock management and trigger support connects with the infrastructure of the system. There are two main situations where synchronization is required; one ADQ7WB to another type of equipment and several ADQ7WB units in a multi-channel application.

The ADQ7WB can act as master and generate timing for the entire system and thereby save additional timing cards. It can also receive trigger and clocks from other devices. Synchronization and GPIO signals allow advanced sequencing.

The methods for synchronize several units in one location according to the application note 15-1583 “ADQ14 synchronizing several units” are also applicable to ADQ7WB.

7.3 Real-time signal processing

The data acquisition engine in the FPGA supports several methods for acquiring data and transfer it to the host PC. Since the data rate from the ADC is high, some parts of the application is preferably integrated into the FPGA to relax the load on the CPU in the host computer. There is a set of application-specific firmware options available to enable efficient real-time signal processing. In addition, the FPGA is open to the user through the ADQ7 Development Kit for integration of custom algorithms.

7.4 System integration

The interface to the host PC is one important parameter in the system integration. To enable an optimal solution, the ADQ7WB offers a wide variety of form factors.

Both the mechanical and electrical properties in various standards are important for the result. The mechanical properties enables an optimal placement of the ADQ7WB inside the target system and also which type of PC to use. The different electrical properties of the interface determine data transfer rate and noise immunity.

7.5 Building the application

The open software development kit (SDK) is a software package including drivers and API (ADQAPI) for integrating the ADQ7WB into an application. The many examples and application notes simplify the integration process and shorten the time-to-market.

Partitioning the application between a high-level analysis software in the host PC and a low-level real-time data analysis in the open FPGA enables high-performance applications to run on a cost-effective PC solution.

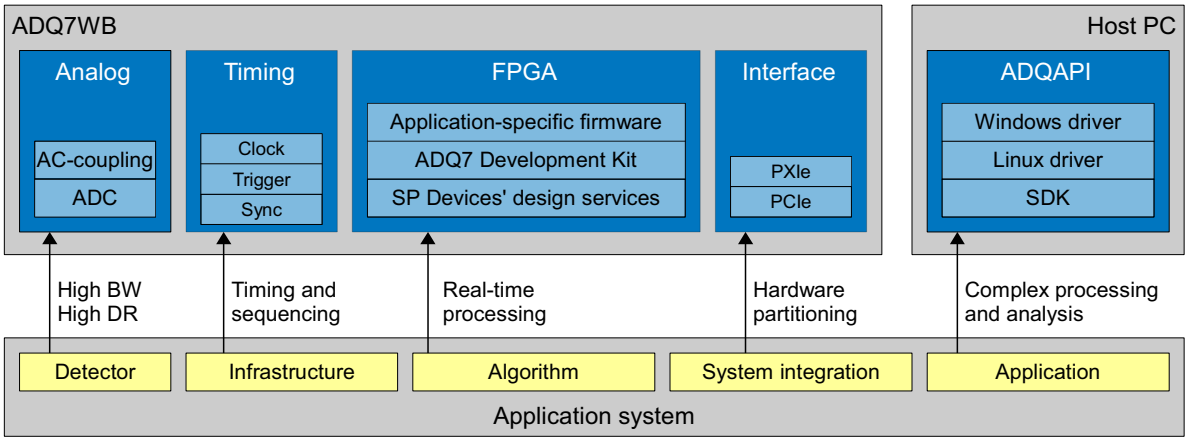


Figure 7: Integrating the ADQ7WB into the system.

8 Software tools

8.1 Operating systems

The software package includes drivers for the most common versions of Windows and several Linux distributions.

8.2 Software development kit, SDK

The ADQ7WB digitizer is easily integrated into the application by using the software development kit, SDK. The SDK is included free of charge with the ADQ7WB. The SDK includes programming examples and reference projects for several platforms. All functions are described in detail in document “14-1351 ADQAPI Reference Guide”. Please note that the data-rate performance is depending on the selected programming environment. Best result is achieved for the C/C++ interface. The SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

8.3 ADCaptureLab GUI for –FWDAQ

The ADQ7WB is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time-domain and frequency-domain analysis, see **Figure 8**. Data can be saved in different file formats for off-line analysis. With ADCaptureLab, the ADQ7WB operates as a benchtop oscilloscope.

Note that the GUI ADCaptureLab only support a subset of the functions offered by the ADQ7WB. The full potential of the ADQ7WB is achieved using the SDK. ADCaptureLab is available for Windows only and the firmware option –FWDAQ only.

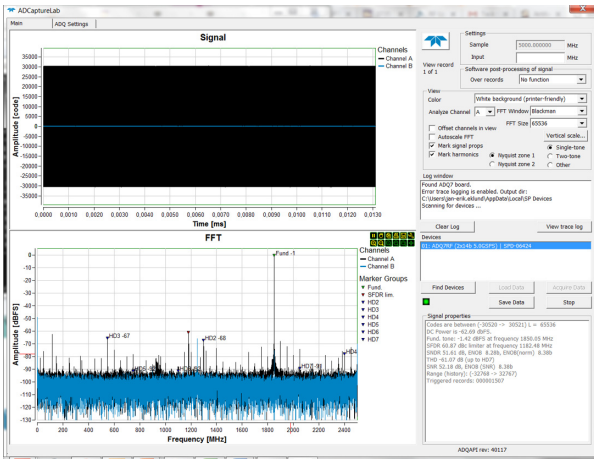


Figure 8: ADCaptureLab screen shot.

9 Block diagram

A detailed block diagram of ADQ7WB is shown in **Figure 9**. The following sections describe the parts of the ADQ7WB in detail. See also “19-2233 ADQ7 Manual” for more details on how to operate the ADQ7WB.

This datasheet describes functions included in the standard data acquisition firmware package –FWDAQ. Functionality of optional application-specific firmware packages is described in their respective datasheets.

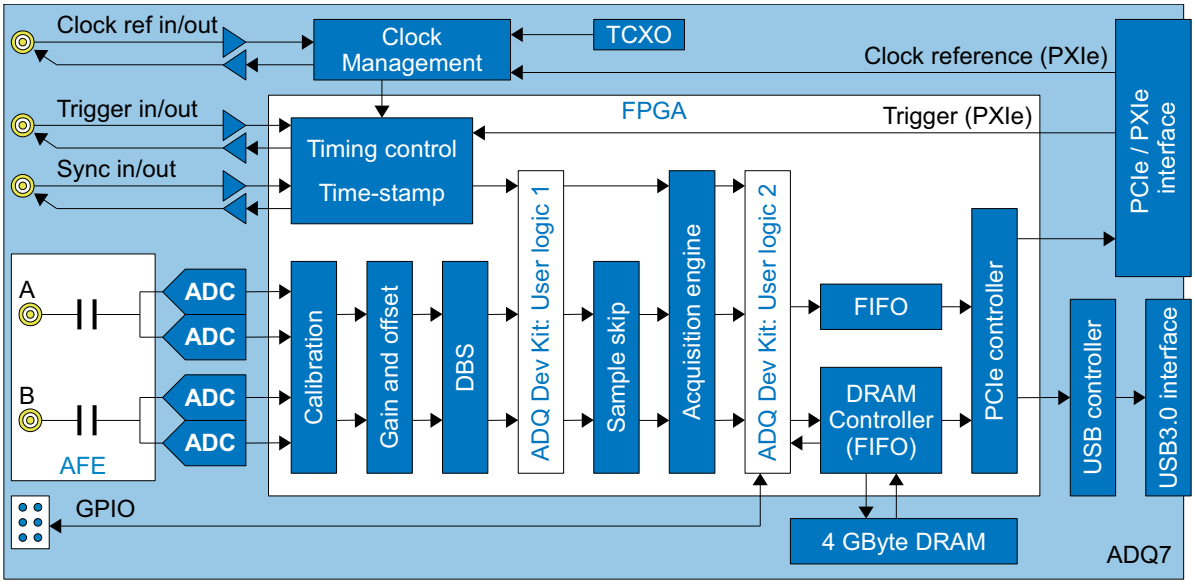
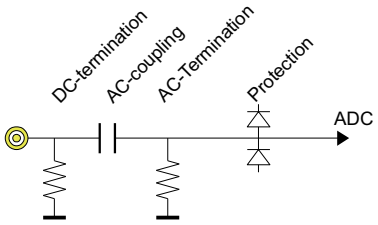


Figure 9: Block diagram for ADQ7WB–FWDAQ (standard firmware).

10 Analog front-end



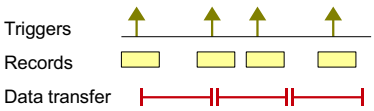
AC-coupling

The AC-coupled analog front-end is designed for high linearity over high bandwidth.

There is a high impedance DC-termination to keep the DC level of the input at 0 V. The 50 Ω matched termination is AC-coupled.

The overvoltage protection protects the sensitive ADC inputs from high signal levels. See **Section 3** for absolute limits without damage.

11 Data recording

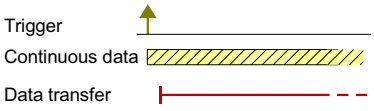


Triggered streaming

Use triggered streaming for maximum throughput.

At each trigger, a record (set of continuous data) is captured. The record is buffered in the DRAM, which acts as a FIFO, and transferred to the host PC. This large 4 GByte FIFO enables bursts of triggers at a very high rate. The large FIFO also guarantees reliable high-speed transfer to the PC.

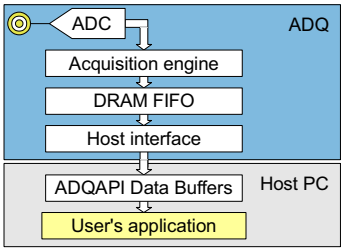
Each record has a header with timestamp and identifiers for post-processing analysis of the data.



Continuous streaming

This mode is for continuous recording of very long events.

The recording is started by a trigger event and continues until it is terminated by the user. The continuous streaming mode produces a large amount of data and is often combined with a data reduction method in the FPGA. This could be, for example, channel masking, DDC and decimation (option –FW4DDC), sample skip, or a custom algorithm implemented using the ADQ7 Development Kit



Data FIFO

Guarantees reliable data transfer.

There is 4 GBytes of on-board DRAM which is typically used as a large FIFO. The FIFO guarantees stable operation over a long time at high data rates. The large FIFO also enables bursts of triggers at high rate.

Data transfer

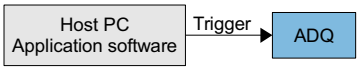
Optimized for high throughput.

ADQ7WB supports several electrical/mechanical interfaces to meet specific systems design requirements. The software methods for data transfer are unified to work the same for all formats. The API supports efficient multi-threaded handling of data buffers. There is example code for fast integration into the application.

ADQ7WB–FWDAQ also offers streaming peer-to-peer to a GPU.

Note that the multi-threading is for handling the data buffers only. The ADQ7WB set up and control has to be a single thread.

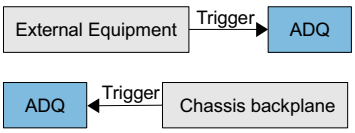
12 Trigger module



Software trigger

This is a user-controlled trigger.

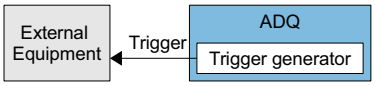
The software trigger is activated from the user's application software. It is used for building oscilloscope applications. The software trigger can also be used for a watch-dog application for surveillance of the experiment.



External trigger

This is for synchronizing the acquisition to an experiment.

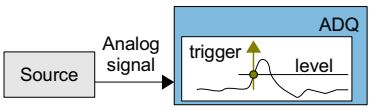
The external trigger is a signal from another unit that initiates the acquisition. External trigger inputs are available on the front panel and in the backplane in the PXIe form factor.



Internal trigger

This is an internally generated signal that can be used for triggering other devices.

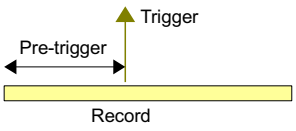
The internal trigger generates a programmable periodic signal that can be used for triggering the digitizer as well as external equipment. It allows the ADQ7WB to act as the timing master of a large system, eliminating the need for additional timing cards. The internal trigger is available to other equipment via a connector on the front panel.



Level trigger

This is a data-driven acquisition.

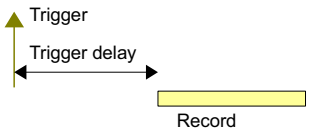
The level trigger reacts when the analog input goes above or below a programmable level. Level trigger is only available with –FWDAQ.



Pre-trigger buffer

Capture data before the trigger.

The pre-trigger buffer allows for capturing of data long before the trigger event occurred. This is useful for analyzing the cause of an event.

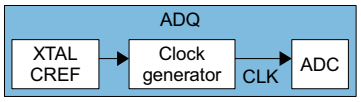


Trigger delay

Capture data long after the trigger event occured.

The trigger delay feature inserts a delay from the trigger event until data collection starts. It is used to reduce the amount of captured data when the interesting signal is known to occur a certain amount of time after the trigger event.

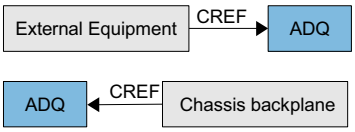
13 Clock module



Internal clock

High-precision clock for stand-alone operation.

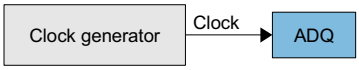
The ADQ7WB is clocked by an internal clock source. The clock reference is an internal high quality temperature compensated crystal oscillator.



External clock reference

This is for synchronizing the acquisition to an experiment.

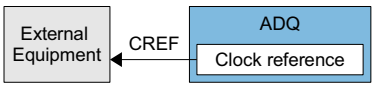
The internal clock generator is locked to an externally provided frequency reference. The frequency reference is provided via a connector on the front panel. The PXIe form factor can also receive the clock reference from the backplane.



External clock

When there is an external clock available.

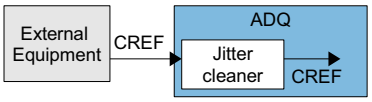
In this mode, the ADQ7WB is clocked directly with an external clock. The sampling frequency is twice the external clock frequency.



Clock reference output

This is for synchronizing the acquisition to an experiment.

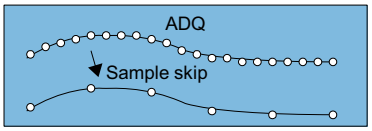
Using the clock reference output, the ADQ7WB can act as the clock reference source for the entire system. The clock reference output can also provide reference clock to another ADQ7WB so that they become synchronized. This function together with the trigger generator can eliminate the need for external timing cards.



Jitter cleaner PLL

For optimized performance with an external clock reference.

If an external clock reference of 10 MHz is used, the internal jitter cleaner will optimize performance.



Sample skip

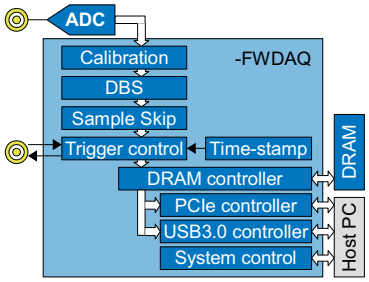
For adapting the sample rate to the situation and minimize the amount of data to be transferred.

The sample skip function can easily adjust the sample rate to limit the amount of data. The ADQ7WB can then adapt to changing situations.

Sample skip is available in –FWDAQ only. Use the decimation function in firmware –FW4DDC.

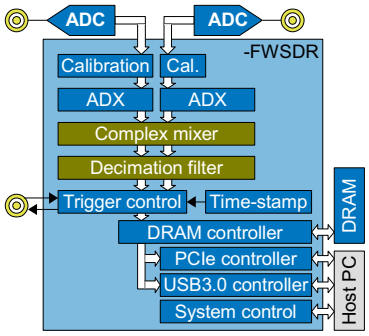
Sample skip cannot be combined with level trigger.

14 Firmware options



Data acquisition firmware (–FWDAQ)

This firmware is always included with the ADQ7WB. It supports the data acquisition modes triggered streaming and continuous streaming. The trigger modes external, internal, software and level trigger are supported as well as internal and external clock references.

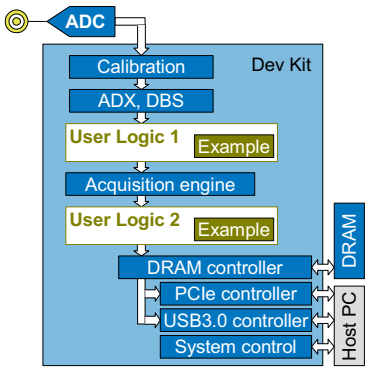


Digital Down Converter (–FW4DDC)

The –FW4DDC firmware option implements four Digital Down-Converters (DDC) for software defined radio support. Each DDC includes I and Q mixer and decimation. The four independent DDCs can be configured to operate on the two analog input streams and generate four separated digital radio channels. After decimation, the data rate is suitable for streaming to the host PC.

The ADX algorithm guarantees high dynamic performance in the interleaved architecture.

15 Feature enhancement options

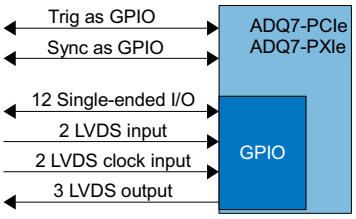


Building real-time custom signal processing firmware through the ADQ7 Development Kit

The ADQ7WB is equipped with a powerful FPGA which is partly available for customized real-time applications.

SP Devices' ADQ7 Development Kit is an optional FPGA design project that enables custom real-time signal processing of the raw data stream. More details about this product can be found in the datasheet for the ADQ Development Kit.

The ADQ7 Development Kit is available for firmware option –FWDAQ. The ADQ7 Development Kit is purchased separately.



General purpose I/O signals

In the standard ADQ7WB, the external trigger and sync signals can be used as general purpose I/O signals (GPIO).

The ADQ7WB–PXIE and ADQ7WB–PCIE have a GPIO connector with 12 single-ended and 7 differential signals as standard.

16 Form factors and data interfaces

Modular instrumentation with cPCIe / PXIe (–PXIE)

- Modular instrumentation

The cPCIe / PXIe form factor is intended for integration into a chassis for modular instrumentation or large scale acquisition. The ADQ7WB can operate in Compact PCI Express or PXI Express chassis. Using the multi-unit sync function, multi-channels systems can be achieved.

ADQ7WB support streaming of at least 5 GBytes/s for sending data to disk or additional computational cards over x8 Gen 3 cPCIe / PXIe backplanes.

In a PXI Express chassis, the clock reference from the backplane can be used as clock reference for the digitizer. Backplane trigger is also supported to simplify integration.

Note that the ADQ7WB occupy 2 slots and extend to the left of the connector.

Systems integration with PCIe interface (–PCIE)

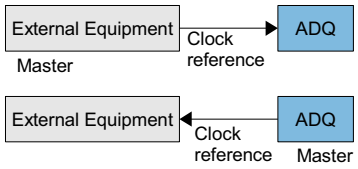
- All in one box
- High performance computing
- Cost effective hardware

The PCIe form factor is for integration into the host PC. The high speed PCIe interface can handle data rates up to 5 GBytes/s over x8 Gen 3 PCIe links. This is especially useful when combining the digitizer with heavy computation in, for example, a GPU in the same PC. The board is half length to enable compact solutions.

USB interface

The –PXIE and –PCIE form factors has a built-in USB3.0 interface. The connector is placed inside the box. This interface is a fully functional interface to the ADQ7WB. However, it is intended to be used for firmware update. This interface is independent of the firmware in the FPGA. If the firmware gets corrupt, for example when using the ADQ7 Development Kit, a new firmware can be uploaded via the USB port.

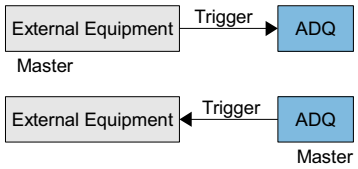
17 Synchronization support



Clock reference input and output

Sharing clock reference guarantees a common timebase.

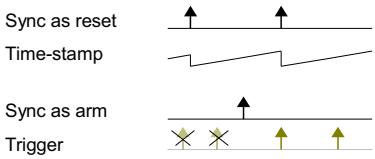
When outputting the internal clock reference the ADQ7WB ac as master. Use the clock reference input when the external equipment supply the clock reference.



Trigger input and output

The trigger starts the operation simultaneously.

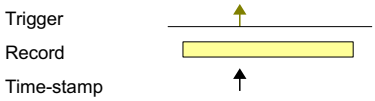
The trigger marks the start of an operation. The ADQ7WB can generate a trigger to start external equipment. It can also take a trigger as input to start the acquisition.



Synchronization input and output

Extra trigger to mark beginning of a sequence.

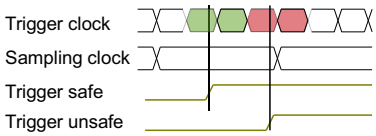
The sync pin can be used as an input for resetting the timestamp counter. It can also be used as an output for broadcasting an arm command to several ADQ7 units.



Time-stamp

A real-time value for each trigger.

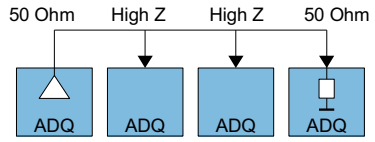
The time-stamp is a real-time value for each trigger event. The time-stamp allows precise analysis of the timing relationship of different acquisitions from the same or different ADQ7WB units.



Sub-sample precision time-stamp

High precision external trigger.

The external trigger timing precision is four times higher than the sampling time period for precise timing analysis. The subsample precision of the timestamp also allows for automatic analysis of trigger signal timing.

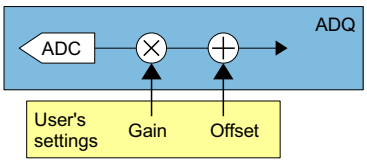


Bussed connection

Save cabling by bussed connections.

The sync, trig and clock reference can be set in high impedance mode to enable bussed connections.For best signal integrity, SMA tee adapters should be used at the high-impedance inputs to minimize the length of the unterminated stubs.

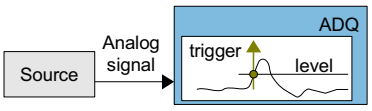
18 Built-in signal processing



Gain and offset calibration

Digital signal tuning in the FPGA.

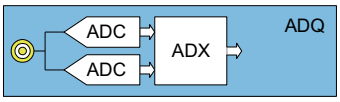
The user can set gain and offset parameters that are applied to the digitized signal immediately after the analog-to-digital converters. This can e.g. be useful to compensate for system offsets and simplify later signal processing in the host computer.



Level trigger

Data driven acquisition.

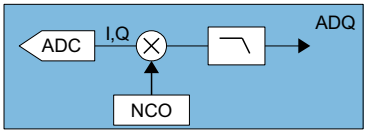
The standard firmware contains a level trigger for data driven acquisition. The level trigger is available in –FWDAQ.



ADX interleaving technology

Maximize spectral purity over a large bandwidth.

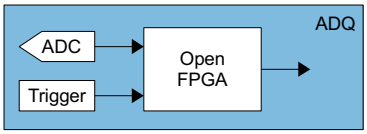
SP Devices' proprietary interleaving technology ADX is available in the firmware option –FW4DDC and in –FWDAQ. ADX dynamically suppresses interleaving artifacts to produce a pure spectrum.



DDC for SDR

Quadrature Mixer and decimation.

The firmware option –FW4DDC is a flexible software defined radio firmware that can operate in several different modes such as an IQ IF receiver or as a dual multi-channel receiver. The firmware incorporates numerically controlled oscillators, quadrature mixers and decimation blocks to extract the channels of interest.



Custom real-time processing

Efficient real-time algorithm implementation.

The ADQ7 Development Kit opens the FPGA for custom implementation of real-time algorithms. See **Section 15** for more information.

19 Appendix

19.1 Connectors

All connectors have some form of locking function to prevent cables from accidentally coming loose.

FUNCTION	CONNECTOR	PLACED	–PXIE	–PCIE	LOCK FUNCTION
Analog	SMA	Front panel	✓	✓	Screw
Trigger I/O	SMA	Front panel	✓	✓	Screw
Clock ref I/O	SMA	Front panel	✓	✓	Screw
Sync I/O	SMA	Front panel	✓	✓	Screw
Power	Board edge	Backplane	✓		Board attachment
Aux Power, **Section 19.4**	PCIe Aux	Internal		✓	Snap-lock
GPIO	HD-DSUB 44	Front panel	✓	✓	Screw
Firmware update USB3.0	Type mini-A	Inside	✓	✓	Friction
Data/control over PCIe	Board edge	Internal	✓	✓	Board attachment

19.2 GPIO

A cable for GPIO is available as a accessory, **Figure 10**. The pin map of GPIO is found in the ADQ7WB manual.

Figure 10: GPIO cable.

19.3 Host interface –PXIE

Note that the ADQ7WB–PXIE occupy 2 slots and extends to the left of the connector.

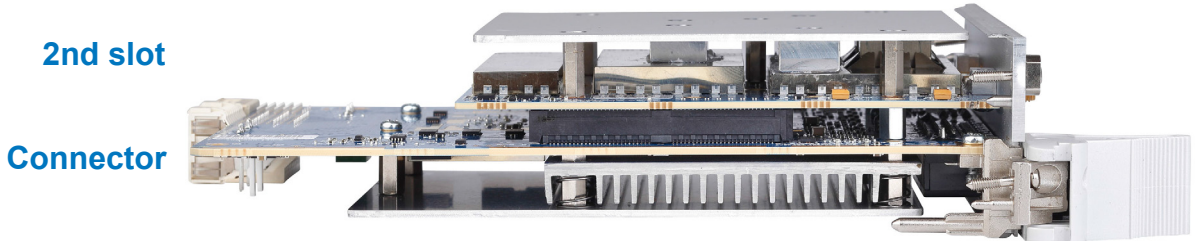


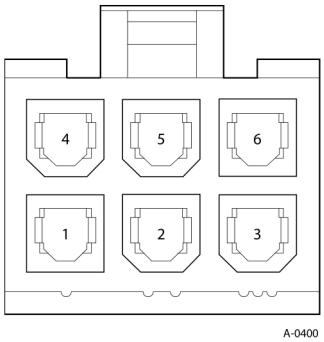
Figure 11: ADQ7WB–PXIE extends to the left of the connector. Bottom view with the handle to the right.

19.4 Host interface –PCIE

The ADQ7WB–PCIE is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary power supply connector, **Figure 13**. The connection in the cable should be as in **Figure 12**.

It is important that the auxiliary power supply is turned on immediately when the PC start. Otherwise, the digitizer will not be recognized on the PCI Express bus.

The ADQ7WB–PCIE requires two slots. Note that the second slot is placed on the solder side of the main slot, **Figure 14**.



(a) Cable connection

Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense
6	Ground

(b) Pin-out table

Figure 12: Power supply of –PCIE

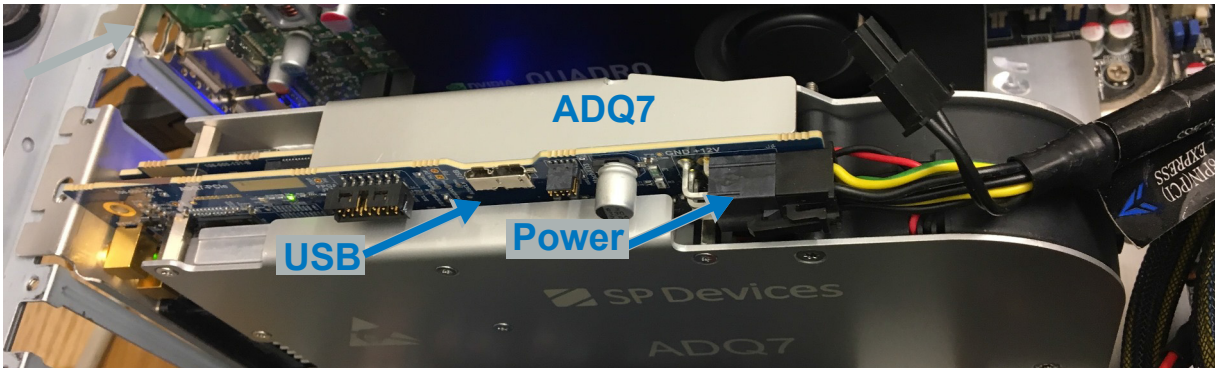


Figure 13: ADQ7WB installed in a PC. Note the power supply cable.

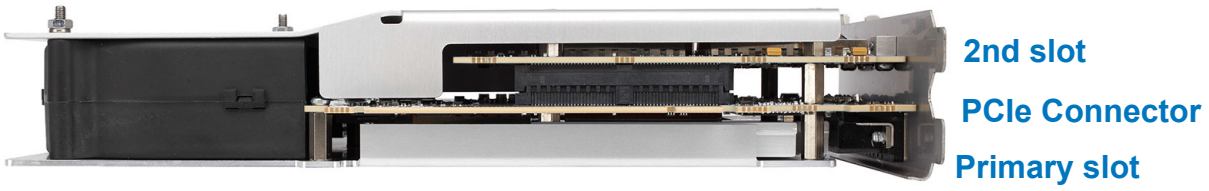


Figure 14: ADQ7WB–PCIE extends to the left of the connector.

Ordering information

ORDERING INFORMATION	
ADQ7WB DC-coupled	ADQ7WB
AVAILABLE OPTIONS	
Host PC interface	–PCIE, –PXIE,
Firmware options	–FWDAQ, –FW4DDC
RELATED PRODUCTS	
ADQ7 Development Kit for FWDAQ	–DEV7DAQ
GPIO cable 1m, 2 connectors	108-004-004

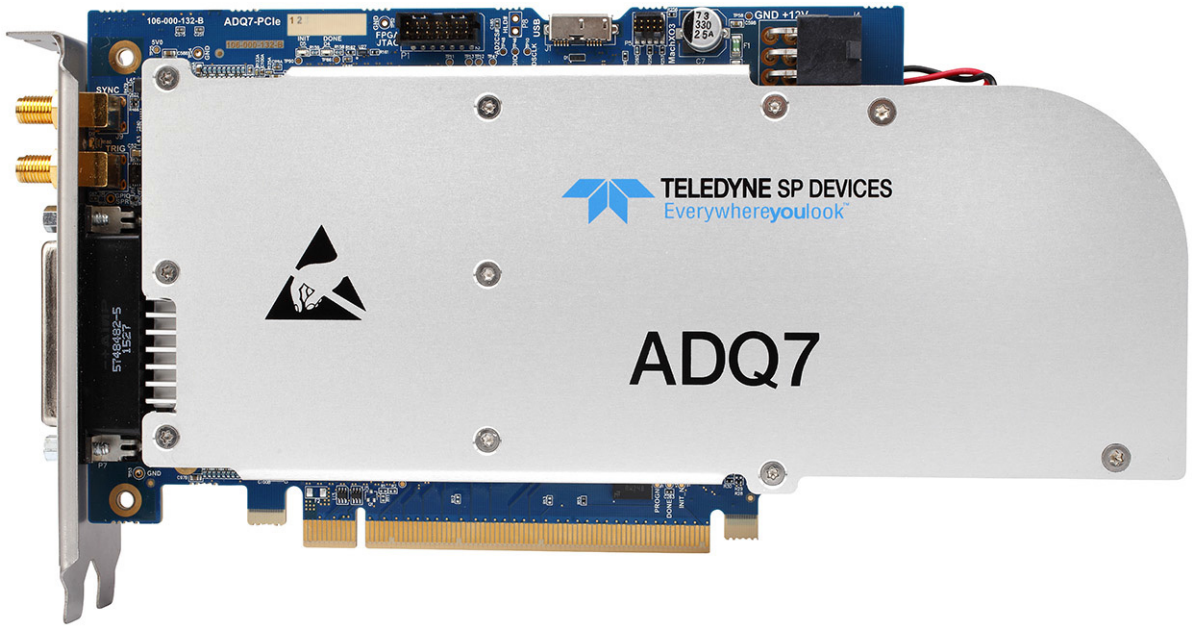
References

16-1795 ADQ7-FW4DDC datasheet

17-2043 ADQ7-FW4DDC user's guide

19-2233 ADQ7WB manual

14-1351 ADQAPI Reference Guide



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