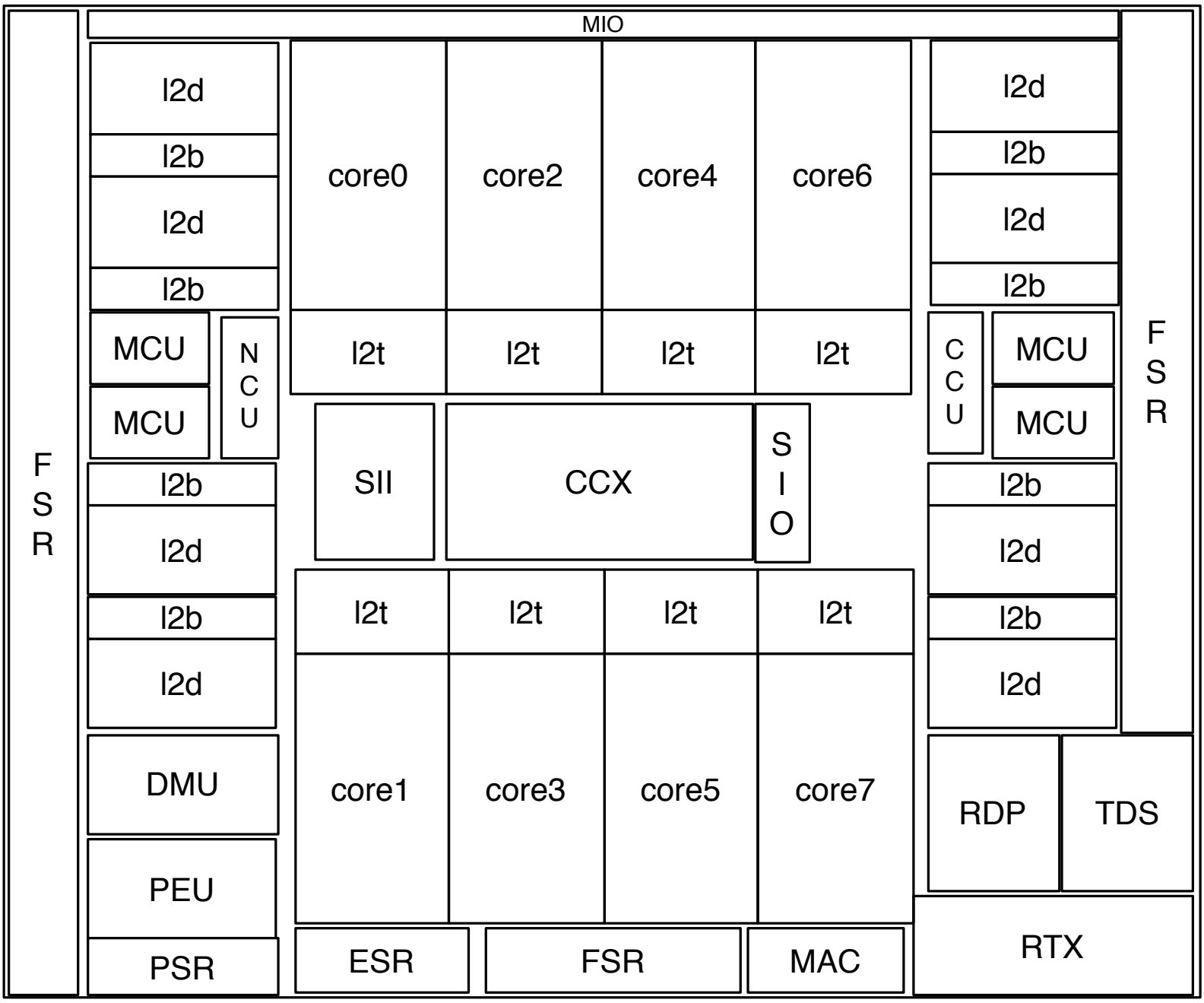
MIO
l2d
l2b
l2d
l2b
core0
core2
core4
core6
l2d
l2b
l2d
l2b
MCU
MCU
NCU
l2t
l2t
l2t
l2t
CCU
MCU
MCU
FSR
FSR
SII
CCX
SIO
l2b
l2d
l2b
l2d
l2t
l2t
l2t
l2t
l2b
l2d
DMU
core1
core3
core5
core7
RDP
TDS
PEU
PSR
ESR
FSR
MAC
RTX