Problems:

2-12 Early examples of CISC and RISC design are the VAX 11/780 and the IBM RS/6000, respectively. Using a typical benchmark program, the following machine characteristics result:

Processor	**Clock Frequency**	**Performance**	**CPU Time**
VAX 11/780	5 MHz	1 MIPS	12 *x* seconds
IBM RS/6000	25 MHz	18 MIPS	*x* seconds

a. What is the relative size of the instruction count of the machine code for this benchmark program running on the two machines?
b. What are the CPI values for the two machines?

Answer

- **MIPS** $= \frac{Ic}{T*10^6} \quad \longrightarrow \quad Ic = MIPS * T * 10^6$
  VAX machine $Ic1 = MIPS * T * 10^6 = 1 * 12x * 10^6$
  IBM machine $Ic2 = MIPS * T * 10^6 = 18 * x * 10^6$
  relative size of the instruction count = $\frac{Ic2}{Ic1} = \frac{18*x*10^6}{1*12x*10^6} = 1.5$
- **MIPS** $= \frac{f}{cpi * 10^6} \quad \longrightarrow \quad \text{cpi} = \frac{f}{\text{MIPS} * 10^6}$
  VAX machine CPI = $\frac{5 * 10^6}{1 * 10^6} = 5$
  IBM machine CPI = $\frac{25 * 10^6}{18 * 10^6} = 1.39$

2-16 consider the execution of a program which results in the execution of 2 million instructions on a 400-MHz processor. The program consists of four major types of instructions. The instruction mix and the CPI for each instruction type are given below based on the result of a program trace experiment:

Instruction Type	**CPI**	**Instruction Mix**
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

a. Determine the average CPI.
b. Determine the corresponding MIPS rate.

Answer

CPI $= 1 * 0.6 + 2 * 0.18 + 4 * 0.12 + 8 * 0.1 = 2.24$

MIPS $= \frac{f}{cpi * 10^6} = \frac{400 * 10^6}{2.24 * 10^6} = 178.57$

Now assume that the program can be executed in eight parallel tasks or threads with roughly equal number of instructions executed in each task. Execution is on an 8-core system with each core (processor) having the same performance as the single processor originally used. Coordination and synchronization between the parts adds an extra 25,000 instruction executions to each task. Assume the same instruction mix as in the example for each task, but increase the CPI for memory reference with cache miss to 12 cycles due to contention for memory.

a. Determine the average CPI.

b. Determine the corresponding MIPS rate.

c. Calculate the speedup factor.

Answer

Instruction Type	**CPI**	**Instruction Mix**
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	12	10%

- CPI $= 1 * 0.6 + 2 * 0.18 + 4 * 0.12 + 12 * 0.1 = 2.64$
- **MIPS** $= \frac{f}{cpi * 10^6} = \frac{400 * 10^6}{2.64 * 10^6} = 151.5151$
- T_old = Ic * cpi / f $= \frac{2 * 10^6 * 2.24}{400 * 10^6} = 11\ ms$
- T_new = Ic * cpi / f $= \frac{(\frac{2 * 10^6}{8} + 25000) * 2.64}{400 * 10^6} = 1.8$ ms
- Speedup $= \frac{\text{time to execute program on a single processor}}{\text{ime to execute program on } N \text{ parallel processors}} = \frac{11}{1.8} = 6.1$

Speedup of one enhancement

- **1 / (1 – F + F / S)**
- **F = fraction of the time the enhancement can be used**
- **S = the speedup of the enhancement itself (that is, how much faster the computer runs when the enhancement is in use)**

Example 1: an integer processor performs FP operations in software routines, a benchmark consists of 14% FP operations, a co-processor could perform all FP operations 4 times faster, if we add the co-processor, our speedup is

- **1 / (1 - .14 + .14 / 4) = 1.12, or a 12% speedup**

Example 2: Faster CPU (10 times faster on computation, 30% CPU operations, 70% I/O)

- **speedup = 1 / (1 - .3 + .3 / 10) = 1.37 (37% speedup)**

Example 3: More hard disk space that improves I/O performance by 2.5

- **speedup = 1 / (1 - .7 + .7 / 2.5) = 1.72 (72% speedup)**

Example 4: A benchmark has 20% FP square root operations, 50% total
FP operations, 50% other

- **Add an FP sqrt unit with a speedup of 10**
    - **speedup = 1 / (1 - .2 + .2 / 10) = 1.22**
- **Add a new FP ALU with a speedup of 1.6 for all FP ops**
    - **speedup = 1 / (1 - .5 + .5 / 1.6) = 1.23**