DATA SHEETNV3030B

240RGB x 320dot, 262,144-color
TFT Controller Driver with Internal RAM

Version 0.6

Jan. 10, 2022

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1. Introduction

NV3030B is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

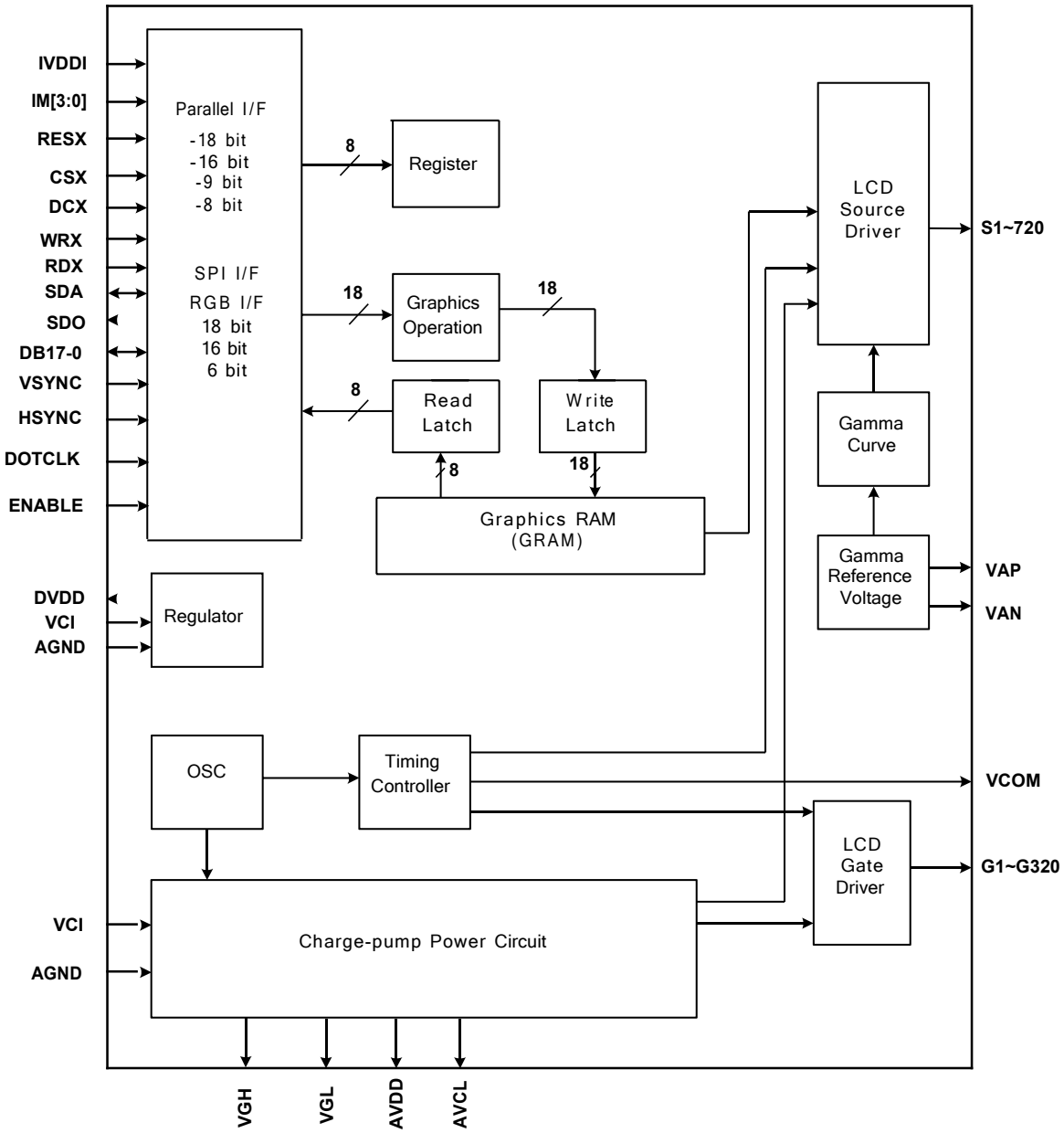
NV3030B supports 8-/9-/16-/18-bit data bus parallel interface, 6-/16-/18-bit data bus RGB interface and 3-/4-wire serial peripheral interface (SPI) and Quad serial peripheral interface (QSPI) . The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

NV3030B can operate with 1.65V ~ 3.6V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. NV3030B supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the NV3030B an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- One-chip controller driver for 240RGB x 320 dot graphics display in 262,144 colors on TFT panel
- One-chip solution for a-Si TFT panel
- System interface
  - 8-, 9-, 16-, 18-bit parallel ports
  - 3-/4-wire serial peripheral interface and 2 data lane SPI
  - Quad Serial Peripheral Interface
- Moving picture display interface
  - RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0) via 6-, 16-, 18-bit ports
- Window address function to specify a rectangular area in the internal RAM to write data
  - Writes data within a rectangular area on the internal RAM via moving picture interface
  - Reduces data transfer by specifying the area on the RAM to rewrite data
  - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
- Display Colors (Color Mode)
  - Full Color:262K, RGB=(666)max.,Idle Mode Off
  - Color Reduce: 8-color, RGB=(111),Idle Mode On
- Low–power consumption architecture (allowing direct input of interface I/O power supply)
  - 8-color display function
  - Input power supply voltages: VDDI = 1.65V ~ 3.6V(interface I/O power supply)
    VCI = 2.5V ~ 3.6 V (liquid crystal analog circuit power supply)
- Driving Algorithm
  - Dot Inversion
  - Column Inversion
- On-Chip Power System
  - Source Voltage (VAP to VAN): +6.4~ -4.6V
  - VCOM level: GND
  - Gate driver HIGH level (VGH to VSSA): +12.5V ~ +16V
  - Gate driver LOW level (VGL to VSSA): -12.5V ~ -9V
- Internal liquid crystal drive circuit: 720-channel source output and 320-channel gate output
- Internal oscillator, Hardware and software Reset
- TFT storage capacitor: Cst only
- Don’t need any external capacitor
- Optimized layout for COG Assembly

3. Block Diagram



4. Pin Function

4.1 Power Supply Pins

Signal	I/O	Connect to	Function
VDDI	I	I/O voltage	Low voltage power supply for interface logic circuits. (1.65~3.6V).
VCI	I	Analog Power	High voltage power supply for analog circuit blocks. Connect to an external power supply of 2.5V ~ 3.4V.
VSSD	I	Logic Ground	System ground level for logic blocks.
VSSA	I	Analog Ground	System ground level for analog circuit blocks. Connect to GND on the FPC to prevent noise.
VSP_EXT	O	-	Source driver power supply.
VSN_EXT	O	-	Source driver power supply.
VGH	O	-	Gate driver positive power supply.
VGL	O	-	Gate driver negative power supply.
VDD	O	-	Digital circuit power pad.
VAP	O	-	A power output of grayscale voltage generator.
VAN	O	-	A power output (Negative) of grayscale voltage generator.
VCMP	O	-	A power output of grayscale voltage generator.
VDDS_EXT	O	-	Source driver power supply.

4.2 Interface Logic Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>
Select the system interface mode.
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">interface Mode</th><th colspan="2">DB pins</th></tr>
<tr><th>Register</th><th>Gram</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>i80-system
8-bit interface I</td><td>DB[7:0]</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>i80-system
16-bit interface I</td><td>DB[7:0]</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>i80-system
9-bit interface I</td><td>DB[7:0]</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>i80-system
18-bit interface I</td><td>DB[7:0]</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>qspi</td><td colspan="2">SDA : in/out
WRX : in
DB[0] : in DB[1] : in
SDO ： out</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-wire 9-bit data
Serial interface I</td><td colspan="2" rowspan="2">SDA : in/out
WRX : in
SDO ： out</td></tr>
<tr><td>2 data lane serial
interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data
Serial interface I</td><td colspan="2">SDA: in/out</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>i80-system
16-bit interface
II</td><td>DB[8:1]</td><td>DB[8:1],
DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>i80-system
8-bit interface II</td><td>DB[17:10]</td><td>DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>i80-system
18-bit interface
II</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>i80-system
9-bit interface II</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data
Serial interface
II</td><td colspan="2">SDA:in/out
SDO ： out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data
Serial interface
II</td><td colspan="2">SDA : in/out
SDO ： out</td></tr>
</table>
If pad not used, please fix this pin to VDDI or VSSD level.
</td></tr>
</table>

RESX	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
CSX	I	A chip select signal. Low: the NV3030B is selected and accessible. High: the NV3030B is not selected and not accessible.
DCX	I	This pin is used to select “Data or Command” in the parallel interface. When DCX = ’1’, data is selected. When DCX = ’0’, command is selected. This pin is used serial interface clock. If not used, this pin should be connected to VDDI or VSSD.
WRX	I	A write strobe signal and enables an operation to write data when the signal is low. Fix to either VDDI or VSSD level when not in use. SPI 4-wire system: Serves as command or parameter select. 2 data lane serial interface: the second data lane. QSPI interface: the second data pin
RDX	I	A read strobe signal and enables an operation to read out data when the signal is low. Fix to VDDI level in parallel I/F when not in use. And fix to either VDDI or VSSD level in other I/F when not in use.
SDA	I/O	When serial I/F I: it is SPI interface input/output pin. When serial I/F Ⅱ: it is SPI interface input pin. The data is latched on the rising edge of the serial interface clock signal. If not used, please fix this pin at VDDI or VSSD level.
SDO	O	SPI interface output pin. The data is outputted on the falling edge of the serial interface clock signal. If not used, open this pin.
TE	O	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	Pixel clock signal in RGB I/F mode. If not used, fix this pin at VDDI or VSSD.
VSYNC	I	Vertical sync. Signal in RGB I/F mode. If not used, fix this pin at VDDI or VSSD.
HSYNC	I	Horizontal sync. Signal in RGB I/F mode. If not used, fix this pin at VDDI or VSSD.
ENABLE	I	Data enable signal in RGB I/F mode. If not used, fix this pin at VDDI or VSSD.
DB17-DB0	I/O	18-bit parallel bi-directional data bus for system interface and RGB interface mode. DB[0]:the third pin of qspi ; DB[1]:the fourth pin of qspi If not used, fix this pin at VDDI or VSSD.

OSC_SW	I	Input pin only for test.
MEC_BPS	I	Input pin only for test.

4.3 Driver Output Pins

Signal	I/O	Function
S1 to S720	O	Source driver output pads.
G1 to G320	O	Gate driver output pads.
VCOM	O	A power supply for the TFT-LCD common electrode.

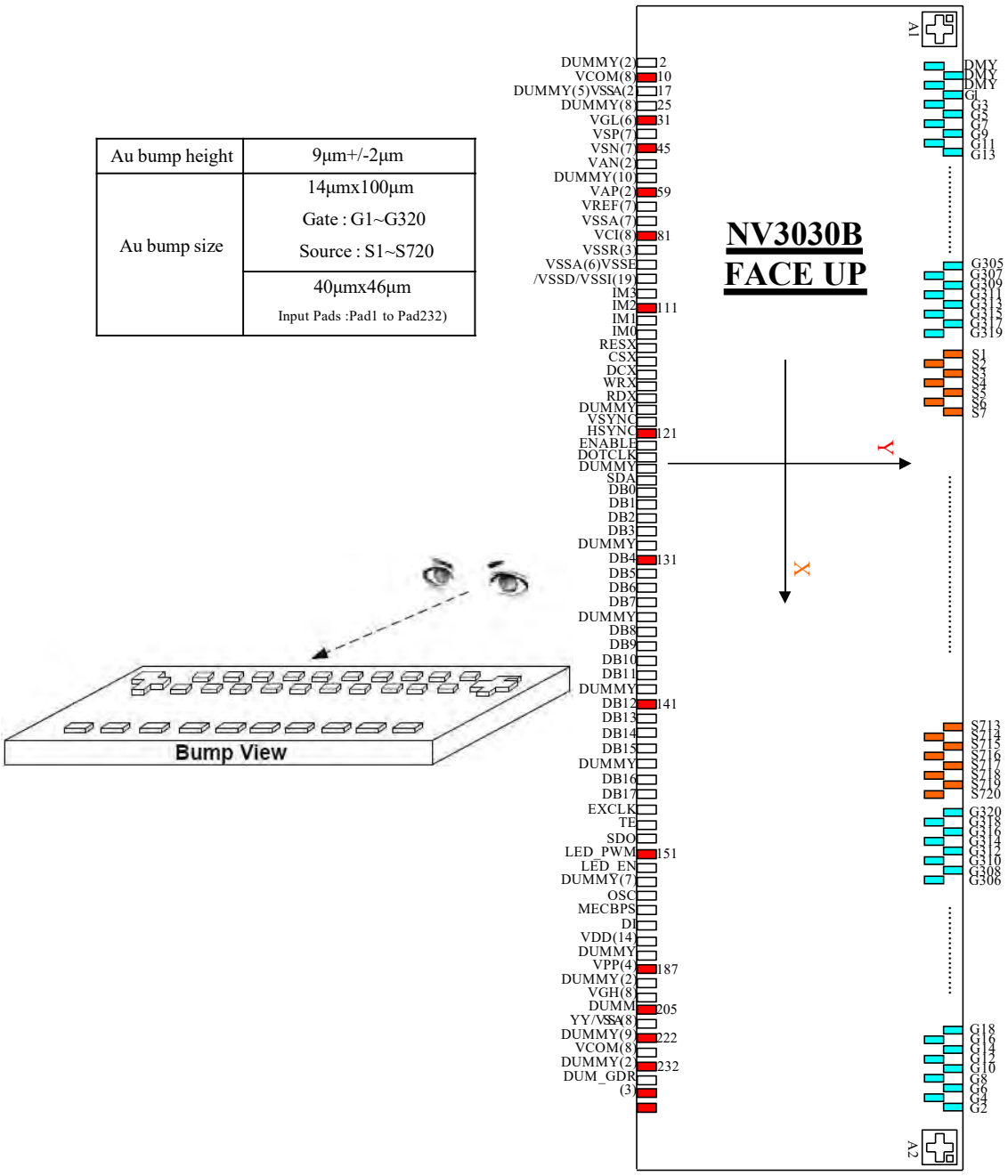
4.4 Test and other pins

Name	I/O	Description
VPP	I	OTP programming power.
BGOUT_TEST/ I_TEST/ VREF_TEST/ OSC_TESTOUT	O	Output pins for testing. Please keep these pins floating.
EXCLK	-	Dummy pin.Leave these pads open.
DMY_GDR/ DMY_GDL	-	These pins are dummy (no electrical characteristic) Can pass signal through these pads on TFT panel. Please open these pins.

5. Pad Arrangement

5.1 Output Bump Dimension

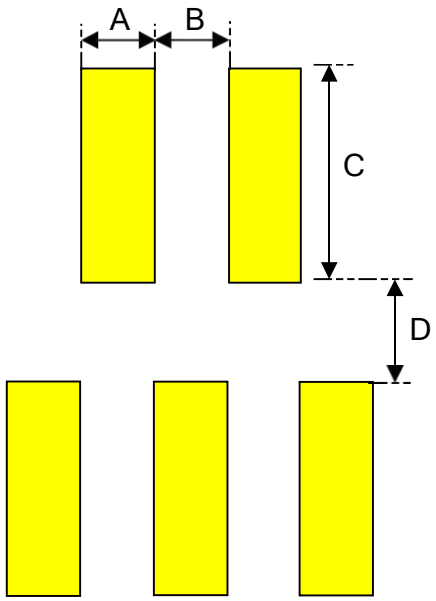
Au bump height	9μm+/-2μm
Au bump size	14μmx100μm Gate : G1~G320 Source : S1~S720
	40μmx46μm Input Pads :Pad1 to Pad232)



5.2 Input Bump Dimension

✧ **Output Pads**S1~S720、G1~G320、VCOM

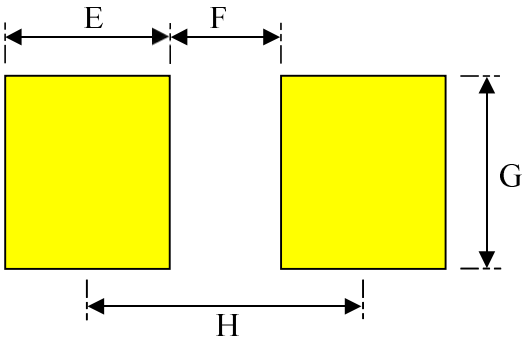
(No.233~1278)



Symbol	Item	Size
A	Bump Width	14um
B	Bump Gap 1 (Horizontal)	14um
C	Bump Height	100um
D	Bump Gap 2 (Vertical)	31um

✧ **Input Pads**

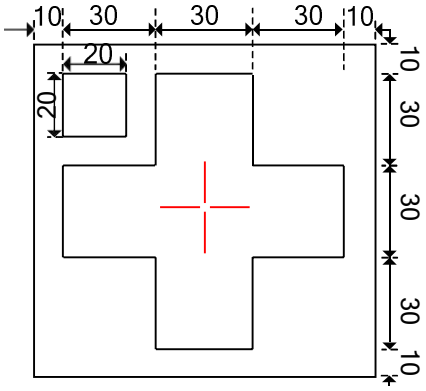
No.1~232



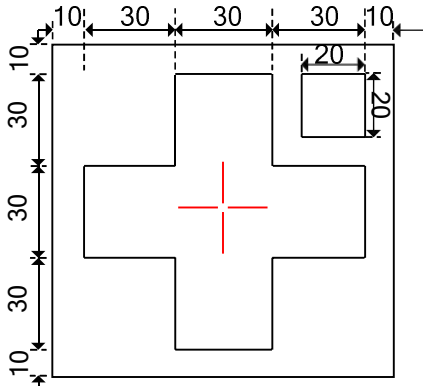
Symbol	Item	Size
E	Bump Width	40 um
F	Bump Gap	20,32.5,45 um
G	Bump Height	46 um
H	Bump Pitch	60,72.5,85 um

5.3 Alignment Mark Dimension

✧ Alignment Mark：A1(X,Y)=(-7480,233.5)



✧ Alignment Mark：A2(X,Y)=(7480,233.5)



5.4 Chip Information

Chip size	15360um x 665um
Chip thickness	250um
Pad Location	Pad center
Coordinate Origin	(-40,0)

6 PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	DUMMY	-7292.5	-259.5	38	VSP	-5072.5	-259.5
2	DUMMY	-7232.5	-259.5	39	VSN	-5012.5	-259.5
3	VCOM	-7172.5	-259.5	40	VSN	-4952.5	-259.5
4	VCOM	-7112.5	-259.5	41	VSN	-4892.5	-259.5
5	VCOM	-7052.5	-259.5	42	VSN	-4832.5	-259.5
6	VCOM	-6992.5	-259.5	43	VSN	-4772.5	-259.5
7	VCOM	-6932.5	-259.5	44	VSN	-4712.5	-259.5
8	VCOM	-6872.5	-259.5	45	VSN	-4652.5	-259.5
9	VCOM	-6812.5	-259.5	46	VAN	-4592.5	-259.5
10	VCOM	-6752.5	-259.5	47	VAN	-4532.5	-259.5
11	DUMMY	-6692.5	-259.5	48	DUMMY	-4472.5	-259.5
12	DUMMY	-6632.5	-259.5	49	DUMMY	-4412.5	-259.5
13	DUMMY	-6572.5	-259.5	50	DUMMY	-4352.5	-259.5
14	DUMMY	-6512.5	-259.5	51	DUMMY	-4292.5	-259.5
15	DUMMY	-6452.5	-259.5	52	DUMMY	-4232.5	-259.5
16	VSSA	-6392.5	-259.5	53	DUMMY	-4172.5	-259.5
17	VSSA	-6332.5	-259.5	54	DUMMY	-4112.5	-259.5
18	DUMMY	-6272.5	-259.5	55	DUMMY	-4052.5	-259.5
19	DUMMY	-6212.5	-259.5	56	DUMMY	-3992.5	-259.5
20	DUMMY	-6152.5	-259.5	57	DUMMY	-3932.5	-259.5
21	DUMMY	-6092.5	-259.5	58	VAP	-3872.5	-259.5
22	DUMMY	-6032.5	-259.5	59	VAP	-3812.5	-259.5
23	DUMMY	-5972.5	-259.5	60	VREF_TEST	-3752.5	-259.5
24	DUMMY	-5912.5	-259.5	61	VREF_TEST	-3692.5	-259.5
25	DUMMY	-5852.5	-259.5	62	VREF_TEST	-3632.5	-259.5
26	VGL	-5792.5	-259.5	63	VREF_TEST	-3572.5	-259.5
27	VGL	-5732.5	-259.5	64	VREF_TEST	-3512.5	-259.5
28	VGL	-5672.5	-259.5	65	VREF_TEST	-3452.5	-259.5
29	VGL	-5612.5	-259.5	66	VREF_TEST	-3392.5	-259.5
30	VGL	-5552.5	-259.5	67	VSSA	-3332.5	-259.5
31	VGL	-5492.5	-259.5	68	VSSA	-3272.5	-259.5
32	VSP	-5432.5	-259.5	69	VSSA	-3212.5	-259.5
33	VSP	-5372.5	-259.5	70	VSSA	-3152.5	-259.5
34	VSP	-5312.5	-259.5	71	VSSA	-3092.5	-259.5
35	VSP	-5252.5	-259.5	72	VSSA	-3032.5	-259.5
36	VSP	-5192.5	-259.5	73	VSSA	-2972.5	-259.5
37	VSP	-5132.5	-259.5	74	VCI	-2912.5	-259.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
75	VCI	-2852.5	-259.5	116	DCX	-392.5	-259.5
76	VCI	-2792.5	-259.5	117	WRX	-332.5	-259.5
77	VCI	-2732.5	-259.5	118	RDX	-272.5	-259.5
78	VCI	-2672.5	-259.5	119	DUMMY	-212.5	-259.5
79	VCI	-2612.5	-259.5	120	VSYNC	-152.5	-259.5
80	VCI	-2552.5	-259.5	121	HSYNC	-92.5	-259.5
81	VCI	-2492.5	-259.5	122	ENABLE	-32.5	-259.5
82	VSSR	-2432.5	-259.5	123	DOTCLK	27.5	-259.5
83	VSSR	-2372.5	-259.5	124	DMY<2>	87.5	-259.5
84	VSSR	-2312.5	-259.5	125	SDA	160	-259.5
85	VSSA	-2252.5	-259.5	126	DB<0>	245	-259.5
86	VSSA	-2192.5	-259.5	127	DB<1>	330	-259.5
87	VSSA	-2132.5	-259.5	128	DB<2>	415	-259.5
88	VSSA	-2072.5	-259.5	129	DB<3>	500	-259.5
89	VSSA	-2012.5	-259.5	130	DUMMY	572.5	-259.5
90	VSSA	-1952.5	-259.5	131	DB<4>	645	-259.5
91	VSSE	-1892.5	-259.5	132	DB<5>	730	-259.5
92	VSSE	-1832.5	-259.5	133	DB<6>	815	-259.5
93	VSSE	-1772.5	-259.5	134	DB<7>	900	-259.5
94	VSSE	-1712.5	-259.5	135	DMY<3>	972.5	-259.5
95	VSSE	-1652.5	-259.5	136	DB<8>	1045	-259.5
96	VSSE	-1592.5	-259.5	137	DB<9>	1130	-259.5
97	VSSE	-1532.5	-259.5	138	DB<10>	1215	-259.5
98	VSSD	-1472.5	-259.5	139	DB<11>	1300	-259.5
99	VSSD	-1412.5	-259.5	140	DMY<4>	1372.5	-259.5
100	VSSD	-1352.5	-259.5	141	DB<12>	1445	-259.5
101	VSSD	-1292.5	-259.5	142	DB<13>	1530	-259.5
102	VSSD	-1232.5	-259.5	143	DB<14>	1615	-259.5
103	VSSD	-1172.5	-259.5	144	DB<15>	1700	-259.5
104	VSSI	-1112.5	-259.5	145	DMY<5>	1772.5	-259.5
105	VSSI	-1052.5	-259.5	146	DB<16>	1845	-259.5
106	I_TEST	-992.5	-259.5	147	DB<17>	1930	-259.5
107	DMY<0>	-932.5	-259.5	148	EXCLK	2002.5	-259.5
108	DMY<1>	-872.5	-259.5	149	TE	2075	-259.5
109	OSC_TESTOUT	-812.5	-259.5	150	SDO	2160	-259.5
110	IM<3>	-752.5	-259.5	151	LED_PWM	2245	-259.5
111	IM<2>	-692.5	-259.5	152	LED_EN	2330	-259.5
112	IM<1>	-632.5	-259.5	153	DUMMY	2402.5	-259.5
113	IM<0>	-572.5	-259.5	154	DUMMY	2462.5	-259.5
114	RESX	-512.5	-259.5	155	DUMMY	2535	-259.5
115	CSX	-452.5	-259.5	156	DUMMY	2620	-259.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
157	DUMMY	2705	-259.5	201	DUMMY	5432.5	-259.5
158	DUMMY	2790	-259.5	202	DUMMY	5492.5	-259.5
159	DUMMY	2875	-259.5	203	DUMMY	5552.5	-259.5
160	OSC_SW	2960	-259.5	204	DUMMY	5612.5	-259.5
161	MEC_BPS	3032.5	-259.5	205	DUMMY	5672.5	-259.5
162	VDDI	3092.5	-259.5	206	VSSA	5732.5	-259.5
163	VDDI	3152.5	-259.5	207	VSSA	5792.5	-259.5
164	VDDI	3212.5	-259.5	208	VSSA	5852.5	-259.5
165	VDDI	3272.5	-259.5	209	VSSA	5912.5	-259.5
166	VDDI	3332.5	-259.5	210	VSSA	5972.5	-259.5
167	VDDI	3392.5	-259.5	211	VSSA	6032.5	-259.5
168	VDDI	3452.5	-259.5	212	VSSA	6092.5	-259.5
169	VDD	3512.5	-259.5	213	VSSA	6152.5	-259.5
170	VDD	3572.5	-259.5	214	DUMMY	6212.5	-259.5
171	VDD	3632.5	-259.5	215	DUMMY	6272.5	-259.5
172	VDD	3692.5	-259.5	216	DUMMY	6332.5	-259.5
173	VDD	3752.5	-259.5	217	DUMMY	6392.5	-259.5
174	VDD	3812.5	-259.5	218	DUMMY	6452.5	-259.5
175	VDD	3872.5	-259.5	219	DUMMY	6512.5	-259.5
176	VDD	3932.5	-259.5	220	DUMMY	6572.5	-259.5
177	VDD	3992.5	-259.5	221	DUMMY	6632.5	-259.5
178	VDD	4052.5	-259.5	222	DUMMY	6692.5	-259.5
179	VDD	4112.5	-259.5	223	VCOM	6752.5	-259.5
180	VDD	4172.5	-259.5	224	VCOM	6812.5	-259.5
181	VDD	4232.5	-259.5	225	VCOM	6872.5	-259.5
182	VDD	4292.5	-259.5	226	VCOM	6932.5	-259.5
183	DUMMY	4352.5	-259.5	227	VCOM	6992.5	-259.5
184	VPP	4412.5	-259.5	228	VCOM	7052.5	-259.5
185	VPP	4472.5	-259.5	229	VCOM	7112.5	-259.5
186	VPP	4532.5	-259.5	230	VCOM	7172.5	-259.5
187	VPP	4592.5	-259.5	231	DUMMY	7232.5	-259.5
188	DUMMY	4652.5	-259.5	232	DUMMY	7292.5	-259.5
189	DUMMY	4712.5	-259.5	233	DMY_GDR	7399	232.5
190	VGH	4772.5	-259.5	234	DMY_GDR	7385	101.5
191	VGH	4832.5	-259.5	235	DMY_GDR	7371	232.5
192	VGH	4892.5	-259.5	236	G<2>	7357	101.5
193	VGH	4952.5	-259.5	237	G<4>	7343	232.5
194	VGH	5012.5	-259.5	238	G<6>	7329	101.5
195	VGH	5072.5	-259.5	239	G<8>	7315	232.5
196	VGH	5132.5	-259.5	240	G<10>	7301	101.5
197	VGH	5192.5	-259.5	241	G<12>	7287	232.5
198	DUMMY	5252.5	-259.5	242	G<14>	7273	101.5
199	DUMMY	5312.5	-259.5	243	G<16>	7259	232.5
200	DUMMY	5372.5	-259.5	244	G<18>	7245	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
245	G<20>	7231	232.5	289	G<108>	6615	232.5
246	G<22>	7217	101.5	290	G<110>	6601	101.5
247	G<24>	7203	232.5	291	G<112>	6587	232.5
248	G<26>	7189	101.5	292	G<114>	6573	101.5
249	G<28>	7175	232.5	293	G<116>	6559	232.5
250	G<30>	7161	101.5	294	G<118>	6545	101.5
251	G<32>	7147	232.5	295	G<120>	6531	232.5
252	G<34>	7133	101.5	296	G<122>	6517	101.5
253	G<36>	7119	232.5	297	G<124>	6503	232.5
254	G<38>	7105	101.5	298	G<126>	6489	101.5
255	G<40>	7091	232.5	299	G<128>	6475	232.5
256	G<42>	7077	101.5	300	G<130>	6461	101.5
257	G<44>	7063	232.5	301	G<132>	6447	232.5
258	G<46>	7049	101.5	302	G<134>	6433	101.5
259	G<48>	7035	232.5	303	G<136>	6419	232.5
260	G<50>	7021	101.5	304	G<138>	6405	101.5
261	G<52>	7007	232.5	305	G<140>	6391	232.5
262	G<54>	6993	101.5	306	G<142>	6377	101.5
263	G<56>	6979	232.5	307	G<144>	6363	232.5
264	G<58>	6965	101.5	308	G<146>	6349	101.5
265	G<60>	6951	232.5	309	G<148>	6335	232.5
266	G<62>	6937	101.5	310	G<150>	6321	101.5
267	G<64>	6923	232.5	311	G<152>	6307	232.5
268	G<66>	6909	101.5	312	G<154>	6293	101.5
269	G<68>	6895	232.5	313	G<156>	6279	232.5
270	G<70>	6881	101.5	314	G<158>	6265	101.5
271	G<72>	6867	232.5	315	G<160>	6251	232.5
272	G<74>	6853	101.5	316	G<162>	6237	101.5
273	G<76>	6839	232.5	317	G<164>	6223	232.5
274	G<78>	6825	101.5	318	G<166>	6209	101.5
275	G<80>	6811	232.5	319	G<168>	6195	232.5
276	G<82>	6797	101.5	320	G<170>	6181	101.5
277	G<84>	6783	232.5	321	G<172>	6167	232.5
278	G<86>	6769	101.5	322	G<174>	6153	101.5
279	G<88>	6755	232.5	323	G<176>	6139	232.5
280	G<90>	6741	101.5	324	G<178>	6125	101.5
281	G<92>	6727	232.5	325	G<180>	6111	232.5
282	G<94>	6713	101.5	326	G<182>	6097	101.5
283	G<96>	6699	232.5	327	G<184>	6083	232.5
284	G<98>	6685	101.5	328	G<186>	6069	101.5
285	G<100>	6671	232.5	329	G<188>	6055	232.5
286	G<102>	6657	101.5	330	G<190>	6041	101.5
287	G<104>	6643	232.5	331	G<192>	6027	232.5
288	G<106>	6629	101.5	332	G<194>	6013	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
333	G<196>	5999	232.5	377	G<284>	5383	232.5
334	G<198>	5985	101.5	378	G<286>	5369	101.5
335	G<200>	5971	232.5	379	G<288>	5355	232.5
336	G<202>	5957	101.5	380	G<290>	5341	101.5
337	G<204>	5943	232.5	381	G<292>	5327	232.5
338	G<206>	5929	101.5	382	G<294>	5313	101.5
339	G<208>	5915	232.5	383	G<296>	5299	232.5
340	G<210>	5901	101.5	384	G<298>	5285	101.5
341	G<212>	5887	232.5	385	G<300>	5271	232.5
342	G<214>	5873	101.5	386	G<302>	5257	101.5
343	G<216>	5859	232.5	387	G<304>	5243	232.5
344	G<218>	5845	101.5	388	G<306>	5229	101.5
345	G<220>	5831	232.5	389	G<308>	5215	232.5
346	G<222>	5817	101.5	390	G<310>	5201	101.5
347	G<224>	5803	232.5	391	G<312>	5187	232.5
348	G<226>	5789	101.5	392	G<314>	5173	101.5
349	G<228>	5775	232.5	393	G<316>	5159	232.5
350	G<230>	5761	101.5	394	G<318>	5145	101.5
351	G<232>	5747	232.5	395	G<320>	5131	232.5
352	G<234>	5733	101.5	396	S<720>	5075	101.5
353	G<236>	5719	232.5	397	S<719>	5061	232.5
354	G<238>	5705	101.5	398	S<718>	5047	101.5
355	G<240>	5691	232.5	399	S<717>	5033	232.5
356	G<242>	5677	101.5	400	S<716>	5019	101.5
357	G<244>	5663	232.5	401	S<715>	5005	232.5
358	G<246>	5649	101.5	402	S<714>	4991	101.5
359	G<248>	5635	232.5	403	S<713>	4977	232.5
360	G<250>	5621	101.5	404	S<712>	4963	101.5
361	G<252>	5607	232.5	405	S<711>	4949	232.5
362	G<254>	5593	101.5	406	S<710>	4935	101.5
363	G<256>	5579	232.5	407	S<709>	4921	232.5
364	G<258>	5565	101.5	408	S<708>	4907	101.5
365	G<260>	5551	232.5	409	S<707>	4893	232.5
366	G<262>	5537	101.5	410	S<706>	4879	101.5
367	G<264>	5523	232.5	411	S<705>	4865	232.5
368	G<266>	5509	101.5	412	S<704>	4851	101.5
369	G<268>	5495	232.5	413	S<703>	4837	232.5
370	G<270>	5481	101.5	414	S<702>	4823	101.5
371	G<272>	5467	232.5	415	S<701>	4809	232.5
372	G<274>	5453	101.5	416	S<700>	4795	101.5
373	G<276>	5439	232.5	417	S<699>	4781	232.5
374	G<278>	5425	101.5	418	S<698>	4767	101.5
375	G<280>	5411	232.5	419	S<697>	4753	232.5
376	G<282>	5397	101.5	420	S<696>	4739	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
421	S<695>	4725	232.5	465	S<651>	4109	232.5
422	S<694>	4711	101.5	466	S<650>	4095	101.5
423	S<693>	4697	232.5	467	S<649>	4081	232.5
424	S<692>	4683	101.5	468	S<648>	4067	101.5
425	S<691>	4669	232.5	469	S<647>	4053	232.5
426	S<690>	4655	101.5	470	S<646>	4039	101.5
427	S<689>	4641	232.5	471	S<645>	4025	232.5
428	S<688>	4627	101.5	472	S<644>	4011	101.5
429	S<687>	4613	232.5	473	S<643>	3997	232.5
430	S<686>	4599	101.5	474	S<642>	3983	101.5
431	S<685>	4585	232.5	475	S<641>	3969	232.5
432	S<684>	4571	101.5	476	S<640>	3955	101.5
433	S<683>	4557	232.5	477	S<639>	3941	232.5
434	S<682>	4543	101.5	478	S<638>	3927	101.5
435	S<681>	4529	232.5	479	S<637>	3913	232.5
436	S<680>	4515	101.5	480	S<636>	3899	101.5
437	S<679>	4501	232.5	481	S<635>	3885	232.5
438	S<678>	4487	101.5	482	S<634>	3871	101.5
439	S<677>	4473	232.5	483	S<633>	3857	232.5
440	S<676>	4459	101.5	484	S<632>	3843	101.5
441	S<675>	4445	232.5	485	S<631>	3829	232.5
442	S<674>	4431	101.5	486	S<630>	3815	101.5
443	S<673>	4417	232.5	487	S<629>	3801	232.5
444	S<672>	4403	101.5	488	S<628>	3787	101.5
445	S<671>	4389	232.5	489	S<627>	3773	232.5
446	S<670>	4375	101.5	490	S<626>	3759	101.5
447	S<669>	4361	232.5	491	S<625>	3745	232.5
448	S<668>	4347	101.5	492	S<624>	3731	101.5
449	S<667>	4333	232.5	493	S<623>	3717	232.5
450	S<666>	4319	101.5	494	S<622>	3703	101.5
451	S<665>	4305	232.5	495	S<621>	3689	232.5
452	S<664>	4291	101.5	496	S<620>	3675	101.5
453	S<663>	4277	232.5	497	S<619>	3661	232.5
454	S<662>	4263	101.5	498	S<618>	3647	101.5
455	S<661>	4249	232.5	499	S<617>	3633	232.5
456	S<660>	4235	101.5	500	S<616>	3619	101.5
457	S<659>	4221	232.5	501	S<615>	3605	232.5
458	S<658>	4207	101.5	502	S<614>	3591	101.5
459	S<657>	4193	232.5	503	S<613>	3577	232.5
460	S<656>	4179	101.5	504	S<612>	3563	101.5
461	S<655>	4165	232.5	505	S<611>	3549	232.5
462	S<654>	4151	101.5	506	S<610>	3535	101.5
463	S<653>	4137	232.5	507	S<609>	3521	232.5
464	S<652>	4123	101.5	508	S<608>	3507	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
509	S<607>	3493	232.5	553	S<563>	2877	232.5
510	S<606>	3479	101.5	554	S<562>	2863	101.5
511	S<605>	3465	232.5	555	S<561>	2849	232.5
512	S<604>	3451	101.5	556	S<560>	2835	101.5
513	S<603>	3437	232.5	557	S<559>	2821	232.5
514	S<602>	3423	101.5	558	S<558>	2807	101.5
515	S<601>	3409	232.5	559	S<557>	2793	232.5
516	S<600>	3395	101.5	560	S<556>	2779	101.5
517	S<599>	3381	232.5	561	S<555>	2765	232.5
518	S<598>	3367	101.5	562	S<554>	2751	101.5
519	S<597>	3353	232.5	563	S<553>	2737	232.5
520	S<596>	3339	101.5	564	S<552>	2723	101.5
521	S<595>	3325	232.5	565	S<551>	2709	232.5
522	S<594>	3311	101.5	566	S<550>	2695	101.5
523	S<593>	3297	232.5	567	S<549>	2681	232.5
524	S<592>	3283	101.5	568	S<548>	2667	101.5
525	S<591>	3269	232.5	569	S<547>	2653	232.5
526	S<590>	3255	101.5	570	S<546>	2639	101.5
527	S<589>	3241	232.5	571	S<545>	2625	232.5
528	S<588>	3227	101.5	572	S<544>	2611	101.5
529	S<587>	3213	232.5	573	S<543>	2597	232.5
530	S<586>	3199	101.5	574	S<542>	2583	101.5
531	S<585>	3185	232.5	575	S<541>	2569	232.5
532	S<584>	3171	101.5	576	S<540>	2555	101.5
533	S<583>	3157	232.5	577	S<539>	2541	232.5
534	S<582>	3143	101.5	578	S<538>	2527	101.5
535	S<581>	3129	232.5	579	S<537>	2513	232.5
536	S<580>	3115	101.5	580	S<536>	2499	101.5
537	S<579>	3101	232.5	581	S<535>	2485	232.5
538	S<578>	3087	101.5	582	S<534>	2471	101.5
539	S<577>	3073	232.5	583	S<533>	2457	232.5
540	S<576>	3059	101.5	584	S<532>	2443	101.5
541	S<575>	3045	232.5	585	S<531>	2429	232.5
542	S<574>	3031	101.5	586	S<530>	2415	101.5
543	S<573>	3017	232.5	587	S<529>	2401	232.5
544	S<572>	3003	101.5	588	S<528>	2387	101.5
545	S<571>	2989	232.5	589	S<527>	2373	232.5
546	S<570>	2975	101.5	590	S<526>	2359	101.5
547	S<569>	2961	232.5	591	S<525>	2345	232.5
548	S<568>	2947	101.5	592	S<524>	2331	101.5
549	S<567>	2933	232.5	593	S<523>	2317	232.5
550	S<566>	2919	101.5	594	S<522>	2303	101.5
551	S<565>	2905	232.5	595	S<521>	2289	232.5
552	S<564>	2891	101.5	596	S<520>	2275	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
597	S<519>	2261	232.5	641	S<475>	1645	232.5
598	S<518>	2247	101.5	642	S<474>	1631	101.5
599	S<517>	2233	232.5	643	S<473>	1617	232.5
600	S<516>	2219	101.5	644	S<472>	1603	101.5
601	S<515>	2205	232.5	645	S<471>	1589	232.5
602	S<514>	2191	101.5	646	S<470>	1575	101.5
603	S<513>	2177	232.5	647	S<469>	1561	232.5
604	S<512>	2163	101.5	648	S<468>	1547	101.5
605	S<511>	2149	232.5	649	S<467>	1533	232.5
606	S<510>	2135	101.5	650	S<466>	1519	101.5
607	S<509>	2121	232.5	651	S<465>	1505	232.5
608	S<508>	2107	101.5	652	S<464>	1491	101.5
609	S<507>	2093	232.5	653	S<463>	1477	232.5
610	S<506>	2079	101.5	654	S<462>	1463	101.5
611	S<505>	2065	232.5	655	S<461>	1449	232.5
612	S<504>	2051	101.5	656	S<460>	1435	101.5
613	S<503>	2037	232.5	657	S<459>	1421	232.5
614	S<502>	2023	101.5	658	S<458>	1407	101.5
615	S<501>	2009	232.5	659	S<457>	1393	232.5
616	S<500>	1995	101.5	660	S<456>	1379	101.5
617	S<499>	1981	232.5	661	S<455>	1365	232.5
618	S<498>	1967	101.5	662	S<454>	1351	101.5
619	S<497>	1953	232.5	663	S<453>	1337	232.5
620	S<496>	1939	101.5	664	S<452>	1323	101.5
621	S<495>	1925	232.5	665	S<451>	1309	232.5
622	S<494>	1911	101.5	666	S<450>	1295	101.5
623	S<493>	1897	232.5	667	S<449>	1281	232.5
624	S<492>	1883	101.5	668	S<448>	1267	101.5
625	S<491>	1869	232.5	669	S<447>	1253	232.5
626	S<490>	1855	101.5	670	S<446>	1239	101.5
627	S<489>	1841	232.5	671	S<445>	1225	232.5
628	S<488>	1827	101.5	672	S<444>	1211	101.5
629	S<487>	1813	232.5	673	S<443>	1197	232.5
630	S<486>	1799	101.5	674	S<442>	1183	101.5
631	S<485>	1785	232.5	675	S<441>	1169	232.5
632	S<484>	1771	101.5	676	S<440>	1155	101.5
633	S<483>	1757	232.5	677	S<439>	1141	232.5
634	S<482>	1743	101.5	678	S<438>	1127	101.5
635	S<481>	1729	232.5	679	S<437>	1113	232.5
636	S<480>	1715	101.5	680	S<436>	1099	101.5
637	S<479>	1701	232.5	681	S<435>	1085	232.5
638	S<478>	1687	101.5	682	S<434>	1071	101.5
639	S<477>	1673	232.5	683	S<433>	1057	232.5
640	S<476>	1659	101.5	684	S<432>	1043	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
685	S<431>	1029	232.5	729	S<387>	413	232.5
686	S<430>	1015	101.5	730	S<386>	399	101.5
687	S<429>	1001	232.5	731	S<385>	385	232.5
688	S<428>	987	101.5	732	S<384>	371	101.5
689	S<427>	973	232.5	733	S<383>	357	232.5
690	S<426>	959	101.5	734	S<382>	343	101.5
691	S<425>	945	232.5	735	S<381>	329	232.5
692	S<424>	931	101.5	736	S<380>	315	101.5
693	S<423>	917	232.5	737	S<379>	301	232.5
694	S<422>	903	101.5	738	S<378>	287	101.5
695	S<421>	889	232.5	739	S<377>	273	232.5
696	S<420>	875	101.5	740	S<376>	259	101.5
697	S<419>	861	232.5	741	S<375>	245	232.5
698	S<418>	847	101.5	742	S<374>	231	101.5
699	S<417>	833	232.5	743	S<373>	217	232.5
700	S<416>	819	101.5	744	S<372>	203	101.5
701	S<415>	805	232.5	745	S<371>	189	232.5
702	S<414>	791	101.5	746	S<370>	175	101.5
703	S<413>	777	232.5	747	S<369>	161	232.5
704	S<412>	763	101.5	748	S<368>	147	101.5
705	S<411>	749	232.5	749	S<367>	133	232.5
706	S<410>	735	101.5	750	S<366>	119	101.5
707	S<409>	721	232.5	751	S<365>	105	232.5
708	S<408>	707	101.5	752	S<364>	91	101.5
709	S<407>	693	232.5	753	S<363>	77	232.5
710	S<406>	679	101.5	754	S<362>	63	101.5
711	S<405>	665	232.5	755	S<361>	49	232.5
712	S<404>	651	101.5	756	S<360>	-49	101.5
713	S<403>	637	232.5	757	S<359>	-63	232.5
714	S<402>	623	101.5	758	S<358>	-77	101.5
715	S<401>	609	232.5	759	S<357>	-91	232.5
716	S<400>	595	101.5	760	S<356>	-105	101.5
717	S<399>	581	232.5	761	S<355>	-119	232.5
718	S<398>	567	101.5	762	S<354>	-133	101.5
719	S<397>	553	232.5	763	S<353>	-147	232.5
720	S<396>	539	101.5	764	S<352>	-161	101.5
721	S<395>	525	232.5	765	S<351>	-175	232.5
722	S<394>	511	101.5	766	S<350>	-189	101.5
723	S<393>	497	232.5	767	S<349>	-203	232.5
724	S<392>	483	101.5	768	S<348>	-217	101.5
725	S<391>	469	232.5	769	S<347>	-231	232.5
726	S<390>	455	101.5	770	S<346>	-245	101.5
727	S<389>	441	232.5	771	S<345>	-259	232.5
728	S<388>	427	101.5	772	S<344>	-273	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
773	S<343>	-287	232.5	817	S<299>	-903	232.5
774	S<342>	-301	101.5	818	S<298>	-917	101.5
775	S<341>	-315	232.5	819	S<297>	-931	232.5
776	S<340>	-329	101.5	820	S<296>	-945	101.5
777	S<339>	-343	232.5	821	S<295>	-959	232.5
778	S<338>	-357	101.5	822	S<294>	-973	101.5
779	S<337>	-371	232.5	823	S<293>	-987	232.5
780	S<336>	-385	101.5	824	S<292>	-1001	101.5
781	S<335>	-399	232.5	825	S<291>	-1015	232.5
782	S<334>	-413	101.5	826	S<290>	-1029	101.5
783	S<333>	-427	232.5	827	S<289>	-1043	232.5
784	S<332>	-441	101.5	828	S<288>	-1057	101.5
785	S<331>	-455	232.5	829	S<287>	-1071	232.5
786	S<330>	-469	101.5	830	S<286>	-1085	101.5
787	S<329>	-483	232.5	831	S<285>	-1099	232.5
788	S<328>	-497	101.5	832	S<284>	-1113	101.5
789	S<327>	-511	232.5	833	S<283>	-1127	232.5
790	S<326>	-525	101.5	834	S<282>	-1141	101.5
791	S<325>	-539	232.5	835	S<281>	-1155	232.5
792	S<324>	-553	101.5	836	S<280>	-1169	101.5
793	S<323>	-567	232.5	837	S<279>	-1183	232.5
794	S<322>	-581	101.5	838	S<278>	-1197	101.5
795	S<321>	-595	232.5	839	S<277>	-1211	232.5
796	S<320>	-609	101.5	840	S<276>	-1225	101.5
797	S<319>	-623	232.5	841	S<275>	-1239	232.5
798	S<318>	-637	101.5	842	S<274>	-1253	101.5
799	S<317>	-651	232.5	843	S<273>	-1267	232.5
800	S<316>	-665	101.5	844	S<272>	-1281	101.5
801	S<315>	-679	232.5	845	S<271>	-1295	232.5
802	S<314>	-693	101.5	846	S<270>	-1309	101.5
803	S<313>	-707	232.5	847	S<269>	-1323	232.5
804	S<312>	-721	101.5	848	S<268>	-1337	101.5
805	S<311>	-735	232.5	849	S<267>	-1351	232.5
806	S<310>	-749	101.5	850	S<266>	-1365	101.5
807	S<309>	-763	232.5	851	S<265>	-1379	232.5
808	S<308>	-777	101.5	852	S<264>	-1393	101.5
809	S<307>	-791	232.5	853	S<263>	-1407	232.5
810	S<306>	-805	101.5	854	S<262>	-1421	101.5
811	S<305>	-819	232.5	855	S<261>	-1435	232.5
812	S<304>	-833	101.5	856	S<260>	-1449	101.5
813	S<303>	-847	232.5	857	S<259>	-1463	232.5
814	S<302>	-861	101.5	858	S<258>	-1477	101.5
815	S<301>	-875	232.5	859	S<257>	-1491	232.5
816	S<300>	-889	101.5	860	S<256>	-1505	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
861	S<255>	-1519	232.5	905	S<211>	-2135	232.5
862	S<254>	-1533	101.5	906	S<210>	-2149	101.5
863	S<253>	-1547	232.5	907	S<209>	-2163	232.5
864	S<252>	-1561	101.5	908	S<208>	-2177	101.5
865	S<251>	-1575	232.5	909	S<207>	-2191	232.5
866	S<250>	-1589	101.5	910	S<206>	-2205	101.5
867	S<249>	-1603	232.5	911	S<205>	-2219	232.5
868	S<248>	-1617	101.5	912	S<204>	-2233	101.5
869	S<247>	-1631	232.5	913	S<203>	-2247	232.5
870	S<246>	-1645	101.5	914	S<202>	-2261	101.5
871	S<245>	-1659	232.5	915	S<201>	-2275	232.5
872	S<244>	-1673	101.5	916	S<200>	-2289	101.5
873	S<243>	-1687	232.5	917	S<199>	-2303	232.5
874	S<242>	-1701	101.5	918	S<198>	-2317	101.5
875	S<241>	-1715	232.5	919	S<197>	-2331	232.5
876	S<240>	-1729	101.5	920	S<196>	-2345	101.5
877	S<239>	-1743	232.5	921	S<195>	-2359	232.5
878	S<238>	-1757	101.5	922	S<194>	-2373	101.5
879	S<237>	-1771	232.5	923	S<193>	-2387	232.5
880	S<236>	-1785	101.5	924	S<192>	-2401	101.5
881	S<235>	-1799	232.5	925	S<191>	-2415	232.5
882	S<234>	-1813	101.5	926	S<190>	-2429	101.5
883	S<233>	-1827	232.5	927	S<189>	-2443	232.5
884	S<232>	-1841	101.5	928	S<188>	-2457	101.5
885	S<231>	-1855	232.5	929	S<187>	-2471	232.5
886	S<230>	-1869	101.5	930	S<186>	-2485	101.5
887	S<229>	-1883	232.5	931	S<185>	-2499	232.5
888	S<228>	-1897	101.5	932	S<184>	-2513	101.5
889	S<227>	-1911	232.5	933	S<183>	-2527	232.5
890	S<226>	-1925	101.5	934	S<182>	-2541	101.5
891	S<225>	-1939	232.5	935	S<181>	-2555	232.5
892	S<224>	-1953	101.5	936	S<180>	-2569	101.5
893	S<223>	-1967	232.5	937	S<179>	-2583	232.5
894	S<222>	-1981	101.5	938	S<178>	-2597	101.5
895	S<221>	-1995	232.5	939	S<177>	-2611	232.5
896	S<220>	-2009	101.5	940	S<176>	-2625	101.5
897	S<219>	-2023	232.5	941	S<175>	-2639	232.5
898	S<218>	-2037	101.5	942	S<174>	-2653	101.5
899	S<217>	-2051	232.5	943	S<173>	-2667	232.5
900	S<216>	-2065	101.5	944	S<172>	-2681	101.5
901	S<215>	-2079	232.5	945	S<171>	-2695	232.5
902	S<214>	-2093	101.5	946	S<170>	-2709	101.5
903	S<213>	-2107	232.5	947	S<169>	-2723	232.5
904	S<212>	-2121	101.5	948	S<168>	-2737	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
949	S<167>	-2751	232.5	993	S<123>	-3367	232.5
950	S<166>	-2765	101.5	994	S<122>	-3381	101.5
951	S<165>	-2779	232.5	995	S<121>	-3395	232.5
952	S<164>	-2793	101.5	996	S<120>	-3409	101.5
953	S<163>	-2807	232.5	997	S<119>	-3423	232.5
954	S<162>	-2821	101.5	998	S<118>	-3437	101.5
955	S<161>	-2835	232.5	999	S<117>	-3451	232.5
956	S<160>	-2849	101.5	1000	S<116>	-3465	101.5
957	S<159>	-2863	232.5	1001	S<115>	-3479	232.5
958	S<158>	-2877	101.5	1002	S<114>	-3493	101.5
959	S<157>	-2891	232.5	1003	S<113>	-3507	232.5
960	S<156>	-2905	101.5	1004	S<112>	-3521	101.5
961	S<155>	-2919	232.5	1005	S<111>	-3535	232.5
962	S<154>	-2933	101.5	1006	S<110>	-3549	101.5
963	S<153>	-2947	232.5	1007	S<109>	-3563	232.5
964	S<152>	-2961	101.5	1008	S<108>	-3577	101.5
965	S<151>	-2975	232.5	1009	S<107>	-3591	232.5
966	S<150>	-2989	101.5	1010	S<106>	-3605	101.5
967	S<149>	-3003	232.5	1011	S<105>	-3619	232.5
968	S<148>	-3017	101.5	1012	S<104>	-3633	101.5
969	S<147>	-3031	232.5	1013	S<103>	-3647	232.5
970	S<146>	-3045	101.5	1014	S<102>	-3661	101.5
971	S<145>	-3059	232.5	1015	S<101>	-3675	232.5
972	S<144>	-3073	101.5	1016	S<100>	-3689	101.5
973	S<143>	-3087	232.5	1017	S<99>	-3703	232.5
974	S<142>	-3101	101.5	1018	S<98>	-3717	101.5
975	S<141>	-3115	232.5	1019	S<97>	-3731	232.5
976	S<140>	-3129	101.5	1020	S<96>	-3745	101.5
977	S<139>	-3143	232.5	1021	S<95>	-3759	232.5
978	S<138>	-3157	101.5	1022	S<94>	-3773	101.5
979	S<137>	-3171	232.5	1023	S<93>	-3787	232.5
980	S<136>	-3185	101.5	1024	S<92>	-3801	101.5
981	S<135>	-3199	232.5	1025	S<91>	-3815	232.5
982	S<134>	-3213	101.5	1026	S<90>	-3829	101.5
983	S<133>	-3227	232.5	1027	S<89>	-3843	232.5
984	S<132>	-3241	101.5	1028	S<88>	-3857	101.5
985	S<131>	-3255	232.5	1029	S<87>	-3871	232.5
986	S<130>	-3269	101.5	1030	S<86>	-3885	101.5
987	S<129>	-3283	232.5	1031	S<85>	-3899	232.5
988	S<128>	-3297	101.5	1032	S<84>	-3913	101.5
989	S<127>	-3311	232.5	1033	S<83>	-3927	232.5
990	S<126>	-3325	101.5	1034	S<82>	-3941	101.5
991	S<125>	-3339	232.5	1035	S<81>	-3955	232.5
992	S<124>	-3353	101.5	1036	S<80>	-3969	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1037	S<79>	-3983	232.5	1081	S<35>	-4599	232.5
1038	S<78>	-3997	101.5	1082	S<34>	-4613	101.5
1039	S<77>	-4011	232.5	1083	S<33>	-4627	232.5
1040	S<76>	-4025	101.5	1084	S<32>	-4641	101.5
1041	S<75>	-4039	232.5	1085	S<31>	-4655	232.5
1042	S<74>	-4053	101.5	1086	S<30>	-4669	101.5
1043	S<73>	-4067	232.5	1087	S<29>	-4683	232.5
1044	S<72>	-4081	101.5	1088	S<28>	-4697	101.5
1045	S<71>	-4095	232.5	1089	S<27>	-4711	232.5
1046	S<70>	-4109	101.5	1090	S<26>	-4725	101.5
1047	S<69>	-4123	232.5	1091	S<25>	-4739	232.5
1048	S<68>	-4137	101.5	1092	S<24>	-4753	101.5
1049	S<67>	-4151	232.5	1093	S<23>	-4767	232.5
1050	S<66>	-4165	101.5	1094	S<22>	-4781	101.5
1051	S<65>	-4179	232.5	1095	S<21>	-4795	232.5
1052	S<64>	-4193	101.5	1096	S<20>	-4809	101.5
1053	S<63>	-4207	232.5	1097	S<19>	-4823	232.5
1054	S<62>	-4221	101.5	1098	S<18>	-4837	101.5
1055	S<61>	-4235	232.5	1099	S<17>	-4851	232.5
1056	S<60>	-4249	101.5	1100	S<16>	-4865	101.5
1057	S<59>	-4263	232.5	1101	S<15>	-4879	232.5
1058	S<58>	-4277	101.5	1102	S<14>	-4893	101.5
1059	S<57>	-4291	232.5	1103	S<13>	-4907	232.5
1060	S<56>	-4305	101.5	1104	S<12>	-4921	101.5
1061	S<55>	-4319	232.5	1105	S<11>	-4935	232.5
1062	S<54>	-4333	101.5	1106	S<10>	-4949	101.5
1063	S<53>	-4347	232.5	1107	S<9>	-4963	232.5
1064	S<52>	-4361	101.5	1108	S<8>	-4977	101.5
1065	S<51>	-4375	232.5	1109	S<7>	-4991	232.5
1066	S<50>	-4389	101.5	1110	S<6>	-5005	101.5
1067	S<49>	-4403	232.5	1111	S<5>	-5019	232.5
1068	S<48>	-4417	101.5	1112	S<4>	-5033	101.5
1069	S<47>	-4431	232.5	1113	S<3>	-5047	232.5
1070	S<46>	-4445	101.5	1114	S<2>	-5061	101.5
1071	S<45>	-4459	232.5	1115	S<1>	-5075	232.5
1072	S<44>	-4473	101.5	1116	G<319>	-5131	101.5
1073	S<43>	-4487	232.5	1117	G<317>	-5145	232.5
1074	S<42>	-4501	101.5	1118	G<315>	-5159	101.5
1075	S<41>	-4515	232.5	1119	G<313>	-5173	232.5
1076	S<40>	-4529	101.5	1120	G<311>	-5187	101.5
1077	S<39>	-4543	232.5	1121	G<309>	-5201	232.5
1078	S<38>	-4557	101.5	1122	G<307>	-5215	101.5
1079	S<37>	-4571	232.5	1123	G<305>	-5229	232.5
1080	S<36>	-4585	101.5	1124	G<303>	-5243	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1125	G<301>	-5257	232.5	1168	G<215>	-5859	101.5
1126	G<299>	-5271	101.5	1169	G<213>	-5873	232.5
1127	G<297>	-5285	232.5	1170	G<211>	-5887	101.5
1128	G<295>	-5299	101.5	1171	G<209>	-5901	232.5
1129	G<293>	-5313	232.5	1172	G<207>	-5915	101.5
1130	G<291>	-5327	101.5	1173	G<205>	-5929	232.5
1131	G<289>	-5341	232.5	1174	G<203>	-5943	101.5
1132	G<287>	-5355	101.5	1175	G<201>	-5957	232.5
1133	G<285>	-5369	232.5	1176	G<199>	-5971	101.5
1134	G<283>	-5383	101.5	1177	G<197>	-5985	232.5
1135	G<281>	-5397	232.5	1178	G<195>	-5999	101.5
1136	G<279>	-5411	101.5	1179	G<193>	-6013	232.5
1137	G<277>	-5425	232.5	1180	G<191>	-6027	101.5
1138	G<275>	-5439	101.5	1181	G<189>	-6041	232.5
1139	G<273>	-5453	232.5	1182	G<187>	-6055	101.5
1140	G<271>	-5467	101.5	1183	G<185>	-6069	232.5
1141	G<269>	-5481	232.5	1184	G<183>	-6083	101.5
1142	G<267>	-5495	101.5	1185	G<181>	-6097	232.5
1143	G<265>	-5509	232.5	1186	G<179>	-6111	101.5
1144	G<263>	-5523	101.5	1187	G<177>	-6125	232.5
1145	G<261>	-5537	232.5	1188	G<175>	-6139	101.5
1146	G<259>	-5551	101.5	1189	G<173>	-6153	232.5
1147	G<257>	-5565	232.5	1190	G<171>	-6167	101.5
1148	G<255>	-5579	101.5	1191	G<169>	-6181	232.5
1149	G<253>	-5593	232.5	1192	G<167>	-6195	101.5
1150	G<251>	-5607	101.5	1193	G<165>	-6209	232.5
1151	G<249>	-5621	232.5	1194	G<163>	-6223	101.5
1152	G<247>	-5635	101.5	1195	G<161>	-6237	232.5
1153	G<245>	-5649	232.5	1196	G<159>	-6251	101.5
1154	G<243>	-5663	101.5	1197	G<157>	-6265	232.5
1155	G<241>	-5677	232.5	1198	G<155>	-6279	101.5
1156	G<239>	-5691	101.5	1199	G<153>	-6293	232.5
1157	G<237>	-5705	232.5	1200	G<151>	-6307	101.5
1158	G<235>	-5719	101.5	1201	G<149>	-6321	232.5
1159	G<233>	-5733	232.5	1202	G<147>	-6335	101.5
1160	G<231>	-5747	101.5	1203	G<145>	-6349	232.5
1161	G<229>	-5761	232.5	1204	G<143>	-6363	101.5
1162	G<227>	-5775	101.5	1205	G<141>	-6377	232.5
1163	G<225>	-5789	232.5	1206	G<139>	-6391	101.5
1164	G<223>	-5803	101.5	1207	G<137>	-6405	232.5
1165	G<221>	-5817	232.5	1208	G<135>	-6419	101.5
1166	G<219>	-5831	101.5	1209	G<133>	-6433	232.5
1167	G<217>	-5845	232.5	1210	G<131>	-6447	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1211	G<129>	-6461	232.5	1255	G<41>	-7077	232.5
1212	G<127>	-6475	101.5	1256	G<39>	-7091	101.5
1213	G<125>	-6489	232.5	1257	G<37>	-7105	232.5
1214	G<123>	-6503	101.5	1258	G<35>	-7119	101.5
1215	G<121>	-6517	232.5	1259	G<33>	-7133	232.5
1216	G<119>	-6531	101.5	1260	G<31>	-7147	101.5
1217	G<117>	-6545	232.5	1261	G<29>	-7161	232.5
1218	G<115>	-6559	101.5	1262	G<27>	-7175	101.5
1219	G<113>	-6573	232.5	1263	G<25>	-7189	232.5
1220	G<111>	-6587	101.5	1264	G<23>	-7203	101.5
1221	G<109>	-6601	232.5	1265	G<21>	-7217	232.5
1222	G<107>	-6615	101.5	1266	G<19>	-7231	101.5
1223	G<105>	-6629	232.5	1267	G<17>	-7245	232.5
1224	G<103>	-6643	101.5	1268	G<15>	-7259	101.5
1225	G<101>	-6657	232.5	1269	G<13>	-7273	232.5
1226	G<99>	-6671	101.5	1270	G<11>	-7287	101.5
1227	G<97>	-6685	232.5	1271	G<9>	-7301	232.5
1228	G<95>	-6699	101.5	1272	G<7>	-7315	101.5
1229	G<93>	-6713	232.5	1273	G<5>	-7329	232.5
1230	G<91>	-6727	101.5	1274	G<3>	-7343	101.5
1231	G<89>	-6741	232.5	1275	G<1>	-7357	232.5
1232	G<87>	-6755	101.5	1276	DMY_GDL	-7371	101.5
1233	G<85>	-6769	232.5	1277	DMY_GDL	-7385	232.5
1234	G<83>	-6783	101.5	1278	DMY_GDL	-7399	101.5
1235	G<81>	-6797	232.5				
1236	G<79>	-6811	101.5				
1237	G<77>	-6825	232.5				
1238	G<75>	-6839	101.5				
1239	G<73>	-6853	232.5				
1240	G<71>	-6867	101.5				
1241	G<69>	-6881	232.5				
1242	G<67>	-6895	101.5				
1243	G<65>	-6909	232.5				
1244	G<63>	-6923	101.5				
1245	G<61>	-6937	232.5				
1246	G<59>	-6951	101.5				
1247	G<57>	-6965	232.5				
1248	G<55>	-6979	101.5				
1249	G<53>	-6993	232.5				
1250	G<51>	-7007	101.5				
1251	G<49>	-7021	232.5				
1252	G<47>	-7035	101.5				
1253	G<45>	-7049	232.5				
1254	G<43>	-7063	101.5				

7. Command

7.1 Public command

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
No operation	W	0	0	0	0	0	0	0	0	(00h)
	W									
Read display ID	W	0	0	0	0	0	1	0	0	(04h)
	R	id1[7:0]								30h
	R	id2[7:0]								30h
	R	id3[7:0]								01h
Read display status	W	0	0	0	0	1	0	0	1	(09h)
	R	boost_ status	madctl[7:2]							00h
	R	X	color_mode[2:0]			idle	partial_ mode	sleep	normal_ mode	61h
	R	scrol l_ mo de		inv_en			display_ en	tear_en		00h
	R	tear_mo de		init_st[2:0]			sys_st[2:0]			28h
Read display Power mode	W	0	0	0	0	1	0	1	0	(0Ah)
	R	boost_ status	idle	partial_ mode	sleep	normal_ mode	display_ en			08h
Read display MADCTL	W	0	0	0	0	1	0	1	1	(0Bh)
	R	madctl[7:0]								00h
Read display Pixel format	W	0	0	0	0	1	1	0	0	(0Ch)
	R	rim	dpi[2:0]				dbi[2:0]			66h
Read display Image mode	W	0	0	0	0	1	1	0	1	(0Dh)
	R			init_st[2:0]			sys_st[2:0]			28h
Read display Signal mode	W	0	0	0	0	1	1	1	0	(0Eh)
	R	te_on_ off	tear_ mode	rcm[2:0]			de_ mode			3Ch
Read display self-diagnosticresult	W	0	0	0	0	1	1	1	1	(0Fh)
	R	reg_loa d_ det	func_ det							00h
Sleep in	W	0	0	0	1	0	0	0	0	(10h)
Sleep out	W	0	0	0	1	0	0	0	1	(11h)
Partial mode on	W	0	0	0	1	0	0	1	0	(12h)

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
normal mode on and partial mode off	W	0	0	0	1	0	0	1	1	(13h)
Display inversion off	W	0	0	1	0	0	0	0	0	(20h)
Display inversion on	W	0	0	1	0	0	0	0	1	(21h)
Display off	W	0	0	1	0	1	0	0	0	(28h)
Display on	W	0	0	1	0	1	0	0	1	(29h)
Column address	W	0	0	1	0	1	0	1	0	(2Ah)
	W	caset_sc[15:8]								00h
	W	caset_sc[7:0]								00h
	W	caset_ec[15:8]								00h
	W	caset_ec[7:0]								EFh
page address	W	0	0	1	0	1	0	1	1	(2Bh)
	W	paset_sp[15:8]								00h
	W	paset_sp[7:0]								00h
	W	paset_ep[15:8]								01h
	W	paset_ep[7:0]								3Fh
memory write	W	0	0	1	0	1	1	0	0	(2Ch)
partial area	W	0	0	1	1	0	0	0	0	(30h)
	W								paset_sr[8]	00h
	W	paset_sr[7:0]								00h
	W								paset_er[8]	01h
	W	paset_er[7:0]								3Fh
Vertical scrolling	W	0	0	1	1	0	0	1	1	(33h)
	W								vscrdef_tfa[8]	00h
	W	vscrdef_tfa[7:0]								00h
	W								vscrdef_vsa[8]	00h
	W	vscrdef_vsa[7:0]								00h
	W								vscrdef_bfa[8]	00h
	W	vscrdef_bfa[7:0]								00h
Tearing effect line off	W	0	0	1	1	0	1	0	0	(34h)
Tearing effect line on	W	0	0	1	1	0	1	0	1	(35h)
	W								tem	00h
MADCTL (memory data access control)	W	0	0	1	1	0	1	1	0	(36h)
	W	my	mx	mv	ml	bgr	mh			00h
Vertical scrolling start address	W	0	0	1	1	0	1	1	1	(37h)
	W								vscrdef_vsp[8]	00h
	W	vscrdef_vsp[7:0]								00h
Idle mode off	W	0	0	1	1	1	0	0	0	(38h)
idle mode on and other mode off	W	0	0	1	1	1	0	0	1	(39h)

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
Interface pixel format	W	0	0	1	1	1	0	1	0	(3Ah)
	W		dpi[2:0]				dbi[2:0]			66h
write memory continue	W	0	0	1	1	1	1	0	0	(3Ch)
set tear scanline	W	0	1	0	0	0	1	0	0	(44h)
	W								sts[8]	00h
	W	sts[7:0]								00h
Get tear scan line	W	0	1	0	0	0	1	0	1	(45h)
	R								gts[8]	00h
	R	gts[7:0]								00h
write display brightess	W	0	1	0	1	0	0	1	1	(53h)
	W						bl			04h
read display brightess	W	0	1	0	1	0	1	0	0	(54h)
	R						bl			04h
read idd3	W	1	1	0	1	0	0	1	1	(D3h)
	R	id4[7:0]								30h
	R	id5[7:0]								30h
	R	id6[7:0]								01h
read display id 1	W	1	1	0	1	1	0	1	0	(DAh)
	R	id1[7:0]								30h
read display id 2	W	1	1	0	1	1	0	1	1	(DBh)
	R	id2[7:0]								30h
read display id 3	W	1	1	0	1	1	1	0	0	(DCh)
	R	id3[7:0]								01h

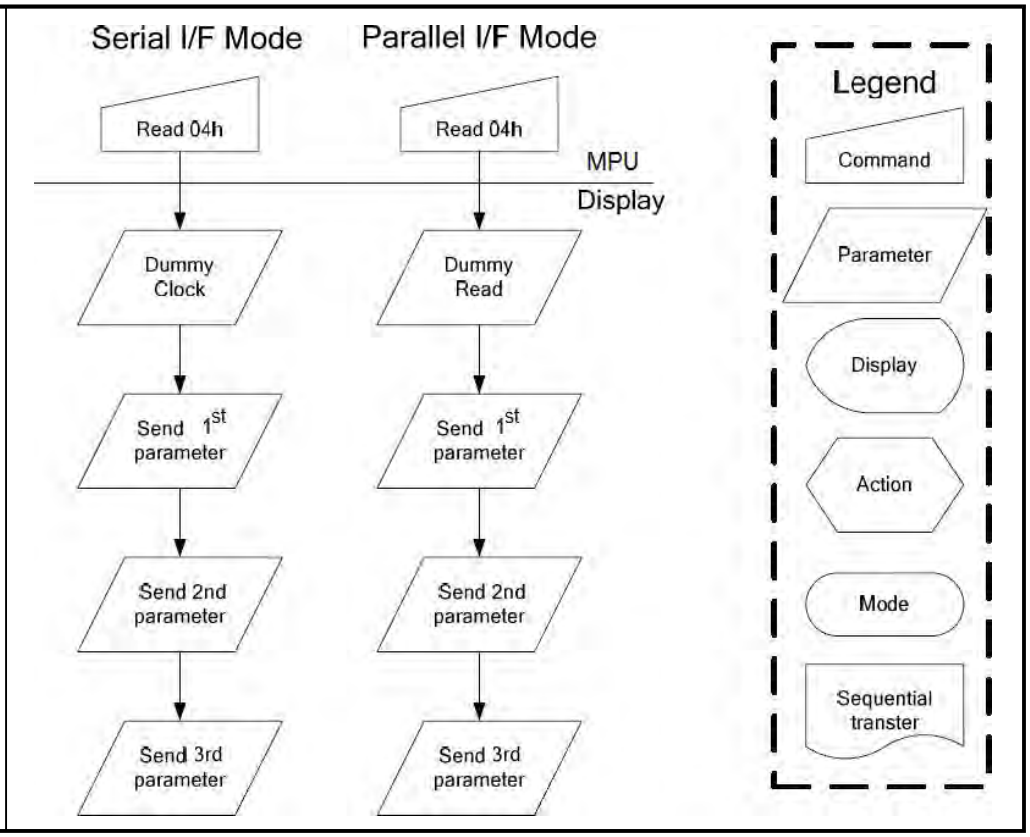
7.1.1 no operation (00h)

<table>
<tr><th>00h</th><th colspan="10">no operation</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>no operation</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(00h)</td></tr>
<tr><td>Parameter</td><td colspan="9">No Parameter.</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is empty command.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.2 read display ID (04h)

<table>
<tr><th>04h</th><th colspan="10">read display ID</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display ID</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(04h)</td></tr>
<tr><td>1st parameter</td><td>R</td><td colspan="8">id1[7:0]</td><td>30h</td></tr>
<tr><td>2nd parameter</td><td>R</td><td colspan="8">id2[7:0]</td><td>30h</td></tr>
<tr><td>3rd parameter</td><td>R</td><td colspan="8">id3[7:0]</td><td>01h</td></tr>
<tr><td>Description</td><td colspan="10">This read byte returns 24-bit display identification information.
id1/2/3:LCD module/driver ID.
Commands RDID1/2/3(Dah, DBh, DCh) read data correspond to the parameters 1,2,3 of the command 04h,respectively.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>id1[7:0]</th><th>id2[7:0]</th><th>id3[7:0]</th></tr><tr><td>Power On Sequence</td><td>30h</td><td>30h</td><td>01h</td></tr><tr><td>S/W Reset</td><td>30h</td><td>30h</td><td>01h</td></tr><tr><td>H/W Reset</td><td>30h</td><td>30h</td><td>01h</td></tr></table></td></tr>
</table>

Flow Chart



7.1.3 read display status (09h)

09h	read display status									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display status	W	0	0	0	0	1	0	0	1	(09h)
1st parameter	R	boost_status	madctl[7:2]						X	00h
2nd parameter	R	X	color_mode[2:0]			idle	partial_mode	sleep	normal_mode	61h
3rd parameter	R	scroll_mode	X	inv_en	X	X	display_en	tear_en	X	00h
4th parameter	R	tear_mode		init_st[2:0]			sys_st[2:0]			28h

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Comment
boost_status	Booster Voltage Status	0	Booster Off
		1	Booster On
madctl [7...2]	Page Address Order	0	Top to Bottom (When memory data access control D7 = '0')
		1	Bottom to Top (When memory data access control D7 = '1')
	Column Address Order	0	Left to Right (When memory data access control D6 = '0')
		1	Right to Left (When memory data access control D6 = '1')
	Page/Column Order	0	Normal Mode (When memory data access control D5 = '0')
		1	Reverse Mode (When memory data access control D5 = '1')
	Line Address Order	0	LCD Refresh Top to Bottom (When memory data access control D4 = '0')
		1	LCD Refresh Bottom to Top (When memory data access control D4 = '1')
	RGB/BGR Order	0	RGB (When memory data access control D3 = '0')
		1	BGR (When memory data access control D3 = '1')
	mh	-	Reserved
idle	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
partial_mode	Partial Mode On/Off	0	Partial Mode Off
		1	Partial Mode On
sleep	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
normal_mode	Display Normal Mode On/Off	0	Display Normal Mode Off
		1	Display Normal Mode On
scroll_mode	Vertical Scrolling Status	0	Vertical Scrolling is Off
		1	Vertical Scrolling is On
inv_en	Inversion Status	0	Inversion is Off
		1	Inversion is On
display_en	Display On/Off	0	Display is Off
		1	Display is On
tear_en	Tearing Effect Line On/Off	0	Tearing Effect Line Off
		1	Tearing Effect Line On
tear_mode	Tearing Effect Output Line Mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking
init_st	Memory bist state machine	0	Describes the Memory bist process
sys_st	System state machine	0	Description System Status

Bits color_mode[2:0]: Interface Color Pixel Format Definition.

Interface Format	color_mode[2]	color_mode[1]	color_mode[0]
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

Note:

1. For Bits madctl [7:5], also refer to Section 8.2.3 MPU to memory write/read direction.
2. For Bits madctl [4:2] also refer to 7.1.27 memory data access control (36h).

"-" Don't care.

Restriction

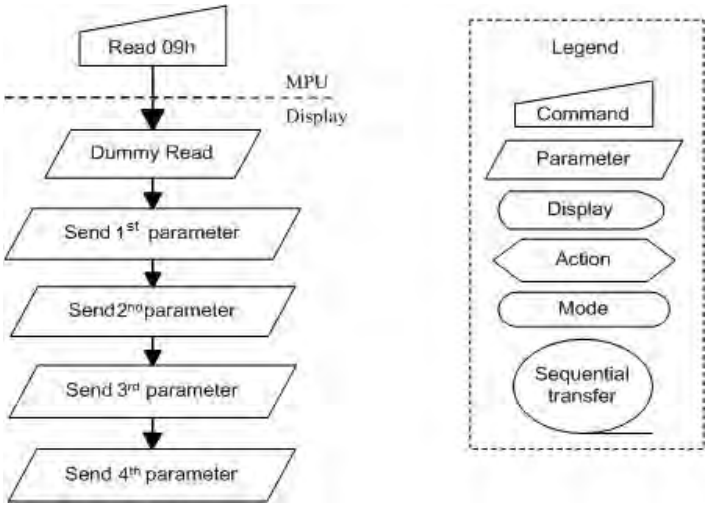
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

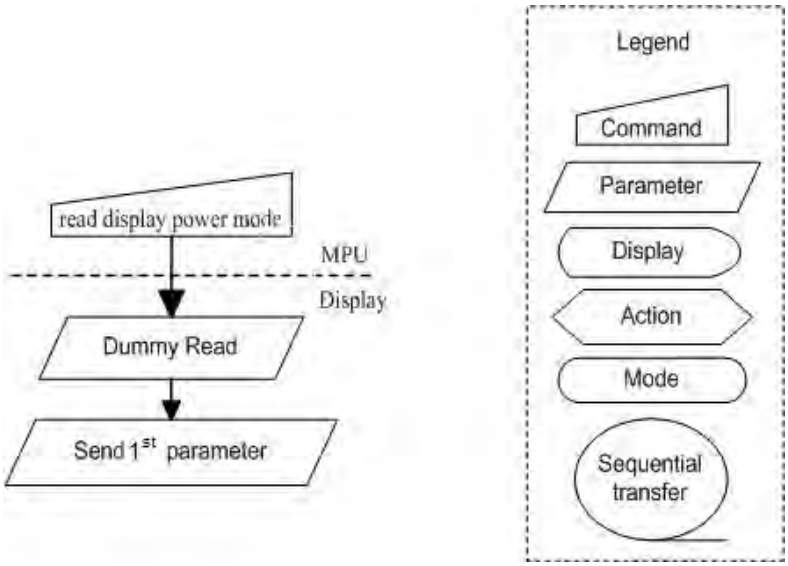
Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart



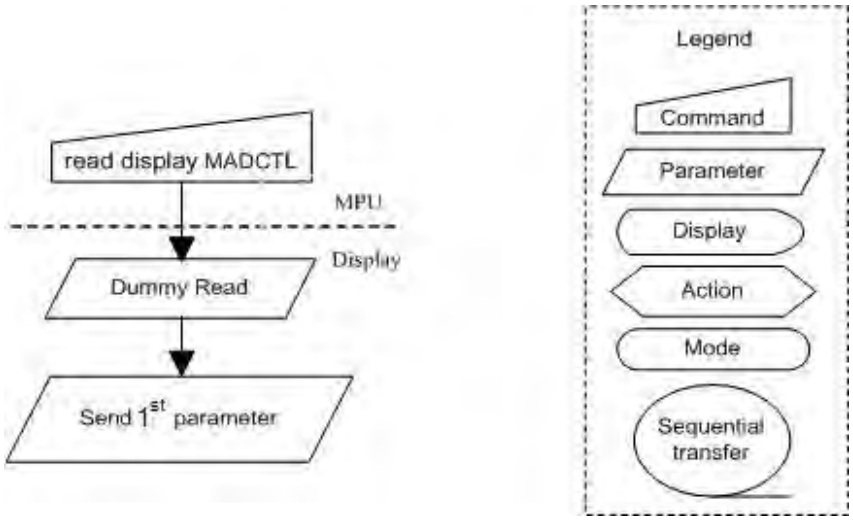
7.1.4 read display power mode (0Ah)

<table>
<tr><th>0Ah</th><th colspan="10">read display power mode</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display power mode</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>(0Ah)</td></tr>
<tr><td>parameter</td><td>R</td><td>boost_status</td><td>idle</td><td>partial_mode</td><td>sleep</td><td>normal_ mode</td><td>display_ en</td><td>X</td><td>X</td><td>08h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Comment</th></tr>
<tr><td rowspan="2">boost_status</td><td rowspan="2">Booster Voltage Status</td><td>0</td><td>Booster Off or has a fault</td></tr>
<tr><td>1</td><td>Booster On and working OK</td></tr>
<tr><td rowspan="2">idle</td><td rowspan="2">Idle Mode On/Off</td><td>0</td><td>Idle Mode Off</td></tr>
<tr><td>1</td><td>Idle Mode On</td></tr>
<tr><td rowspan="2">partial_mode</td><td rowspan="2">Partial Mode On/Off</td><td>0</td><td>Partial Mode Off</td></tr>
<tr><td>1</td><td>Partial Mode On</td></tr>
<tr><td rowspan="2">sleep</td><td rowspan="2">Sleep In/Out</td><td>0</td><td>Sleep In Mode</td></tr>
<tr><td>1</td><td>Sleep Out Mode</td></tr>
<tr><td rowspan="2">normal_mode</td><td rowspan="2">Display Normal Mode On/Off</td><td>0</td><td>Display Normal Mode Off</td></tr>
<tr><td>1</td><td>Display Normal Mode On</td></tr>
<tr><td rowspan="2">display_en</td><td rowspan="2">Display On/Off</td><td>0</td><td>Display Off</td></tr>
<tr><td>1</td><td>Display On</td></tr>
<tr><td>others</td><td>-</td><td>0</td><td>Set to ‘0’</td></tr>
</table>
“X“ Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>08h</td></tr>
<tr><td>S/W Reset</td><td>08h</td></tr>
<tr><td>H/W Reset</td><td>08h</td></tr>
</table>
</td></tr>
</table>

Flow Chart	 read display power mode MPU Display Dummy Read Send 1st parameter Legend Command Parameter Display Action Mode Sequential transfer

7.1.5 read display MADCTL (0Bh)

<table>
<tr><th>0Bh</th><th colspan="10">read display MADCTL</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display MADCTL</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>(0Bh)</td></tr>
<tr><td>1st parameter</td><td>R</td><td colspan="8">madctl[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Comment</th></tr>
<tr><td rowspan="2">Madctl[7]</td><td rowspan="2">Page Address Order</td><td>0</td><td>Top to Bottom (When memory data access control D7=’0’).</td></tr>
<tr><td>1</td><td>Bottom to Top (When memory data access control D7=’1’).</td></tr>
<tr><td rowspan="2">Madctl[6]</td><td rowspan="2">Column Address Order</td><td>0</td><td>Left to Right (When memory data access control D6=’0’)</td></tr>
<tr><td>1</td><td>Right to Left (when memory data access control D6=’1’</td></tr>
<tr><td rowspan="2">Madctl[5]</td><td rowspan="2">Page/Column Order</td><td>0</td><td>Normal Mode (When memory data access control D5=’0’).</td></tr>
<tr><td>1</td><td>Reverse Mode (When memory data access control D5=’1’)</td></tr>
<tr><td rowspan="2">Madctl[4]</td><td rowspan="2">Line Address Order</td><td>0</td><td>LCD Refresh Top to Bottom (When memory data access control D4=’0’)</td></tr>
<tr><td>1</td><td>LCD Refresh Bottom to Top (When memory data access control D4=’1’)</td></tr>
<tr><td rowspan="2">Madctl[3]</td><td rowspan="2">RGB/BGR Order</td><td>0</td><td>RGB (When memory data access control D3=’0’)</td></tr>
<tr><td>1</td><td>“1”: BGR (When memory data access control D3=’1’)</td></tr>
<tr><td>Madctl[2]</td><td>mh</td><td>-</td><td>Reserved</td></tr>
<tr><td>others</td><td>-</td><td>0</td><td>Set to ‘0’</td></tr>
</table>
Note:
1. For Bits Madctl[7…5], also refer to Section 8.2.3 MPU to memory write/read direction.
2. For Bits Madctl [4:2] also refer to 7.1.27 memory dataaccess control (36h).
“X” Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
</table>

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

7.1.6 read display pixel format (0Ch)

0Ch	read display pixel format									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display pixel format	W	0	0	0	0	1	1	0	0	(0Ch)
1st parameter	R	rim	dpi[2:0]			X	dbi[2:0]			66h

Description

This command indicates the current status of the display as described in the table below:

rim	dpi[2:0]			RGB interface Format
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	16bit/pixel
0	1	1	0	18bit/pixel
0	1	1	1	Reserved
1	1	0	1	16bit/pixel(6-bit 3 times data transfer)
1	1	1	0	18bit/pixel(6-bit 3 times data transfer)

dbi[2:0]			system Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	12bit/pixel
1	0	0	Reserved
1	0	1	16bit/pixel
1	1	0	18bit/pixel
1	1	1	Reserved

Restriction

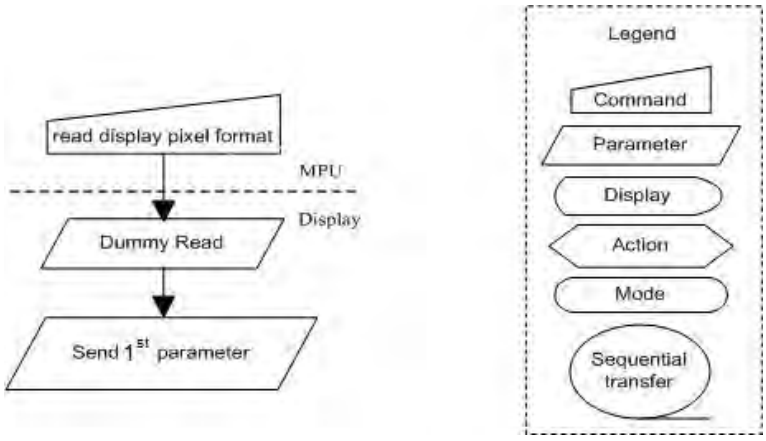
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66h
S/W Reset	No change
H/W Reset	66h

Flow Chart



7.1.7 read display image mode (0Dh)

0Dh	read display image mode									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display image mode	W	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	R			init_st[2:0]			sys_st[2:0]			28h

Restriction

init_st: Describes the Memory bist process.

000	ST_POR
001	ST_OTP_S
010	ST_OTP_ACT
011	ST_MBIST_S
100	ST_MBIST_ACT
101	ST_INIT_DONE

sys_st: Description System Status.

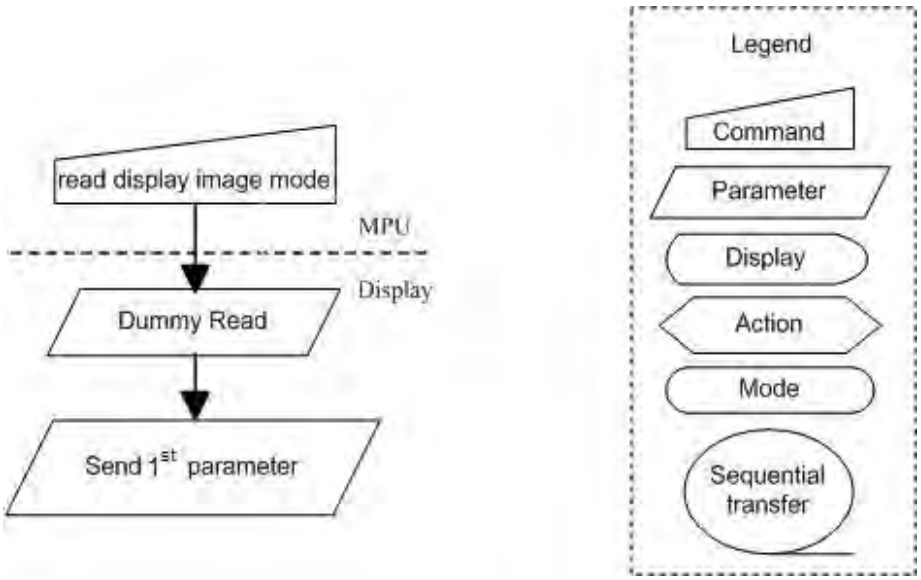
000	ST_IDLE
001	ST_SLP_OUT
011	ST_BLANK
010	ST_NORMAL
110	ST_SLP_IN
101	ST_WAIT_NM
111	ST_WAIT_BLANK
100	ST_DSTB

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

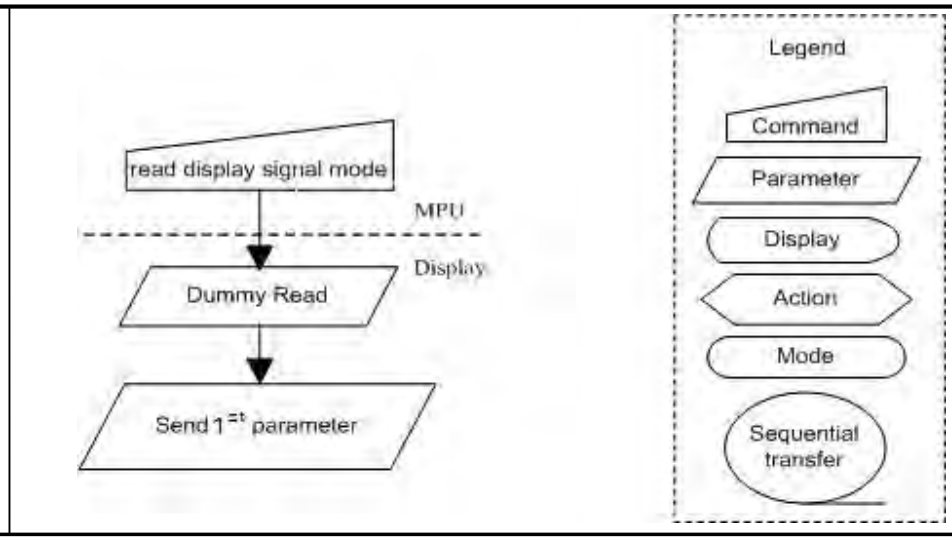
Default

Status	Default Value
Power On Sequence	28h
S/W Reset	no change
H/W Reset	28h

Flow Chart	 read display image mode MPU Display Dummy Read Send 1st parameter Legend Command Parameter Display Action Mode Sequential transfer

7.1.8 read display signal mode (0Eh)

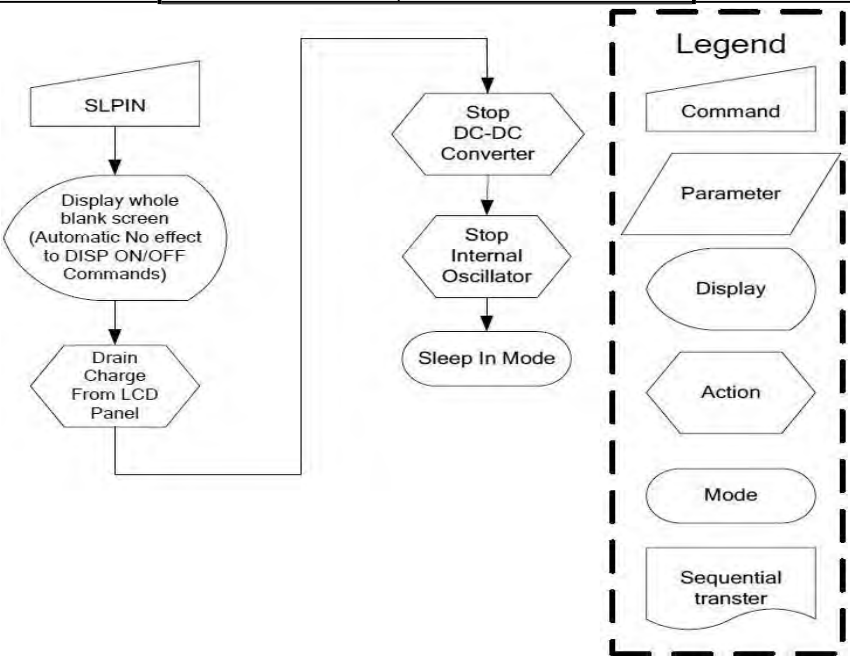
<table>
<tr><th>0Eh</th><th colspan="10">read display signal mode</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display signal mode</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>(0Eh)</td></tr>
<tr><td>1st parameter</td><td>R</td><td>te_on_off</td><td>tear_mode</td><td>rcm[1]</td><td>rcm[1]</td><td>rcm[1]</td><td>de_mode</td><td>X</td><td>X</td><td>3Ch</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="2">te_on_off</td><td>0</td><td>Tearing Effect Line Off</td></tr>
<tr><td>1</td><td>Tearing Effect Line On</td></tr>
<tr><td rowspan="2">tear_mode</td><td>0</td><td>Mode 1 （ Tearing Effect Line Output Mode, see section 8.4.1）</td></tr>
<tr><td>1</td><td>Mode 2（Tearing Effect Line Output Mode, see section 8.4.1）</td></tr>
<tr><td>de_mode</td><td>-</td><td>RGB DE mode.</td></tr>
</table>
<table>
<tr><th>rcm[1]</th><th>de_mode</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td rowspan="2">MCU interface</td></tr>
<tr><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>DE mode</td></tr>
<tr><td>1</td><td>1</td><td>SYNC mode</td></tr>
</table>
“X” Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>3Ch</td></tr>
<tr><td>S/W Reset</td><td>3Ch</td></tr>
<tr><td>H/W Reset</td><td>3Ch</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>


read display signal mode
MPU
Display
Dummy Read
Send 1st parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transfer

7.1.9 read display self-diagnostic result (0Fh)

<table>
<tr><th>0Fh</th><th colspan="10">read display self-diagnostic result</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display self-diagnostic result</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>(0Fh)</td></tr>
<tr><td>parameter</td><td>R</td><td>reg_load_det</td><td>func_det</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table><tr><th>Bit</th><th>Description</th><th>Action</th></tr><tr><td>reg_load_det</td><td>Register loading detection</td><td>Inverting the D7 bit if registers values loading work properly</td></tr><tr><td>func_det</td><td>Functionality detection</td><td>Inverting the D6 bit if the display is on function</td></tr><tr><td>others</td><td>-</td><td>Set to‘0’</td></tr></table>
“X”Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

7.1.10 sleep in (10h)

<table>
<tr><th>10h</th><th colspan="9">sleep in</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>sleep in</td><td>W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(10h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command causes the LCD module to enter the minimum power consumption mode.
In this mode the DC-DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped.
Interface and memory are still working and the memory keeps its contents.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h).
It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep in mode</td></tr><tr><td>S/W Reset</td><td>Sleep in mode</td></tr><tr><td>H/W Reset</td><td>Sleep in mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.1.11 sleep out (11h)

11h	sleep out									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
sleep out	W	0	0	0	1	0	0	0	1	(11h)
parameter	No Parameter									
Description	This command turn off sleep mode. In this mode the DC-DC converter is enabled, internal display oscillator is started, and panel scanning is started.									
Restriction	This command has no effect when module is already in sleep out mode. Sleep out mode can only be left by the sleep in command (10h). It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode)before sending an sleep in command. The display module runs the self-diagnostic functions after this command is received.									

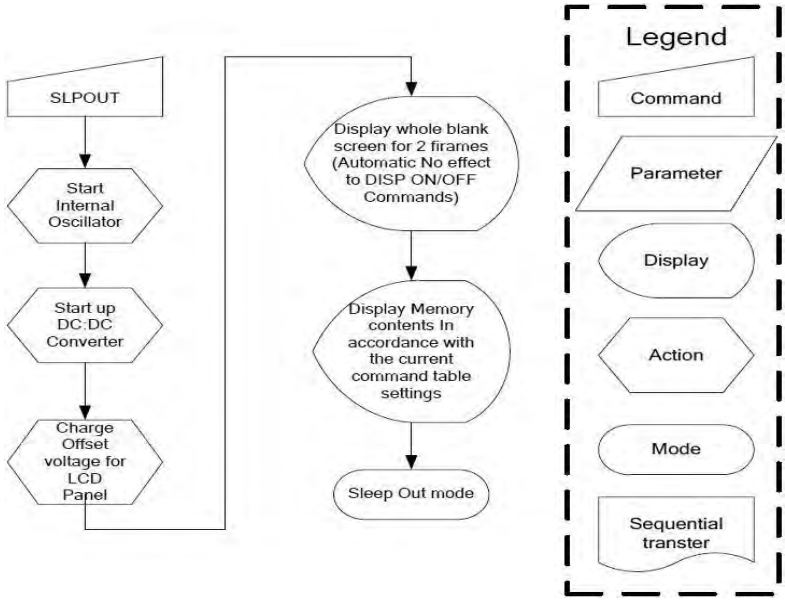
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart



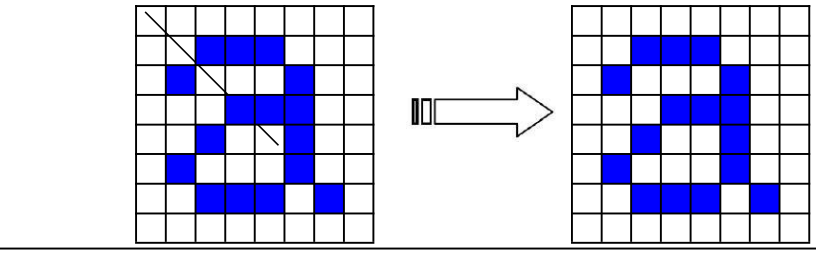
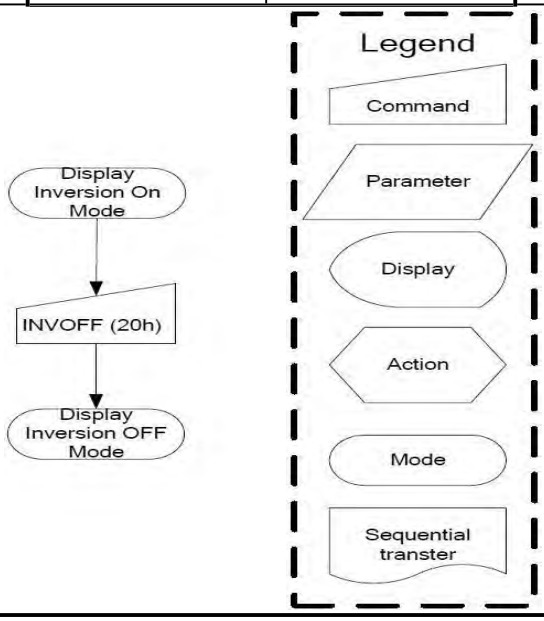
7.1.12 partial mode on (12h)

<table>
<tr><th>12h</th><th colspan="9">partial mode on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>partial mode on</td><td>W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>(12h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h).
To leave Partial mode, the Normal Display Mode On command (13h) should be written.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode on</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode on</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode on</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10">See Partial Area (30h).</td></tr>
</table>

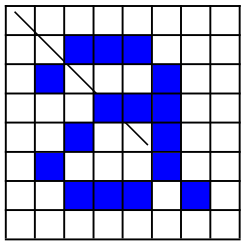
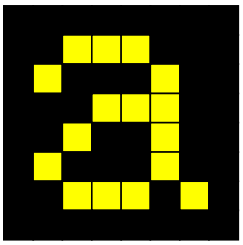
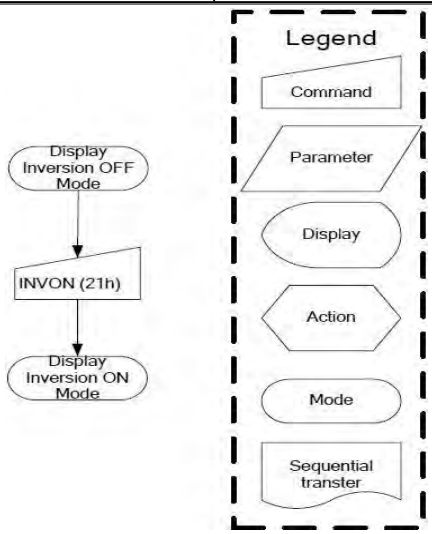
7.1.13 normal mode on and partial mode off (13h)

<table>
<tr><th>13h</th><th colspan="9">normal mode on and partial mode off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>normal mode on and partial mode off</td><td>W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(13h)</td></tr>
<tr><td>parameter</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="9">This command turns the display to normal mode.
Normal display mode on means partial mode off.
Exit from normal mode on by the partial mode on command.</td></tr>
<tr><td>Restriction</td><td colspan="9">This command has no effect when normal display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="9"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="9"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal display mode on</td></tr><tr><td>S/W Reset</td><td>Normal display mode on</td></tr><tr><td>H/W Reset</td><td>Normal display mode on</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="9">See Partial Area (30h).</td></tr>
</table>

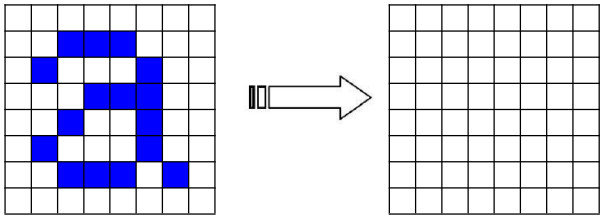
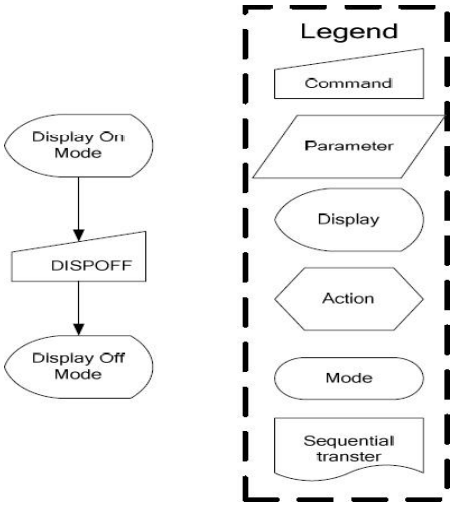
7.1.14 display inversion off (20h)

<table>
<tr><th>20h</th><th colspan="9">display inversion off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display inversion off</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(20h)</td></tr>
<tr><td>parameter</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to recover from display inversion mode.
(Example)
Top-Left(0,0) Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="9">This command has no effect when module is already in inversion off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="9"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="9"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="9"> 
</td></tr>
</table>

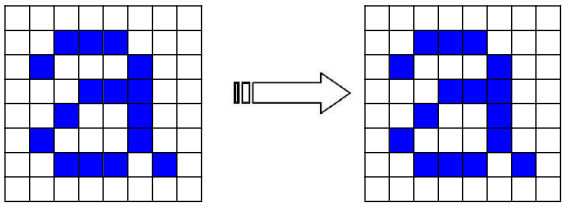
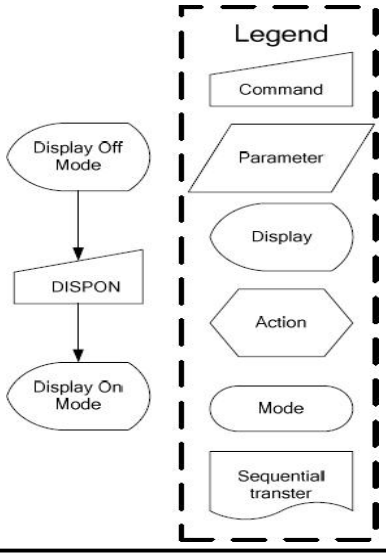
7.1.15 display inversion on (21h)

<table>
<tr><th>21h</th><th colspan="9">display inversion on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display inversion on</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(21h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into display inversion mode.
(Example)
Top-Left(0,0)
 
  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in inversion on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

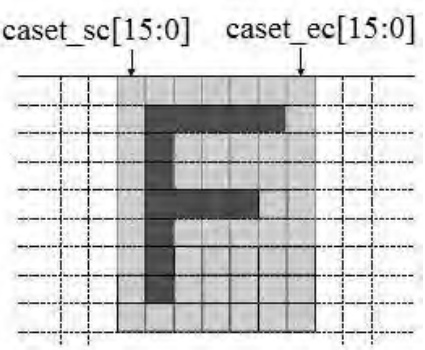
7.1.16 display off (28h)

<table>
<tr><th>28h</th><th colspan="9">display off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display off</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>(28h)</td></tr>
<tr><td>parameter</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to enter into display off mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
Exit from this command by Display On (29h) .
(Example)
Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="9">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="9"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="9"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>S/W Reset</td><td>Display off</td></tr><tr><td>H/W Reset</td><td>Display off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="9"> 
</td></tr>
</table>

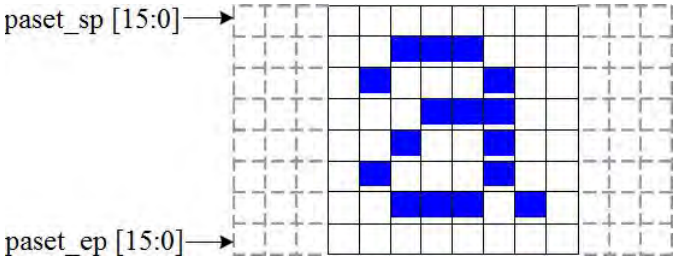
7.1.17 display on (29h)

<table>
<tr><th>29h</th><th colspan="9">display on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display on</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>(29h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from display off mode.
Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)
Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>S/W Reset</td><td>Display off</td></tr><tr><td>H/W Reset</td><td>Display off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.1.18 column address (2Ah)

<table>
<tr><th>2Ah</th><th colspan="10">column address</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>column address</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>(2Ah)</td></tr>
<tr><td>1st parameter</td><td>W</td><td colspan="8">caset_sc[15:8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td colspan="8">caset_sc[7:0]</td><td>00h</td></tr>
<tr><td>3rd parameter</td><td>W</td><td colspan="8">caset_ec[15:8]</td><td>00h</td></tr>
<tr><td>4th parameter</td><td>W</td><td colspan="8">caset_ec[7:0]</td><td>EFh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to define area of frame memory where system interface can access. This command makes no change on the other driver status.
The values of caset_sc[15:0] and caset_ec[15:0] are referred when memory write command comes. Each value represents one column line in the Frame Memory.
(Example)
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">caset_sc [15:0] always must be equal to or less than caset_ec [15:0].
When caset_sc [15:0] or caset_ec [15:0] is greater than maximum address like below, data of out of range will be ignored.
(Parameter range: 0 < caset_sc [15:0] < caset_ec [15:0] < =239(00EFh)): mv=”0”)
(Parameter range: 0 < caset_sc [15:0] < caset_ec [15:0] < =319(013Fh)): mv=”1”)</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>caset_sc[15:0]</th><th>caset_ec[15:0]</th></tr><tr><td>Power On Sequence</td><td>0000h</td><td>00EFh</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>If MADCTL’s D5=0: caset_ec[15:0]=00EFh
If MADCTL’s D5=1: caset_ec[15:0]=013Fh</td></tr><tr><td>H/W Reset</td><td>0000h</td><td>00EFh</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

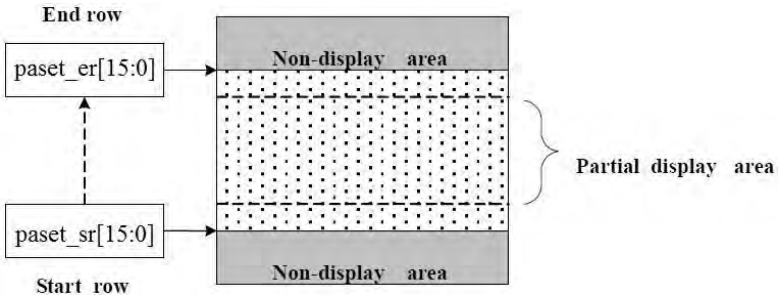
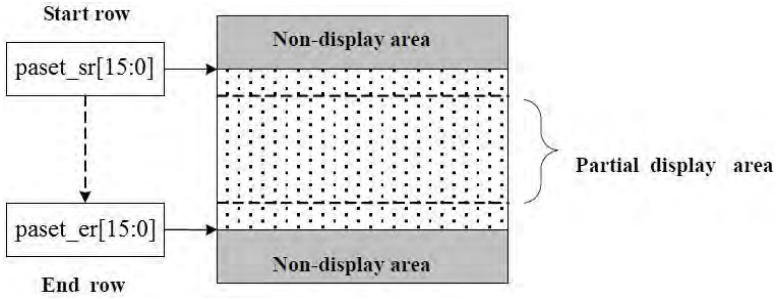
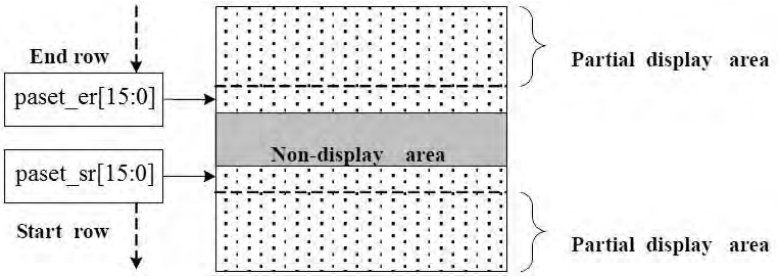
7.1.19 page address (2Bh)

<table>
<tr><th>2Bh</th><th colspan="9">page address</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>page address</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>(2Bh)</td></tr>
<tr><td>1st parameter</td><td>W</td><td colspan="8">paset_sp[15:8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td colspan="8">paset_sp[7:0]</td><td>00h</td></tr>
<tr><td>3rd parameter</td><td>W</td><td colspan="8">paset_ep[15:8]</td><td>01h</td></tr>
<tr><td>4th parameter</td><td>W</td><td colspan="8">paset_ep[7:0]</td><td>3Fh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to defined area of frame memory where system interface can access.
The value of paset_sp [15:0] and paset_ep [15:0] are referred when memory write command comes.
Each value represents one page line in the Frame Memory.
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">paset_sp[15:0] always must be equal to or less than paset_ep[15:0].
When paset_sp[15:0] or paset_ep[15:0] is greater than maximum address like below, data of out of range will be ignored.
(Parameter range: 0 < paset_sp[15:0] < paset_ep[15:0] <239 (00EFh)): mv=”1”)
(Parameter range: 0 < paset_sp[15:0] < paset_ep[15:0] <319 (013Fh)): mv=”0”)</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>paset_sp[15:0]</th><th>paset_ep[15:0]</th></tr><tr><td>Power On Sequence</td><td>0000h</td><td>013Fh</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>If MADCTL’s D5=0: paset_ep[15:0]=013Fh
If MADCTL’s D5=1: paset_ep[15:0]=00EFh</td></tr><tr><td>H/W Reset</td><td>0000h</td><td>013Fh</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.20 memory write (2Ch)

<table>
<tr><th>2Ch</th><th colspan="9">memory write</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>memory write</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(2Ch)</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to transfer data from MPU to frame memory.
When this command is accepted, the column register and the page register are reset to the start column/start page positions.
The start column/start page positions are different in accordance with MADCTL setting.
Sending any other command can stop frame write.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

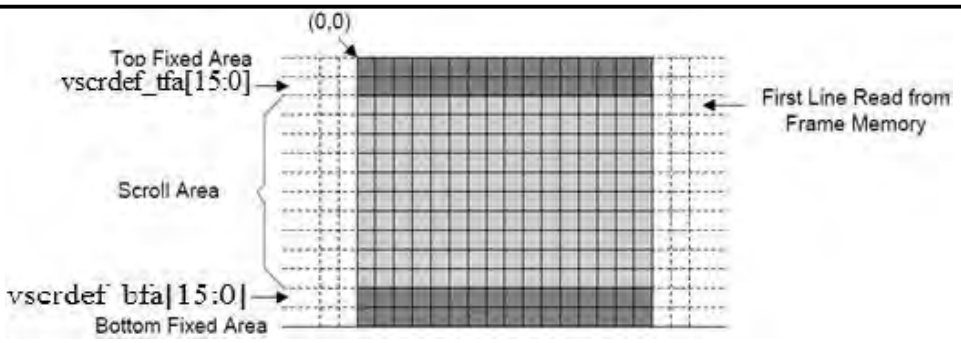
7.1.21 partial area (30h)

30h	partial area									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
partial area	W	0	0	1	1	0	0	0	0	(30h)
1st parameter	W								paset_sr[8]	00h
2nd parameter	W	paset_sr[7:0]								00h
3rd parameter	W								paset_er[8]	01h
4th parameter	W	paset_er[7:0]								3Fh
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (paset_sr[8:0]) and the second the End Row (paset_er[8:0]), as illustrated in the figures below. paset_sr[8:0] and paset_er[8:0] refer to the Frame Memory row address counter. If End Row > Start Row, when MADCTL ml='1'  If End Row > Start Row, when MADCTL ml='0'  If End Row < Start Row, when MADCTL ml='0'  If End Row = Start Row then the Partial Area will be one row deep.									
Restriction	paset_sr[15:0] and paset_er[15:0] cannot be 0000h nor exceed 013Fh.									

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>paset_sr[15:0]</th><th>paset_er[15:0]</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td><td>013Fh</td></tr>
<tr><td>S/W Reset</td><td>0000h</td><td>013Fh</td></tr>
<tr><td>H/W Reset</td><td>0000h</td><td>013Fh</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

7.1.22 vertical scrolling (33h)

33h	vertical scrolling									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
vertical scrolling	W	0	0	1	1	0	0	1	1	(33h)
1st parameter	W								vscrdef_tfa[8]	00h
2nd parameter	W	vscrdef_tfa[7:0]								00h
3rd parameter	W								vscrdef_vsa[8]	00h
4th parameter	W	vscrdef_vsa[7:0]								00h
5th parameter	W								vscrdef_bfa[8]	00h
6th parameter	W	vscrdef_bfa[7:0]								00h
Description	This command defines the Vertical Scrolling Area of the display. **When MADCTL ml = '0'** The 1st &2nd parameter vscrdef_tfa[8:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd &4th parameter vscrdef_vsa[8:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter vscrdef_bfa[8:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). vscrdef_tfa[8:0], vscrdef_vsa[8:0] and vscrdef_bfa[8:0] refer to the Frame Memory Line Pointer.									

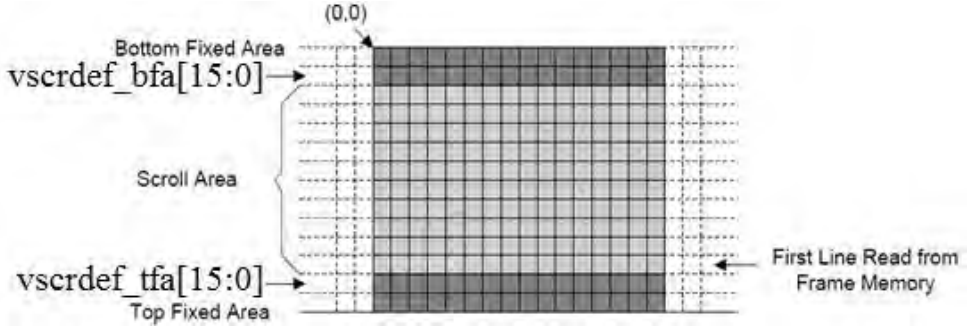


When MADCTL ml = '1'

The 1st &2nd parameter vscrdef_tfa[8:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd &4th parameter vscrdef_vsa[8:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th &6th parameter vscrdef_bfa[8:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



See also Section 8.2.2.2 and 8.2.2.3 for details of Vertical Scroll Mode and Vertical Scroll example.

Restriction

Register Availability

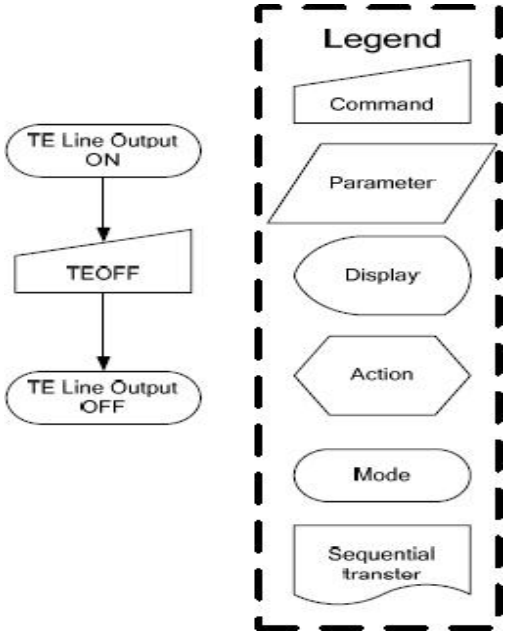
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

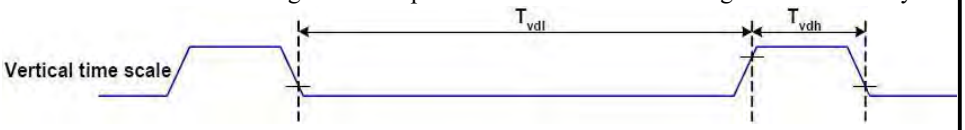
Status	Default Value		
	vscrdef_tfa[15:0]	vscrdef_vsa[15:0]	vscrdef_bfa[15:0]
Power On Sequence	0000h	0140h	0000h
S/W Reset	0000h	0140h	0000h
H/W Reset	0000h	0140h	0000h

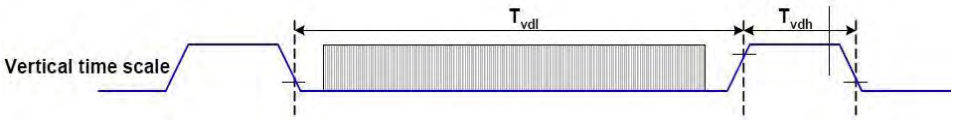
Flow Chart

7.1.23 tearing effect line off (34h)

<table>
<tr><th>34h</th><th colspan="9">tearing effect line off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>tearing effect line off</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(34h)</td></tr>
<tr><td>parameter</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.</td></tr>
<tr><td>Restriction</td><td colspan="9">This command has no effect when tearing effect output is already off.</td></tr>
<tr><td>Register Availability</td><td colspan="9"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="9"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Off</td></tr><tr><td>S/W Reset</td><td>Off</td></tr><tr><td>H/W Reset</td><td>Off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="9"> 
</td></tr>
</table>

7.1.24 tearing effect line on (35h)

<table>
<tr><th>35h</th><th colspan="9">tearing effect line on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>tearing effect line on</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(35h)</td></tr>
<tr><td>parameter</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>tem</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to turn on the Tearing Effect output signal from the TE signal line.
This output is not affected by changing MADCTL bit ml.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.
When tem =’0’: The Tearing Effect output line consists of V-Blanking information only:
 

When tem =’1’: The Tearing Effect output Line consists of both V-Blanking and H-Blanking information:
 

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when tearing effect output is already on.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

7.1.25 MADCTL(memory data access control) (36h)

36h	MADCTL(memory data access control)									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
MADCTL(memory data access control)	W	0	0	1	1	0	1	1	0	(36h)
parameter	W	my	mx	mv	ml	bgr	mh	X	X	00h
Description	This command defines read/write scanning direction of frame memory.									

Bit	name	Description
D7	my	Page Address Order
D6	mx	Column Address Order
D5	mv	Page/Column Order
D4	ml	Line Address Order
D3	bgr	RGB/BGR Order
D2	mh	Reserved

-Bit Assignment

Bit D7- Page Address Order

“0” = Top to Bottom (When MADCTL D7=”0”).

“1” = Bottom to Top (When MADCTL D7=”1”).

Bit D6- Column Address Order

“0” = Left to Right (When MADCTL D6=”0”).

“1” = Right to Left (When MADCTL D6=”1”).

Bit D5- Page/Column Order

“0” = Normal Mode (When MADCTL D5=”0”).

“1” = Reverse Mode (When MADCTL D5=”1”)

Bit D4- Line Address Order

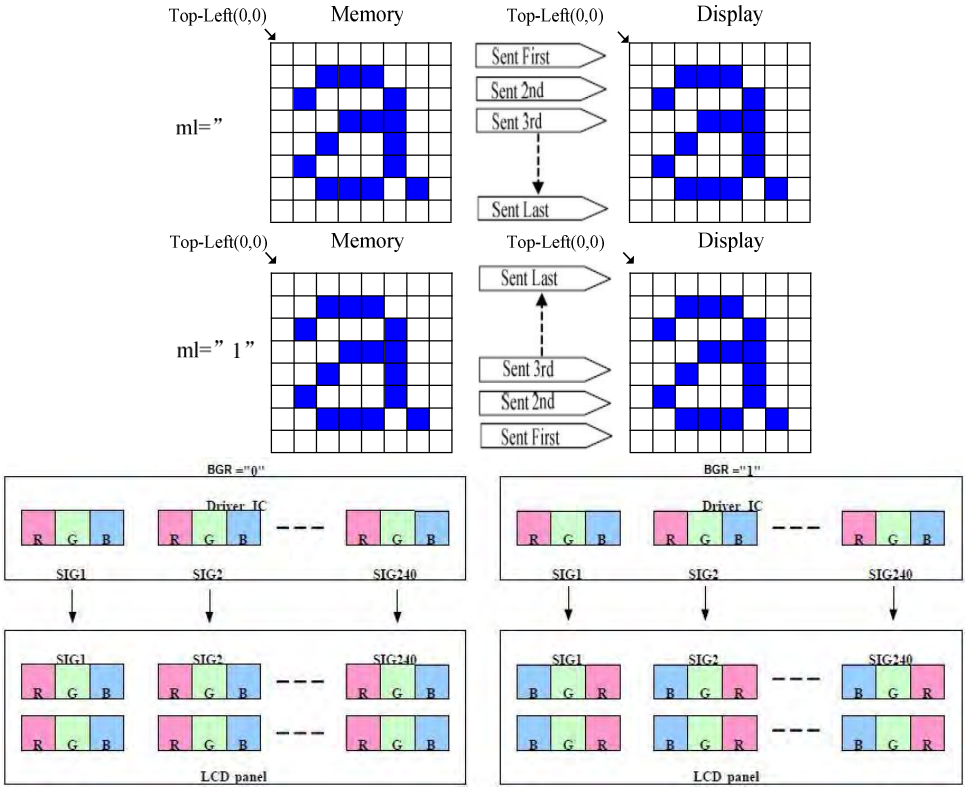
“0” = LCD Refresh Top to Bottom (When MADCTL D4=”0”)

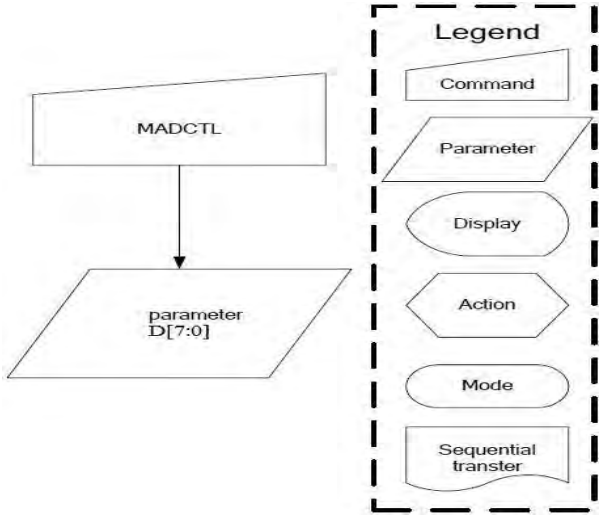
“1” = LCD Refresh Bottom to Top (When MADCTL D4=”1”)

Bit D3- RGB/BGR Order

“0” = RGB (When MADCTL D3=”0”)

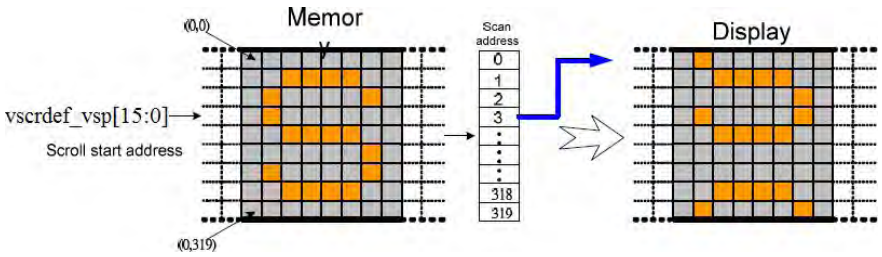
“1” = BGR (When MADCTL D3=”1”)

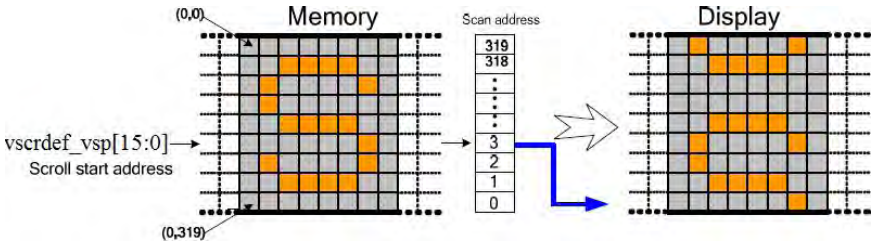


<table>
<tr><td></td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>no change</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

7.1.26 vertical scrolling start address (37h)

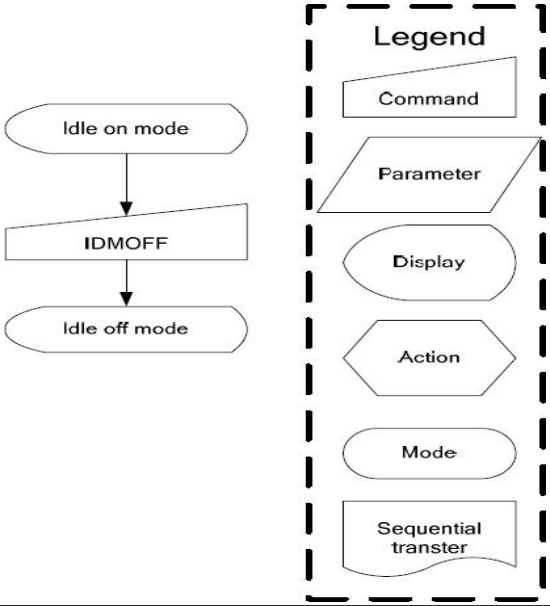
37h	vertical scrolling start address									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
vertical scrolling start address	W	0	0	1	1	0	1	1	1	(37h)
1st parameter	W								vscrdef_vsp[8]	00h
2nd parameter	W	vscrdef_vsp[7:0]								00h

<table>
<tr><td>Description</td><td>
This command is used together with Vertical scrolling (33h).
These two commands describe the scrolling area and the scrolling mode.
The Vertical scrolling start address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
When ml='0'
Example:
When Top Fixed Area = Bottom Fixed Area = 00, vertical scrolling area = 320 and vscrdef_vsp = '3'.


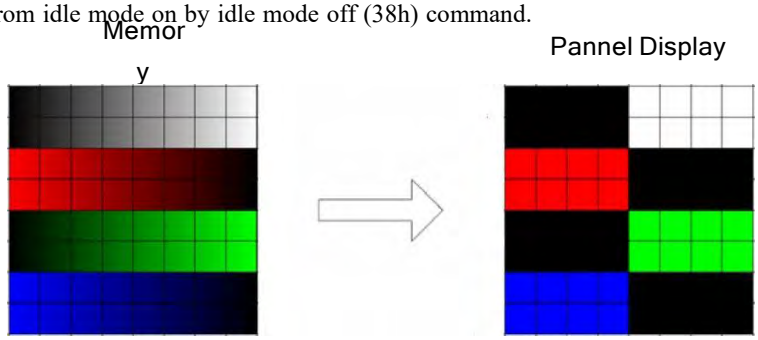
When ml='1'
Example:
When Top Fixed Area = Bottom Fixed Area = 00, vertical scrolling area = 320 and vscrdef_vsp = '3'.


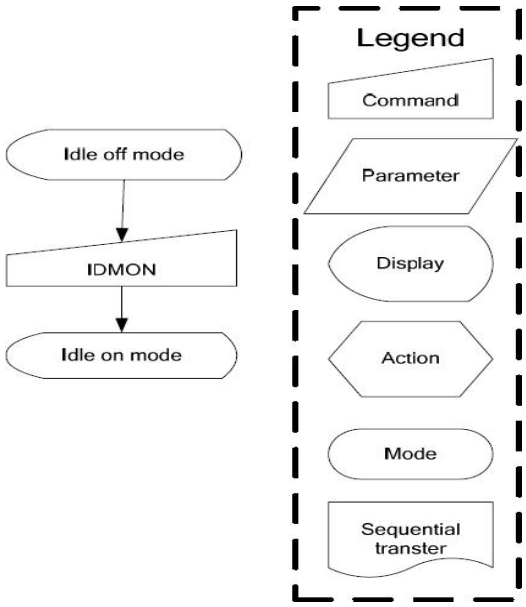
Note: When new pointer position and picture data are sent, the result on the display will happen at the next panel scan to avoid tearing effect.
Vscrdef_vsp refers to the Frame Memory line pointer.
</td></tr>
<tr><td>Restriction</td><td>Since the value of the vertical scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by vertical scrolling (33h)- otherwise undesirable image will be displayed on the panel).</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

7.1.27 idle mode off (38h)

<table>
<tr><th>38h</th><th colspan="9">idle mode off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>idle mode off</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>(38h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from idle mode on.
In the idle off mode
1. LCD can display 65k or 262k colors.
2. Normal frame frequency is applied.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode off</td></tr><tr><td>S/W Reset</td><td>Idle mode off</td></tr><tr><td>H/W Reset</td><td>Idle mode off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

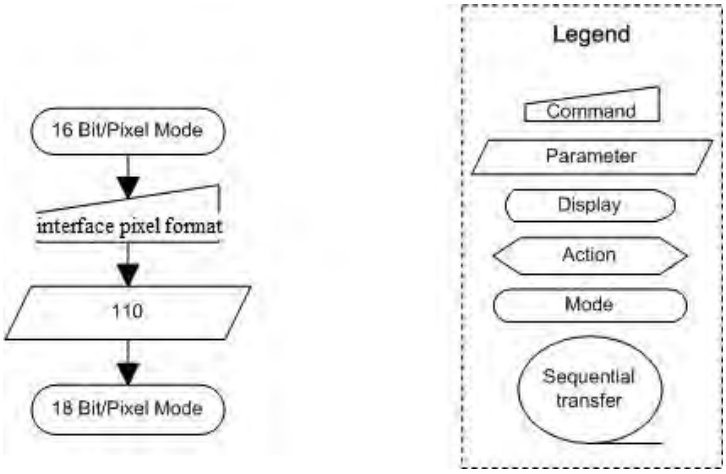
7.1.28 idle mode on and other mode off (39h)

<table>
<tr><th>39h</th><th colspan="9">idle mode on and other mode off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>idle mode on and other mode off</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>(39h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the idle on mode,
1. Color expression is reduced. The colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from idle mode on by idle mode off (38h) command.
 
<table><tr><th>Color</th><th>R5 R4 R3 R2 R1 R0</th><th>G5 G4 G3 G2 G1 G0</th><th>B5 B4 B3 B4 B1 B0</th></tr><tr><td>Black</td><td>0xxxxx</td><td>0xxxxx</td><td>0xxxxx</td></tr><tr><td>Blue</td><td>0xxxxx</td><td>0xxxxx</td><td>1xxxxx</td></tr><tr><td>Red</td><td>1xxxxx</td><td>0xxxxx</td><td>0xxxxx</td></tr><tr><td>Magenta</td><td>1xxxxx</td><td>0xxxxx</td><td>1xxxxx</td></tr><tr><td>Green</td><td>0xxxxx</td><td>1xxxxx</td><td>0xxxxx</td></tr><tr><td>Cyan</td><td>0xxxxx</td><td>1xxxxx</td><td>1xxxxx</td></tr><tr><td>Yellow</td><td>1xxxxx</td><td>1xxxxx</td><td>0xxxxx</td></tr><tr><td>White</td><td>1xxxxx</td><td>1xxxxx</td><td>1xxxxx</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in idle on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode off</td></tr><tr><td>S/W Reset</td><td>Idle mode off</td></tr><tr><td>H/W Reset</td><td>Idle mode off</td></tr></table></td></tr>
</table>

Flow Chart	 Idle off mode IDMON Idle on mode Legend Command Parameter Display Action Mode Sequential transter

7.1.29 pixel format (3Ah)

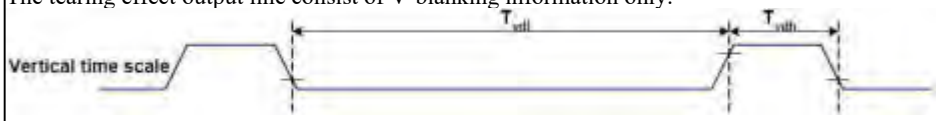
<table>
<tr><th>3Ah</th><th colspan="10">pixel format</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>pixel format</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>(3Ah)</td></tr>
<tr><td>1st Parameter</td><td>W</td><td>X</td><td colspan="3">dpi[2:0]</td><td>X</td><td colspan="3">dbi[2:0]</td><td>66h</td></tr>
<tr><td>Description</td><td colspan="10">dpi[2:0] is the pixel format select of RGB interface.
dbi[2:0] is the pixel format of system interface. If using RGB interface, serial interface must be selected.
<table>
<tr><th colspan="3">dpi[2:0]</th><th>RGB interface format</th><th colspan="3">dbi[2:0]</th><th>system interface format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>reserved</td><td>0</td><td>0</td><td>0</td><td>reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>reserved</td><td>0</td><td>0</td><td>1</td><td>reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>reserved</td><td>0</td><td>1</td><td>0</td><td>reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>reserved</td><td>0</td><td>1</td><td>1</td><td>12 bits/pixel</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>reserved</td><td>1</td><td>0</td><td>0</td><td>reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits/pixel</td><td>1</td><td>0</td><td>1</td><td>16 bits/pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits/pixel</td><td>1</td><td>1</td><td>0</td><td>18 bits/pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>reserved</td><td>1</td><td>1</td><td>1</td><td>reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">There is no visible effect until the Frame Memory is written to.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>66h</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>66h</td></tr>
</table></td></tr>
</table>

Flow Chart	Example: 

7.1.30 write memory continue (3Ch)

<table>
<tr><th>3Ch</th><th colspan="10">write memory continue</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>write memory continue</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(3Ch)</td></tr>
<tr><td>Description</td><td colspan="10">This command transfers image data from the host processor to the display module’s frame memory continuing from the pixel location following the previous write memory continue or memory write command.
If mv= ‘0’:
Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (caset_ec) value. The column register is then reset to caset_sc and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (paset_ep) value and the column register equals the caset_ec value, or the host processor sends another command. If the number of pixels exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1) the extra pixels are ignored.
If mv= ‘1’:
Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (paset_ep) value. The page register is then reset to paset_sp and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (caset_ec) value and the page register equals the paset_ep value, or the host processor sends another command. If the number of pixels exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1) the extra pixels are ignored.</td></tr>
<tr><td>Restriction</td><td colspan="10">A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

7.1.31 set tear scanline (44h)

<table>
<tr><th>44h</th><th colspan="10">set tear scanline</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>Set tear scan line</td><td>W</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(44h)</td></tr>
<tr><td>1st Parameter</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>sts[8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td colspan="8">sts[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command turns on the display module’s tearing effect output signal on the TE signal line when the display module reaches line sts.
The TE signal is not affected by changing mv.
The tearing effect line on has one parameter that describes the tearing effect output line mode.
The tearing effect output line consist of V-blanking information only.
 

Note:
That set tear scanline with sts = ‘0’ is equivalent to tearing effect line on with tear_mode= ‘0’.
The tearing effect output line shall be low when the display module is in sleep mode.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>S/W Reset</td><td>0000h</td></tr><tr><td>H/W Reset</td><td>0000h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.32 get tear scan line (45h)

<table>
<tr><th>45h</th><th colspan="10">get tear scan line</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>get tear scan line</td><td>W</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(45h)</td></tr>
<tr><td>1st Parameter</td><td>R</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>gts[8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>R</td><td colspan="8">gts[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">The display module returns the current scanline gts, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.When in sleep in mode, the value returned by get scanline is undefined.
“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>S/W Reset</td><td>0000h</td></tr><tr><td>H/W Reset</td><td>0000h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.33 write display brightess (53h)

<table>
<tr><th>53h</th><th colspan="10">write display brightess</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>write display brightess</td><td>W</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(53h)</td></tr>
<tr><td>1st Parameter</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>bl</td><td>X</td><td>X</td><td>04h</td></tr>
<tr><td>Description</td><td colspan="10">bl : Used to adjust the display brightness, This register is configured for interfaces only.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>S/W Reset</td><td>0000h</td></tr><tr><td>H/W Reset</td><td>0000h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.34 read display brightess (54h)

<table>
<tr><th>54h</th><th colspan="9">read display brightess</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display brightess</td><td>W</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(54h)</td></tr>
<tr><td>1st Parameter</td><td>R</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>bl</td><td>X</td><td>X</td><td>04h</td></tr>
<tr><td>Description</td><td colspan="10">Used to read the value of the bl register.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>S/W Reset</td><td>0000h</td></tr><tr><td>H/W Reset</td><td>0000h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.35 read idd3 (D3h)

<table>
<tr><th>D3h</th><th colspan="10">read idd3</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read idd3</td><td>W</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(D3h)</td></tr>
<tr><td>1st parameter</td><td>R</td><td colspan="8">id4[7:0]</td><td>30h</td></tr>
<tr><td>2nd parameter</td><td>R</td><td colspan="8">Id5[7:0]</td><td>30h</td></tr>
<tr><td>3rd parameter</td><td>R</td><td colspan="8">Id6[7:0]</td><td>01h</td></tr>
<tr><td>Description</td><td colspan="10">This read byte returns 24-bits display identification information.
Id4/5/6:LCD module/driver ID.
Id4 can be configured using OTP address 7BH, 7CH, and 7DH.
Id5 can be configured using OTP address 7EH,7FH, and 80H.
Id6 can be configured using OTP address 81H,82H, and 83H.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.36 read display id 1 (DAh)

DAh	read display id 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display id 1	W	1	1	0	1	1	0	1	0	(DAh)
1st parameter	R	id1[7:0]								30h
Description	id1[7:0]:LCD module/driver ID. Id1 can be configured using OTP address 1H, 4H, and 7H.									
Restriction	-									

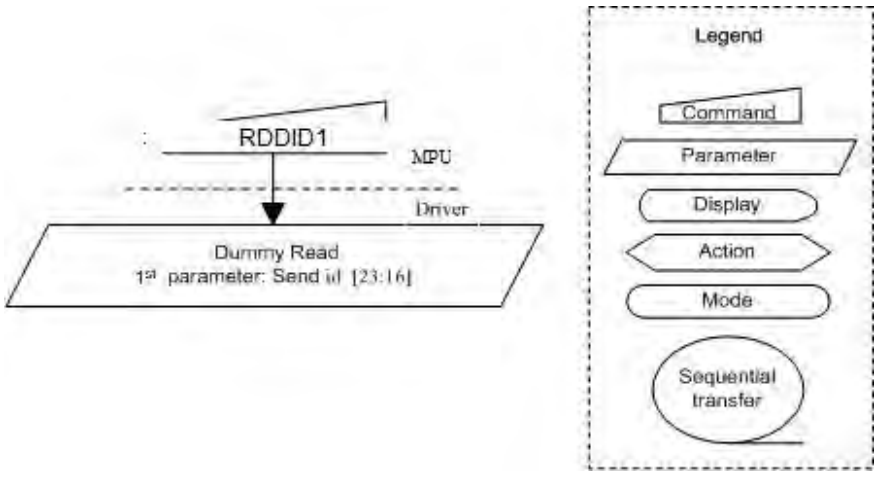
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

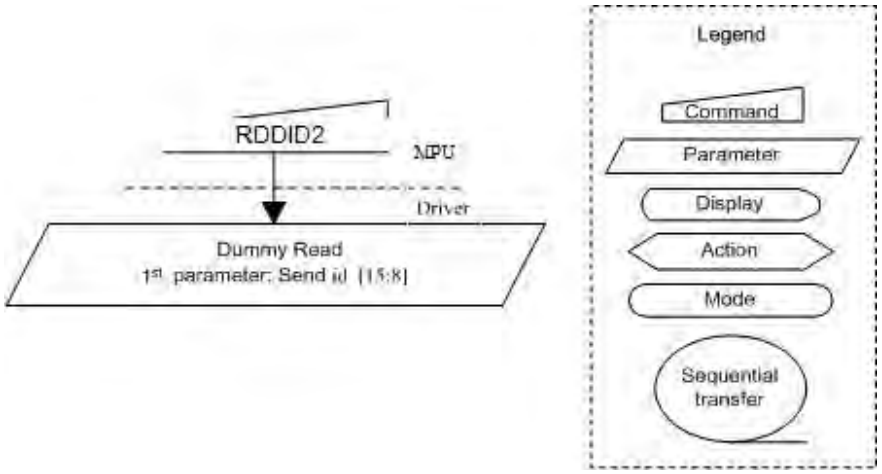
Default

Status	Default Value
Power On Sequence	30h
S/W Reset	30h
H/W Reset	30h

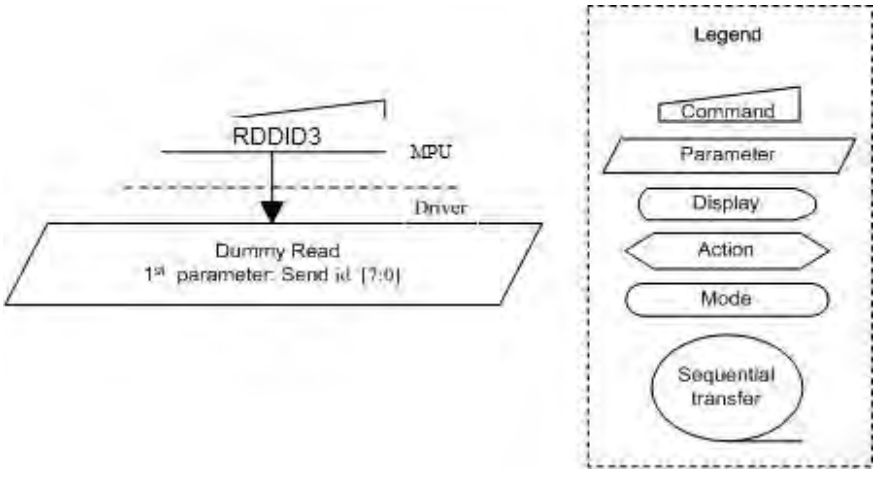
Flow Chart



7.1.37 read display id 2 (DBh)

<table>
<tr><td>DBh</td><td colspan="10">read display id 2</td></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display id 2</td><td>W</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>(DBh)</td></tr>
<tr><td>1st parameter</td><td>R</td><td colspan="8">id2[7:0]</td><td>30h</td></tr>
<tr><td>Description</td><td colspan="10">id2[7:0]:LCD module/driver ID.
Id2 can be configured using OTP address 2H, 5H, and 8H.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>30h</td></tr><tr><td>S/W Reset</td><td>30h</td></tr><tr><td>H/W Reset</td><td>30h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.1.38 read display id 3 (DCh)

<table>
<tr><td>DCh</td><td colspan="10">read display id 3</td></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display id 3</td><td>W</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(DCh)</td></tr>
<tr><td>1st parameter</td><td>R</td><td colspan="8">id3[7:0]</td><td>01h</td></tr>
<tr><td>Description</td><td colspan="10">id3[7:0]:LCD module/driver ID.
Id3 can be configured using OTP address 3H, 6H, and 9H.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>01h</td></tr><tr><td>S/W Reset</td><td>01h</td></tr><tr><td>H/W Reset</td><td>01h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.2 Private command

When enter read/write private register,need send 06h, 08h to FDh register;When exit read/write private register,need send fah, fch to FDh register.

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
osc setting	W	0	1	1	0	0	0	0	0	(60h)
	W					osc_user_adj[3:0]				01h
dvdd setting	W	0	1	1	0	0	0	0	1	(61h)
	W				vdd_dly		vdd_adj[2:0]			00h
	W						vdd_slp_adj[2:0]			00h
bias setting	W	0	1	1	0	0	0	1	0	(62h)
	W					ibias_bg_adj[3:0]				00h
	W		ibias_sd_gma_adj[2:0]				ibias_gma_ref_adj[2:0]			44h
	W		ibias_pump_adj[2:0]				ibias_test_nlsh_adj[2:0]			44h
	W					vref_adj[3:0]				00h
vgl setting	W	0	1	1	0	0	0	1	1	(63h)
	W		Pump5_clamp_en		Pump5_sel		Pump5_trim[2:0]			41h
	W						Pump5_clamp[2:0]			02h
vgh setting	W	0	1	1	0	0	1	0	0	(64h)
	W			Pump4_sel[1:0]			Pump4_clamp[2:0]			25h
	W		Pump4_trim[2:0]				Pump4_clamp_en			01h
VSP setting	W	0	1	1	0	0	1	0	1	(65h)
	W					Pump1_clamp_en		Pump1_clamp[1:0]		09h
VSN setting	W	0	1	1	0	0	1	1	0	(66h)
	W					Pump2_clamp_en		Pump2_clamp[1:0]		09h

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
pump clock sel	W	0	1	1	0	0	1	1	1	(67h)
	W		vgh_pump_sel[2:0]				mv_pump_sel[2:0]			22h
	W		vgl_pump_sel[2:0]							40h
gamma ref 1	W	0	1	1	0	1	0	0	0	(68h)
	W	VAP[7:0]								90h
	W	VAN[7:0]								30h
	W		VCMP[6:0]							27h
	W		VCOM_OFC[6:0]							21h
OTP setting	W	0	1	1	0	1	1	0	0	(6ch)
	W						reg_otp_v_sel		reg_otp_en	00h
lvd setting	W	0	1	1	0	1	1	0	1	(6dh)
	W		lvd_vgh_clk_en	lvd_vgh_sel_en	lvd_width[1:0]		lvd_sel[1:0]		lvd_en	60h
RGB interface control	W	1	0	1	1	0	0	0	0	(B0h)
	W		rcm[1:0]			vspl	hspl	dpl	epl	40h
frame rate	W	1	0	1	1	0	0	0	1	(B1h)
	W			fr_h[5:0]						0fh
	W				fr_v[4:0]					02h
	W						fr_div[2:0]			04h
display pol control	W	1	0	1	1	0	1	0	0	(B4h)
	W						dinv[2:0]			02h
blanking porch	W	1	0	1	1	0	1	0	1	(B5h)
	W		vfp[6:0]							02h
	W		vbp[6:0]							02h
	W		hfp[6:0]							0Ah
	W		hbp[6:0]							14h

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
display function	W	1	0	1	1	0	1	1	0	(B6h)
	W		rev		sm		ptg		pts	04h
	W		gs		ss				normal_ black	00h
	W	nl[7:0]								9fh
	W	scn[7:0]								00h
	W					isc[3:0]				02h
entry mode set	W	1	0	1	1	0	1	1	1	(B7h)
	W						gon	dte		06h
OTP_CTRL0	W	1	1	0	0	0	0	1	0	(c2h)
	W	vpp_src_sel	OTP_SEL	VPP_SEL	PRD	PWE	PTM[1:0]		PPROG	00h
OTP_CTRL1	W	1	1	0	0	0	0	1	1	(c3h)
	W	PA[7:0]								00h
OTP_CTRL2	W	1	1	0	0	0	1	0	0	(c4h)
	W	PDIN1[7:0]								ffh
OTP_CTRL3	W	1	1	0	0	0	1	1	0	(c6h)
	W		TPPS_ADJ	TAS_ADJ	TAH_ADJ	TDH_ADJ	TPPR_ADJ	TPW_ADJ[9:8]		00h
OTP_CTRL4	W	1	1	0	0	0	1	1	1	(c7h)
	W	TVR_ADJ[7:0]								02h
OTP_CTRL5	W	1	1	0	0	1	0	0	0	(c8h)
	W	TPW_ADJ[7:0]								6eh
OTP_CTRL8	W	1	1	0	0	1	0	0	1	(c9h)
	R	OTP_RD_DAT								
OTP_CTRL6	W	1	1	0	0	1	0	1	0	(cah)
	W							ONE_PROG_SEL[1:0]		00h
gamma positive 1	W	1	1	1	0	0	0	0	0	(E0h)
	W				pkp0[4:0]					15h
	W				pkp1[4:0]					14h
	W				pkp2[4:0]					13h
	W				pkp3[4:0]					16h
	W				pkp4[4:0]					16h
	W				pkp5[4:0]					14h
	W				pkp6[4:0]					13h
	W				pkp7[4:0]					0ch
gamma positive 2	W	1	1	1	0	0	0	0	1	(E1h)
	W		prp0[6:0]							41h
	W		prp1[6:0]							50h

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma positive 3	W	1	1	1	0	0	0	1	0	(E2h)
	W			vrp0[5:0]						00h
	W			vrp1[5:0]						25h
	W			vrp2[5:0]						2dh
	W			vrp3[5:0]						14h
	W			vrp4[5:0]						1ch
	W			vrp5[5:0]						3fh
gamma negative 1	W	1	1	1	0	0	0	1	1	(E3h)
	W				pkn0[4:0]					06h
	W				pkn1[4:0]					10h
	W				pkn2[4:0]					14h
	W				pkn3[4:0]					16h
	W				pkn4[4:0]					16h
	W				pkn5[4:0]					13h
	W				pkn6[4:0]					13h
	W				pkn7[4:0]					13h
gamma negative 2	W	1	1	1	0	0	1	0	0	(E4h)
	W		prn0[6:0]							64h
	W		prn1[6:0]							41h
gamma negative 3	W	1	1	1	0	0	1	0	1	(E5h)
	W			vrn0[5:0]						3fh
	W			vrn1[5:0]						1ch
	W			vrn2[5:0]						14h
	W			vrn3[5:0]						2dh
	W			vrn4[5:0]						25h
	W			vrn5[5:0]						00h
SRC_CTRL1	W	1	1	1	0	0	1	1	0	(E6h)
	W	chk_cnt_inv	chk_data_h	chk_cnt_sel					SC_EN_START[8]	00h
	W	SC_EN_START[7:0]								f0h
SRC_CTRL2	W	1	1	1	0	0	1	1	1	(E7h)
	W					CS_START[3:0]				01h
	W						scdt_inv_sel		cs_vp_en	04h
	W	CS1_WIDTH[7:0]								12h
	W	CS2_WIDTH[7:0]								12h
	W	PREC_START[7:0]								06h
	W	PREC_WIDTH[7:0]								1fh

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
SRC_CTRL3	W	1	1	1	0	1	0	0	0	(E8h)
	W	vdds_oe								00h
	W		chopper_sel[2:0]							40h
	W		gchopper_sel[2:0]							00h
Charge Share	W	1	1	1	0	1	0	0	1	(E9h)
	W								CS_FLAG	00h
SRC_CTRL4	W	1	1	1	0	1	0	1	0	(EAh)
	W					PNCS_SEL[1:0]			PNCS_EN	0dh
	W	PNCS_WIDTH[7:0]								12h
Gate driver timing	W	1	1	1	0	1	1	0	0	(ECh)
	W	gate_oe_setup[3:0]				gate_oe_hold[3:0]				47h
tearing effect	W	1	1	1	1	0	0	0	1	(F1h)
	W							te_pol	tem_extend	00h
	W	te_v_start[7:0]								01h
	W	te_v_end[7:0]								1fh
	W	te_h_start[7:0]								01h
	W	te_h_end[7:0]								3fh
led	W	1	1	1	1	0	0	1	0	(F2h)
	W					ledpwm_oe	ledpwm	ledon_oe	ledon	0eh
rgb sync width	W	1	1	1	1	0	1	0	0	(F4h)
	W		vsync_width[6:0]							00h
	W		hsync_width[6:0]							00h
interface control	W	1	1	1	1	0	1	1	0	(F6h)
	W	my_eor	mx_eor	mv_eor	0	bgr_eor	0	0	we_mode	01h
	W	cs_delay_sel[1:0]		epf[1:0]				mdt[1:0]		10h
	W		endian			dm[1:0]			rim	00h
	W		spi_2wire_mode						rm	00h
color palette enable	W	1	1	1	1	1	0	1	1	(FBh)
	W							cpe1	cpe0	00h
color palette data	W	1	1	1	1	1	1	0	0	(FCh)
	W	cps[1:0]		cpd[5:0]						00h
private access	W	1	1	1	1	1	1	0	1	(FDh)
	W	private_access[15:8]								00h
	W	private_access[7:0]								00h

7.2.1 osc setting (60h)

<table>
<tr><th>60h</th><th colspan="10">osc setting</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>osc setting</td><td>W</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(60h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td></td><td></td><td></td><td></td><td colspan="4">osc_user_adj[3:0]</td><td>01h</td></tr>
<tr><td>Description</td><td colspan="10">osc_user_adj[3:0]: Osc clock frequency adjust registers.
<table>
<tr><th>osc_user_adj[3:0]</th><th>Freq(MHz)</th><th>osc_user_adj[3:0]</th><th>freq(MHz)</th></tr>
<tr><td>0000</td><td>45.64</td><td>1000</td><td>43.31</td></tr>
<tr><td>0001</td><td>47.85</td><td>1001</td><td>41.57</td></tr>
<tr><td>0010</td><td>49.54</td><td>1010</td><td>40.29</td></tr>
<tr><td>0011</td><td>52.41</td><td>1011</td><td>38.84</td></tr>
<tr><td>0100</td><td>54.44</td><td>1100</td><td>37.95</td></tr>
<tr><td>0101</td><td>57.73</td><td>1101</td><td>36.55</td></tr>
<tr><td>0110</td><td>60.3</td><td>1110</td><td>35.54</td></tr>
<tr><td>0111</td><td>64.68</td><td>1111</td><td>34.45</td></tr>
</table></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>01h</td></tr>
<tr><td>S/W Reset</td><td>no change</td></tr>
<tr><td>H/W Reset</td><td>01h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.2 dvdd setting (61h)

<table>
<tr><th>61h</th><th colspan="10">dvdd setting</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>dvdd setting</td><td>W</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(61h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td></td><td></td><td></td><td>vdd_dly</td><td></td><td colspan="3">vdd_adj[2:0]</td><td>00h</td></tr>
<tr><td>2st parameter</td><td>W</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">vdd_slp_adj[2:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">vdd_dly: Select whether to delay vdd_en by 40us.
vdd_adj[1:0]:VDD setting is as below:
<table><tr><th>vdd_adj[2:0]</th><th>Value(V)</th><th>vdd_slp_adj[2:0]</th><th>Value(V)</th></tr><tr><td>000</td><td>1.532</td><td>000</td><td>1.53</td></tr><tr><td>001</td><td>1.478</td><td>001</td><td>1.47</td></tr><tr><td>010</td><td>1.427</td><td>010</td><td>1.41</td></tr><tr><td>011</td><td>1.38</td><td>011</td><td>1.35</td></tr><tr><td>100</td><td>1.578</td><td>100</td><td>1.29</td></tr><tr><td>101</td><td>1.628</td><td>101</td><td>1.59</td></tr><tr><td>110</td><td>1.68</td><td>110</td><td>1.64</td></tr><tr><td>111</td><td>1.736</td><td>111</td><td>1.7</td></tr></table></td></tr>
<tr><td></td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>no change</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.3 bias setting (62h)

62h	bias setting									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
bias setting	W	0	1	1	0	0	0	1	0	(62h)
1st parameter	W					ibias_bg_adj[3:0]				00h
2st parameter	W		ibias_sd_gma_adj[2:0]				ibias_gma_ref_adj[2:0]			44h
3st parameter	W		ibias_pump_adj[2:0]				ibias_test_nlsh_adj[2:0]			44h
4st parameter	W					vref_adj[3:0]				00h

Description

ibias_bg_adj[3:0]	VBGR	vref_adj[3:0]	VREF2V
0000	1.3124	0000	2
0001	1.3215	0001	1.98
0010	1.331	0010	1.96
0011	1.3401	0011	1.94
0100	1.3499	0100	1.92
0101	1.359	0101	1.9
0110	1.3685	0110	1.88
0111	1.3776	0111	1.82
1000	1.3024	1000	2.02
1001	1.2932	1001	2.05
1010	1.2838	1010	2.07
1011	1.2746	1011	2.09
1100	1.2649	1100	2.11
1101	1.2557	1101	2.13
1110	1.2463	1110	2.15
1111	1.2371	1111	2.19

ibias_sd_gma_adj[2:0]	I_current	ibias_gma_ref_adj[2:0]	I_current
000	0.28uA	000	0.28uA
001	0.385uA	001	0.385uA
010	0.44uA	010	0.44uA
011	0.513uA	011	0.513uA
100	0.615uA	100	0.615uA
101	0.768uA	101	0.768uA
110	1.022uA	110	1.022uA
111	1.49uA	111	1.49uA
控制TESTI/SD_SOP電流		控制VAP/VAN/VCMP/N_LSH<0>電流	

ibias_pump_adj[2:0]	I_current	ibias_test_nlsh_adj[2:0]	I_current
000	0.28uA	000	0.28uA
001	0.385uA	001	0.385uA
010	0.44uA	010	0.44uA
011	0.513uA	011	0.513uA
100	0.615uA	100	0.615uA
101	0.768uA	101	0.768uA

<table>
<tr><td></td><td>
<table>
<tr><td>110</td><td>1.022uA</td><td>110</td><td>1.022uA</td></tr>
<tr><td>111</td><td>1.49uA</td><td>111</td><td>1.49uA</td></tr>
<tr><td colspan="2">控制PUMP電流</td><td colspan="2">控制N_LSH<1>/GMA電流</td></tr>
</table>
</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

7.2.4 vgl setting(63h)

<table>
<tr><th>63h</th><th colspan="10">vgl setting</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>vgl setting</td><td>W</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(63h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td>X</td><td>Pump5_clamp_en</td><td></td><td>Pump5_sel</td><td></td><td colspan="3">Pump5_trim[2:0]</td><td>41h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td>X</td><td></td><td></td><td></td><td></td><td colspan="3">Pump5_clamp[2:0]</td><td>02h</td></tr>
<tr><td>Description</td><td colspan="10">
PUMP5_CLAMP_EN: Enable VGL clamp level.
<table>
<tr><th>Pump5_clamp_en</th><th>VGL clamp function</th></tr>
<tr><td>0</td><td>Disable</td></tr>
<tr><td>1</td><td>Enable</td></tr>
</table>
PUMP5_SEL: Sets the factor used in the step-up circuits for VGL.
Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.
<table>
<tr><th>Pump5_sel</th><th>VGL OUTPUT</th></tr>
<tr><td>0</td><td>VGL Pump to -5*VCI</td></tr>
<tr><td>1</td><td>VGL Pump to -6*VCI</td></tr>
</table>
Pump5_trim[2:0]: VSN voltage adjustment.
<table>
<tr><th>Pump5_trim[2:0]</th><th>VSN(unit:V)</th></tr>
<tr><td>000</td><td>-10.3</td></tr>
<tr><td>001</td><td>-10.11</td></tr>
<tr><td>010</td><td>-10</td></tr>
<tr><td>011</td><td>-9.92</td></tr>
<tr><td>100</td><td>-10.5</td></tr>
<tr><td>101</td><td>-10.7</td></tr>
<tr><td>110</td><td>-10.9</td></tr>
<tr><td>111</td><td>-10.3</td></tr>
</table>
PUMP5_CLAMP: Sets the VGL clamp level.
<table>
<tr><th>Pump5_clamp[2:0]</th><th>VGL clamp level(V)</th></tr>
<tr><td>000</td><td>-9.0</td></tr>
<tr><td>001</td><td>-9.5</td></tr>
<tr><td>010</td><td>-10.0</td></tr>
<tr><td>011</td><td>-10.5</td></tr>
<tr><td>100</td><td>-11.0</td></tr>
<tr><td>101</td><td>-11.5</td></tr>
<tr><td>110</td><td>-12</td></tr>
<tr><td>111</td><td>-12.5</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td></td><td></td><td><table>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td><td></td></tr>
<tr><td>Default</td><td colspan="3"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="3"></td></tr>
</table>

7.2.5 vgh setting (64h)

<table>
<tr><td>64h</td><td colspan="10">vgh setting</td></tr>
<tr><td>Inst / Para</td><td>WR</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>vgh setting</td><td>W</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(64h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td></td><td></td><td colspan="2">Pump4_sel[1:0]</td><td></td><td colspan="3">Pump4_clamp[2:0]</td><td>25h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td></td><td colspan="3">Pump4_trim[2:0]</td><td></td><td colspan="2">Pump4_clamp_en</td><td></td><td>01h</td></tr>
<tr><td>Description</td><td colspan="10">
PUMP4_SEL: Sets the factor used in the step-up circuits for VGH.
Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.
<table>
<tr><th>PUMP4_SEL[1:0]</th><th>VGH OUTPUT</th></tr>
<tr><td>00</td><td>5*VCI</td></tr>
<tr><td>01</td><td>6*VCI</td></tr>
<tr><td>10</td><td>7*VCI</td></tr>
<tr><td>11</td><td>8*VCI</td></tr>
</table>
PUMP4_CLAMP: Sets the VGH clamp level.
<table>
<tr><th>PUMP4_CLAMP[2:0]</th><th>VGH clamp level(V)</th></tr>
<tr><td>000</td><td>12.5</td></tr>
<tr><td>001</td><td>13</td></tr>
<tr><td>010</td><td>13.5</td></tr>
<tr><td>011</td><td>14</td></tr>
<tr><td>100</td><td>14.5</td></tr>
<tr><td>101</td><td>15</td></tr>
<tr><td>110</td><td>15.5</td></tr>
<tr><td>111</td><td>16</td></tr>
</table>
Pump4_trim[2:0]: HV-regulator VGH voltage adjustment.
<table>
<tr><th>PUMP4_TRIM[2:0]</th><th>VGH(umit:V)</th></tr>
<tr><td>000</td><td>15</td></tr>
<tr><td>001</td><td>14.8</td></tr>
<tr><td>010</td><td>14.6</td></tr>
<tr><td>011</td><td>14.4</td></tr>
<tr><td>100</td><td>15.2</td></tr>
<tr><td>101</td><td>15.4</td></tr>
<tr><td>110</td><td>15.7</td></tr>
<tr><td>111</td><td>15</td></tr>
</table>
PUMP4_CLAMP_EN: Enable VGH camp level.
<table>
<tr><th>PUMP4_CLAMP_EN</th><th>VGH clamp function</th></tr>
<tr><td>0</td><td>Disable</td></tr>
<tr><td>1</td><td>Enable</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.6 vsp setting (65h)

<table>
<tr><td>65h</td><td colspan="10">vsp setting</td></tr>
<tr><td>Inst / Para</td><td>WR</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>vsp setting</td><td>W</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(65h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td></td><td></td><td></td><td></td><td>Pump1_clamp_en</td><td></td><td colspan="2">Pump1_clamp[1:0]</td><td>09h</td></tr>
<tr><td>Description</td><td colspan="10">PUMP1_CLAMP_EN :
<table><tr><th>PUMP1_CLAMP_EN</th><th>Status</th></tr><tr><td>0</td><td>Disable VSP pump clamp function</td></tr><tr><td>1</td><td>Enable VSP pump clamp function</td></tr></table>
PUMP1_CLAMP[1:0]: Set the VSP clamp level.
<table><tr><th colspan="2">PUMP1_CLAMP</th><th>VSP clamp level(V)</th></tr><tr><td>0</td><td>0</td><td>6.2</td></tr><tr><td>0</td><td>1</td><td>6.4</td></tr><tr><td>1</td><td>0</td><td>6.6</td></tr><tr><td>1</td><td>1</td><td>6.8</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.7 vsn setting (66h)

<table>
<tr><th>66h</th><th colspan="10">vsn setting</th></tr>
<tr><td>Inst / Para</td><td>WR</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>vsn setting</td><td>W</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>(66h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td></td><td></td><td></td><td></td><td>Pump2_clamp_en</td><td></td><td colspan="2">Pump2_clamp[1:0]</td><td>09h</td></tr>
<tr><td>Description</td><td colspan="10">PUMP2_CLAMP_EN :
<table><tr><th>PUMP2_CLAMP_EN</th><th>Status</th></tr><tr><td>0</td><td>Disable VSN pump clamp function</td></tr><tr><td>1</td><td>Enable VSN pump clamp function</td></tr></table>PUMP2_CLAMP[1:0]: Set the VSN clamp level.<table><tr><th colspan="2">PUMP2_CLAMP</th><th>VSN clamp level(V)</th></tr><tr><td>0</td><td>0</td><td>-3.8</td></tr><tr><td>0</td><td>1</td><td>-4.0</td></tr><tr><td>1</td><td>0</td><td>-4.2</td></tr><tr><td>1</td><td>1</td><td>-4.4</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.8 pump clock sel (67h)

<table>
<tr><th>67h</th><th colspan="10">pump clock sel</th></tr>
<tr><td>Inst / Para</td><td>WR</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>pump clock sel</td><td>W</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>(67h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td></td><td colspan="3">vgh_pump_sel[2:0]</td><td></td><td colspan="3">mv_pump_sel[2:0]</td><td>22h</td></tr>
<tr><td>2st parameter</td><td>W</td><td></td><td colspan="3">vgl_pump_sel[2:0]</td><td></td><td></td><td></td><td></td><td>40h</td></tr>
<tr><td>Description</td><td colspan="10">
<table>
<tr><th></th><th>vgh_pump_sel</th><th>vgl_pump_sel</th><th>mv_pump_sel</th></tr>
<tr><td>000</td><td>16 div</td><td>22 div</td><td>12 div</td></tr>
<tr><td>001</td><td>20 div</td><td>30 div</td><td>16 div</td></tr>
<tr><td>010</td><td>24 div</td><td>38 div</td><td>20 div</td></tr>
<tr><td>011</td><td>28 div</td><td>48 div</td><td>22 div</td></tr>
<tr><td>100</td><td>32 div</td><td>58 div</td><td>24 div</td></tr>
<tr><td>101</td><td>36 div</td><td>72 div</td><td>28 div</td></tr>
<tr><td>110</td><td>40 div</td><td>84 div</td><td>34 div</td></tr>
<tr><td>111</td><td>44 div</td><td>100 div</td><td>40 div</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.9 gamma ref 1 (68h)

68h	gamma ref 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma ref 1	W	0	1	1	0	1	0	0	0	(68h)
1st parameter	W	VAP[7:0]								90h
2nd parameter	W	VAN[7:0]								30h
3rd parameter	W		VCMP[6:0]							27h
4th parameter	W		VCOM_OFC[6:0]							21h

Description

VAP_CTRL value must lower than VSP

VAP	Value(V)
8'B00000000	3.6
:	:
8'B10001110	5.375
8'B10001111	5.3875
8'B10010000	5.4
:	:
8'B01111111	6.7875

VAN_CTRL value must higher than VSN

VAN	Value(V)
8'B00000000	-4.9875
:	:
8'B01101111	-3.6
8'B01110000	-3.5875
8'B01110001	-3.575
:	:
8'B01111111	-1.8

VCMP	Value(V)
7'B0000000	0.0125
:	:
7'B1001110	0.9875
7'B1001111	1
7'B1010000	1.0125
:	:
7'B0111111	1.6

Trim gamma voltage.
VAP = VAP[7:0] + VCOM_OFC[6:0]
VAN = VAN[7:0] + VCOM_OFC[6:0]
VCMP = VCMP[6:0] + VCOM_OFC[6:0]

Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes

<table>
<tr><td></td><td></td><td><table><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td><td></td></tr>
<tr><td>Default</td><td colspan="2"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td><td></td></tr>
<tr><td>Flow Chart</td><td colspan="3"></td></tr>
</table>

7.2.10 OTP setting (6ch)

6ch	OTP setting									
Inst / Para	WR	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
OTP setting	W	0	1	1	0	1	1	0	0	(6ch)
1stparameter	W						reg_otp_v_sel		reg_otp_en	00h
Description	reg_otp_en:OTP programming built-in power enable signal, high level valid reg_otp_v_sel:OTP programming built-in power voltage amplitude selection 0:7.6V 1:7.8V									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.11 lvd setting (6dh)

6dh	lvd setting									
Inst / Para	WR	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
lvd setting	W	0	1	1	0	1	1	0	1	(6dh)
1stparameter	W		lvd_vgh_clk_en	lvd_vgh_sel_en	lvd_width[1:0]		lvd_sel[1:0]		lvd_en	60h

Description

lvd_sel[1:0]		LVD(V)
0	0	2
0	1	2.1
1	0	2.2
1	1	2.3

lvd_vgh_clk_en: Enable d2a in LVD mode_ VGH_ PUMP_ CLK configuration, d2a in LVD mode_ VGH_ PUMP_ CLK will be configured as 5'd3 (4 div)

lvd_vgh_sel_en: Enable the configuration of D2A_VGH_SEL in LVD mode. In LVD mode, D2A_VGH_SEL is set to 2'b11.

lvd_width[1:0]: Adjust the filtering time for entering LVD mode.

lvd_en: LVD mode enable register.

Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.12 RGB interface control (B0h)

<table>
<tr><th>B0h</th><th colspan="10">RGB interface control</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>RGB interface control</td><td>W</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(B0h)</td></tr>
<tr><td>parameter</td><td>W</td><td></td><td colspan="2">rcm[1:0]</td><td></td><td>vspl</td><td>hspl</td><td>dpl</td><td>epl</td><td>40h</td></tr>
<tr><td>Description</td><td colspan="10">Set the operation status of display interface. The setting becomes effective as soon as the command is seted.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Comment</th></tr>
<tr><td rowspan="2">bypass_mode</td><td rowspan="2">Select the display data bypass</td><td>0</td><td>through memory</td></tr>
<tr><td>1</td><td>direct to shift register</td></tr>
<tr><td rowspan="2">vspl</td><td rowspan="2">VSYNC polarity</td><td>0</td><td>Low level sync clock</td></tr>
<tr><td>1</td><td>High level sync clock</td></tr>
<tr><td rowspan="2">hspl</td><td rowspan="2">HSYNC polarity</td><td>0</td><td>Low level sync clock</td></tr>
<tr><td>1</td><td>High level sync clock</td></tr>
<tr><td rowspan="2">dpl</td><td rowspan="2">Dot clock polarity</td><td>0</td><td>data fetched at the rising time</td></tr>
<tr><td>1</td><td>data fetched at the falling time</td></tr>
<tr><td rowspan="2">epl</td><td rowspan="2">DE polarity</td><td>0</td><td>High enable for RGB interface</td></tr>
<tr><td>1</td><td>Low enable for RGB interface</td></tr>
</table>
rcm[1:0]:RGB interface enable mode selection.
<table>
<tr><th>rcm[1:0]</th><th>Mode</th></tr>
<tr><td>00</td><td rowspan="2">system interface</td></tr>
<tr><td>01</td></tr>
<tr><td>10</td><td>RGB DE mode</td></tr>
<tr><td>11</td><td>RGB SYNC mode</td></tr>
</table>
“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
</table></td></tr>
</table>

		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes
Default			
Flow Chart			

Status	Default Value
Power On Sequence	40h
S/W Reset	40h
H/W Reset	40h

7.2.13 frame rate (B1h)

B1h	frame rate									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
frame rate1	W	1	0	1	1	0	0	0	1	(B1h)
1st parameter	W	X	X	fr1_h[5:0]						0fh
2nd parameter	W	X	X	X	fr1_v[4:0]					02h
3rd parameter	W	X	X	X	X	X	fr1_div[2:0]			04h

Description

It is adjustable frame rate in normal mode.

fr1_h[5:0]: Adjustable the number of clocks.

fr1_v[4:0]: Adjustable the number of lines.

fr1_div[1:0]:set the division ratio of the internal oscillation clock, when NV3030B's display operation is synchronized with internal oscillation clock. NV3030B's internal operation is synchronized with the frequency divided internal oscillation clock. When changing the fr1_div[1:0] setting, the width of the reference clock for liquid crystal panel control signals is changed.

fr1_div[1:0]	Division Ratio	Internal Operation Clock Unit
2'h0	1/1 fosc	One OSC clock
2'h1	1/2 fosc	2 OSC clock
2'h2	1/3 fosc	3 OSC clock
2'h3	1/4 fosc	4 OSC clock

Frame Frequency Calculation

$$\text{Frame Frequency} = \frac{\text{Fosc}}{\text{fr1\_div[1:0]} \times (240 + \text{src\_h} + \text{fr1\_h[5:0]}) \times (320 + \text{src\_v} + \text{fr1\_v[4:0]})}$$

1.Fosc:RC oscillation frequency,adjustment by osc_trim and osc_fresh.

2.src_h:row pitch during source normal work.Source current row pitch is clock number.Insure source finished transfer and latched data when adjust the frame frequency.

3.src_v: interval frame during normal work.

4. fr1_h[5:0]: Adjustable the number of clocks. fr1_v[4:0]:Adjustable the number of lines.

5. fr1_div[1:0]: Division Ratio of clocks.

"X" = Don't care.

Restriction

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

7.2.14 display pol control (B4h)

<table>
<tr><th>B4h</th><th colspan="10">display pol control</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display pol control</td><td>W</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(B4h)</td></tr>
<tr><td>parameter</td><td>W</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">dinv[2:0]</td><td>02h</td></tr>
<tr><td>Description</td><td colspan="10">dinv: Inversion setting in full colors normal mode (Normal Mode On).
<table><tr><th colspan="3">dinv</th><th>Inversion</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Colum Inversion</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 dot inversion</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 dot inversion</td></tr><tr><td>0</td><td>1</td><td>1</td><td>3 dot inversion</td></tr><tr><td>1</td><td>0</td><td>0</td><td>4 dot inversion</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Colum Inversion</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Colum Inversion</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Colum Inversion</td></tr></table>“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>02h</td></tr><tr><td>S/W Reset</td><td>02h</td></tr><tr><td>H/W Reset</td><td>02h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.15 blanking porch (B5h)

B5h	blanking porch									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
blanking porch	W	1	0	1	1	0	1	0	1	(B5h)
1st parameter	W	X	vfp[6:0]							02h
2nd parameter	W	X	vbp[6:0]							02h
3rd parameter	W	X	hfp[6:0]							0Ah
4th parameter	W	X	hbp[6:0]							14h
Description	vfp[6:0]/vbp[6:0]:The vfp[6:0] and vbp[6:0] bits specify the line number of vertical front and back porch period respectively. hfp[6:0]/ hbp[6:0]:The hfp[6:0] and hbp [6:0] bits specify the dotclk number of horizontal front and back porch period respectively. Note:when rim == 1，porch size is according to clock counter，isn't according to pixel counter. "X"：Don't care.									
Restriction	-									
Register Availability										
Default										
Flow Chart										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

7.2.16 display function (B6h)

<table>
<tr><th>B6h</th><th colspan="10">display function</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display function</td><td>W</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>(B6h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td></td><td>rev</td><td></td><td>sm</td><td></td><td>ptg</td><td></td><td>pts</td><td>04h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td></td><td>gs</td><td></td><td>ss</td><td></td><td></td><td></td><td>normal_black</td><td>00h</td></tr>
<tr><td>3rd parameter</td><td>W</td><td></td><td></td><td colspan="7">nl[5:0]</td><td>9fh</td></tr>
<tr><td>4th parameter</td><td>W</td><td></td><td></td><td colspan="7">scn[5:0]</td><td>00h</td></tr>
<tr><td>5th parameter</td><td>W</td><td></td><td></td><td></td><td></td><td colspan="5">isc[3:0]</td><td>02h</td></tr>
<tr><td>Description</td><td colspan="11">
normal_black: Panel selection. normal_black=’0’,normal white; normal_black=’1’,normal black.
pts: Determine source output in a non-display area in the partial display mode.
<table>
<tr><th>pts</th><th>Source output on non-display area</th></tr>
<tr><td>0</td><td>V63</td></tr>
<tr><td>1</td><td>V0</td></tr>
</table>
ptg:Set the scan mode in non-display area.
<table>
<tr><th>ptg</th><th>Gate outputs in non-display area</th></tr>
<tr><td>0</td><td>normal scan</td></tr>
<tr><td>1</td><td>Interval scan</td></tr>
</table>
rev: xor display inversion setting.
nl[5:0]: Set the number of gate line.
<table>
<tr><th>nl[5:0]</th><th>The number of gate line</th></tr>
<tr><td>0x00</td><td>8 gate line</td></tr>
<tr><td>0x01</td><td>16 gate line</td></tr>
<tr><td>0x02</td><td>24 gate line</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>0x27</td><td>320 gate line</td></tr>
</table>
gs: Gate scan direction.gs=”0”: Gate scan direction is 0→319;gs=”1”: Gate scan direction is 319 →0.
ss: selects the shift direction of outputs of the source driver. 0: Source output S1→S720; 1: Source output S720→S1.
sm: Gate interlace mode selection.sm=”0”: Gate scan using interlace mode. sm=”1”: Gate scan using non-interlace mode.
isc[3:0]: Specify the scan cycle of the gate driver when the ptg is seted to “1” in non-display area. The scan cycle can be set in odd number of frames from 0 to 31. In this case, polarity is inverted every scan cycle.
<table>
<tr><th>Isc[3:0]</th><th>Scan cycle</th><th>(Ffrm)=60HZ</th></tr>
<tr><td>0000</td><td>0 frame</td><td>-</td></tr>
<tr><td>0001</td><td>3 frame</td><td>50ms</td></tr>
<tr><td>0010</td><td>5 frame</td><td>84ms</td></tr>
<tr><td>0011</td><td>7 frame</td><td>117ms</td></tr>
<tr><td>0100</td><td>9 frame</td><td>150ms</td></tr>
<tr><td>0101</td><td>11 frame</td><td>184ms</td></tr>
</table>
</td></tr>
</table>

	0110	13frame	217ms
	0111	15frame	251ms
	1000	17frame	284ms
	1001	19frame	317ms
	1010	21frame	351ms
	1011	23 frame	384ms
	1100	25frame	418ms
	1101	27frame	451ms
	1110	29 frame	484ms
	1111	31frame	518ms

"X" = Don't care.

Restriction	-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.17 entry mode set (B7h)

<table>
<tr><th>B7h</th><th colspan="9">entry mode set</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>entry mode set</td><td>W</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>(B7h)</td></tr>
<tr><td>parameter</td><td>W</td><td></td><td></td><td></td><td></td><td></td><td>gon</td><td>dte</td><td></td><td>06h</td></tr>
<tr><td>Description</td><td colspan="10">gon/dte: Set the output level of gate driver:
<table><tr><th>gon</th><th>dte</th><th>G1~G320 Gate Output</th></tr><tr><td>0</td><td>0</td><td>VGH</td></tr><tr><td>0</td><td>1</td><td>VGH</td></tr><tr><td>1</td><td>0</td><td>VGL</td></tr><tr><td>1</td><td>1</td><td>Normal display</td></tr></table>“X”：Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>06h</td></tr><tr><td>S/W Reset</td><td>06h</td></tr><tr><td>H/W Reset</td><td>06h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.18 OTP_CTRL0 (C2h)

C2h	OTP_CTRL0									
Inst/Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HWRST
OTP_CTRL0	W	1	1	0	0	0	0	1	0	(C2h)
parameter	W	vpp_src_sel	OTP_SEL	VPP_SEL	PRD	PWE	PTM[1:0]		PPROG	00h
Description	vpp_src_sel : D2A_VSP_BTVS output selection signal 0 : 2'd0 1 : Configure via register(65H) OTP_SEL : Read otp enable signal. VPP_SEL : VPP signal source during manual programming. PRD : OTP read clock. PWE : OTP program clock. PTM[1:0] : Test mode enabling. PPROG : Program mode enabling.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.19 OTP_CTRL1 (C3h)

<table>
<tr><th>C3h</th><th colspan="10">OTP_CTRL1</th></tr>
<tr><td>Inst/Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>OTP_CTRL1</td><td>W</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(C3h)</td></tr>
<tr><td>parameter</td><td>W</td><td colspan="8">PA[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">PA[7:0] : Program or read address of OTP.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.20 OTP_CTRL2 (C4h)

<table>
<tr><th>C4h</th><th colspan="10">OTP_CTRL2</th></tr>
<tr><td>Inst/Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>OTP_CTRL2</td><td>W</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(C4h)</td></tr>
<tr><td>parameter</td><td>W</td><td colspan="8">PDIN1[7:0]</td><td>ffh</td></tr>
<tr><td>Description</td><td colspan="10">PDIN1[7:0] : OTP program data.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.21 OTP_CTRL3(C6h)

<table>
<tr><th>C6h</th><th colspan="10">OTP_CTRL3</th></tr>
<tr><td>Inst/Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>OTP_CTRL3</td><td>W</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>(C6h)</td></tr>
<tr><td>parameter</td><td>W</td><td></td><td>TPPS_ADJ</td><td>TAS_ADJ</td><td>TAH_ADJ</td><td>TDH_ADJ</td><td>TPPR_ADJ</td><td colspan="2">TPW_ADJ[9:8]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">TPPS_ADJ : Used to adjust the width of Tpps in the program timing (step : 1 clk_sys cycle)
TAS_ADJ : Used to adjust the width of Tas in the program timing (step : 1 clk_sys cycle)
TAH_ADJ : Used to adjust the width of Tah in the program timing (step : 1 clk_sys cycle)
TDH_ADJ : Used to adjust the width of Tdh in the program timing (step : 1 clk_sys cycle)
TPPR_ADJ : Used to adjust the width of Tppr in the program timing (step : 1 clk_sys cycle)
TPW_ADJ[9:8] : Used to adjust the width of Tpw in the program timing , this is the higher 2 bits of the register (step : 16 clk_sys cycle)</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.22 OTP_CTRL4 (C7h)

C7h	OTP_CTRL4									
Inst/Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HWRST
OTP_CTRL4	W	1	1	0	0	0	1	1	1	(C7h)
parameter	W	TVR_ADJ[7:0]								02h
Description	TVR_ADJ[7:0] : Used to adjust the width of Tvr in the program timing (step : 64 clk_sys cycle)									
Restriction	-									
Register Availability										
Default										
Flow Chart										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

7.2.23 OTP_CTRL5(C8h)

<table>
<tr><th>C8h</th><th colspan="10">OTP_CTRL5</th></tr>
<tr><td>Inst/Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>OTP_CTRL5</td><td>W</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>(C8h)</td></tr>
<tr><td>parameter</td><td>W</td><td colspan="8">TPW_ADJ[7:0]</td><td>6eh</td></tr>
<tr><td>Description</td><td colspan="10">TPW_ADJ[7:0] : Used to adjust the width of Tpw in the program timing , this is the lower 8 bits of the register (step : 16 clk_sys cycle)</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.24 OTP_CTRL8 (C9h)

<table>
<tr><th>C9h</th><th colspan="9">OTP_CTRL8</th></tr>
<tr><td>Inst/Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>OTP_CTRL8</td><td>W</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>(C9h)</td></tr>
<tr><td>parameter</td><td>R</td><td colspan="8">OTP_RD_DAT</td><td></td></tr>
<tr><td>Description</td><td colspan="10">OTP_RD_DAT : Read OTP data.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.25 OTP_CTRL6(CAh)

<table>
<tr><th>CAh</th><th colspan="10">OTP_CTRL6</th></tr>
<tr><td>Inst/Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>OTP_CTRL6</td><td>W</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>(CAh)</td></tr>
<tr><td>parameter</td><td>W</td><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2">ONE_PROG_SEL[1:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">ONE_PROG_SEL[1:0] : OTP program mode selection.
00 : OTP automatic program mode, program 1 bit at a time.
01 : OTP automatic program mode, program 1 byte at a time.
10 : OTP manual program mode, program 1 byte at a time.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.26 gamma positive 1 (E0h)

E0h	gamma positive 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma positive 1	W	1	1	1	0	0	0	0	0	(E0h)
1st parameter	W				pkp0[4:0]					15h
2nd parameter	W				pkp1[4:0]					14h
3rd parameter	W				pkp2[4:0]					13h
4th parameter	W				pkp3[4:0]					16h
5th parameter	W				pkp4[4:0]					16h
6th parameter	W				pkp5[4:0]					14h
7th parameter	W				pkp6[4:0]					13h
8th parameter	W				pkp7[4:0]					0ch
Description	E0h is gamma adjust registers.See gamma correction section for reference.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.27 gamma positive 2 (E1h)

E1h	gamma positive 2									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma positive 2	W	1	1	1	0	0	0	0	1	(E1h)
1st parameter	W		prp0[6:0]							41h
2nd parameter	W		prp1[6:0]							50h
Description	E1h is gamma adjust registers.See gamma correction section for reference.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	4150h
S/W Reset	no change
H/W Reset	4150h

Flow Chart

7.2.28 gamma positive 3 (E2h)

E2h	gamma positive 3									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma positive3	W	1	1	1	0	0	0	1	0	(E2h)
1st parameter	W			vrp0[5:0]						00h
2nd parameter	W			vrp1[5:0]						25h
3rd parameter	W			vrp2[5:0]						2dh
4th parameter	W			vrp3[5:0]						14h
5th parameter	W			vrp4[5:0]						1ch
6th parameter	W			vrp5[5:0]						3fh
Description	E2h is gamma adjust registers.See gamma correction section for reference.									
Restriction	-									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.29 gamma negative 1 (E3h)

E3h	gamma negative 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma negative 1	W	1	1	1	0	0	0	1	1	(E3h)
1st parameter	W				pkn0[4:0]					06h
2nd parameter	W				pkn1[4:0]					10h
3rd Parameter	W				pkn2[4:0]					14h
4th Parameter	W				pkn3[4:0]					16h
5th parameter	W				pkn4[4:0]					16h
6th Parameter	W				pkn5[4:0]					13h
7th Parameter	W				pkn6[4:0]					13h
8th Parameter	W				pkn7[4:0]					13h
Description	E3h is gamma adjust registers.See gamma correction section for reference.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.30 gamma negative 2 (E4h)

<table>
<tr><th>E4h</th><th colspan="10">gamma negative 2</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>gamma negative 2</td><td>W</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(E4h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td></td><td colspan="7">prn0[6:0]</td><td>64h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td></td><td colspan="7">prn1[6:0]</td><td>41h</td></tr>
<tr><td>Description</td><td colspan="10">E4h is gamma adjust registers.See gamma correction section for reference.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>6441h</td></tr><tr><td>S/W Reset</td><td>no change</td></tr><tr><td>H/W Reset</td><td>6441h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.31 gamma negative 3 (E5h)

E5h	gamma negative 3									
Inst / Para	W//R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma negative 3	W	1	1	1	0	0	1	0	1	(E5h)
1st parameter	W			vrn0[5:0]						3fh
2nd parameter	W			vrn1[5:0]						1ch
3rd parameter	W			vrn2[5:0]						14h
4th parameter	W			vrn3[5:0]						2dh
5th parameter	W			vrn4[5:0]						25h
6th parameter	W			vrn5[5:0]						00h
Description	E5h is gamma adjust registers.See gamma correction section for reference.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.32 SRC_CTRL1 (E6h)

<table>
<tr><th>E6h</th><th colspan="10">SRC_CTRL1</th></tr>
<tr><td>Inst/Para</td><td>W//R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>SRC_CTRL1</td><td>W</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>(E6h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td>chk_cnt_inv</td><td>chk_data_h</td><td colspan="6">chk_cnt_sel</td><td>SC_EN_START[8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td colspan="9">SC_EN_START[7:0]</td><td>f0h</td></tr>
<tr><td>Description</td><td colspan="11">The main function of these registers is to debug source.
chk_cnt_inv : check counter sequence selection.
1 : 242 - chk_cnt_sel
0 : chk_cnt_sel
chk_data_h : Source Data high and low 8-bit selection.
1 : D2A_SD_D[15:8]
0 : D2A_SD_D[7:0]
chk_cnt_sel : check counter selection.
SC_EN_START[8:0] : Specifies the end location of the source enable signal.</td></tr>
<tr><td>Restriction</td><td colspan="11">-</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="11"></td></tr>
</table>

7.2.33 SRC_CTRL2 (E7h)

E7h	SRC_CTRL2									
Inst/Para	W//R	D7	D6	D5	D4	D3	D2	D1	D0	HWRST
SRC_CTRL2	W	1	1	1	0	0	1	1	1	(E7h)
1st parameter	W					CS_START[3:0]				01h
2nd parameter	W						scdt_inv_sel		cs_vp_en	04h
3rd parameter	W	CS1_WIDTH [7:0]	12h	CS1_WIDTH[7:0]						12h
4th parameter	W	CS2_WIDTH [7:0]	12h	CS2_WIDTH[7:0]						12h
5th parameter	W	PREC_START [7:0]	06h	PREC_START[7:0]						06h
6th parameter	W	PREC_WIDTH [7:0]	1fh	PREC_WIDTH[7:0]						1fh
Description	CS_START[3:0] : Specifies the starting position of D2A_SD_PNCS、D2A_SD_CS_POP_EN and D2A_SD_CS_NOP_EN. scdt_inv_sel[1:0] : Don't use. cs_vp_en : cs_cnt enable signal whether to count in the VBP region. CS1_WIDTH[7:0] : Specifies the end position of D2A_SD_CS_POP_EN. CS2_WIDTH[7:0] : Specifies the end position of D2A_SD_PNCS. PREC_START[7:0] : Specifies the starting position of D2A_SD_PREC. PREC_WIDTH[7:0] : Specifies the end position of D2A_SD_PREC.									
Restriction	-									
Register Availability										
Default										
Flow Chart										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

7.2.34 SRC_CTRL3 (E8h)

<table>
<tr><th>E8h</th><th colspan="10">SRC_CTRL3</th></tr>
<tr><td>Inst/Para</td><td>W//R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>SRC_CTRL3</td><td>W</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>(E8h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td>vdds_oe</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td></td><td colspan="3">chopper_sel[2:0]</td><td></td><td></td><td></td><td></td><td>40h</td></tr>
<tr><td>3rd parameter</td><td>W</td><td></td><td colspan="3">gchopper_sel[2:0]</td><td></td><td></td><td></td><td></td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">vdds_oe： Enable signal of VDDS signal.
chopper_sel[2:0]： D2A_SD_OFC mode selection.
000 : 1’b0
001 : Reverse every frame.
010 : Reverse every two frames.
011 : Reverse every three frames.
100 : Reverse every line and swap polarity every frame.
101 : Reverse every two lines and swap polarity every frame.
110 : Reverse every line and swap polarity every two frames.
111 : Reverse every two lines and swap polarity every two frame.
gchopper_sel[2:0]：
① D2A_GMA_CHOP mode selection.
000 : 1’b0
001 : Reverse every frame.
010 : Reverse every two frames.
011 : Reverse every three frames.
100 : Reverse every line and swap polarity every frame.
101 : Reverse every two lines and swap polarity every frame.
110 : Reverse every line and swap polarity every two frames.
111 : Reverse every two lines and swap polarity every two frame.
② Controls the D2A_GMA_EN signal to be turned off briefly when the D2A_GMA_CHOP signal is flipped.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr></table></td></tr>
</table>

		S/W Reset		
		H/W Reset		
Flow Chart				

7.2.35 Charge Share (E9h)

<table>
<tr><th>E9h</th><th colspan="9">Charge Share</th></tr>
<tr><td>Inst/Para</td><td>W//R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>Charge Share</td><td>W</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>(E9h)</td></tr>
<tr><td>parameter</td><td>W</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>CS_FLAG</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">CS_FLAG： One of the enable signals of cs_cnt.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.36 SRC_CTRL4 (EAh)

EAh	SRC_CTRL4									
Inst/Para	W//R	D7	D6	D5	D4	D3	D2	D1	D0	HWRST
SRC_CTRL4	W	1	1	1	0	1	0	1	0	(EAh)
1st parameter	W					PNCS_SEL[1:0]			PNCS_EN	0dh
2nd parameter	W	PNCS_WIDTH[7:0]								12h
Description	PNCS_SEL[1:0]： D2A_SD_PNCS Mode selection. 00, 10, 11 are not much different, only slightly different at the beginning and end, but they are very different from 01, which has only one pulse at the end of a frame. PNCS_EN： D2A_SD_PNCS enable signal. PNCS_WIDTH[7:0]： It used to specify the end position of D2A_SD_PNCS, but it is not actually used now.									
Restriction	-									

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.37 Gate driver timing (ECh)

<table>
<tr><th>ECh</th><th colspan="10">Gate driver timing</th></tr>
<tr><td>Inst/Para</td><td>W//R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>Gate driver timing</td><td>W</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(ECh)</td></tr>
<tr><td>parameter</td><td>W</td><td colspan="4">gate_oe_setup[3:0]</td><td colspan="4">gate_oe_hold[3:0]</td><td>47h</td></tr>
<tr><td>Description</td><td colspan="10">gate_oe_setup[3:0]： Used to control the starting position of D2A_GD_OER/L and the position of D2A_GD_ROWR/L address switching
gate_oe_hold[3:0]： Used to control the end position of D2A_GD_OER/L.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.38 tearing effect (F1h)

<table>
<tr><th>F1h</th><th colspan="10">tearing effect</th></tr>
<tr><td>Inst/Para</td><td>W//R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>tearing effect</td><td>W</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(F1h)</td></tr>
<tr><td>1st parameter</td><td>W</td><td></td><td></td><td></td><td></td><td></td><td></td><td>te_pol</td><td>tem_extend</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td colspan="8">te_v_start[7:0]</td><td>01h</td></tr>
<tr><td>3rd parameter</td><td>W</td><td colspan="8">te_v_end[7:0]</td><td>1fh</td></tr>
<tr><td>4th parameter</td><td>W</td><td colspan="8">te_h_start[7:0]</td><td>01h</td></tr>
<tr><td>5th parameter</td><td>W</td><td colspan="8">te_h_end[7:0]</td><td>3fh</td></tr>
<tr><td>Description</td><td colspan="10">te_v_start[7:0] : In extend mode, specify which line of a frame the te signal starts.
te_v_end[7:0] : In extend mode, specify which line of a frame the te is closed.
te_h_start[7:0] : In extend mode, specifies which column of a row the te signal begins.
te_h_end[7:0] : In extend mode, Specifies from which column of a row the te signal is closed.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.39 led (F2h)

F2h	led									
Inst/Para	W//R	D7	D6	D5	D4	D3	D2	D1	D0	HWRST
led	W	1	1	1	1	0	0	1	0	(F2h)
1st parameter	W					ledpwm_oe	ledpwm	ledon_oe	ledon	0eh
Description	ledpwm_oe : Enable signal of D2P_LEDPWM. ledpwm : Adjust the backlight brightness. ledon_oe : Enable signal of D2P_LECON. ledon : Backlight switch signal.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0eh
S/W Reset	0eh
H/W Reset	0eh

Flow Chart

7.2.40 tearing effect (F4h)

F4h	rgb sync width									
Inst/Para	W//R	D7	D6	D5	D4	D3	D2	D1	D0	HWRST
rgb sync width	W	1	1	1	1	0	1	0	0	(F4h)
1st parameter	W		vsync_width[6:0]							00h
2st parameter	W		hsync_width[6:0]							00h
Description	Used for RGB interface sync mode to receive data: vsync_width[6:0] : Used to calculate VBP. hsync_width[6:0] : Used to calculate HBP.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart

7.2.41 Interface control (F6h)

F6h	Interface control									
Inst / Para	W/ R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
Interface control	W	1	1	1	1	0	1	1	0	F6h
1st parameter	W	my_eor	mx_eor	mv_eor	0	bgr_eor	0	0	we_mode	01h
2nd parameter	W	cs_delay_sel[1:0]		epf[1:0]				mdt[1:0]		10h
3rd parameter	W		endian			dm[1:0]			rim	00h
4th parameter	W		spi_2wire_ mode						rm	00h

Description

my_eor/mx_eor/mv_eor/bgr_eor:the set of value MADCTL is used in the IC is derived as exclusive OR between first parameter of interface control and MADCTL parameter.

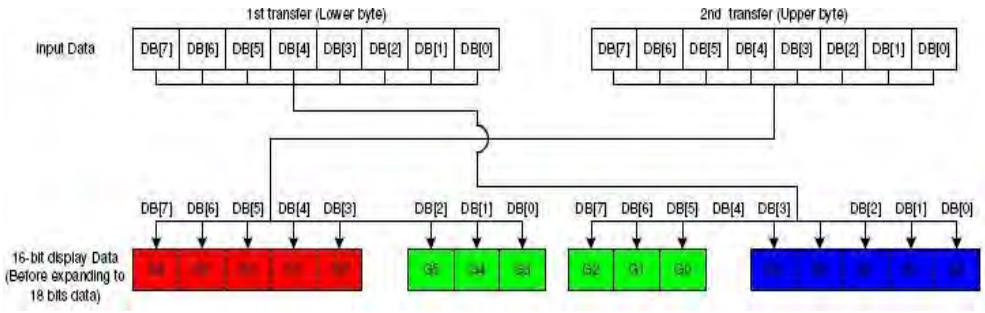
mdt[1:0]:select the method of display data transferring.
we_mode:memory write control.
we_mode=0:when the transfer number of data exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1), the exceeding data will be ignored.
we_mode=1:when the transfer number of data exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

spi_2wire_mode:enable 2 data lane serial interface mode.

endian: select the little endian interface bit. At little endian mode, the MPU sends LSB data first.

endian	Data transfer mode
0	Normal (MSB first)
1	Little endian (LSB first)

Note: the little endian is valid on only 65k 8bit and 9bit parallel interface mode.



dm[1:0]: select the display operation mode.

dm[1]	dm[0]	Display operation mode
0	0	Internal clock operation
0	1	RGB interface mode
1	0	reserved
1	1	reserved

The dm[1:0] setting allows switching between internal clock operation mode and external display interface operation mode.
rm:select the interface to access the GRAM.

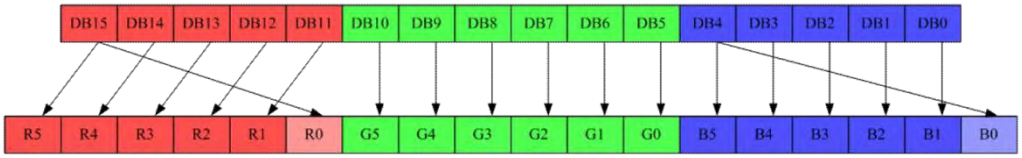
rm	Interface for RAM access
0	system interface
1	RGB interface

rim: specify the RGB interface mode when RGB interface is used. These bits should be set before display operation through RGB interface and should not be set during operation.

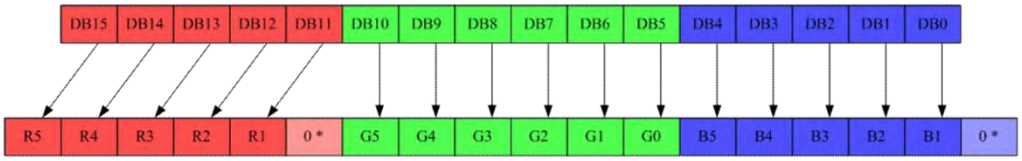
rim	dpi[1:0]	Display operation mode
0	110(262k color)	18 bit RGB interface (1 transfer/pixel)
	101(65k color)	16 bit RGB interface (1 transfer/pixel)
1	110(262k color)	6 bit RGB interface (3 transfer/pixel)
	101(65k color)	6 bit RGB interface (3 transfer/pixel)

epf[1:0]:

epf = 00

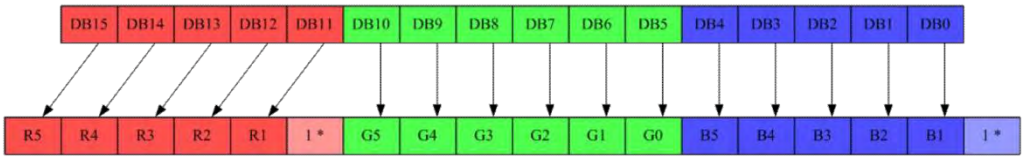


epf = 01



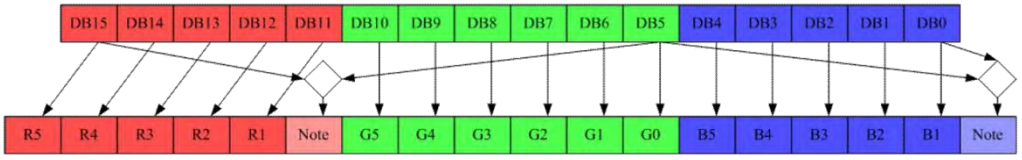
Note: Exception
1. R0 = 1 when R5~R1 = 1111
2. B0 = 1 when B4~B1 = 1111

epf = 10



Note: Exception
1. R0 = 0 when R5~R1 = 0000
2. B0 = 0 when B4~B1 = 0000

epf = 11



Note:

1. If DB15~DB11 = DB10~DB6, R0 = DB5, else R0 = DB15
2. If DB4~DB0 = DB10~DB16, B0 = DB5, else B0 = DB0

"X" = Don't care.

Restriction	

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

7.2.42 color palette enable (FBh)

<table>
<tr><th>FBh</th><th colspan="10">color palette enable</th></tr>
<tr><td>Inst/Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>color palette enable</td><td>W</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>FBh</td></tr>
<tr><td>1st Parameter</td><td>W</td><td></td><td></td><td></td><td></td><td></td><td></td><td>cpe1</td><td>cpe0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">For CP test used
cpe1 : Select whether the data output to Source will be read RAM or written by the interface for CP testing.
cpe0 : Select whether the data to be written to RAM is cpdat or pxl_dat for CP testing.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.43 color palette data (FCh)

<table>
<tr><th>Fch</th><th colspan="10">color palette data</th></tr>
<tr><td>Inst/Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HWRST</td></tr>
<tr><td>color palette data</td><td>W</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>FCh</td></tr>
<tr><td>1st Parameter</td><td>W</td><td colspan="2">cps[1:0]</td><td colspan="6">cpd[5:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">cps[1:0] : cpdat mode selection.
cpd[5:0] : CP test data.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.44 Private access (FDh)

<table>
<tr><th>FDh</th><th colspan="10">Private access</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>Private access</td><td>W</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>FDh</td></tr>
<tr><td>1st Parameter</td><td>W</td><td colspan="8">private_access[15:8]</td><td>00h</td></tr>
<tr><td>2nd Parameter</td><td>W</td><td colspan="8">private_access[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">private_access[15:0] : private registers access control.
<table>
<tr><th>private access</th><th>private_access[15:8]</th><th>private_access[7:0]</th></tr>
<tr><td>enter private registers mode</td><td>06h</td><td>08h</td></tr>
<tr><td>exit private registers mode</td><td>FAh</td><td>FCh</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

8. Functional description

8.1 Interface

8.1.1 Serial Interface

PAD Name	Serial Interface Pin Name	Description
CSX	CSX	A chip select signal.Signal is active low.
DCX	SCL	This pin is used serial interface clock.
WRX	DCX/SDI2	SPI 4-wire system: Serves as command or parameter select. 2 data lane serial interface: the second data lane. QSPI interface: the second data pin
SDA	SDA/SDI	SDA(When serial I/F I): it is SPI and QSPIinterface input/output pin. SDI(When serial I/F Ⅱ): it is SPI interface input pin.
SDO	SDO	SPI interface output pin.
DB[0]	DB[0]	the third pin of qspi
DB[1]	DB[1]	the fourth pin of qspi

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

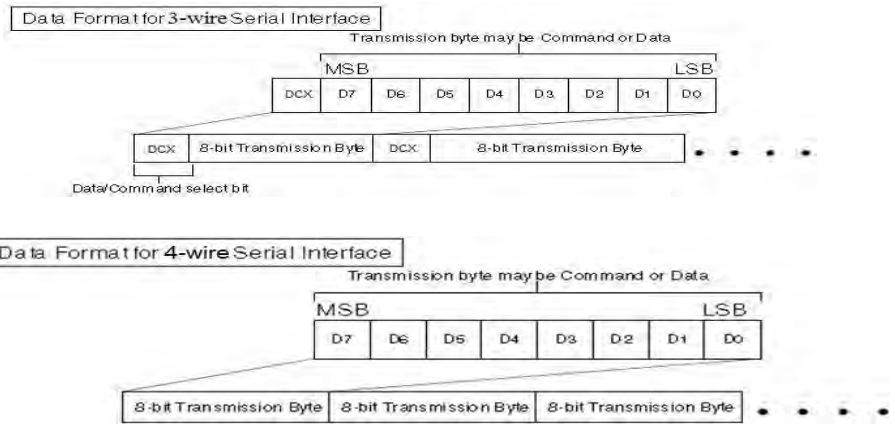
IM3	IM2	IM1	IM0	System Interface Mode	CSX	DCX	SCL	Function
0	1	0	0	qspi	“L”	-		Read/Write command, parameter or display data.
0	1	0	1	3-wire serial interface 2 data lane serial interface	“L”	-		Read/Write command, parameter or display data.
0	1	1	0	4-wire serial interface	“L”	“H/L”		Read/Write command, parameter or display data.
1	1	0	1	3-wire serial interface	“L”	-		Read/Write command, parameter or display data.
1	1	1	0	4-wire serial interface	“L”	“H/L”		Read/Write command, parameter or display data.

NV3030B supplies 3-wire/ 9-bit and 4-wire/8-bit bi-directional serial interfaces for communication between MPU and NV3030B. The 3-wire serial mode consists of the chip enable input (CSX), the serial clock input (SCL) andserial data Input/Output (SDA or SDA/SDO). The 4-wire serial mode consists of the Data/Command selection input (DCX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDA/SDO) for data transmission. The data bus (D[17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary.

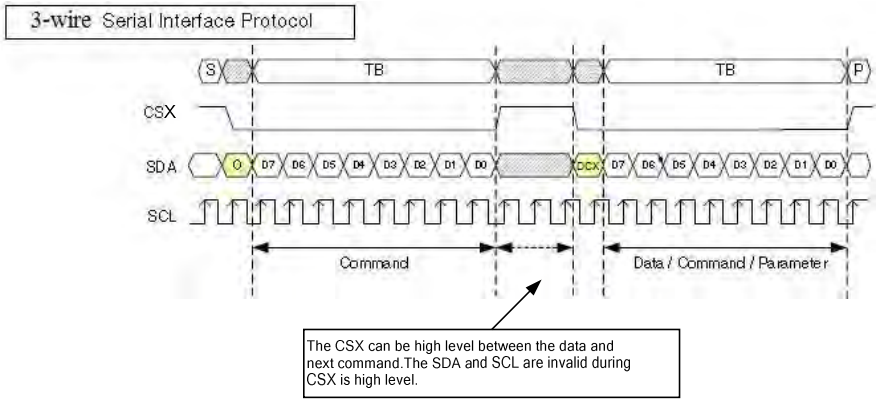
8.1.1.1 Write Cycle Sequence

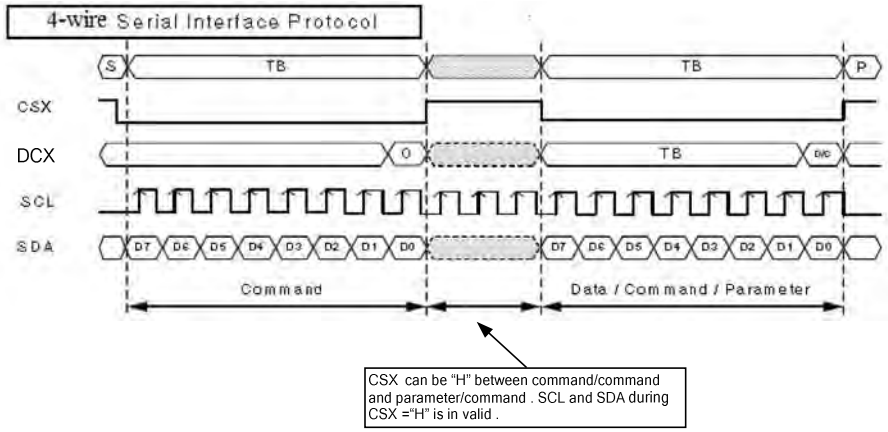
The write mode of the interface means that MPU writes commands or data to NV3030B. The 3-wire serial data packet contains a data/command select bit (DCX) and a transmission byte. If the DCX bit is “low”, the transmission byte is interpreted as a command byte. If the DCX bit is “high”, the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to NV3030B and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-wire serial interface.



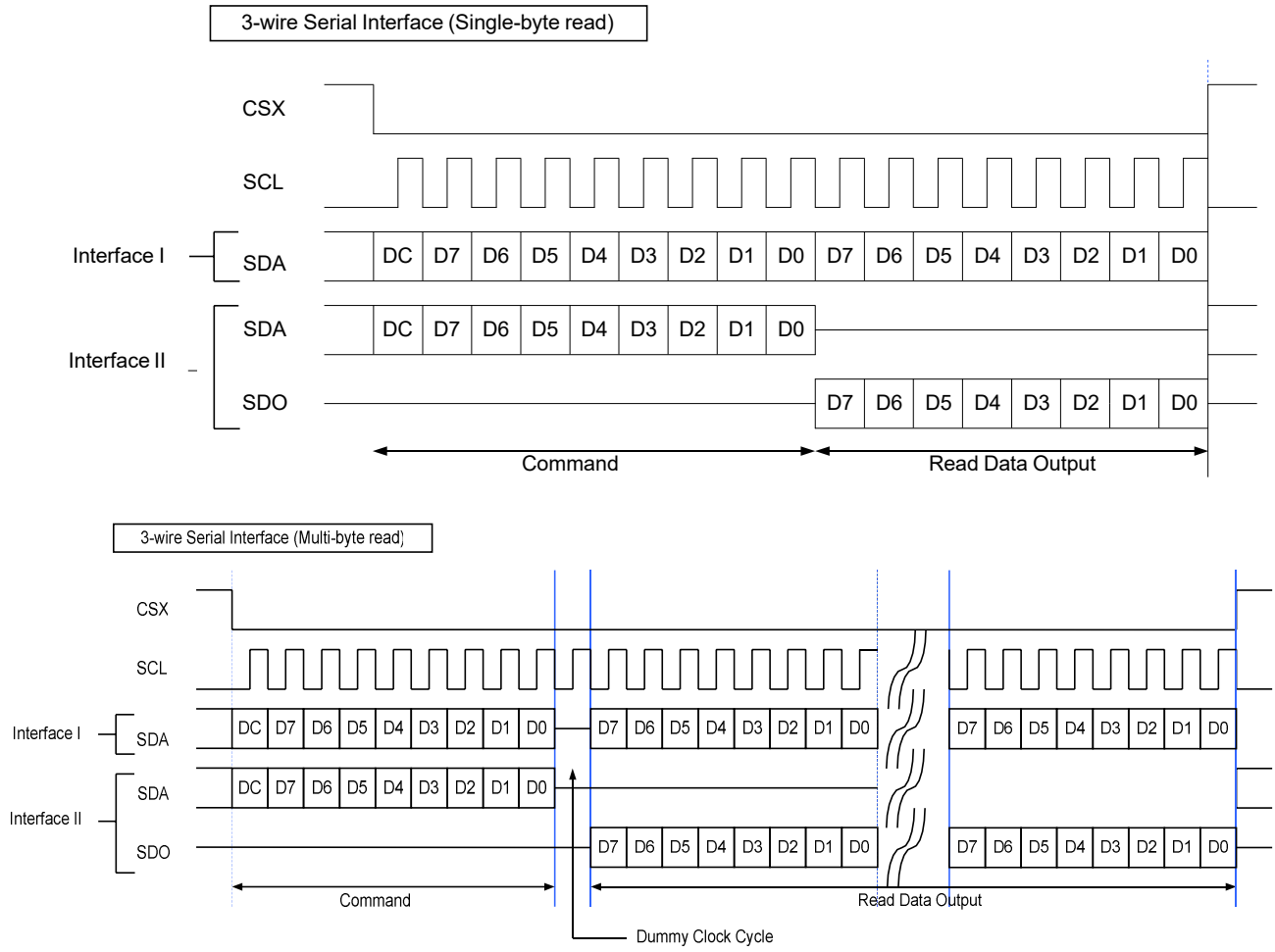
MPU drives the CSX pin to low and starts by setting the DCX bit on SDA. The bit is read by NV3030B on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the MPU. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional DCX signal is used, a byte is eight read cycle width. The 3/4-wire serial interface writes sequence described in the figure as below.



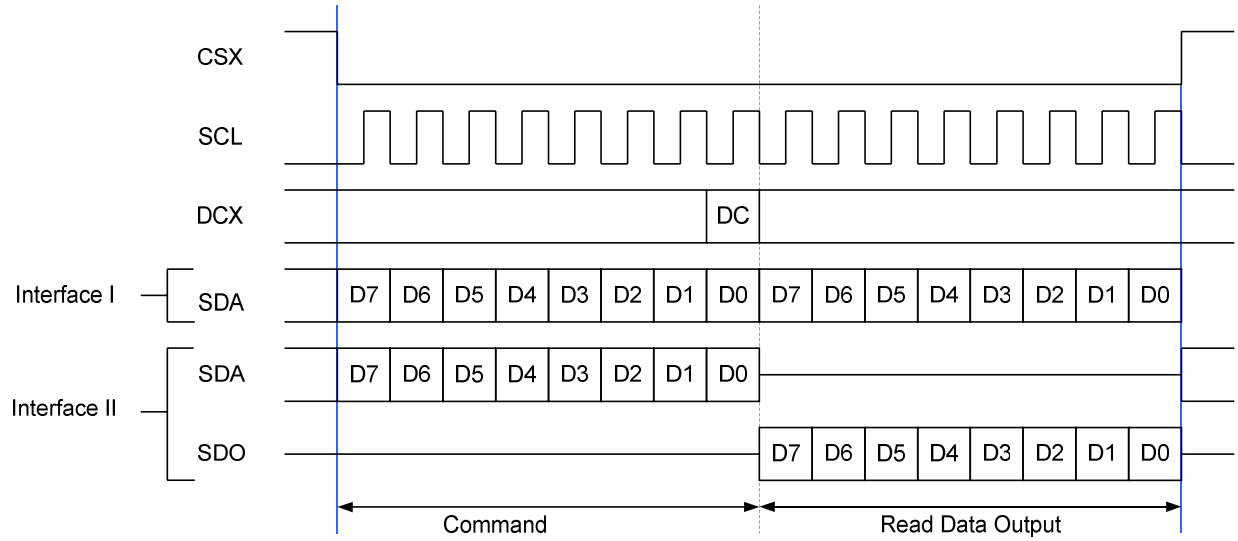


8.1.1.2 Read Cycle Sequence

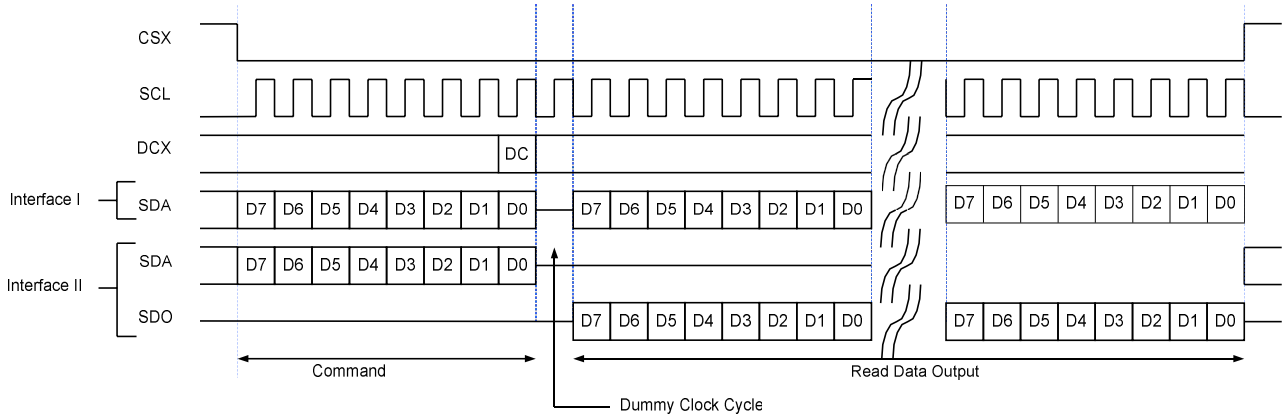
The read mode of interface means that the MPU reads register's parameter from NV3030B. The MPU has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. NV3030B latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data)at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri- state and no later than at the falling edge of SCL of the last bit. The read mode has two types of transmitted command data (single/multi-byte) according to command code.



4-wire Serial Interface (Single-byte read)

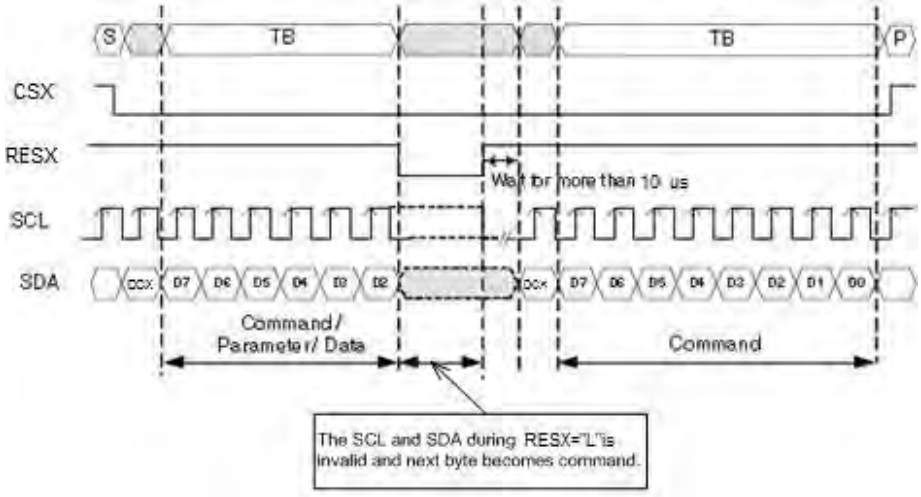


4-wire Serial Interface (Multi-byte read)

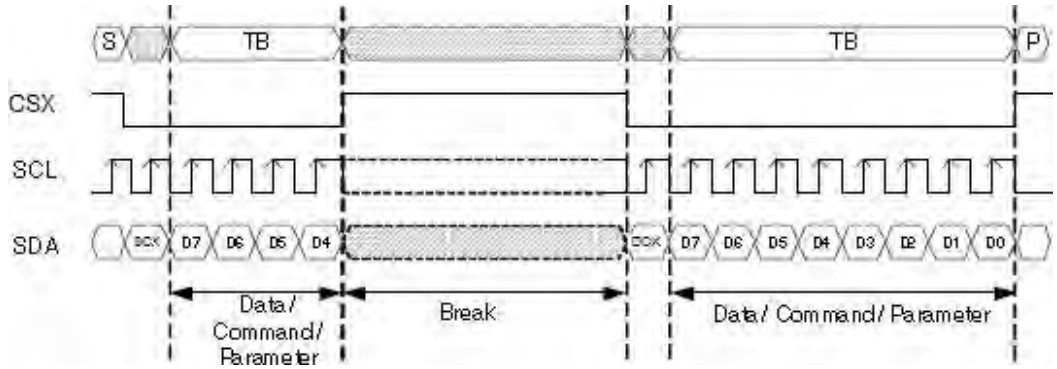


8.1.1.3 Data Transfer Break and Recovery

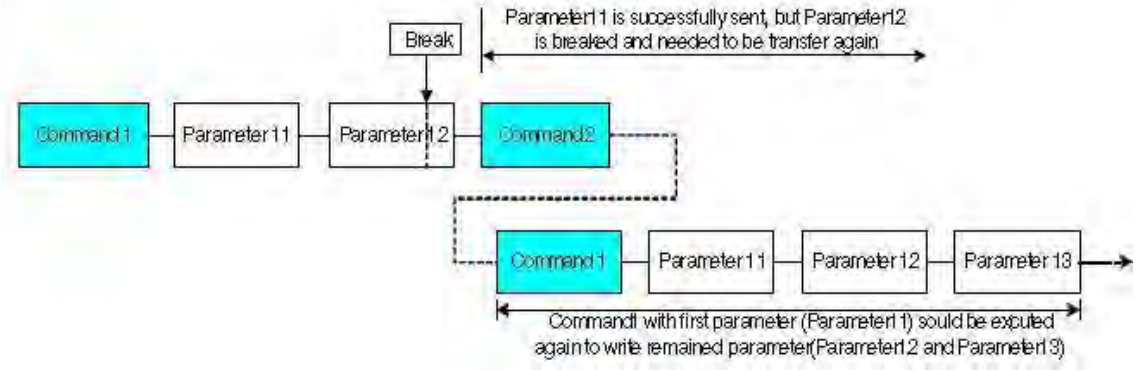
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



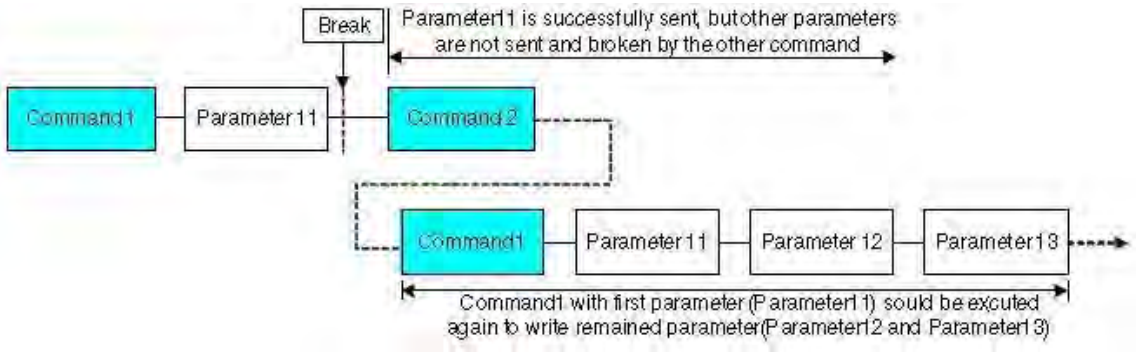
If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the MPU then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

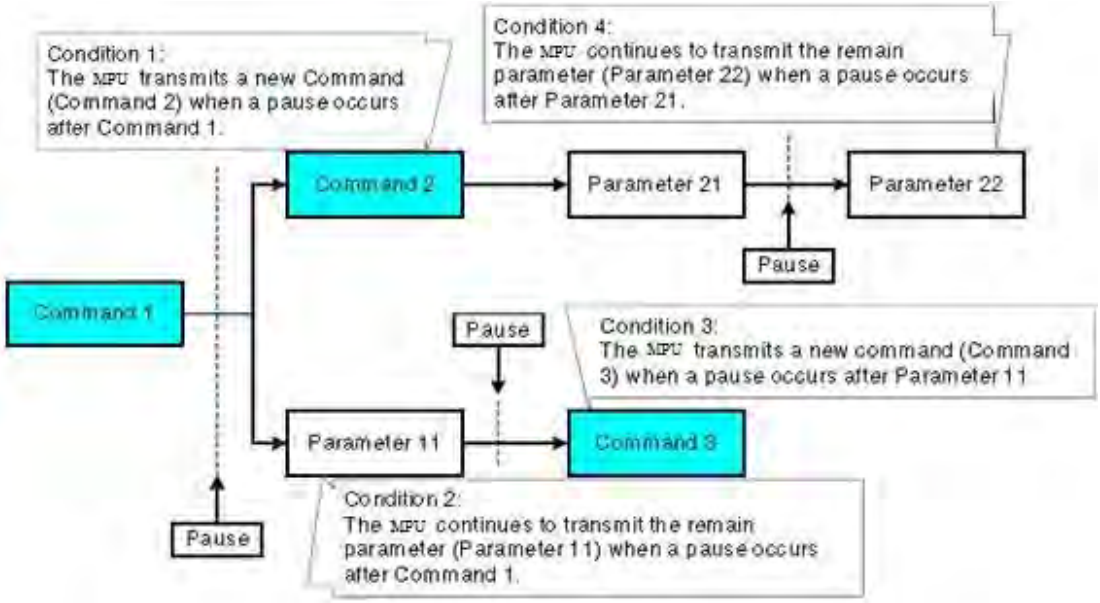
8.1.1.4 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then NV3030B will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.



This applies to the following 4 conditions:

1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter



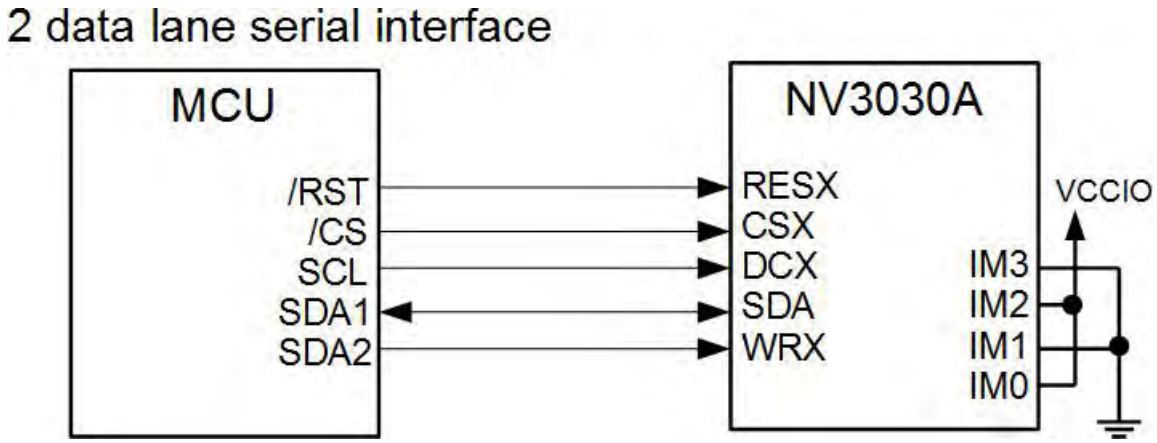
8.1.1.5 2 data lane serial interface

Interface selection:

IM3	IM2	IM1	IM0	Interface
0	1	0	1	2 data lane serial interface

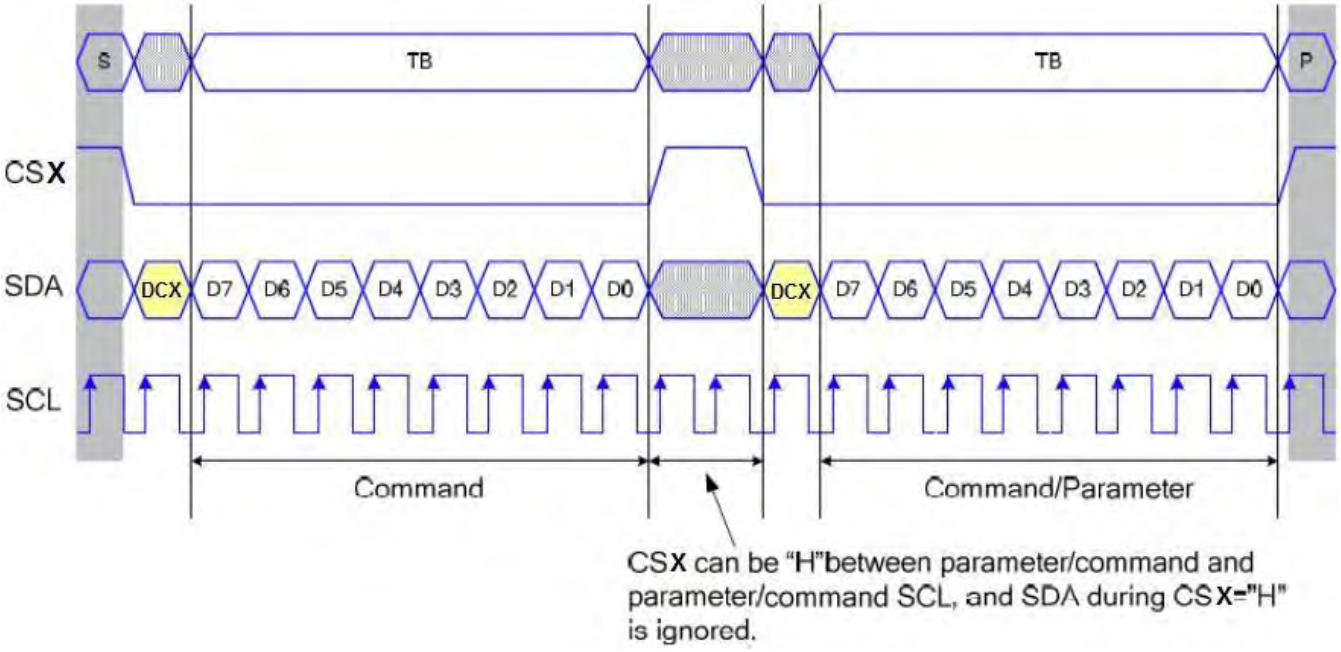
2 data lane serial interface use: CSX (chip enable), DCX (serial clock) and SDA (serial data input/output 1), and WRX (serial data input 2). To enter this interface, register spi_2wire_mode, which is located in the 3rd parameter of command F6h, should be set.

2 data lane hardware suggestion and Pin description:
2 data lane serial interface, IM[3:0]=0101



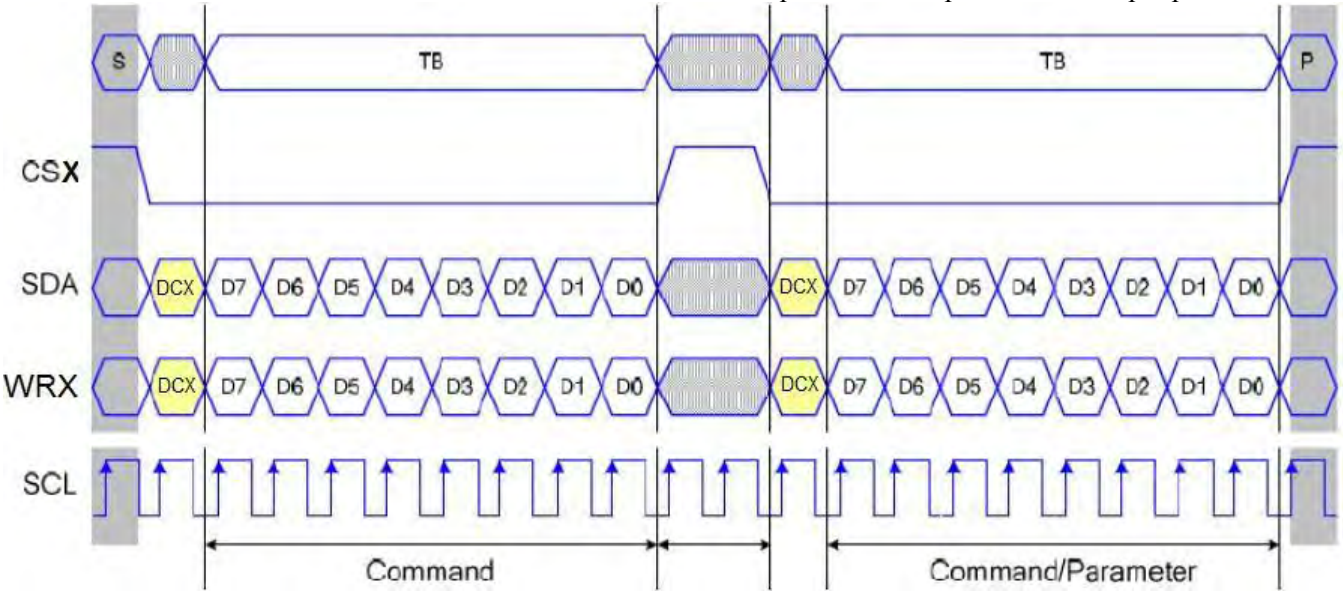
Pin Name	Description
CSX	Chip selection signal
DCX	Clock signal
SDA	Serial data input/output1
WRX	Serial data input2

Command write mode:
The command write protocol of 2 data lane serial interface is the same with the 3-wire serial interface,so users can ignore the input data of WRX.
Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.



SRAM write mode:

The SRAM write mode of 2 data line serial interface need use SDA pin and WRX pin to be data input pins.



Read function:

The read mode of 2 data lane serial interface is the same with the 3-wire serial interface and WRX pin can be ignored.

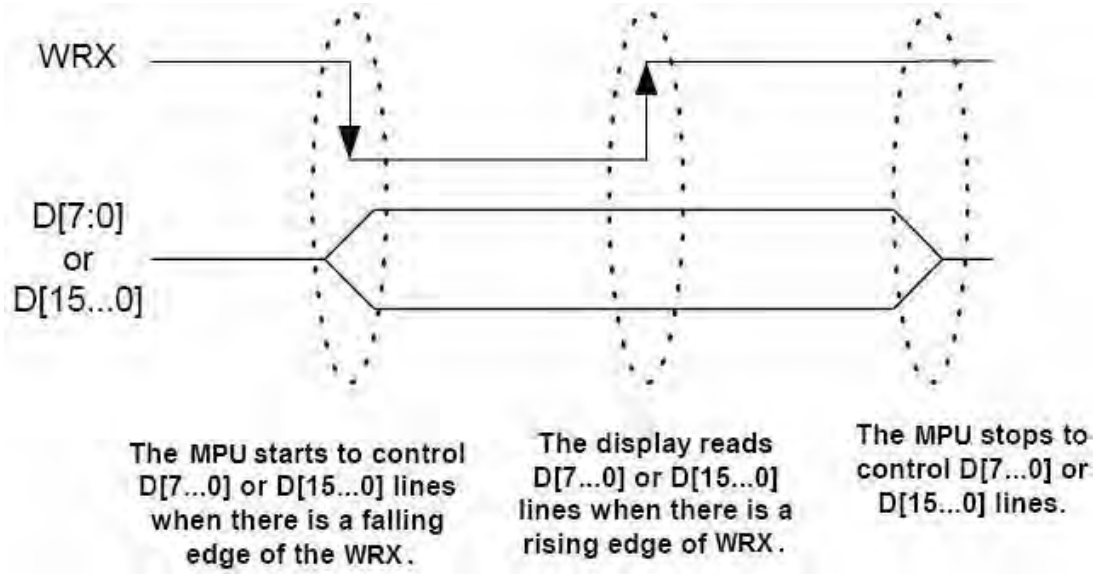
8.1.2 Parallel Interface

The Module uses a 11-wires 8-data parallel interface (IM0 = Low) or 19-wires 16-bit parallel interface (IM0 = High). The chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[7…0] or D[15…0] is parallel data.
The Graphics Controller Chip reads the data at the rising edge of WRX signal. The DCX is data/command flag. When DCX = "1", D15 (or D7) to D0 bits are display RAM data or command parameters. When DCX = "0" D15 (or D7) to D0 bits are commands.

8.1.2.1 Write Cycle/Sequence

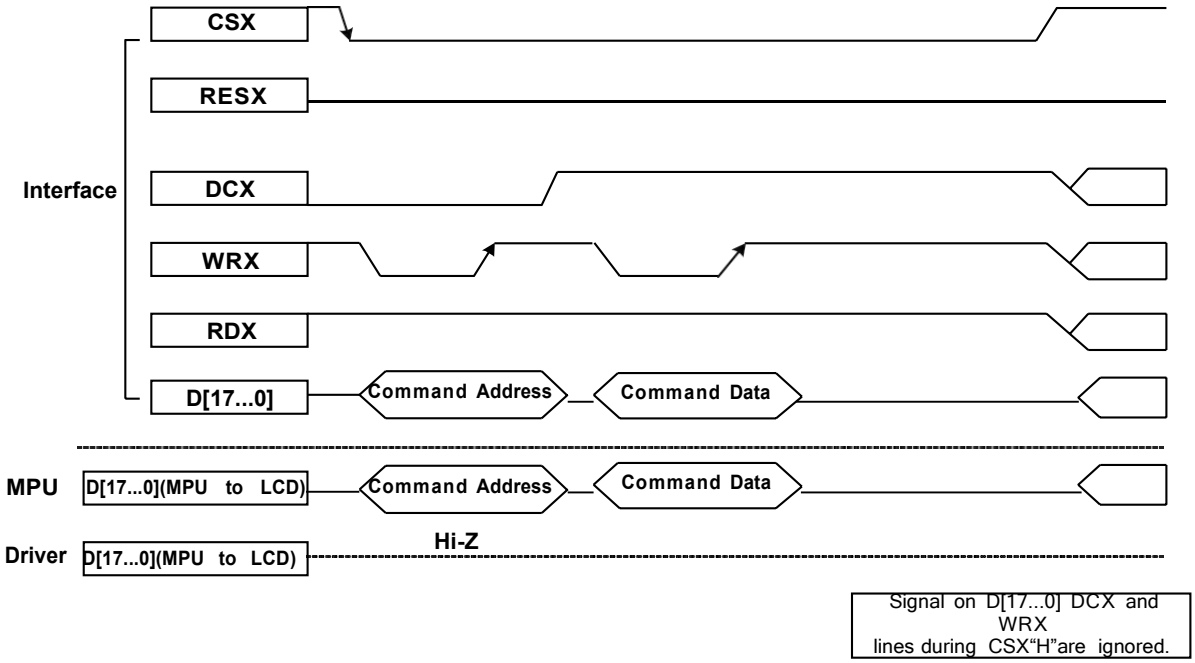
The write cycle means that the MPU writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, WRX) and 8 (D[7..0]) or 16 (D[15…0]) data signals. DCX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (='0') and vice versa it is data ('1').

The write cycle is described in the following figure.



Note: WRX is an unsynchronized signal (it can be stopped).

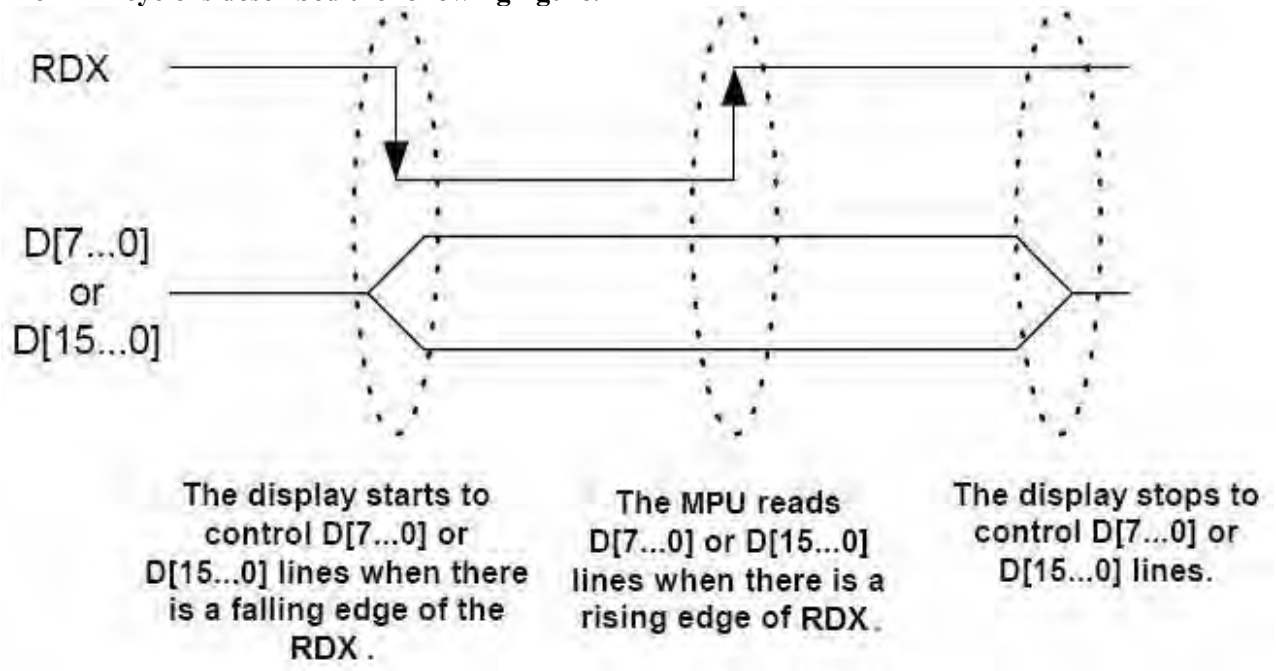
Parallel I/F write Sequence-Example



8.1.2.2 Read Cycle/Sequence

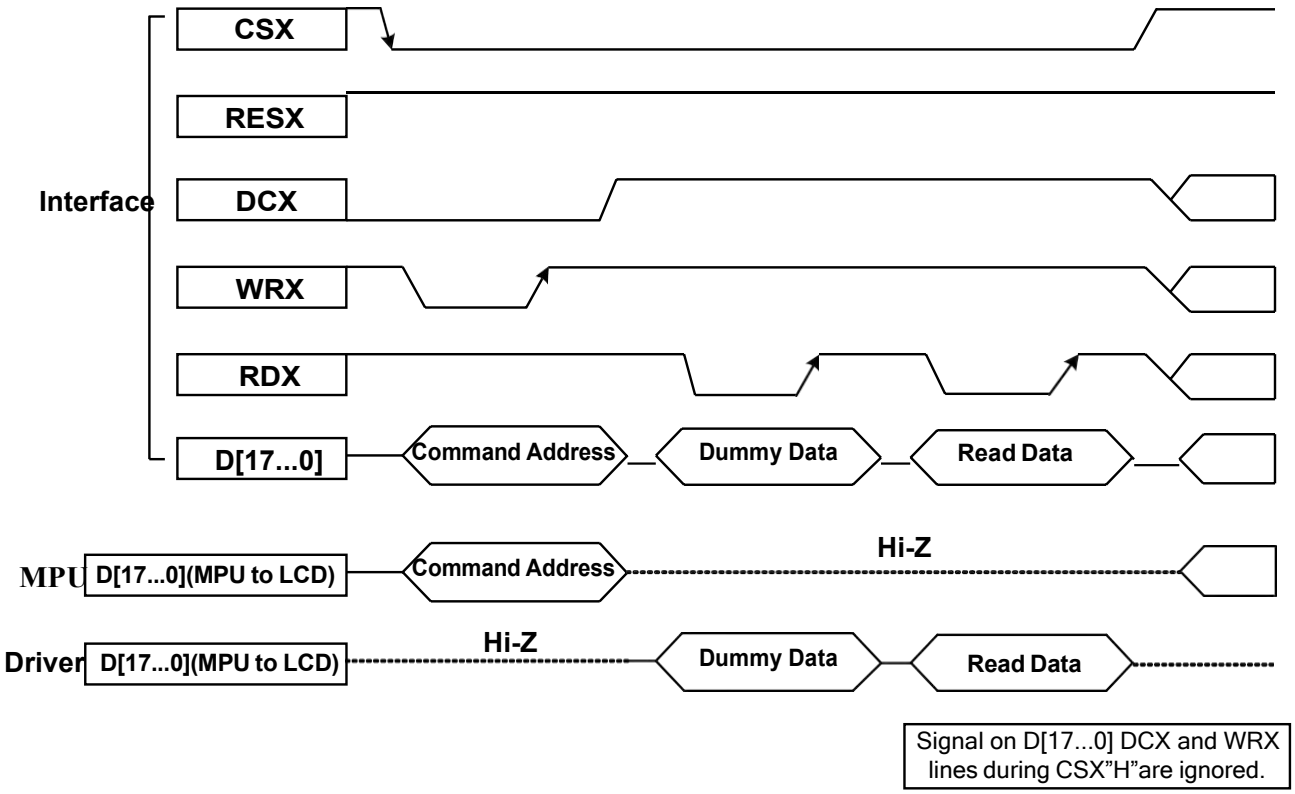
The read cycle (RDX high-low-high sequence) means that the MPU reads information from the display via interface. The display sends data (D[7...0] or D[15…0]) to the MPU when there is a falling edge of RDX and the MPU reads data when there is a rising edge of RDX.

The RDX cycle is described the following figure.



Note: RDX is an unsynchronized signal (it can be stopped).

Parallel I/F Read Sequence-example



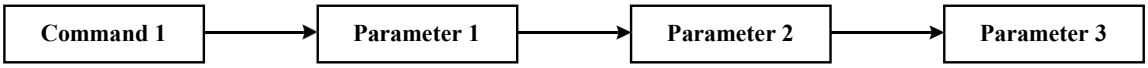
Note:

Read Data is only valid when DCX input is set High, if DCX is set Low during read then Driver Data line will be High Impedance.

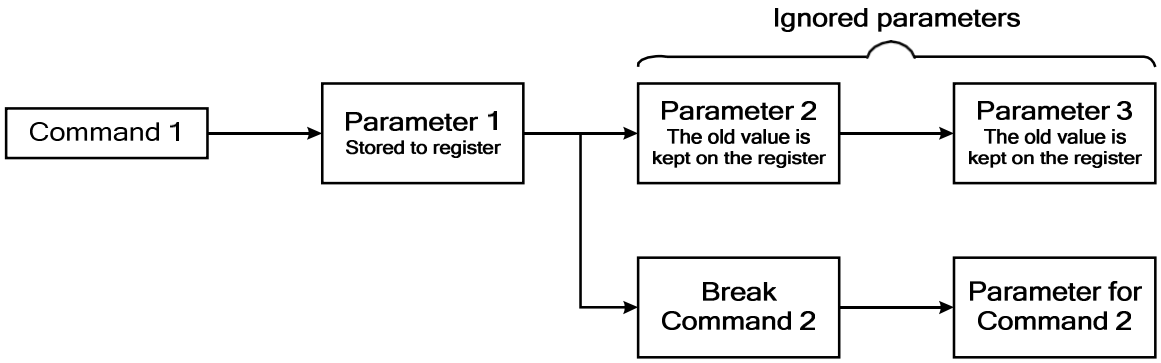
8.1.2.3 Display Module Data Transfer Break

If parameter 1 or more parameter command is being sent and a break occurs sending before the last parameter of the command and if the MPU then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameters after the break occurred is rejected if there is a new command as shown in the following example:

Without break

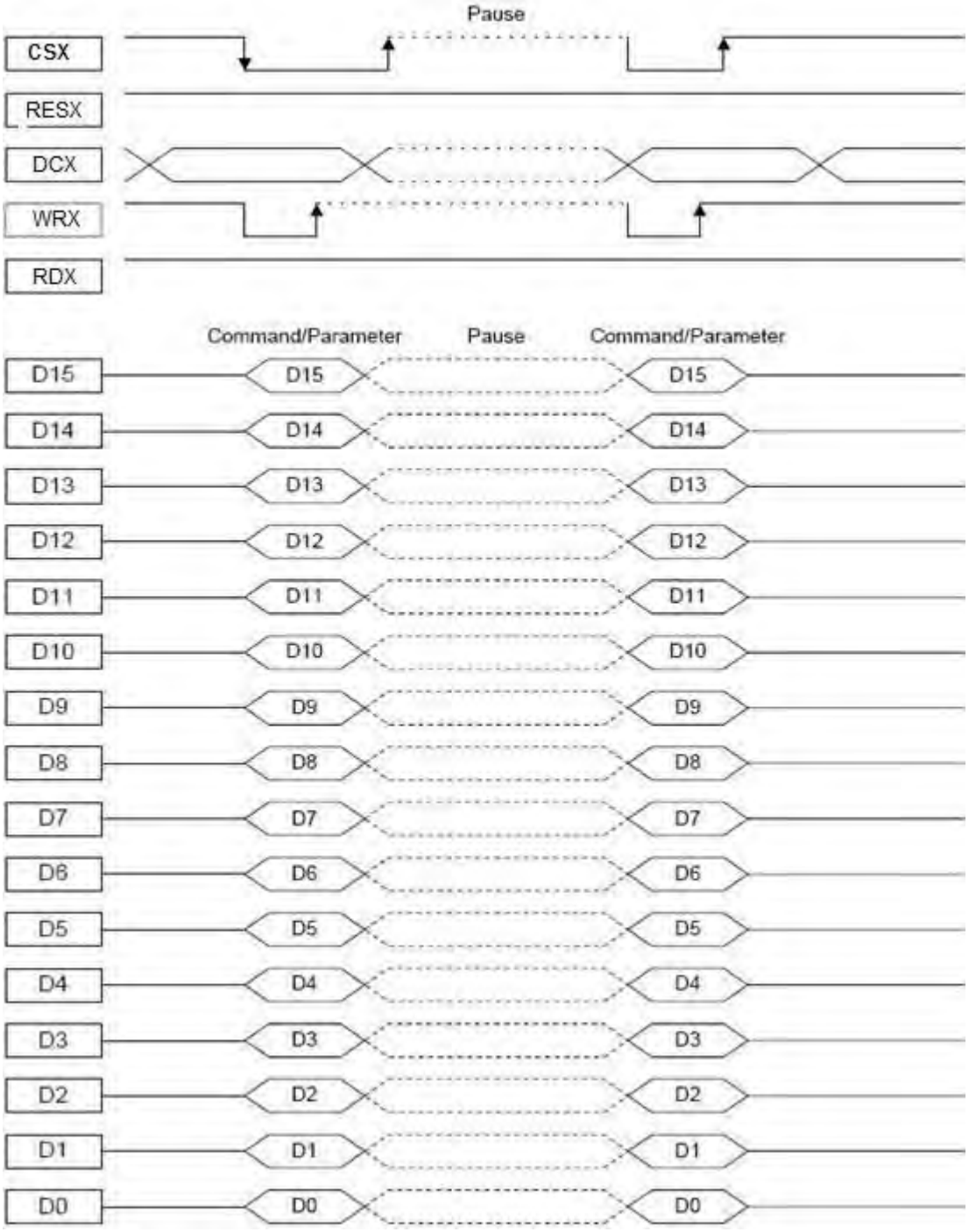


With break



Break can be another command or noise pulse.

8.1.2.4 Display Module Data Transfer Pause



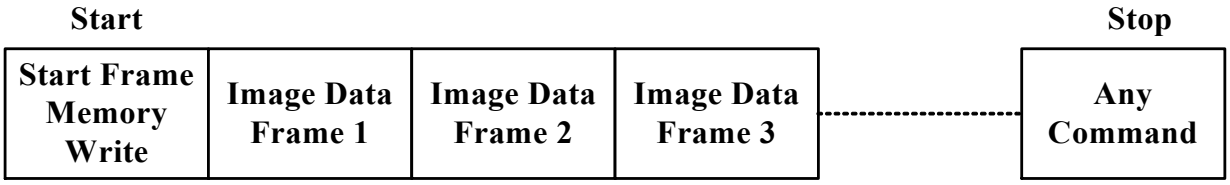
This applies to the following 4 conditions:
1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

8.1.2.5 Display Module Data Transfer Modes

The module has four color modes for transferring data to the display data RAM. These are 16-bit color per pixel, 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

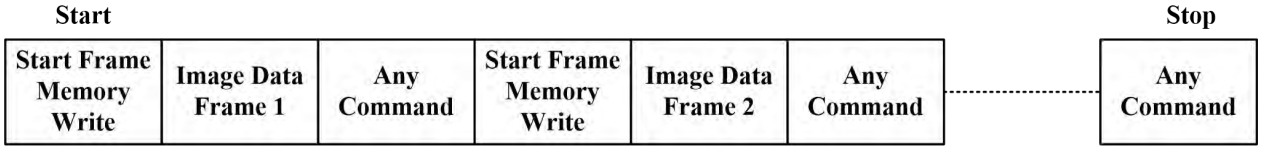
8.1.2.5.1 Method 1

The image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



8.1.2.5.2 Method 2

The image data is sent and at end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame downloaded.



Note:
1. These apply to all Data Transfer Color modes on Parallel interface;
2. The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored to the Frame Memory.

8.1.3 RGB Interface

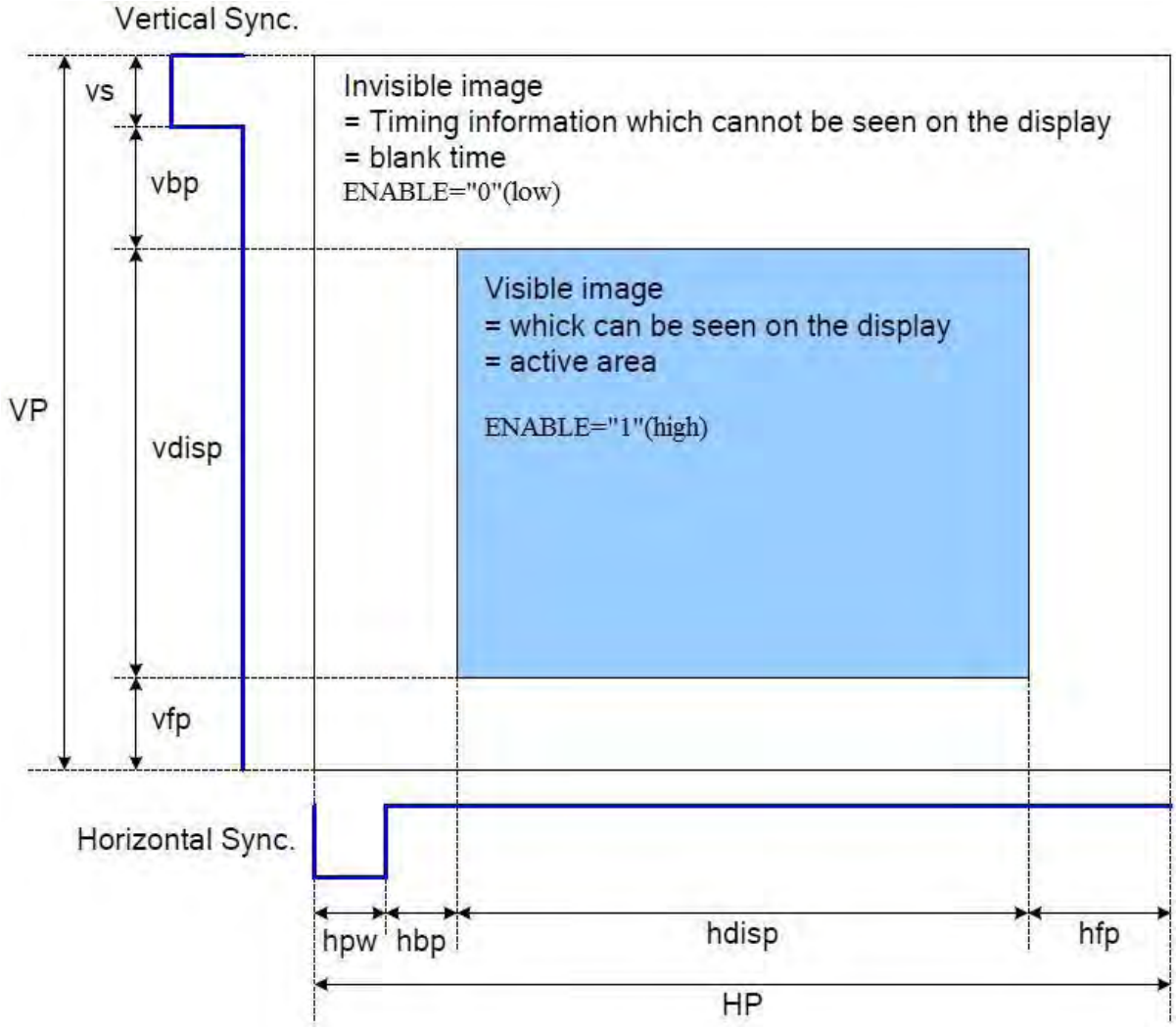
8.1.3.1 RGB interface Selection

The color format selection of RGB Interface for NV3030B is selected by setting the rim and dpi[2:0].

rim	dpi[2:0]	RGB Interface Mode	Data pins
0	110	18-bit 262K RGB Interface	DB[17:0]
0	101	16-bit 65K RGB Interface	DB[17:13], DB[11:1]
1	110	6-bit 262K RGB Interface	DB[5:0]
1	101	6-bit 65K RGB Interface	DB[5:0]

8.1.3.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	4	10	hpw+hbp=31	Clock
Horizontal Sync. Back Porch	hbp	8	10		Clock
Horizontal Sync. Front Porch	hfp	4	38	-	Clock
Vertical Sync. Width	vs	2	4	vs+vbp=127	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

8.1.3.3 RGB Interface Mode Selection

NV3030B supports two kinds of RGB interface, DE mode and SYNC mode. Each mode also can select with ram and without ram. The table shown below uses command B0h to select RGB interface mode.

RCM[1:0]	bypass_mode	Mode	Data Path	Control Signals
10	0	DE mode	without Ram	DOTCLK, ENABLE, VSYNC(optional), HSYNC(optional)
	1		Ram	
11	0	SYNC mode	without Ram	DOTCLK, VSYNC, HSYNC
	1		Ram	

The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Graphics operation function	Not available	Available

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

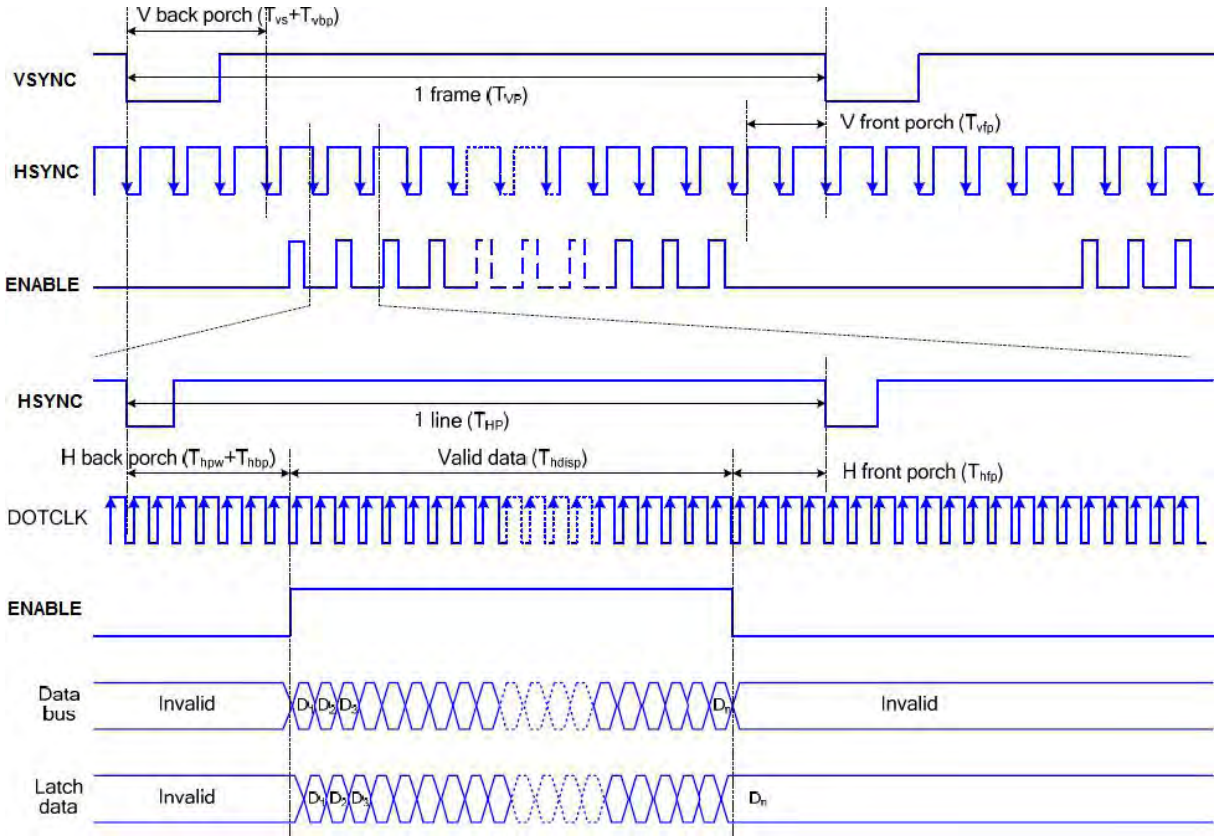
In 6-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

In 6-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

Switching between the internal operation mode and the external RGB interface mode is prohibited.

8.1.3.4 RGB Interface Timing Diagram

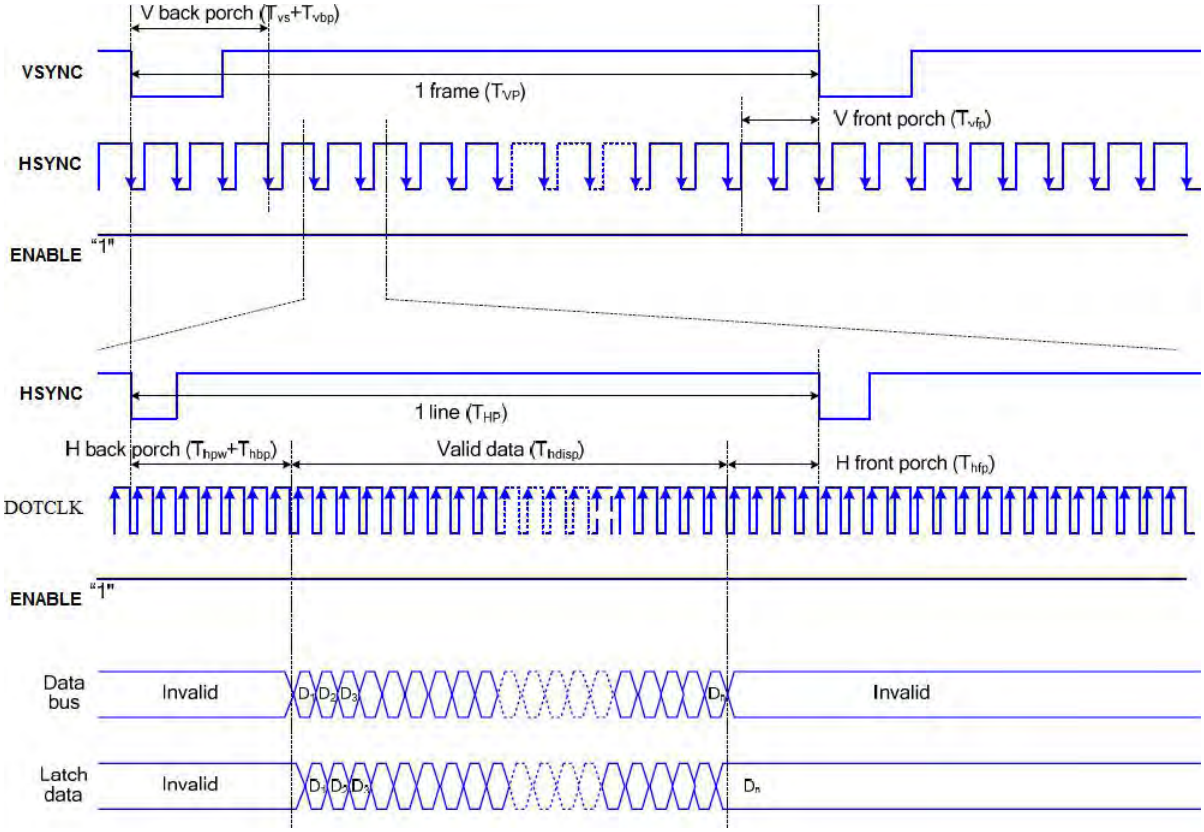
The timing chart of RGB interface DE mode is shown as follows.



Timing Chart of Signals in RGB Interface DE Mode

Note: The setting of front porch and back porch in MPU must match that in IC as this mode.

The timing chart of RGB interface SYNC mode is shown as follows.

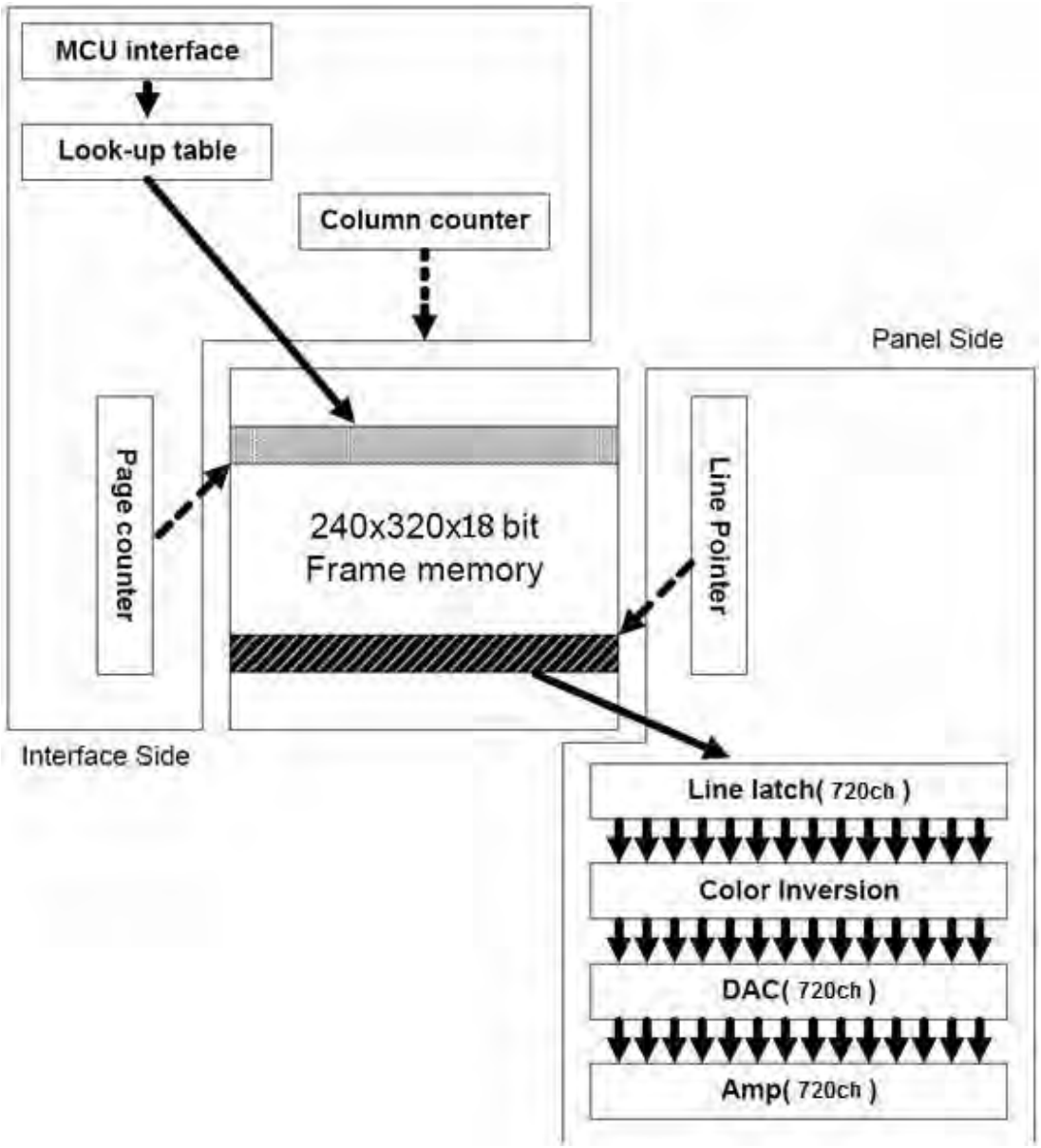


Timing chart of RGB interface SYNC mode

8.2 Display Data RAM

8.2.1 Configuration

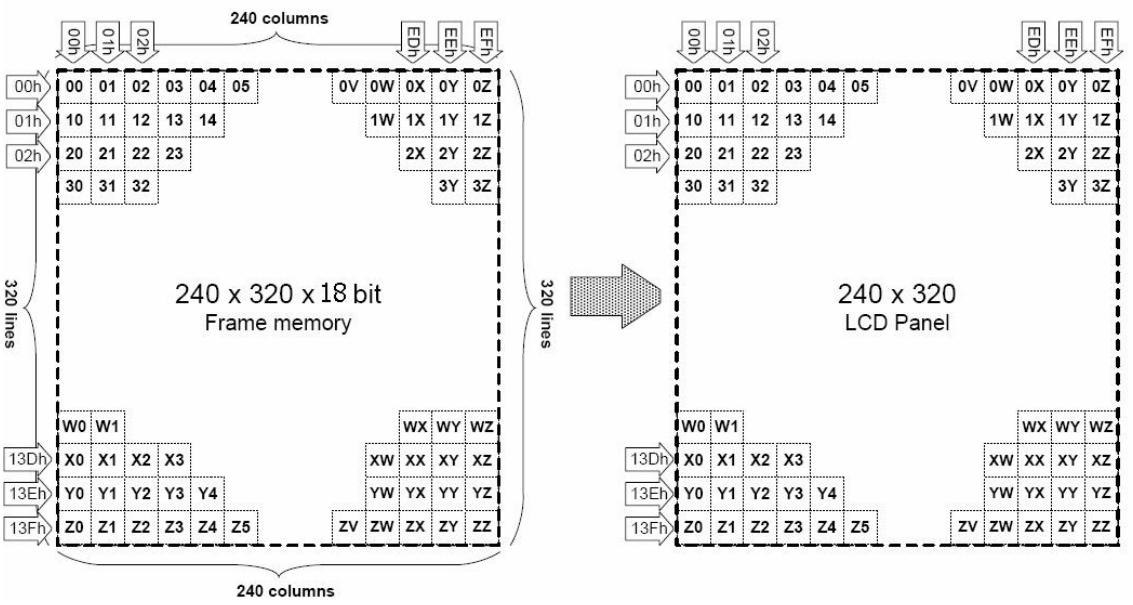
The display data RAM stores display dots and consists of 1,382,400 bits (240×320×18 bits).There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



8.2.2 Memory to Display Address Mapping

8.2.2.1 Normal Display On or Partial Mode On, Vertical Scroll Off

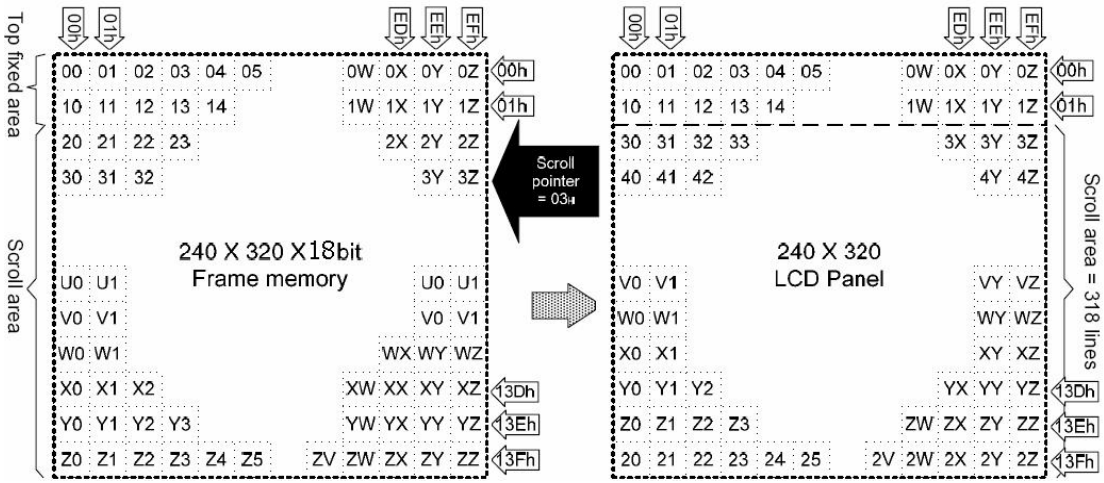
In this mode, contents of the frame memory within an area where column pointer is 0000h to 00Efh and page pointer is 0000h to 013Fh is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0).



8.2.2.2 Vertical Scroll Mode

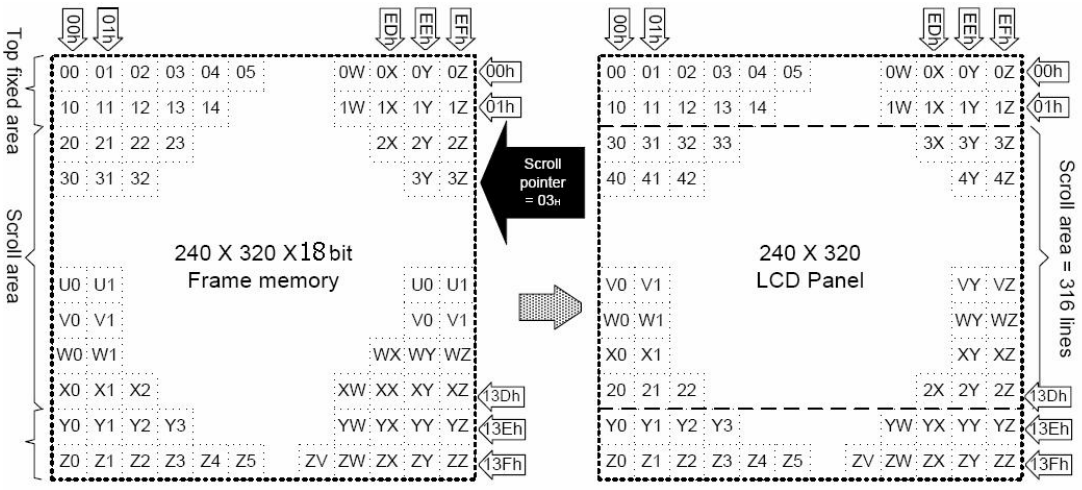
There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling” (33h) and “Vertical Scrolling Start Address” (37h).

Example 1
TFA= 2, VSA = 318, BFA = 0 when MADCTL Bit B4 = 0



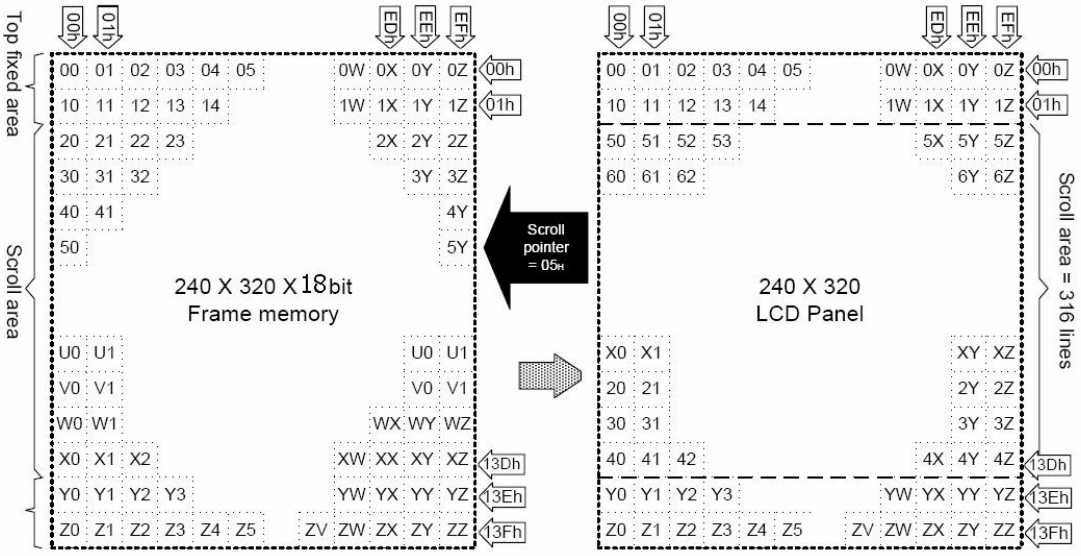
Example 2

TFA=2,VSA=316,BFA=2 when MADCTL bit B4=0



Example 3

TFA=2,VSA=316,BFA=4 when MADCTL bit B4=0



Note:

When Vertical Scrolling Parameters(TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.

8.2.2.3 Vertical Scroll example

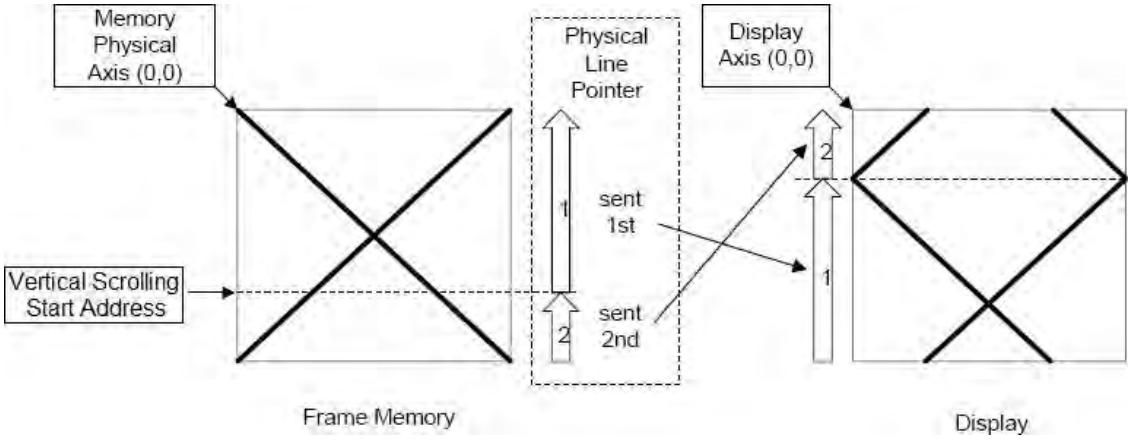
Case 1: TFA + VSA + BFA < 320

N/A. Do not set TFA + VSA + BFA < 320, unless unexpected picture will be shown.

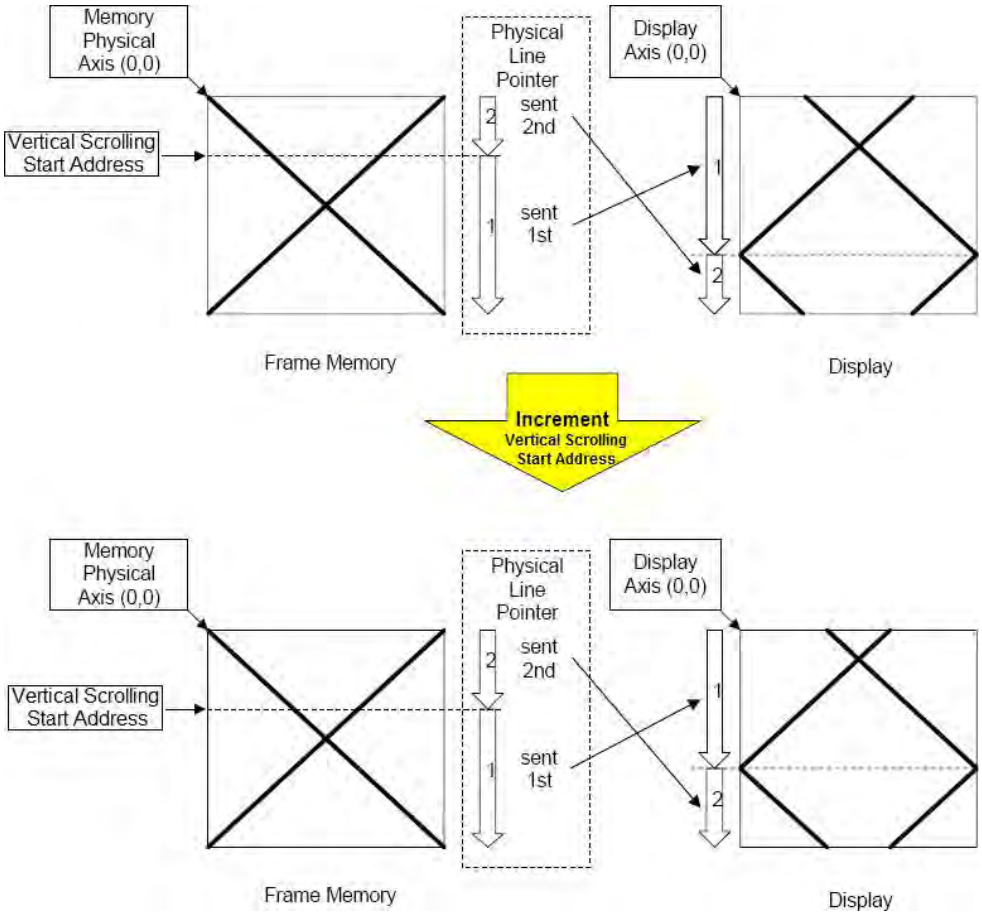
Case 2: TFA + VSA + BFA = 320 (Rolling Scrolling)

Example 2-a. When TFA = 0, VSA = 320, BFA = 0 and Vertical Scrolling Start Address = 40.

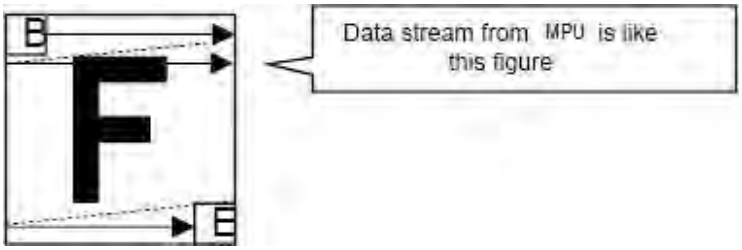
MADCTL parameter B4= “0”



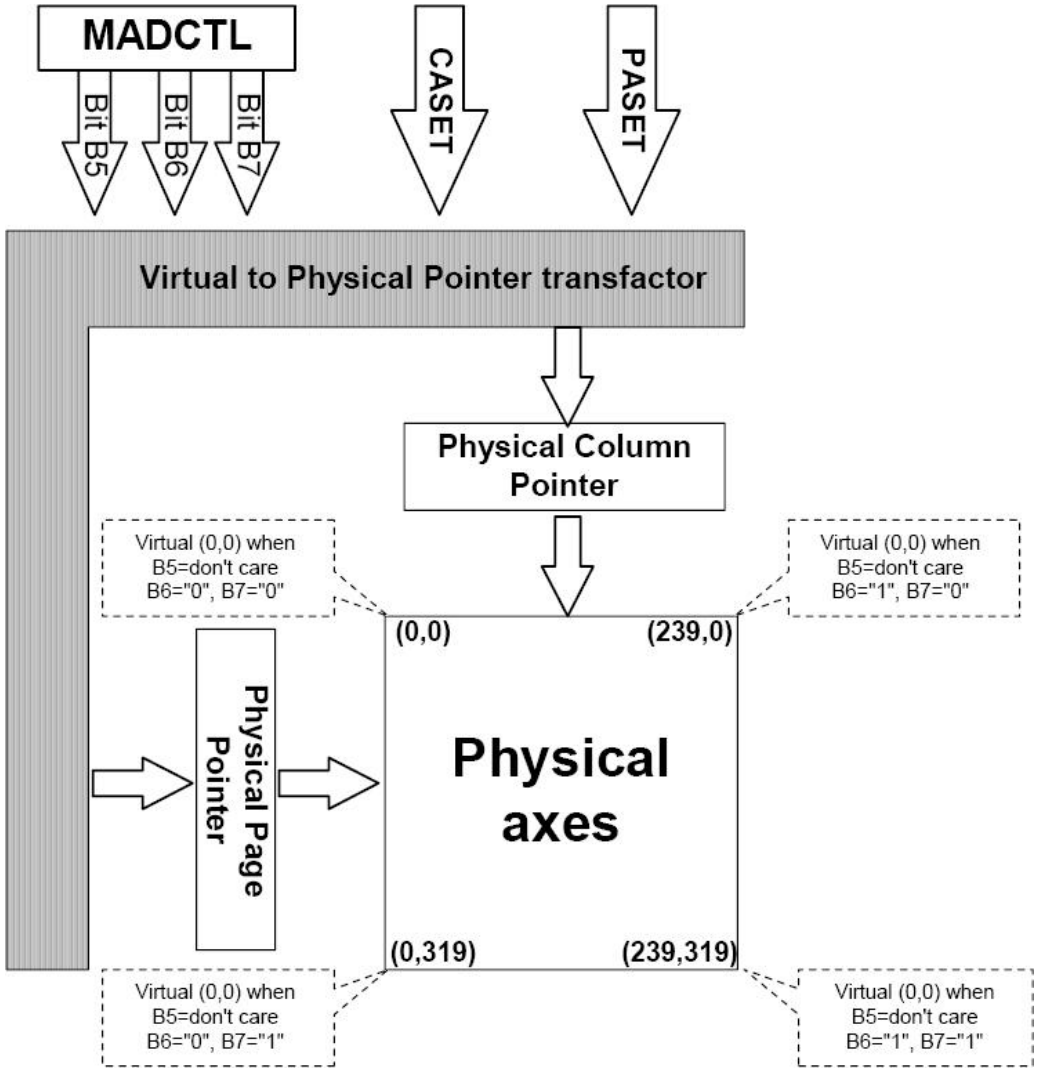
MADCTL parameter B4= “1”



8.2.3 MPU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” command, Bits B5, B6, B7 as described below.



For each image orientation, the controls for the column and page counters apply as below:

B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direc to(239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When memory write/memory read command is accepted	Return to “Start Column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than “End Column”	Return to “Start Column”	Increment by 1
The Column counter value is larger than “End Column” and the Page counter value is larger than “End Page”	Return to “Start Column”	Return to “Start Page”

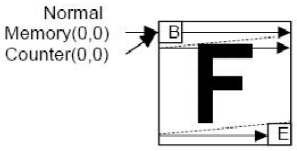
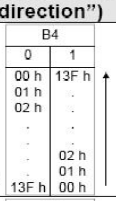
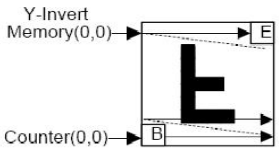
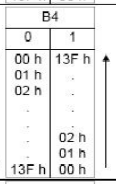
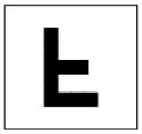
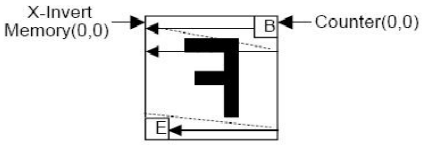
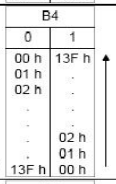
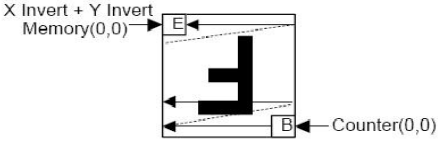
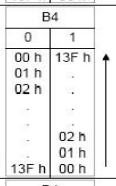
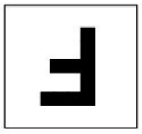
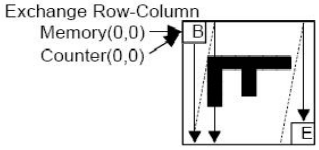
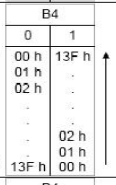
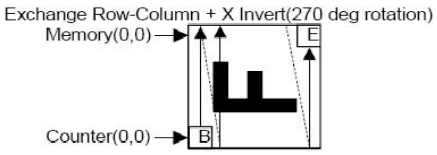
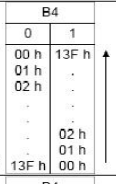
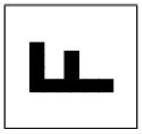
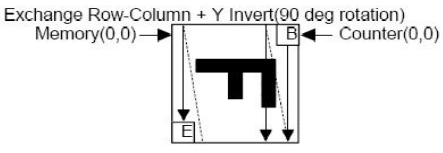
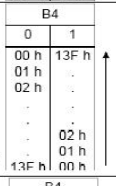
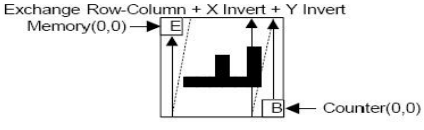
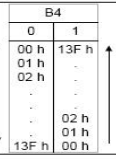
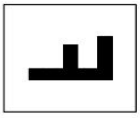
Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

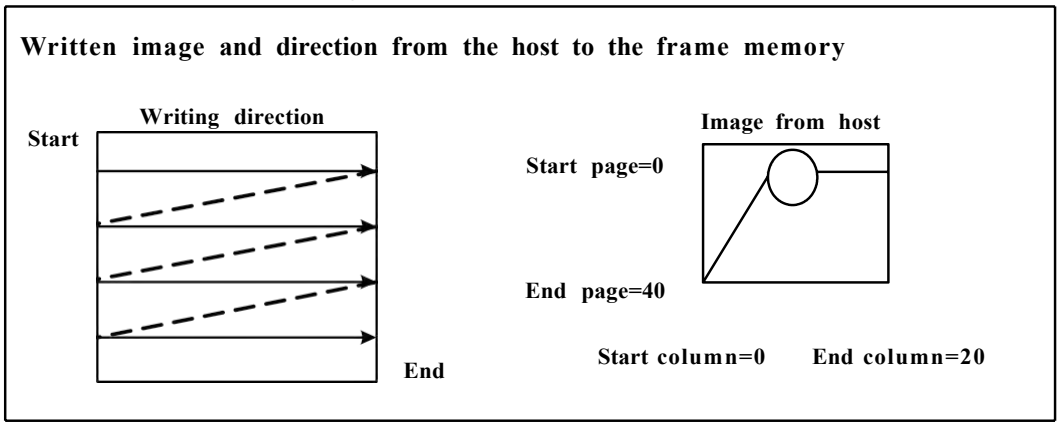
One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

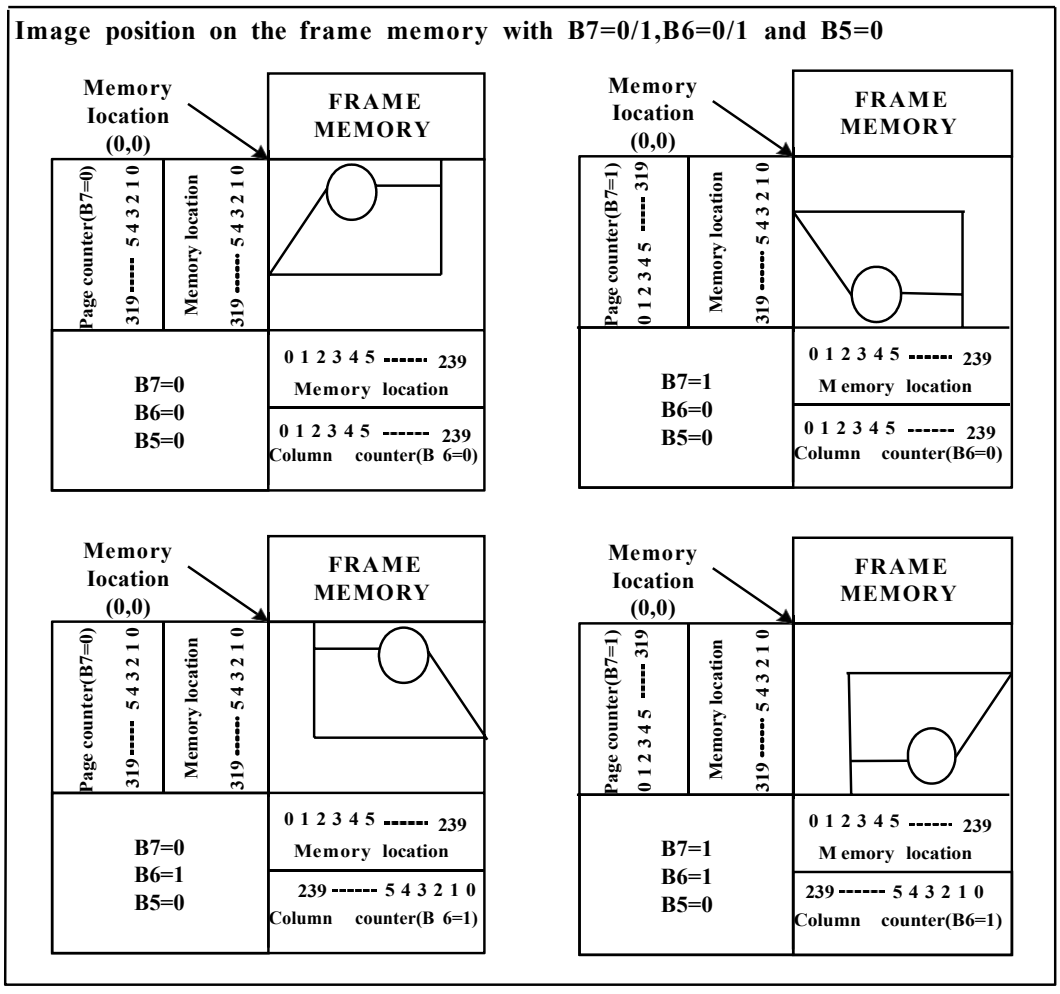
This resultant image for each orientation setting is illustrated below:

B5 B6 B7 (Bits)	Image in the memory ("→" means "MCU to memory read/write direction")	B4 Bit ("→" means "RAM to display scan direction")	Image in the Display
0 0 0			
0 0 1			
0 1 0			
0 1 1			
1 0 0			
1 0 1			
1 1 0			
1 1 1			

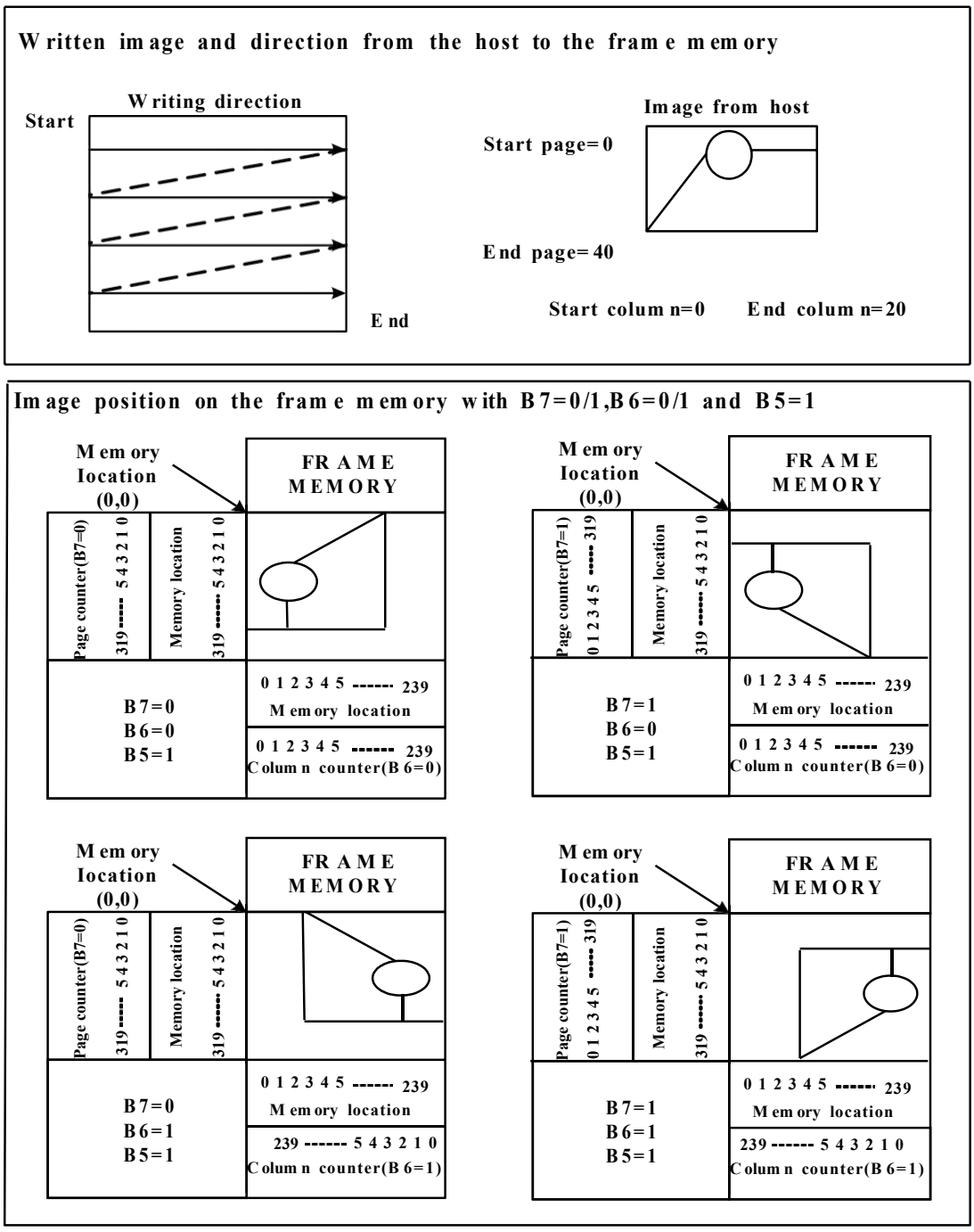
Example for rotation with B7, B6 and B5
This example is using following values:
start page = 0, end page = 40, start column = 0 and end column = 20
= Commands: page address set (0,40) and column address set (0,20).

The sent figure is as follows and its sending order is as follows:





The sent figure is as follows and its sending order is as follows:



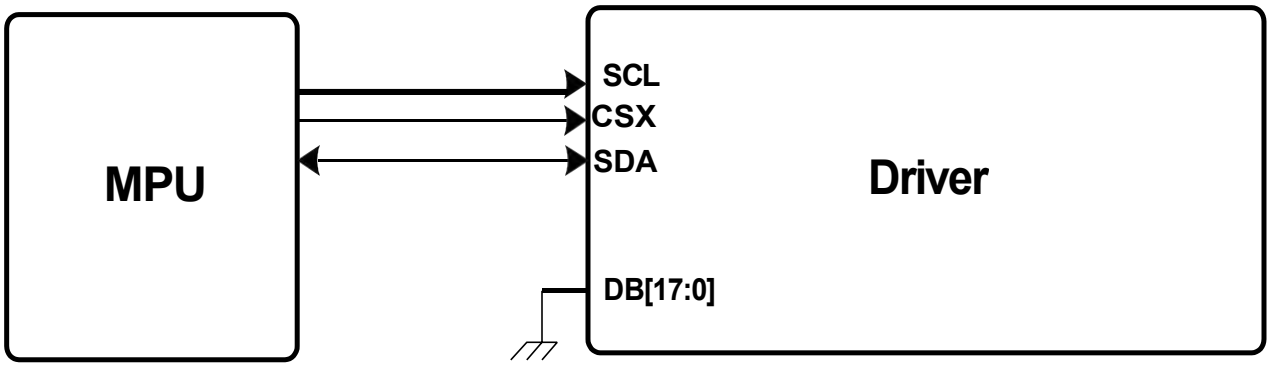
8.3 Display Data Format

NV3030B supplies 18-/16-/9-/8-bit parallel interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-wire serial interface and 6-/16-18-bit parallel RGB interface. The parallel interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters rcm[1:0].

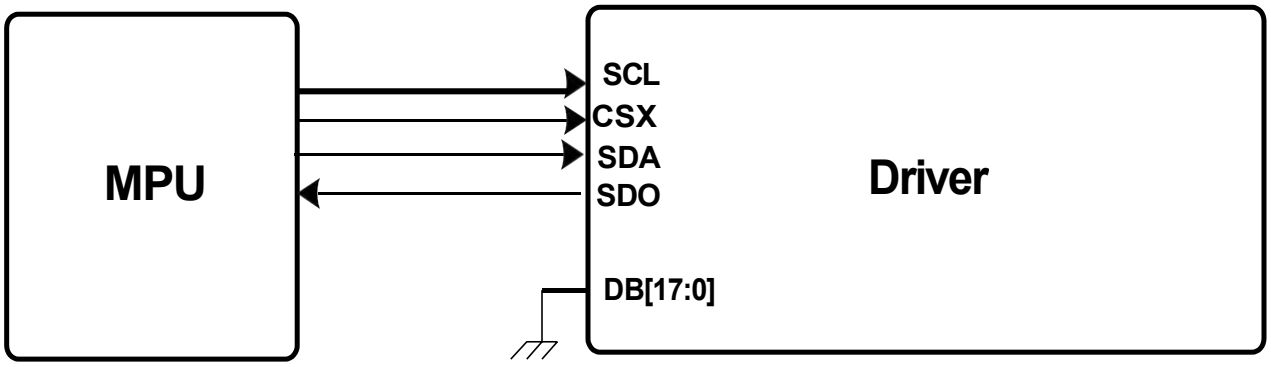
8.3.1 3-wire Serial Interface

The 3-wire/9-bit serial bus interface of NV3030B can be used by setting external pin as IM [3:0] to "0101" for serial interface I or IM [3:0] to "1101" for serial interface II. The shown figure is the example of 3-wire SPI interface.

3-wire Serial interface I

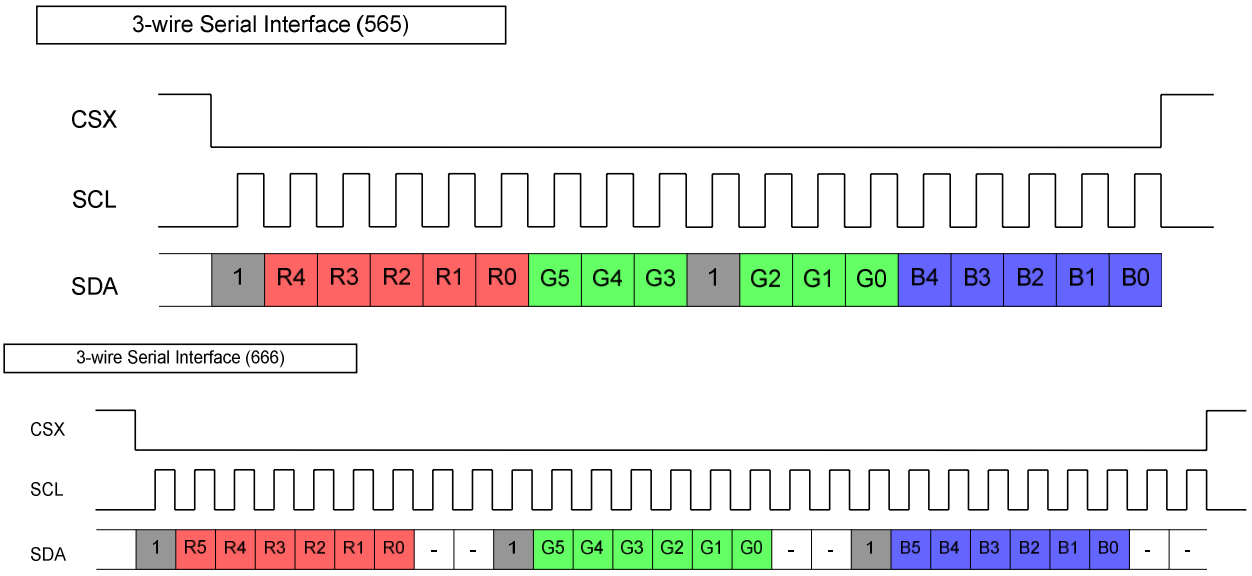


3-wire Serial interface II



In 3-wire serial interface, different display data format is available for two color depths supported by the LCM listed below:

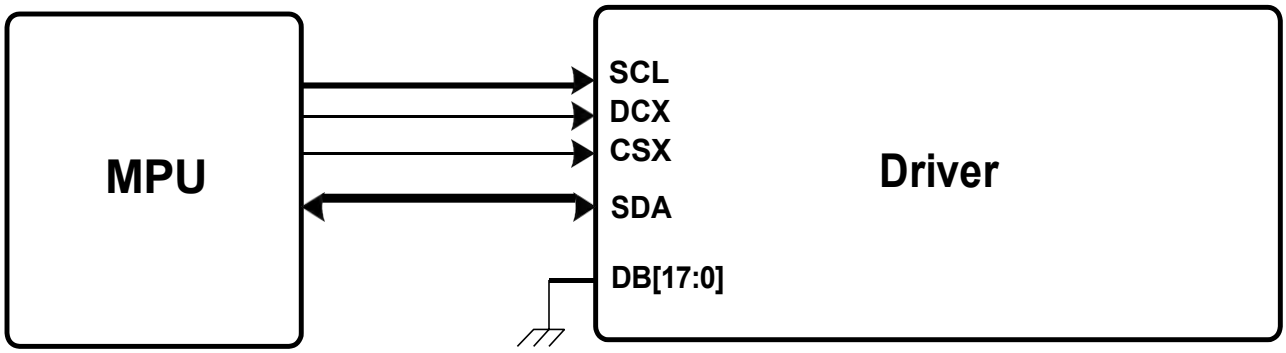
1. -65k colors, RGB 5, 6, 5 –bits input.
2. -262k colors, RGB 6, 6, 6 –bits input.



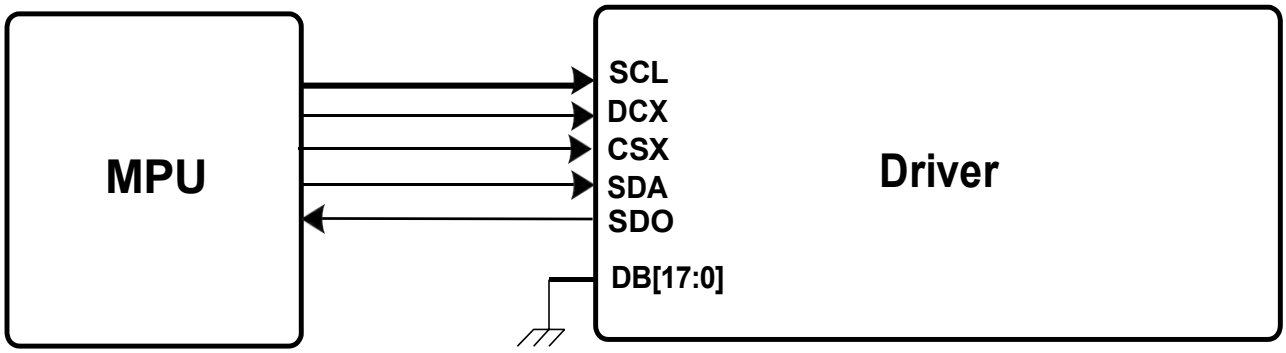
8.3.2 4-wire Serial Interface

The 4-wire/8-bit serial bus interface of NV3030B can be used by setting external pin as IM [3:0] to “0110” for serial interface I or IM [3:0] to “1110” for serial interface II. The shown figure is the example of 4-wire SPI interface.

4- wire Serial interface I

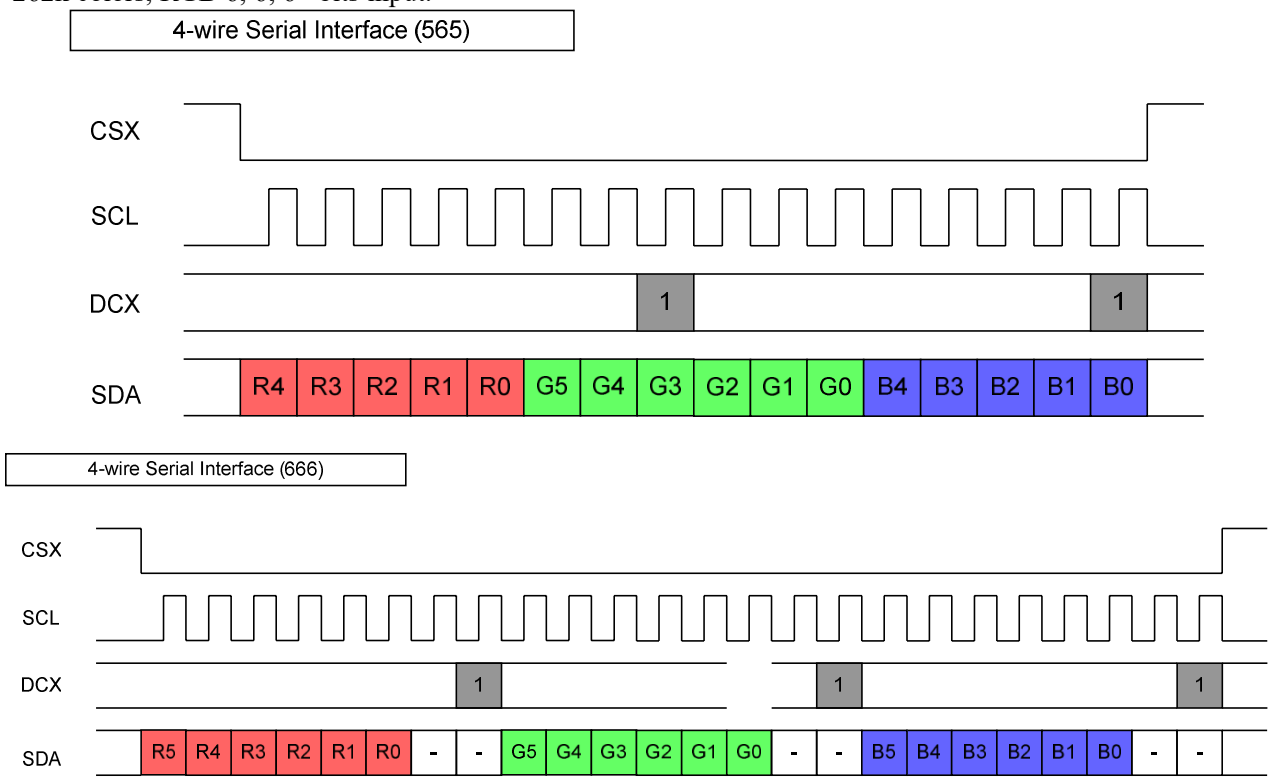


4-wire Serial interface II



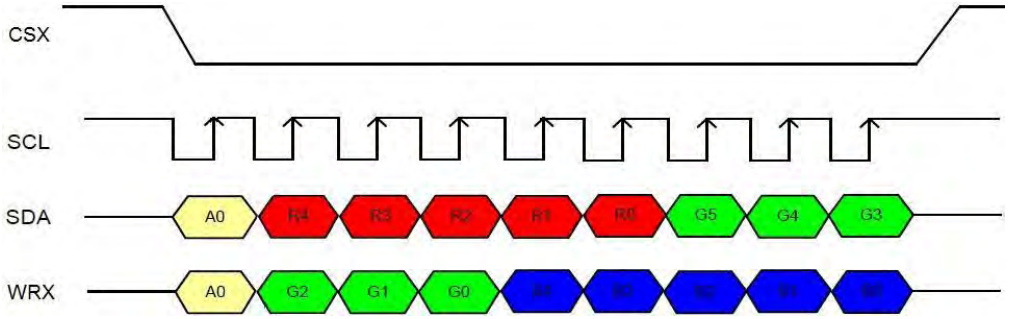
In 4-wire serial interface, different display data format is available for two color depths supported by the LCM listed below:

1. -65k colors, RGB 5, 6, 5 –bits input.
2. -262k colors, RGB 6, 6, 6 –bits input.

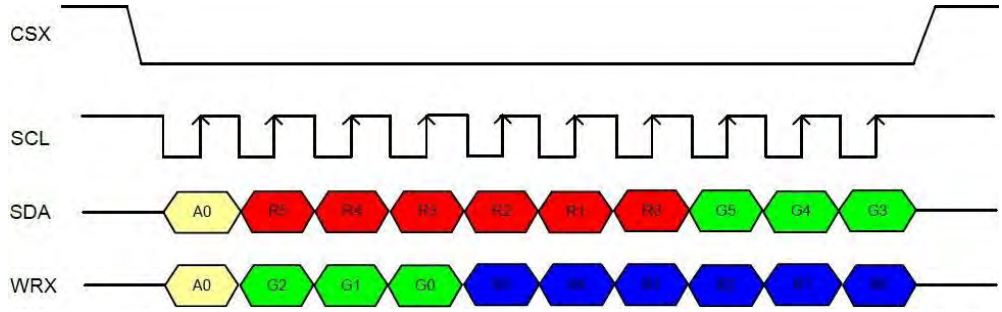


8.3.3 2 data lane serial interface

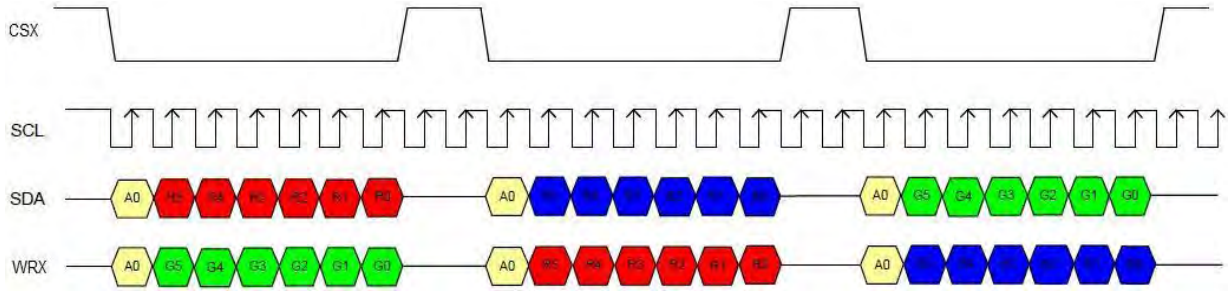
1) RGB565



2) RGB666,mdt=00



3) RGB666,mdt=01



8.3.4 Parallel Interface

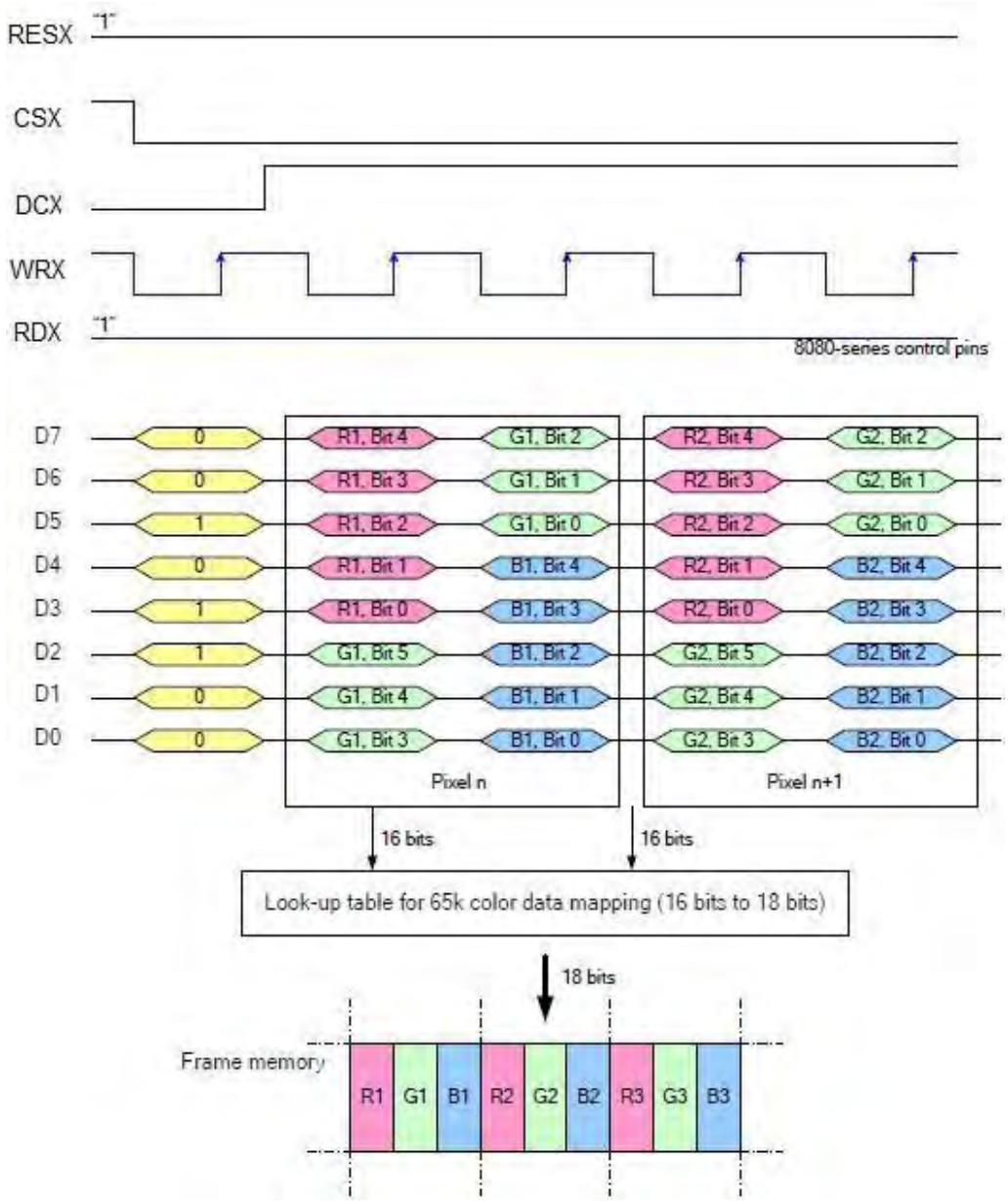
8.3.4.1 8080-Ⅰ series 8-bit Parallel Interface

The 8080-Ⅰ series 8-bit parallel interface of NV3030B can be used by setting IM[3:0]=”0000b”. Different display data formats are available for two Colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

8.3.4.1.1 16-bit/pixel

There is 1pixel (3 sub-pixels) per 2-byte



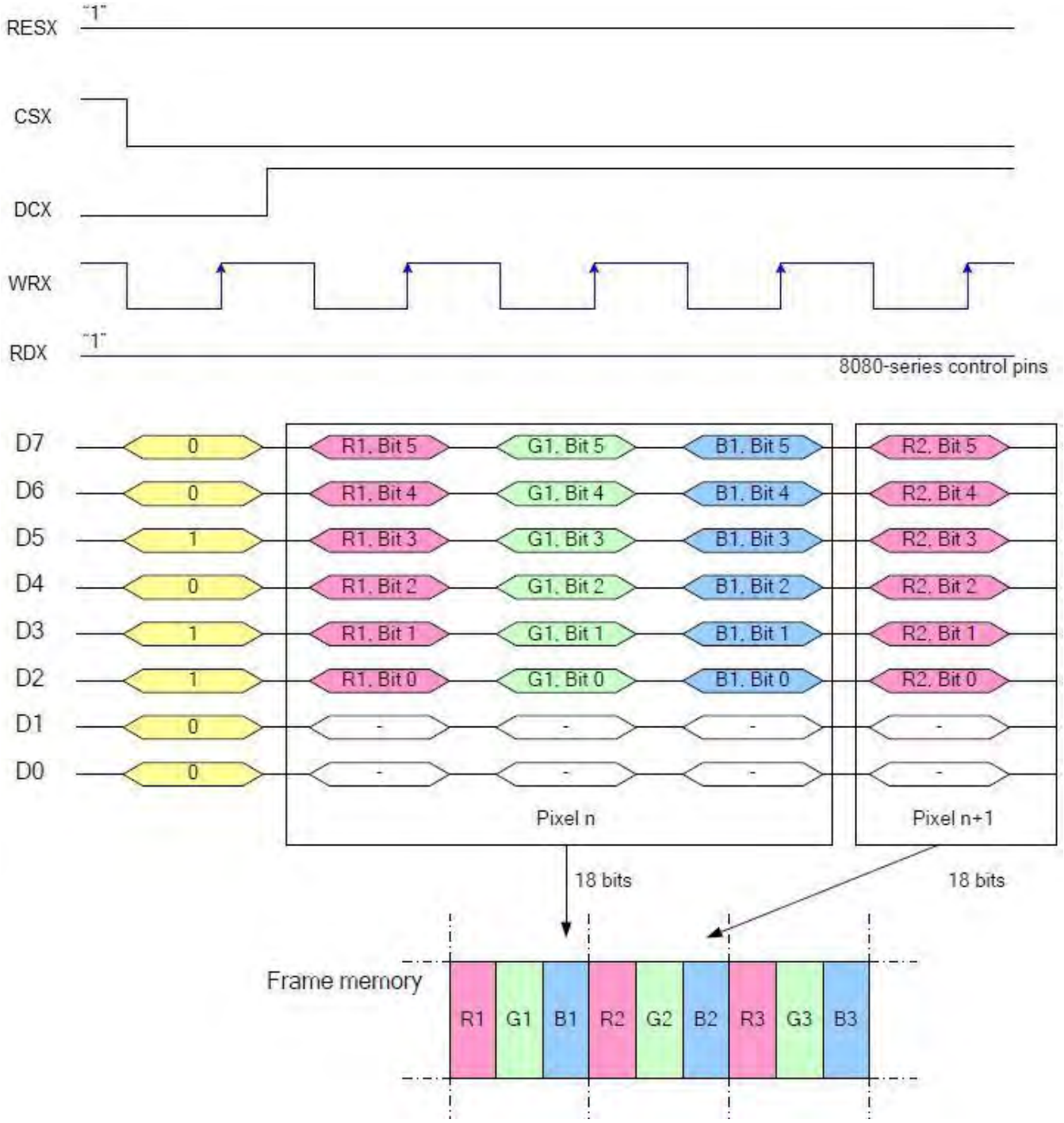
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.1.2 18-bit/pixel

There is 1pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

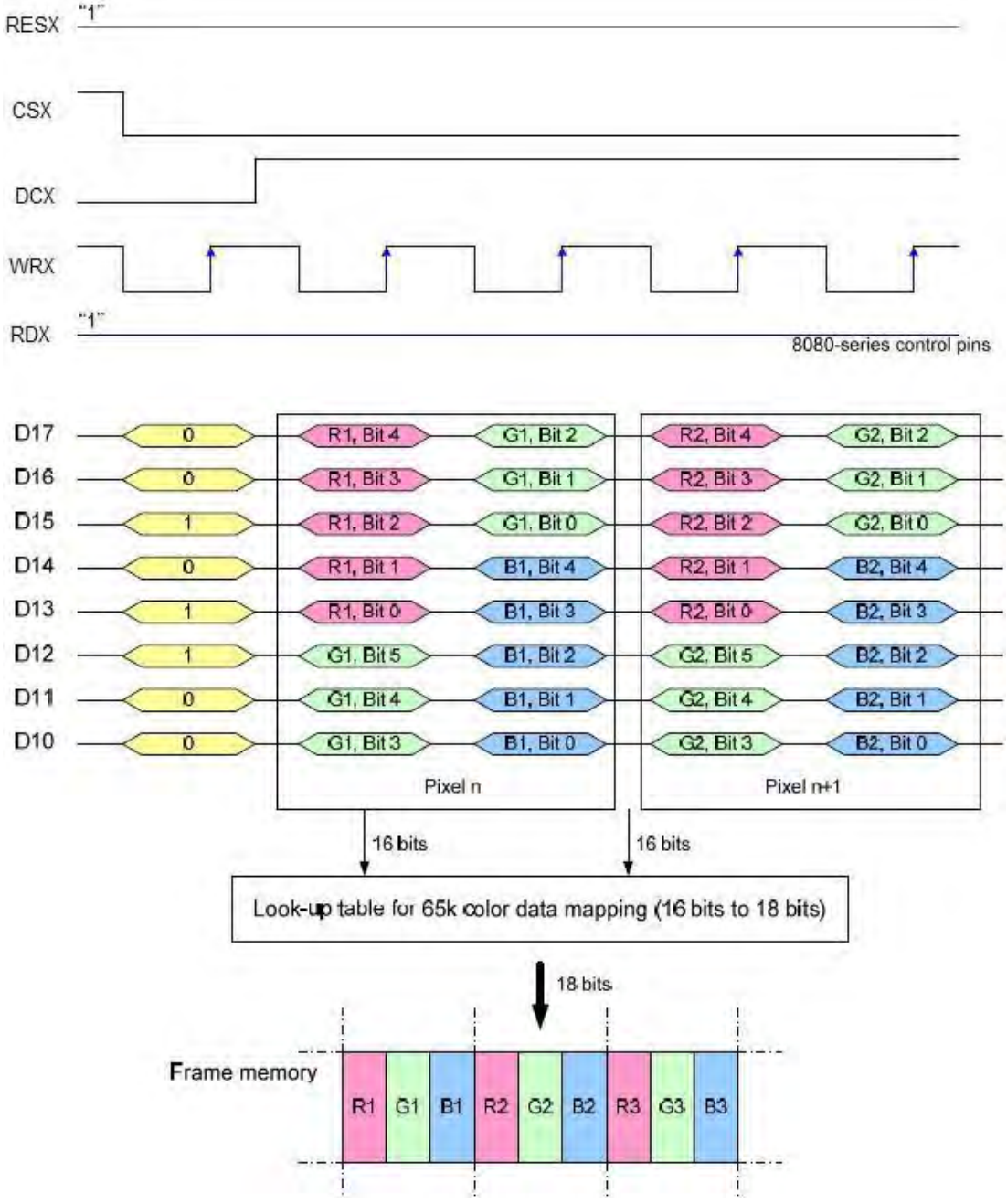
Note 3: '-' = Don't care – Can be set to '0' or '1'.

8.3.4.2 8080-Ⅱ series 8-bit Parallel Interface

The 8080-Ⅱ series 8-bit parallel interface of NV3030B can be used by setting IM[3:0]=”1001b”. Different display data formats are available for two Colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

8.3.4.2.1 16-bit/pixel

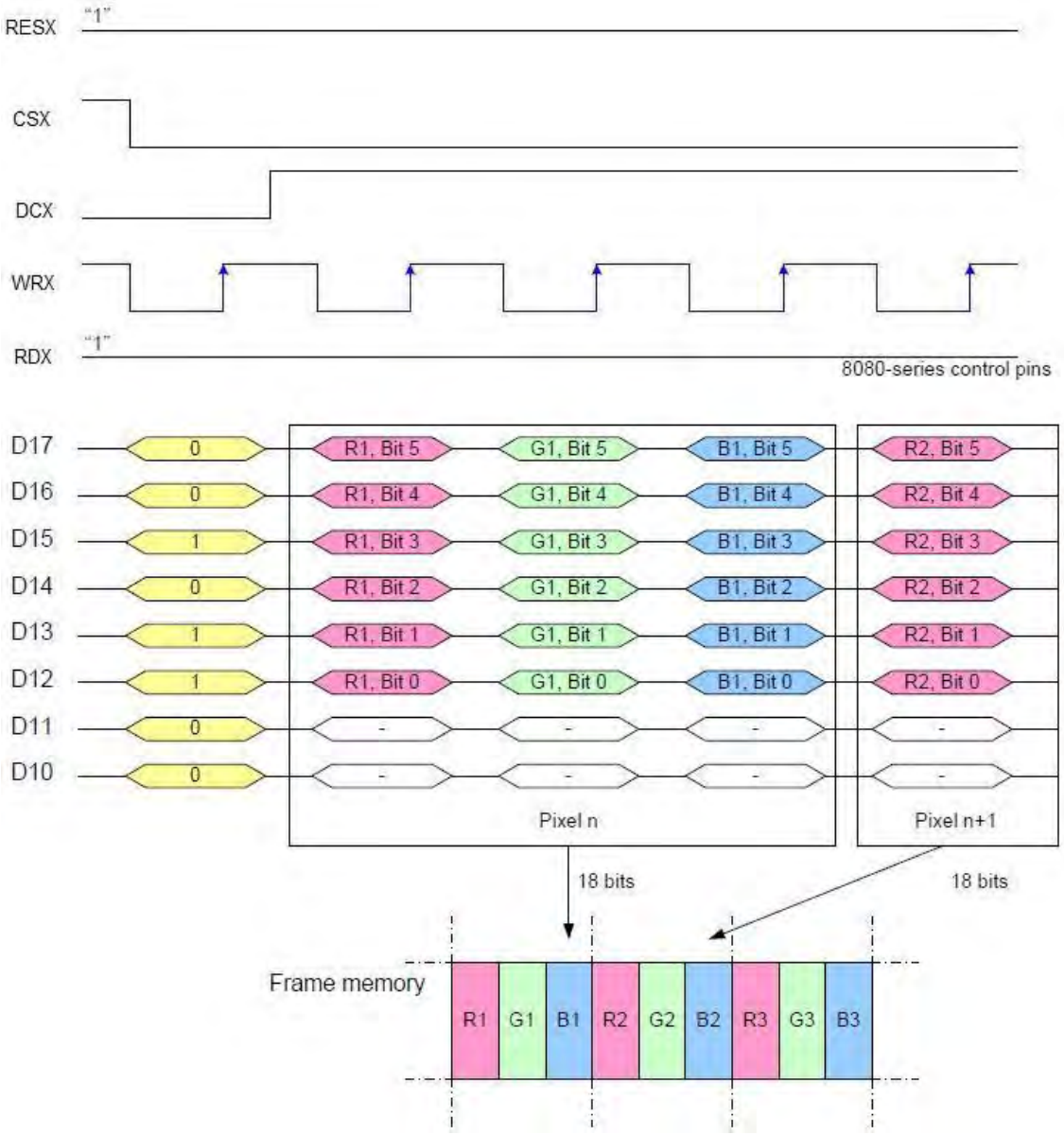


Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.2.2 18-bit/pixel



Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

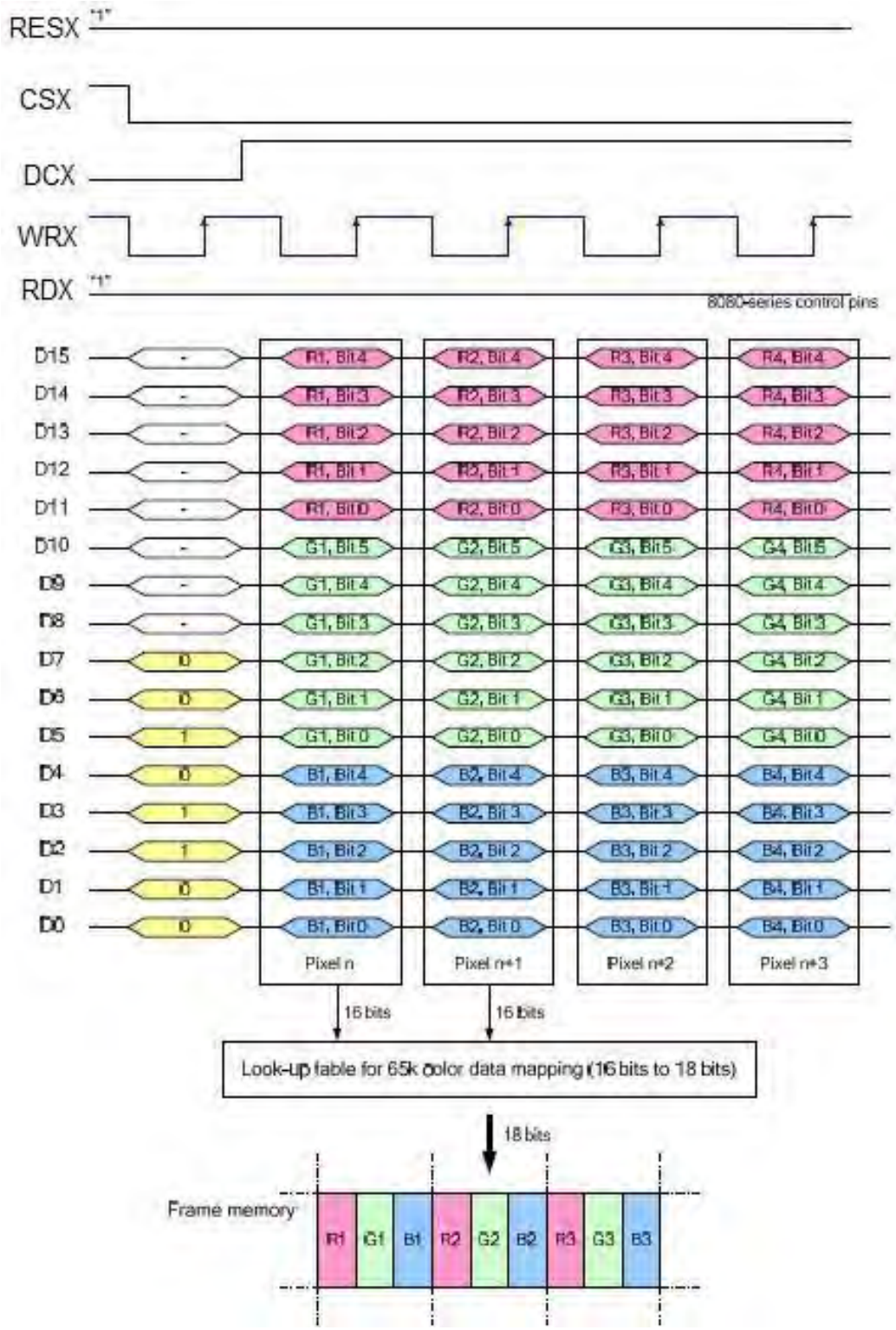
8.3.4.3 8080-Ⅰ series 16-Bit Parallel Interface

The 8080-Ⅰ series 16-bit parallel interface of NV3030B can be used by setting IM[3:0]="0001b". Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

8.3.4.3.1 16-bit/pixel

There is 1 pixel (3 sub-pixels) per 1 byte



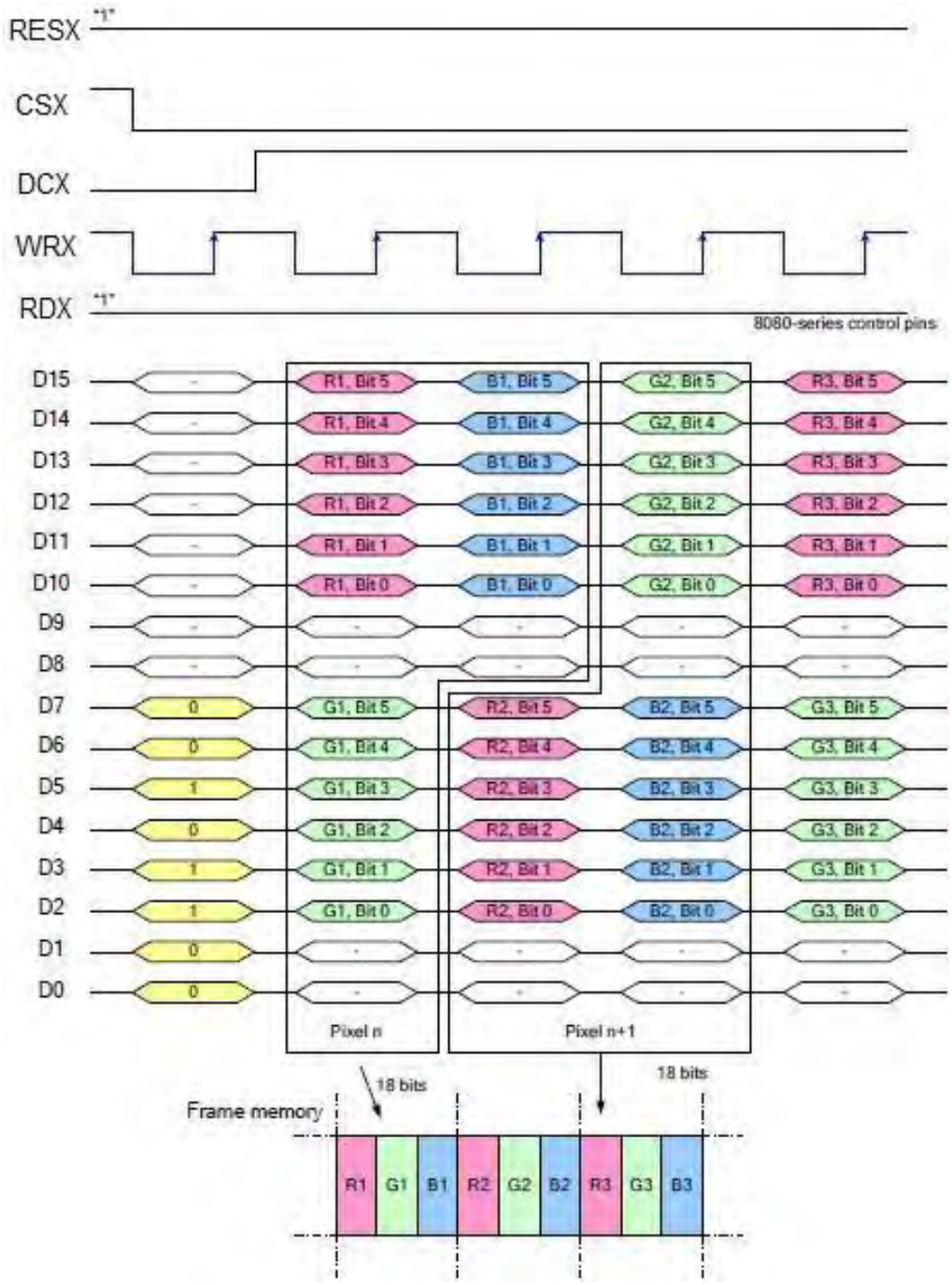
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1' .

8.3.4.3.2 18-bit/pixel(MDT[1:0]=”00b”)

There are 2 pixels (6 sub-pixels) per 3 bytes

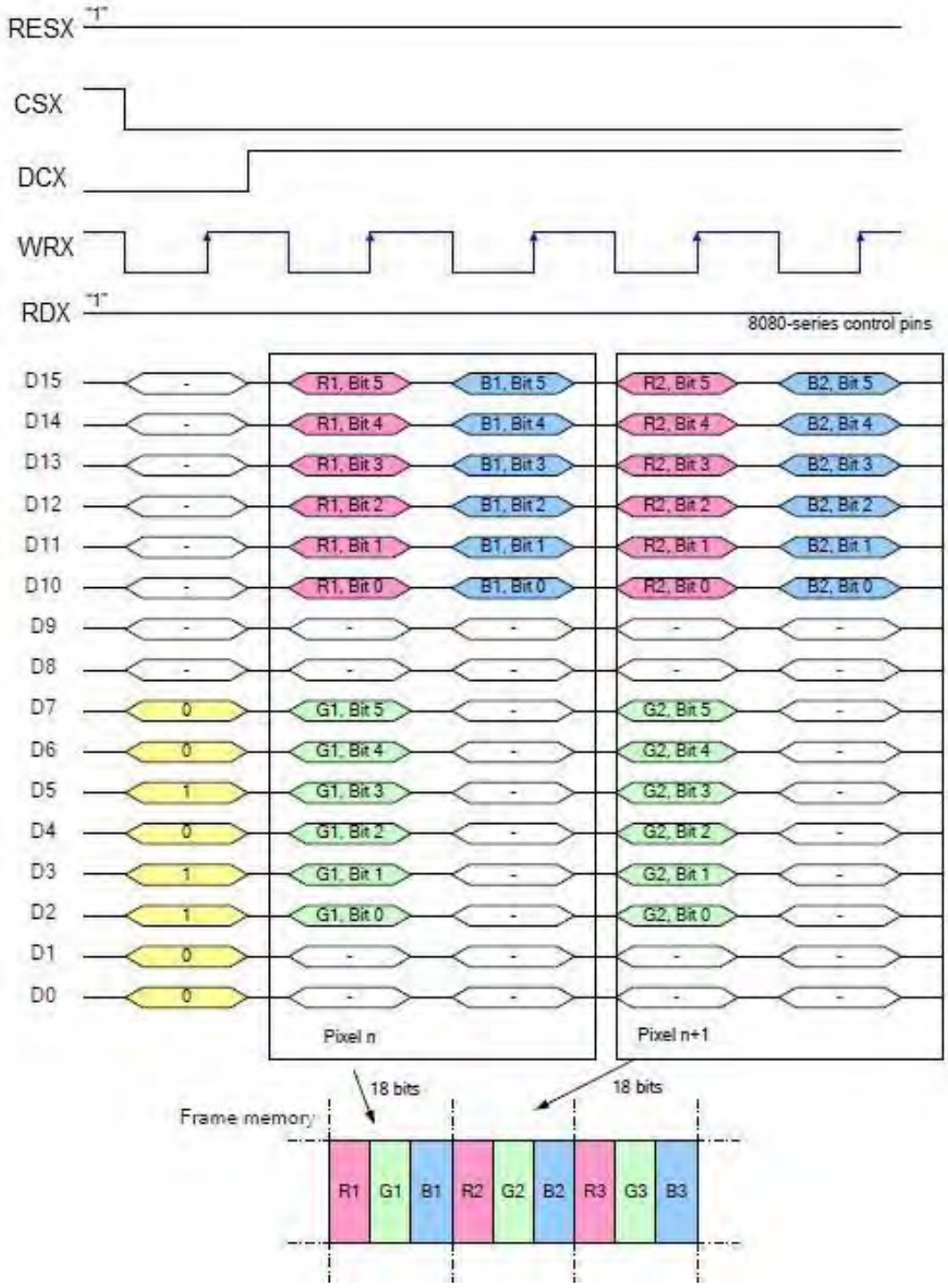


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.3.3 18-bit/pixel(MDT[1:0]=”01b”)

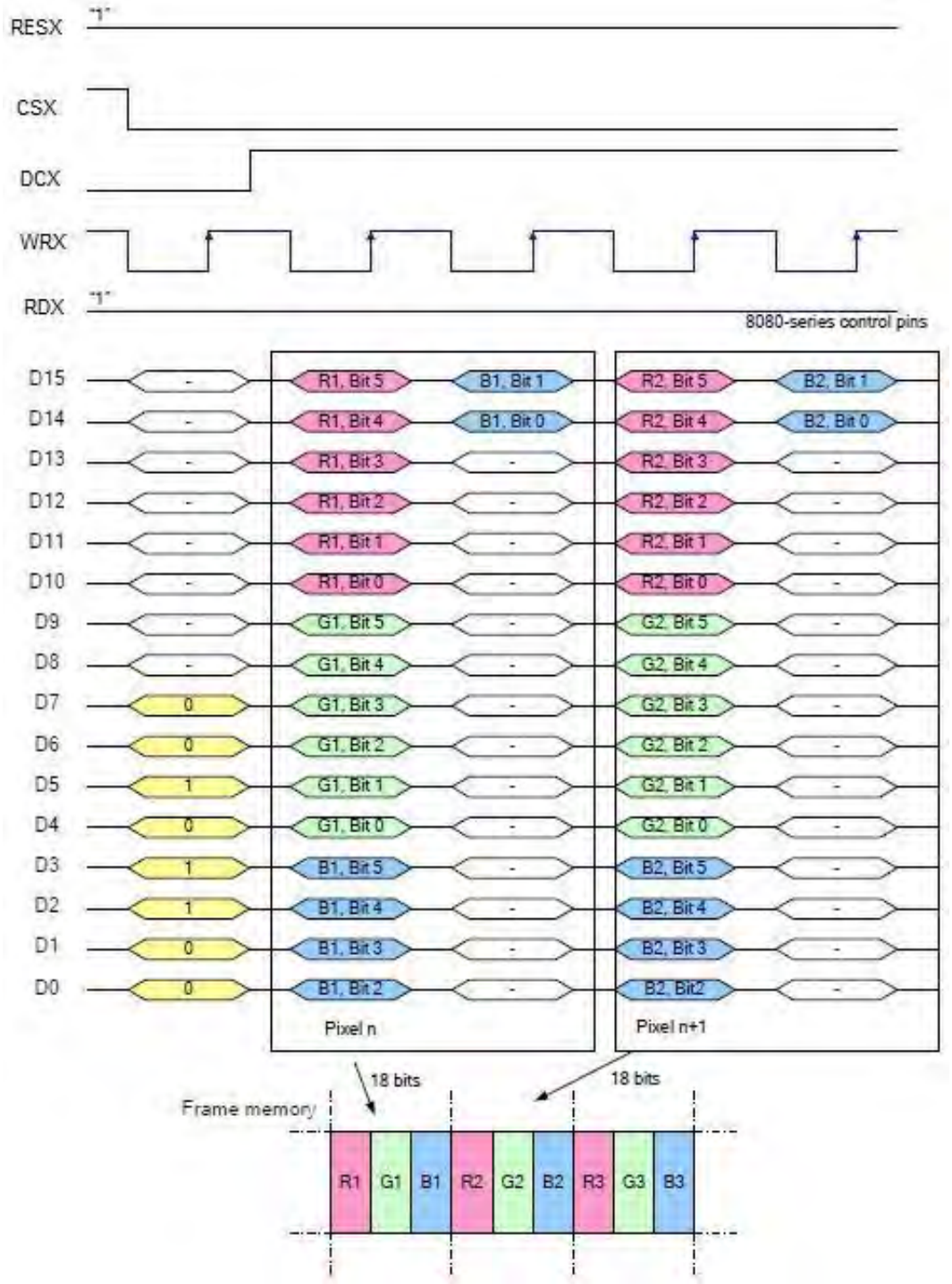


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’= Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.3.4 18-bit/pixel(MDT[1:0]=”10b”)

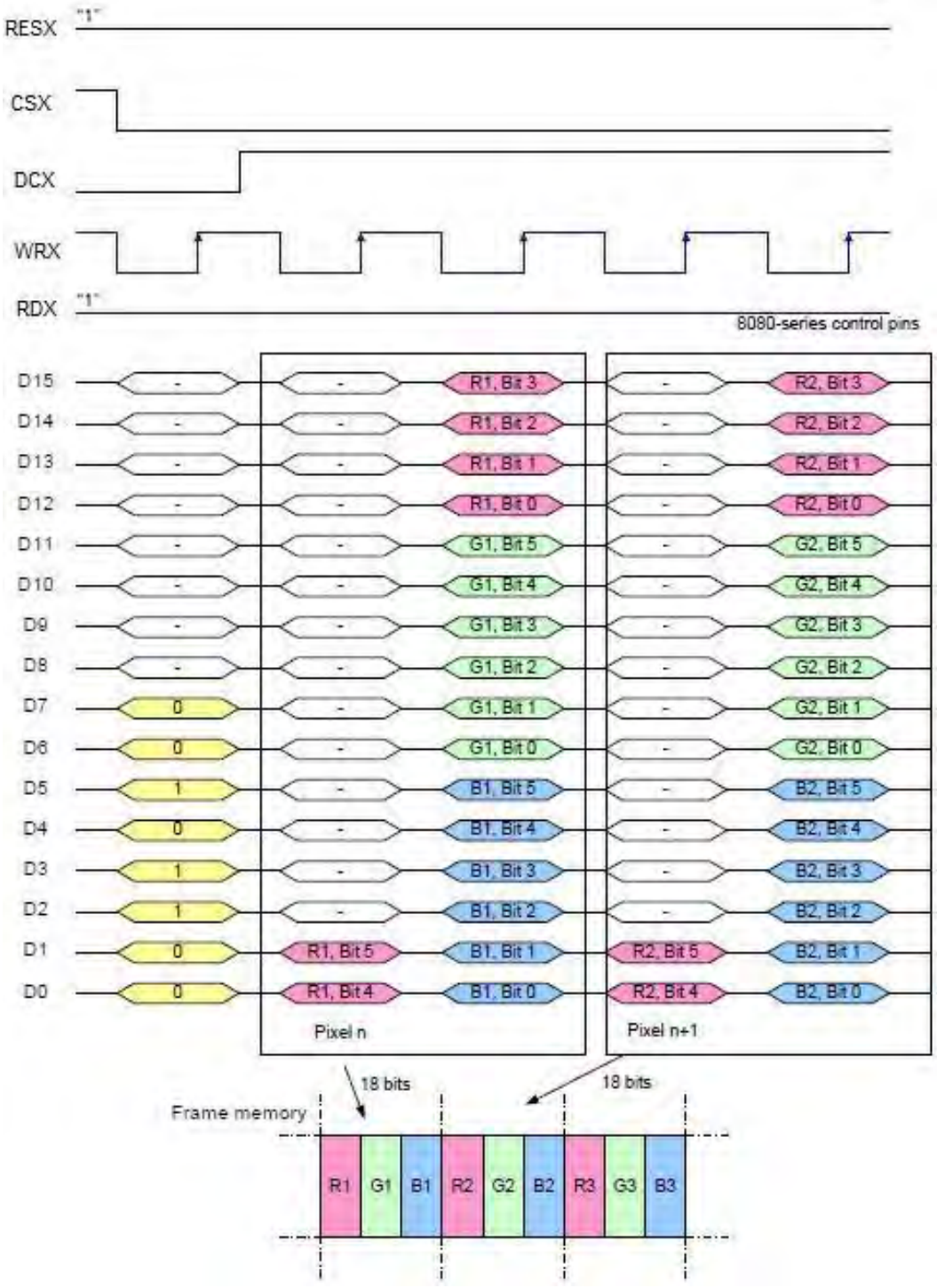


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.3.5 18-bit/pixel (MDT[1:0]="11b")



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'.

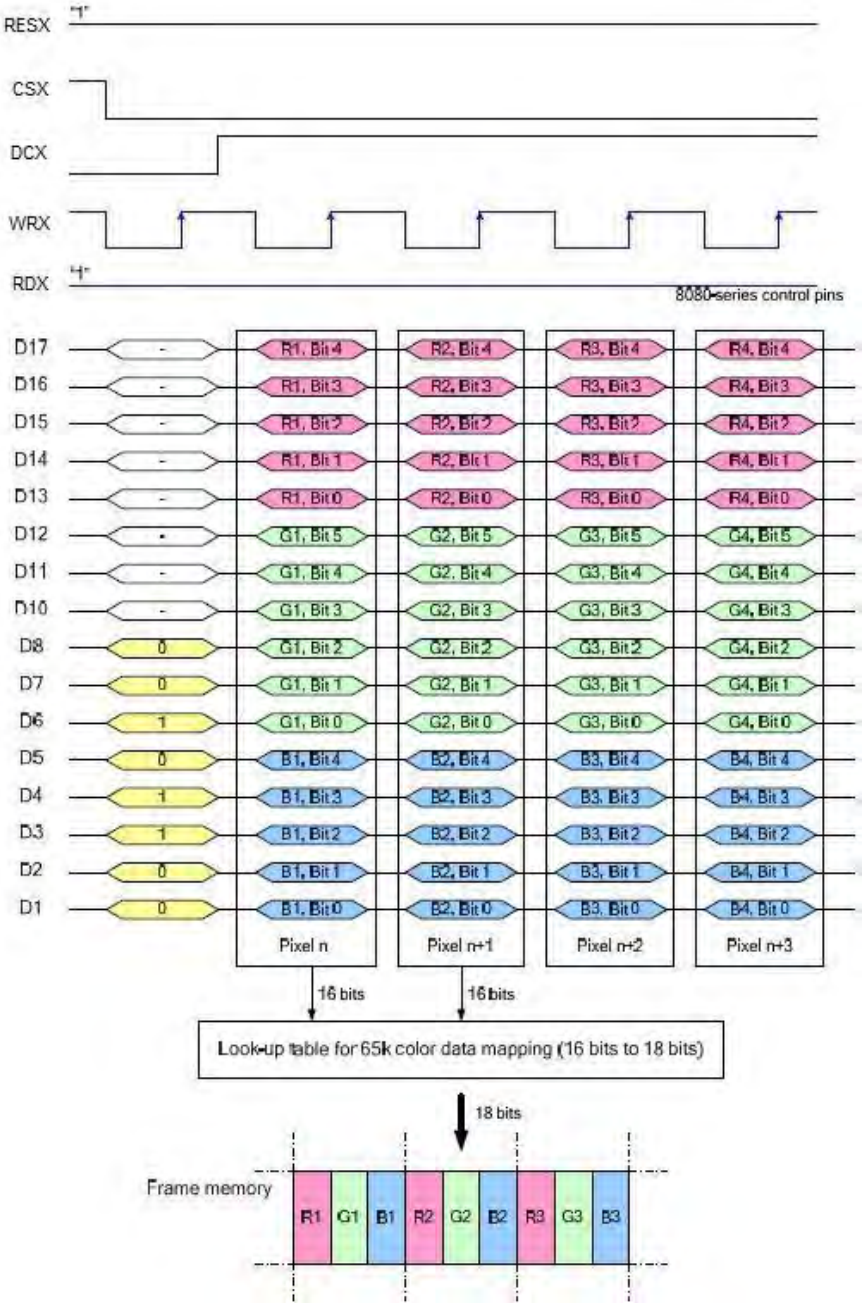
8.3.4.4 8080-Ⅱ series 16-Bit Parallel Interface

The 8080-Ⅱ series 16-bit parallel interface of NV3030B can be used by setting IM[3:0]=”1000b”. Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

8.3.4.4.1 16-bit/pixel

There is 1 pixel (3 sub-pixels) per 1 byte



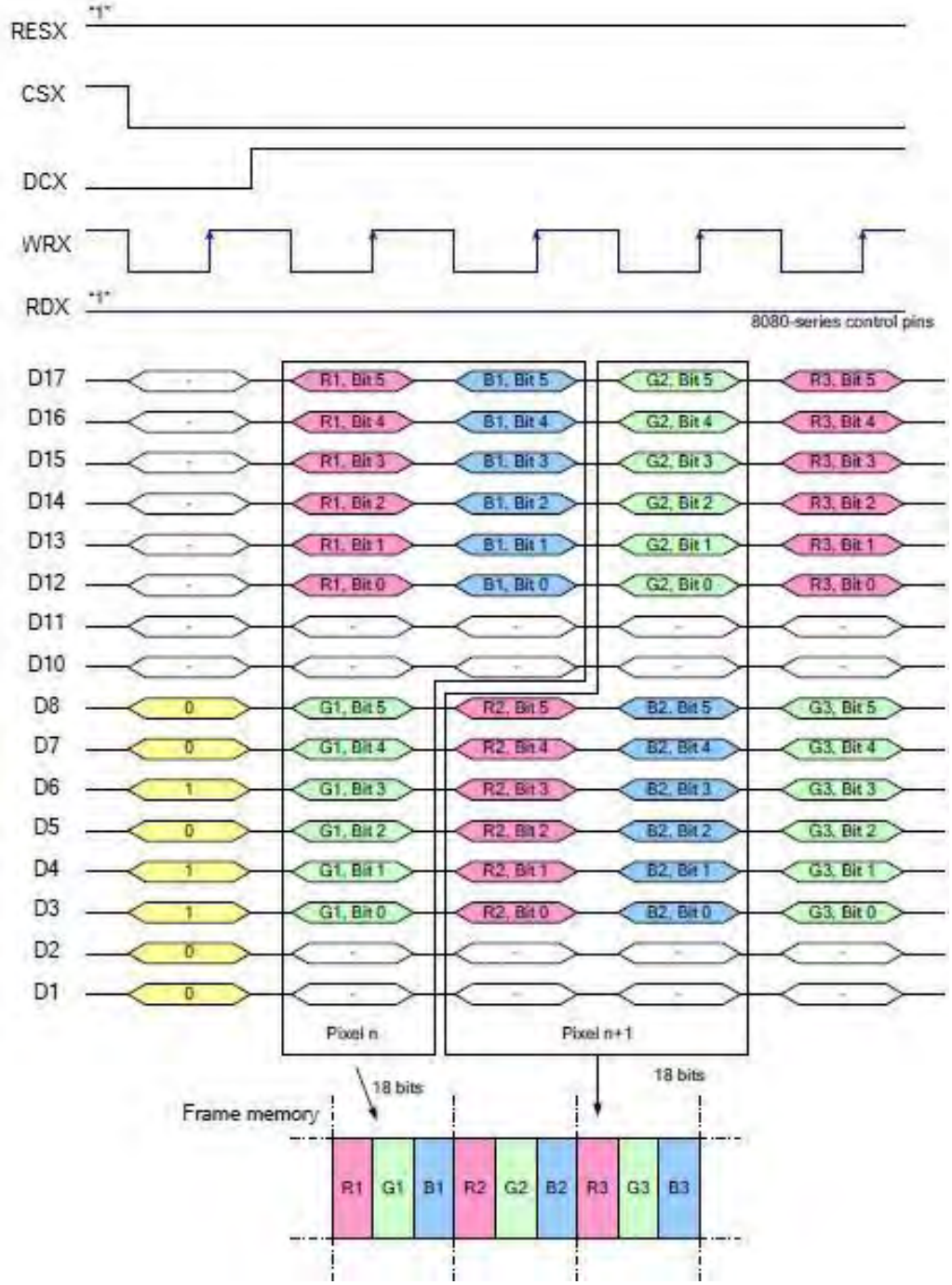
Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D17~D10, D8~D1) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-'= Don't care – Can be set to '0' or '1'.

8.3.4.4.2 18-bit/pixel(MDT[1:0]="00b")

There are 2 pixels (6 sub-pixels) per 3 bytes

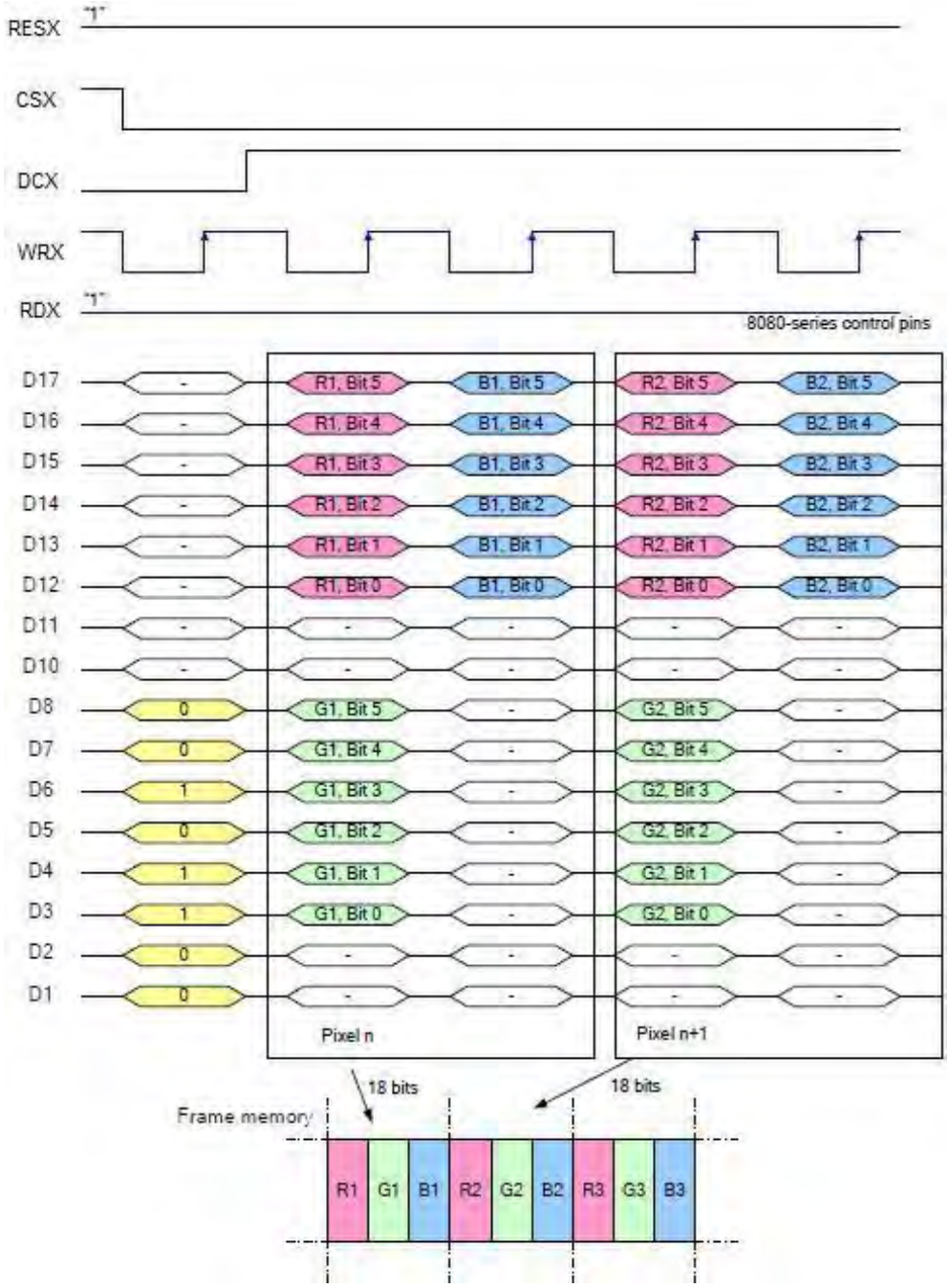


Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'.

8.3.4.4.3 18-bit/pixel(MDT[1:0]=”01b”)

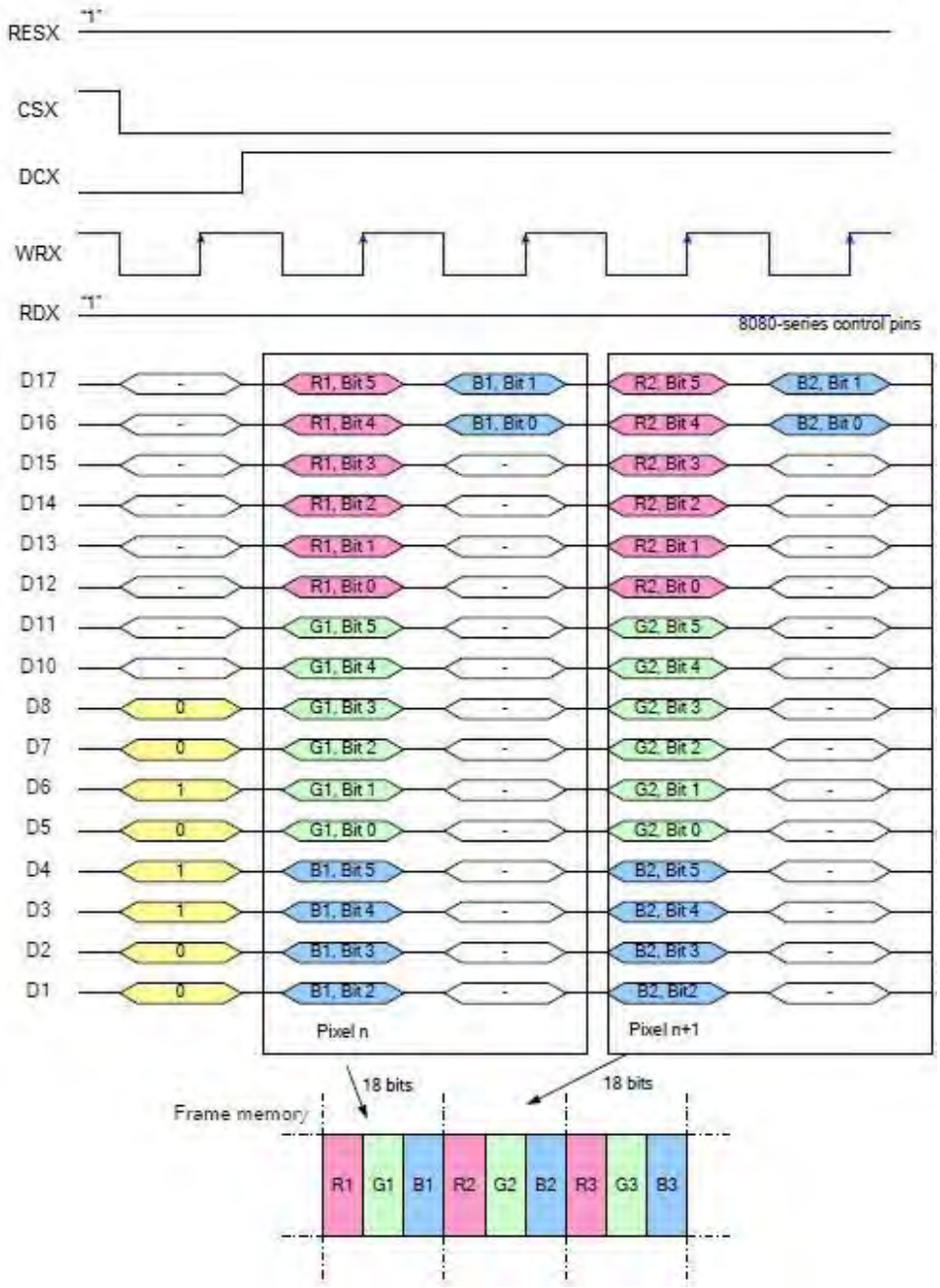


Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.4.4 18-bit/pixel(MDT[1:0]=”10b”)

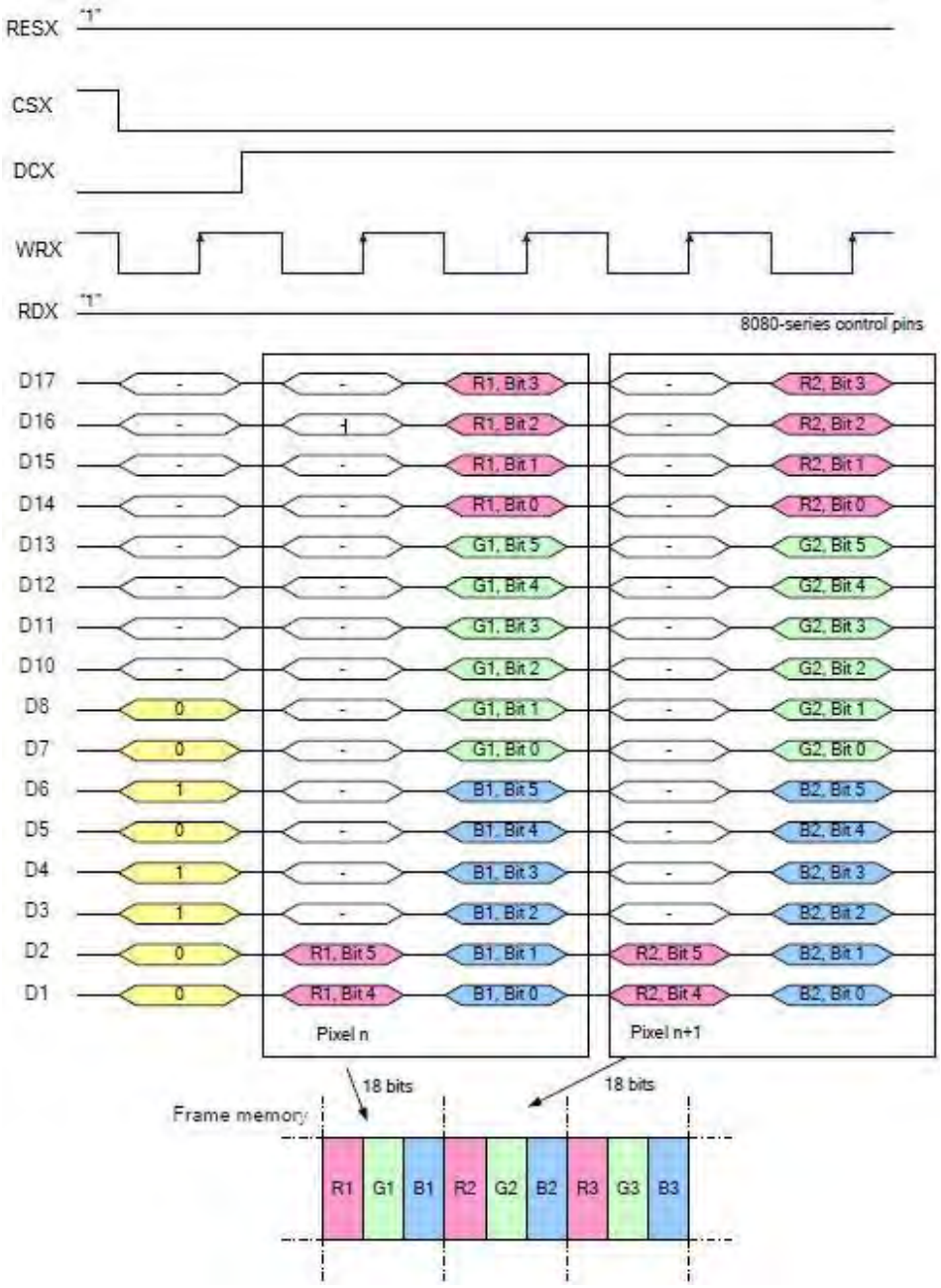


Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.4.5 18-bit/pixel(MDT[1:0]=”11b”)



Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

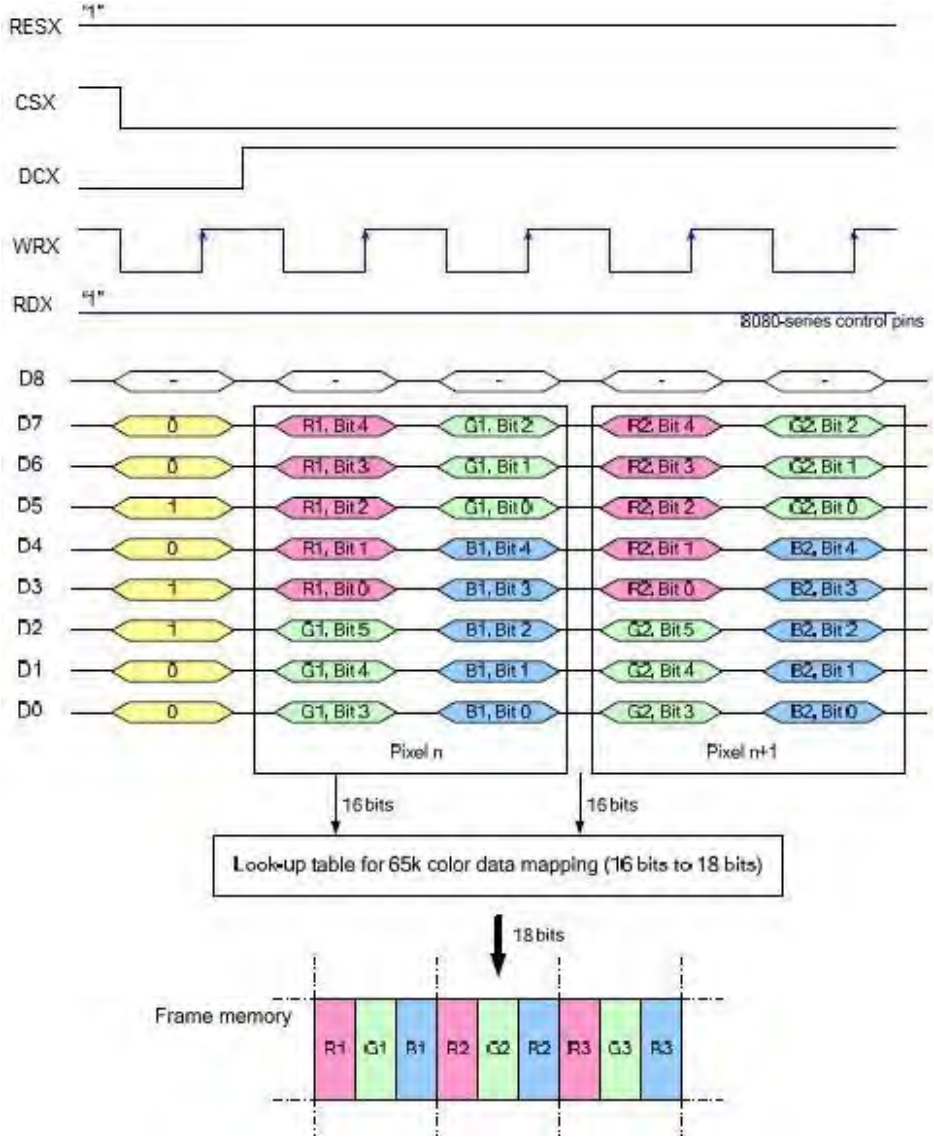
8.3.4.5 8080-Ⅰ series 9-Bit Parallel Interface

The 8080-Ⅰ series 9-bit parallel interface of NV3030B can be used by setting IM[3:0]=”0010b” Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5,6,5-bit input

-262k colors, RGB 6,6,6-bit input

8.3.4.5.1 16-bit/pixel



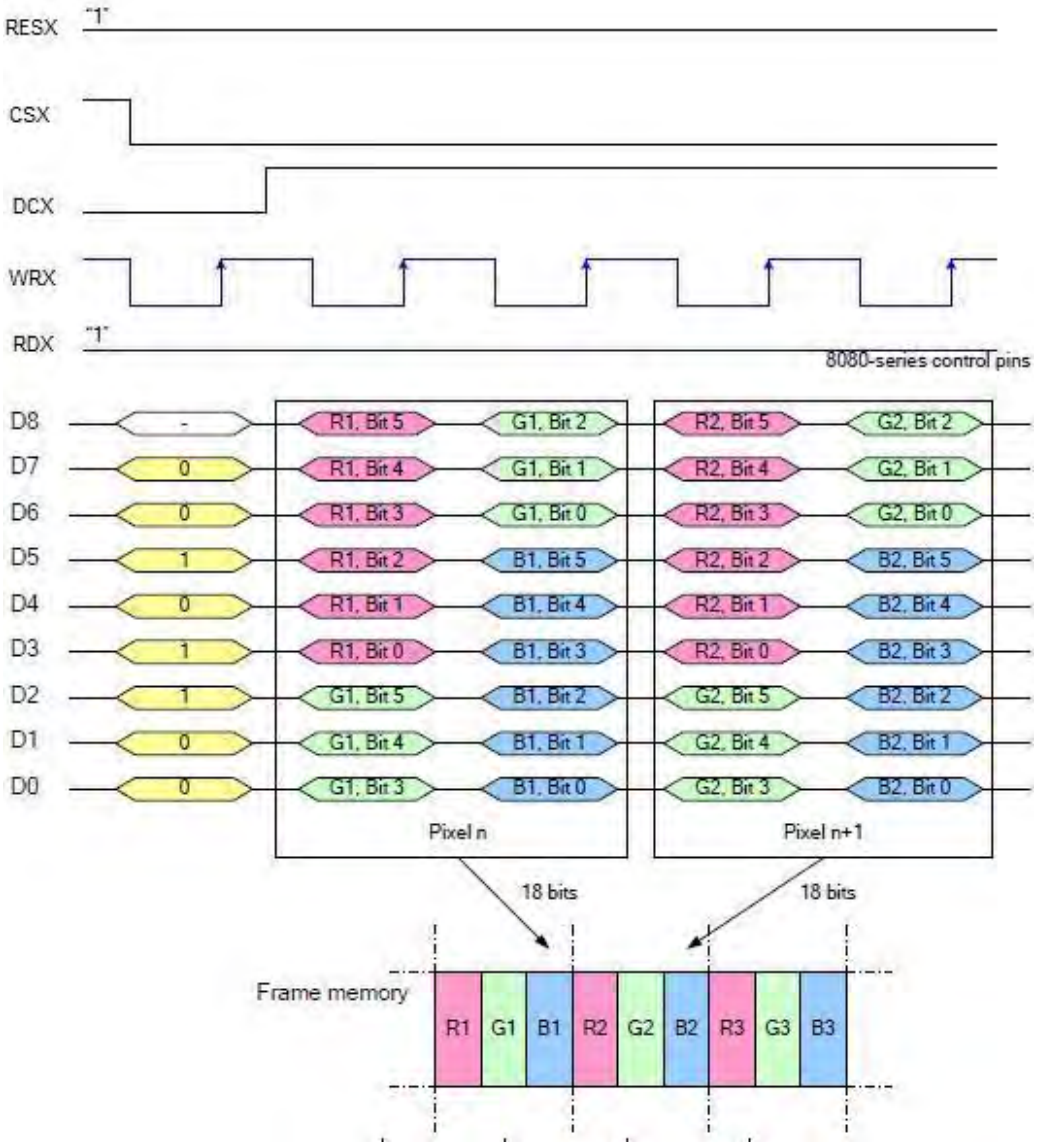
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 4, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.5.2 18-bit/pixel(MDT[1:0]=”00b”)

There is 1 pixel (3 sub-pixels) per 2bytes

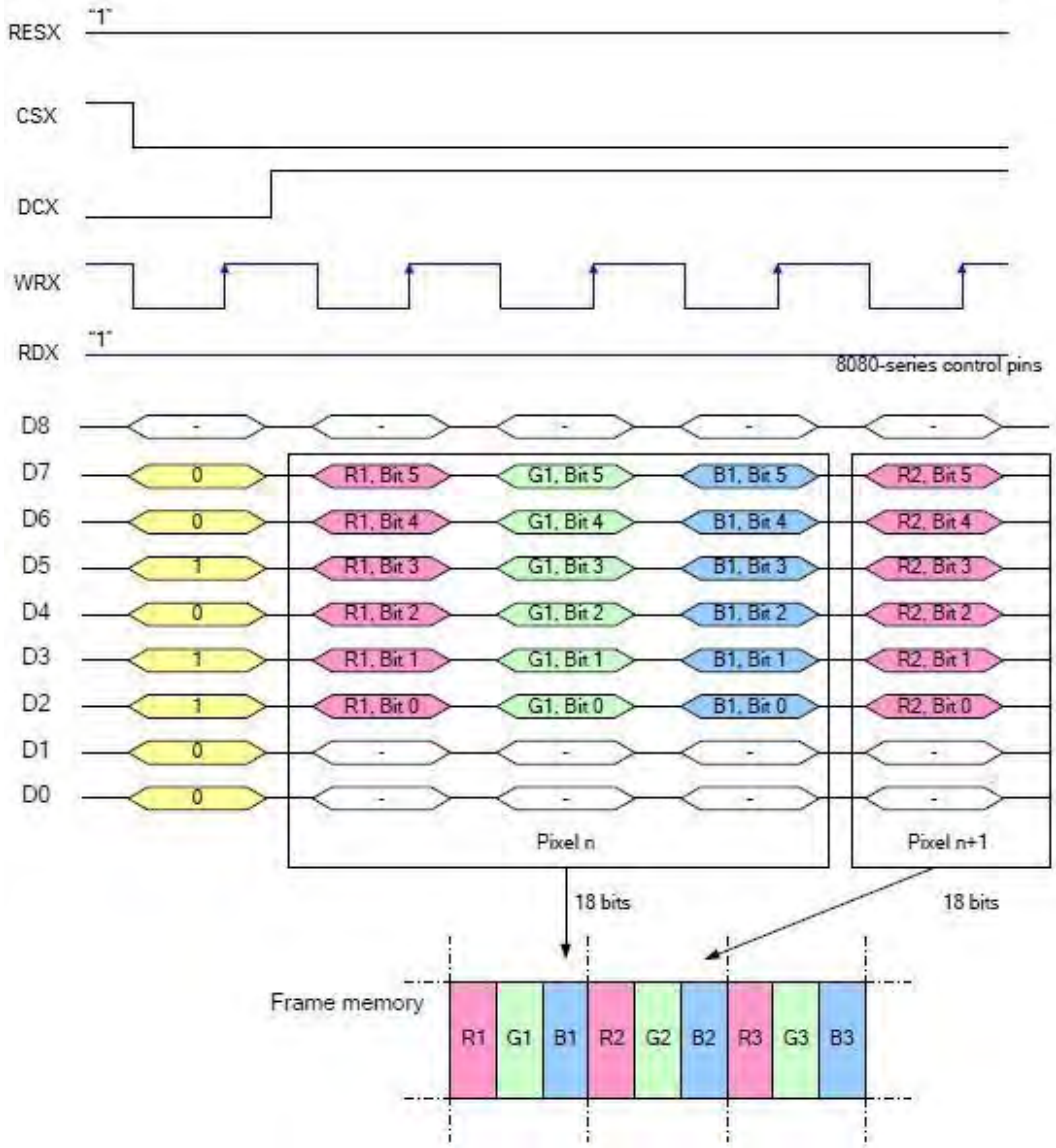


Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Greenand Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.5.3 18-bit/pixel(MDT[1:0]=”01b”)



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

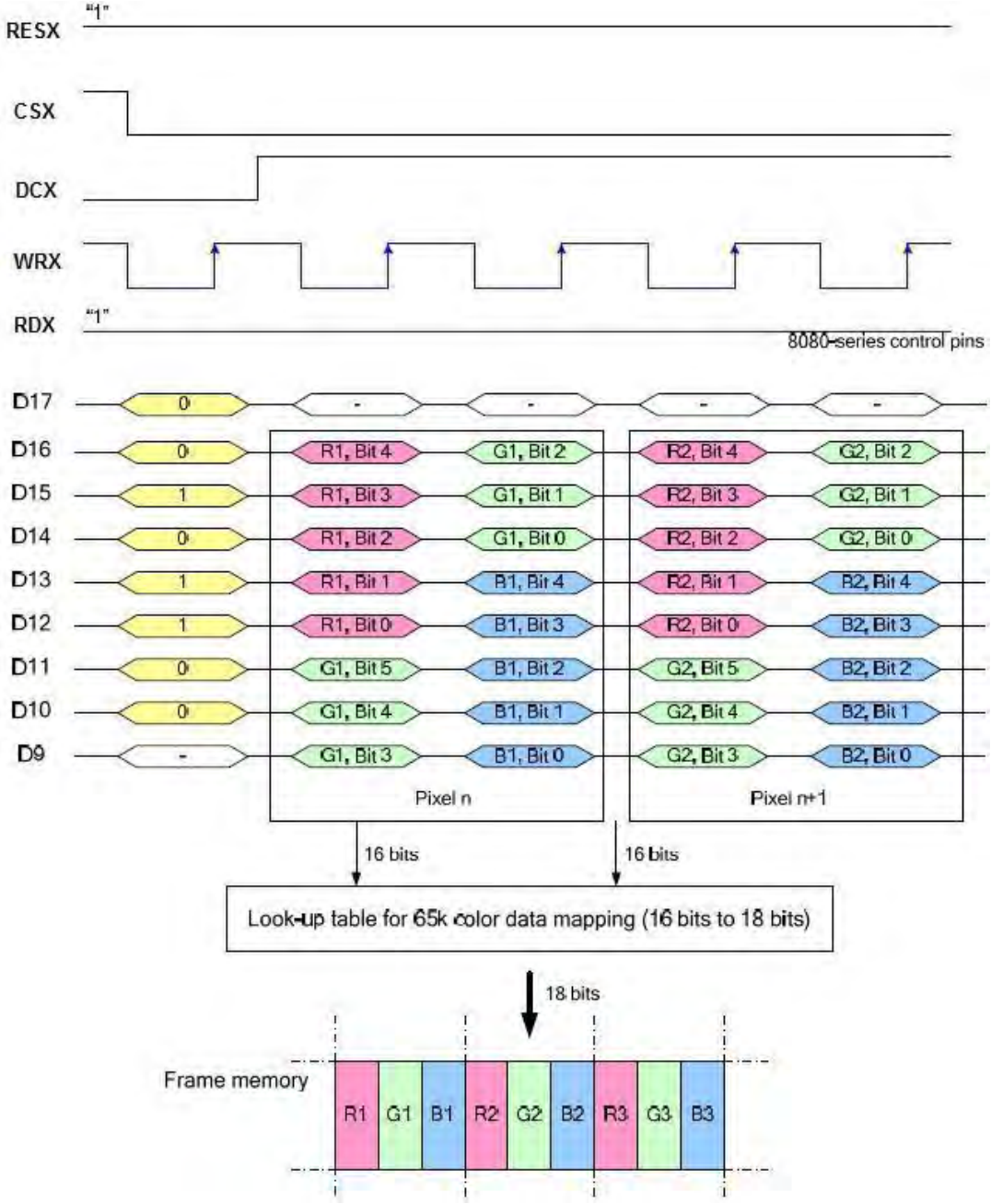
8.3.4.6 8080-Ⅱ series 9-bit Parallel Interface

The 8080-Ⅱ series 9-bit parallel interface of NV3030B can be used by setting IM[3:0]=”1011b”Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5,6,5-bit input

-262k colors, RGB 6,6,6-bit input

8.3.4.6.1 16-bit/pixel



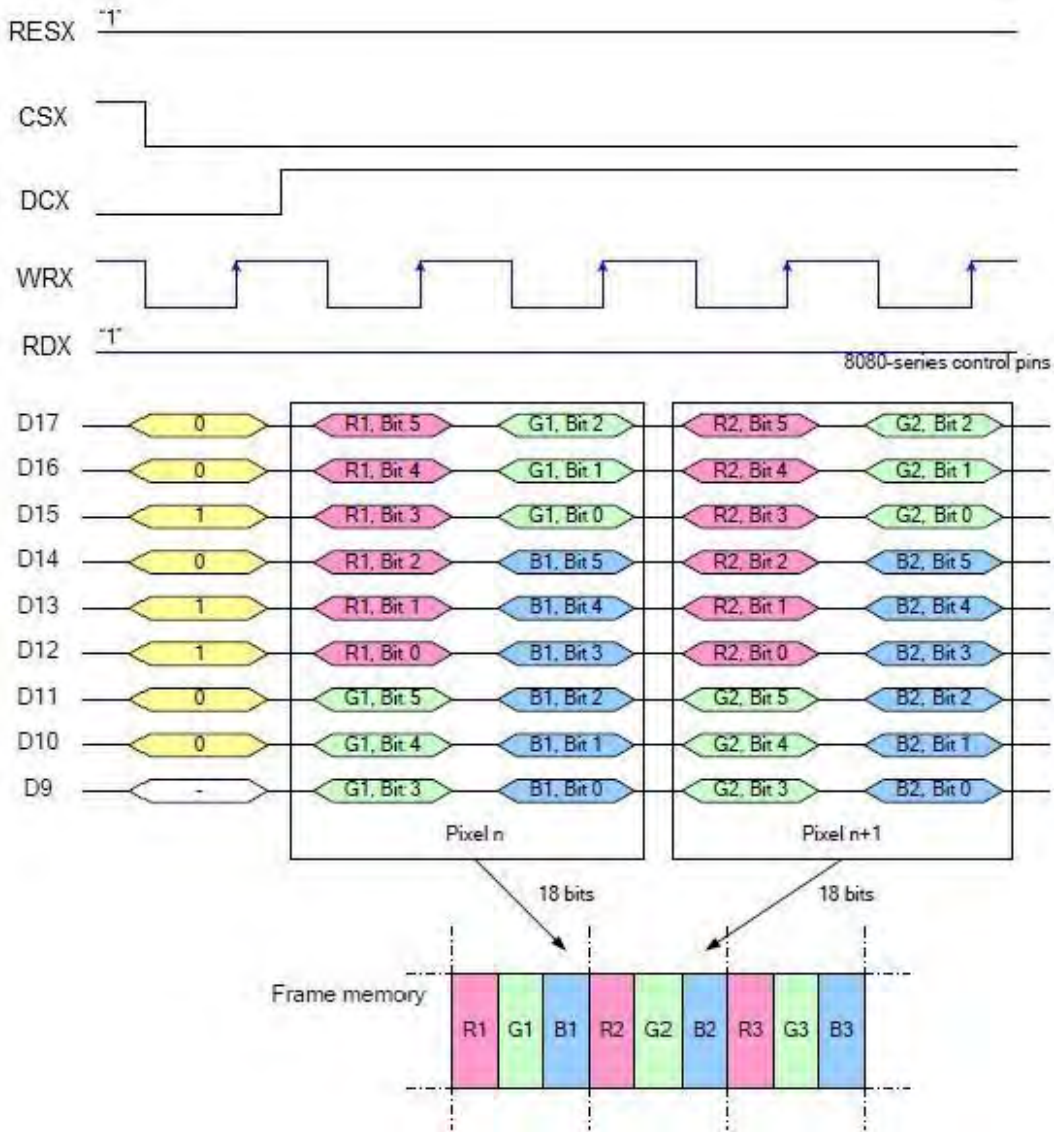
Note 1: The data order is as follows, MSB=D16, LSB=D9 and picture data is MSB=Bit 4, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.6.2 18-bit/pixel(MDT[1:0]=”00b”)

There is 1 pixel (3 sub-pixels) per 2bytes

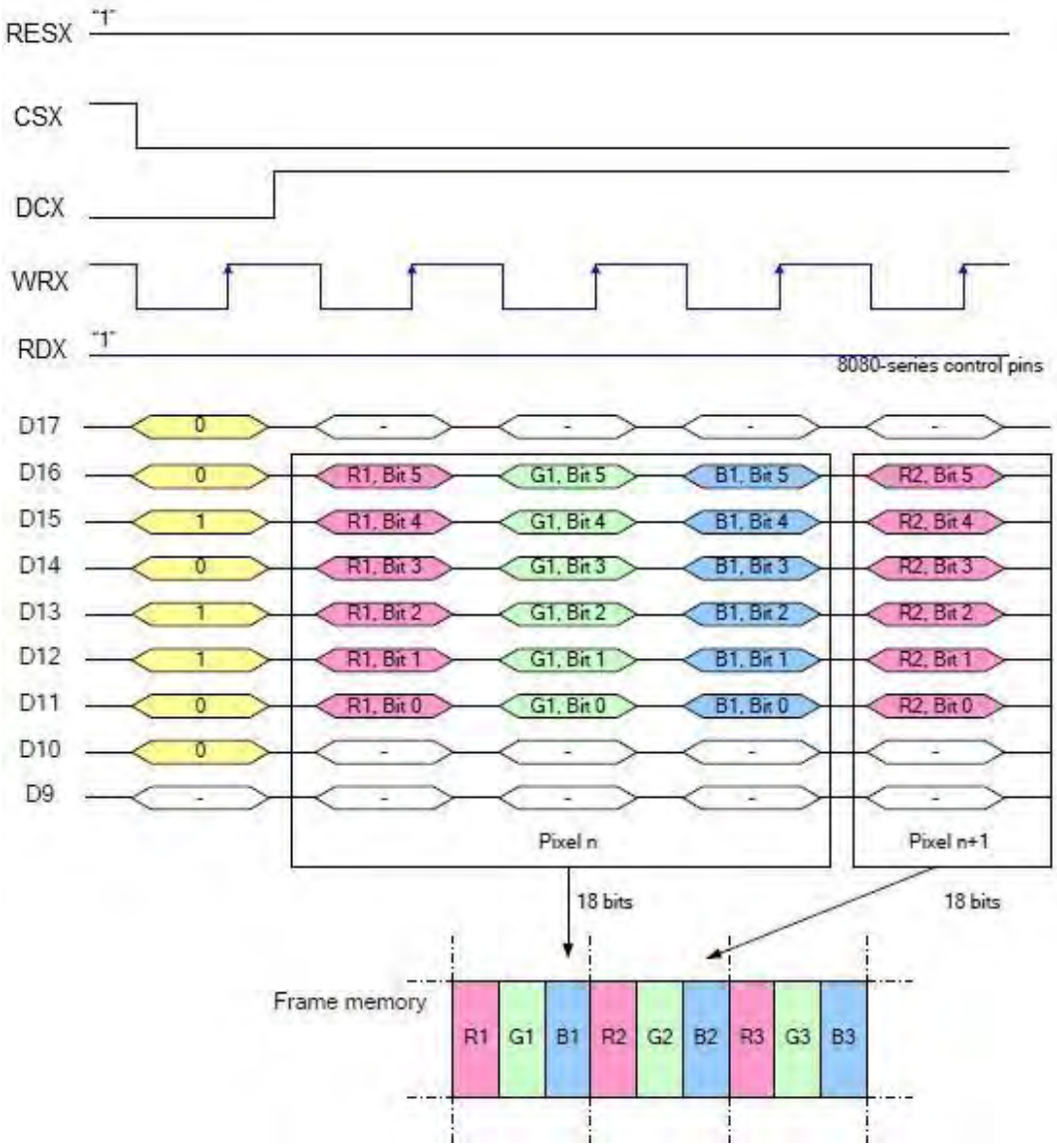


Note 1: The data order is as follows, MSB=D17, LSB=D9 and picture data is MSB=Bit 5, LSB=Bit 0 for Red,Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.6.3 18-bit/pixel(MDT[1:0]=”01b”)



Note 1: The data order is as follows, MSB=D16, LSB=D11 and picture data is MSB=Bit 5, LSB=Bit 0 for Red,Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

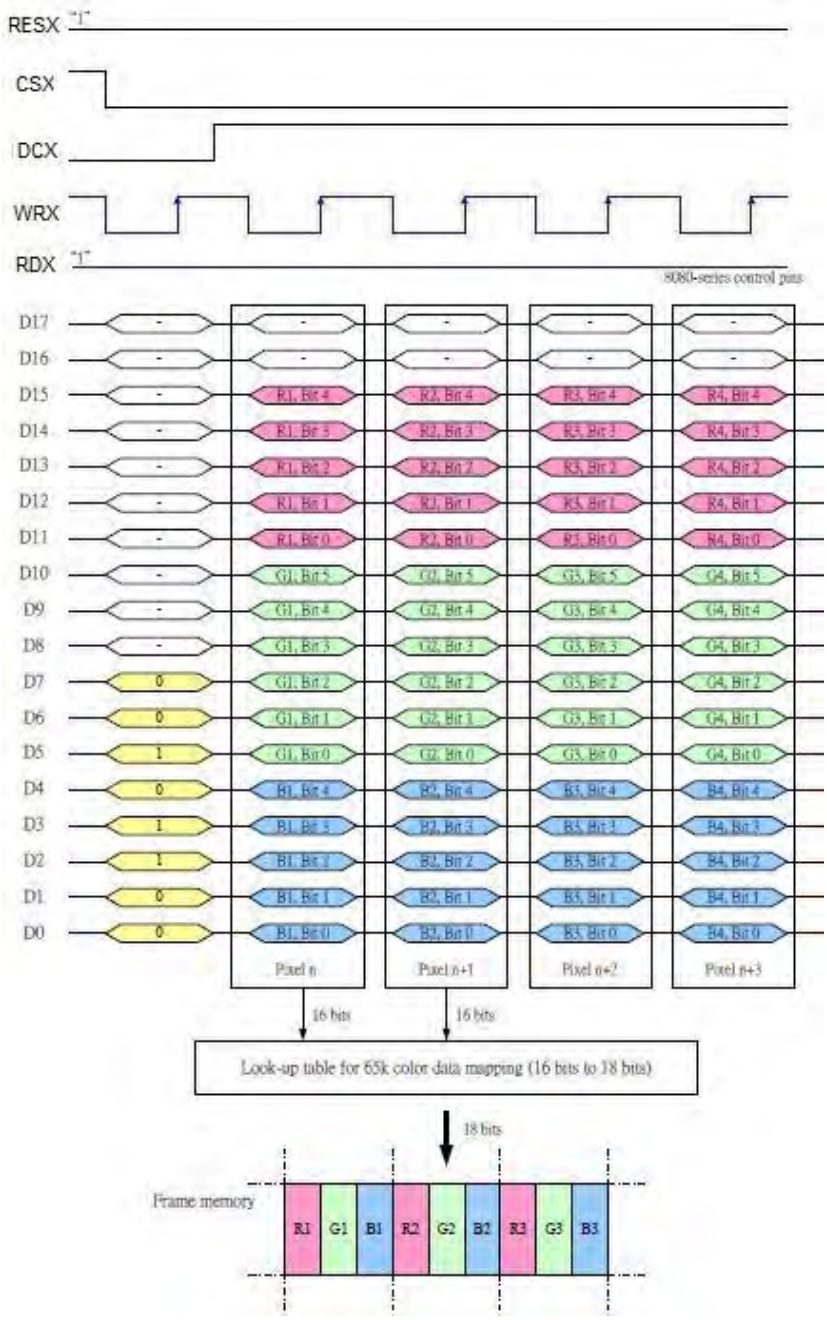
8.3.4.7 8080-Ⅰ series 18-Bit Parallel Interface

The 8080-Ⅰ series 18-bit parallel interface of NV3030B can be used by setting IM[3:0]=”0011b”. Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

8.3.4.7.1 16-bit/pixel

There is one pixel (3 sub-pixels) per byte

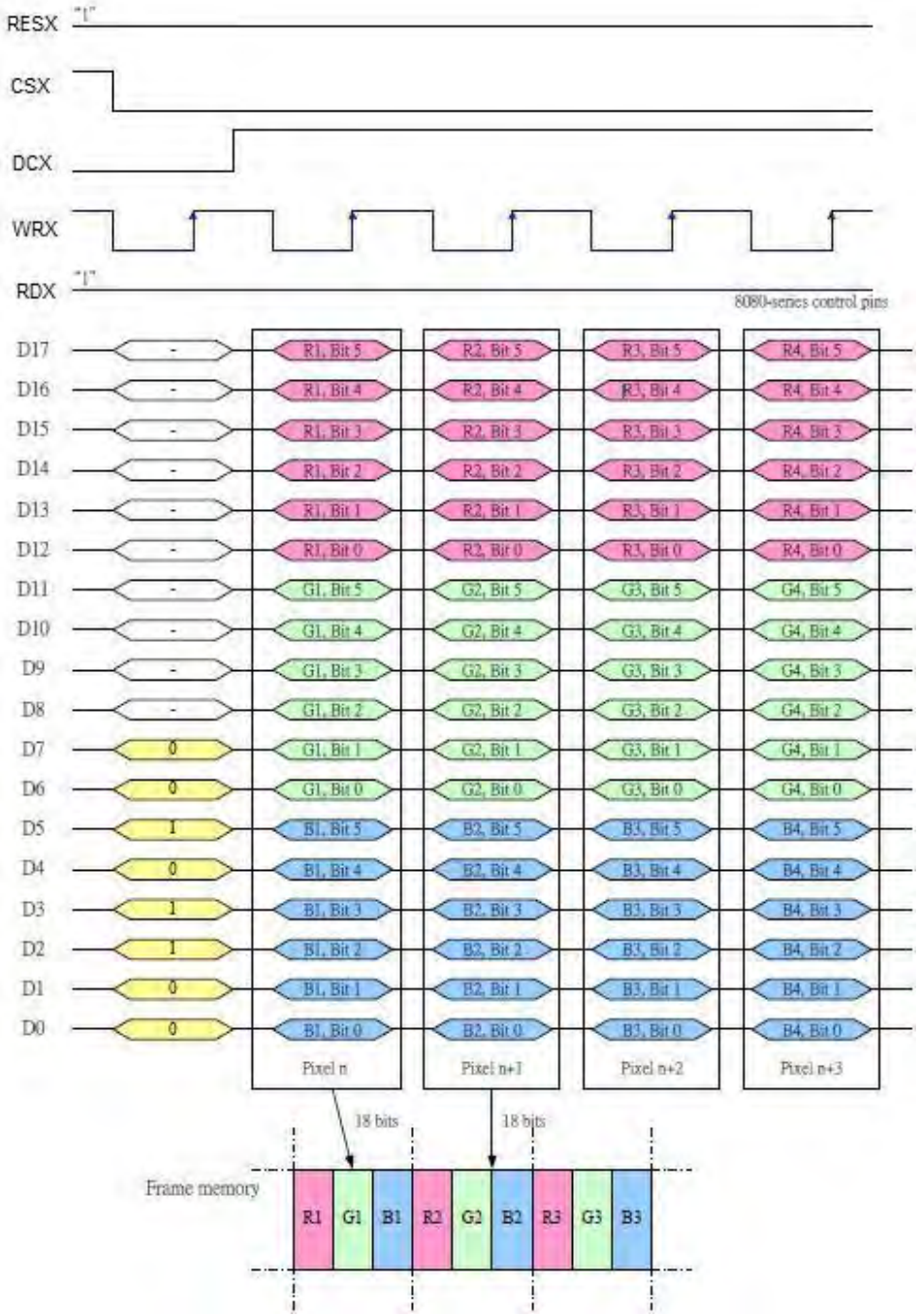


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

8.3.4.7.2 18-bit/pixel

There is 1 pixel (3 sub-pixels) per byte



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read,Green and Blue data.

Note 2: 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

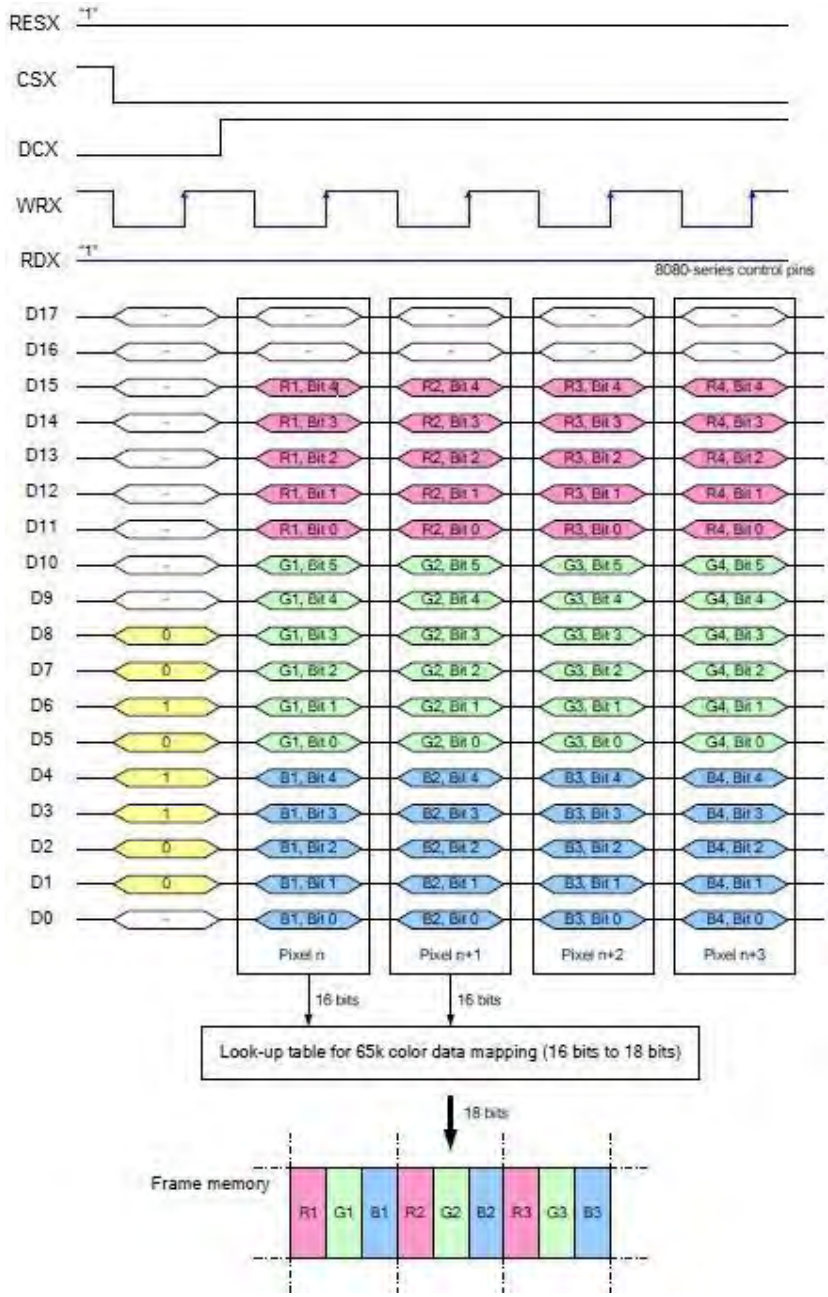
8.3.4.8 8080-Ⅱ series 18-Bit Parallel Interface

The 8080-Ⅱ series 18-bit parallel interface of NV3030B can be used by setting IM[3:0]=”1010b”. Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.
-

8.3.4.8.1 16-bit/pixel

There is one pixel (3 sub-pixels) per byte

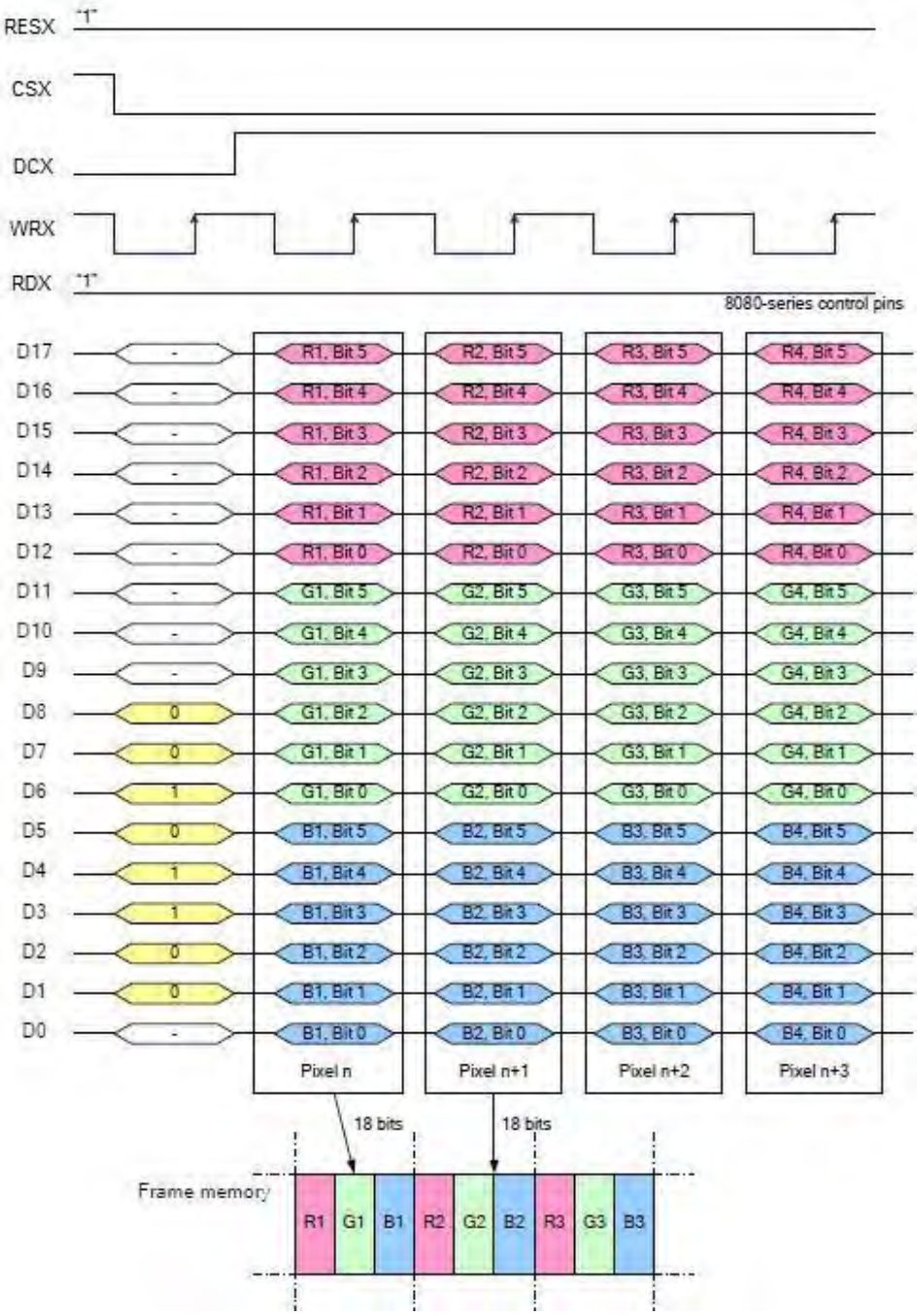


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green,and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

8.3.4.8.2 18-bit/pixel

There is 1 pixel (3 sub-pixels) per byte

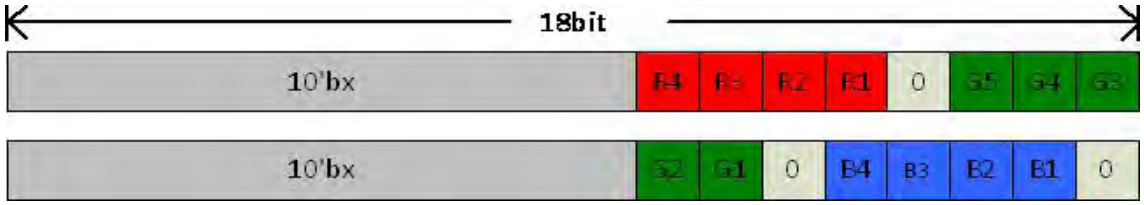


Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

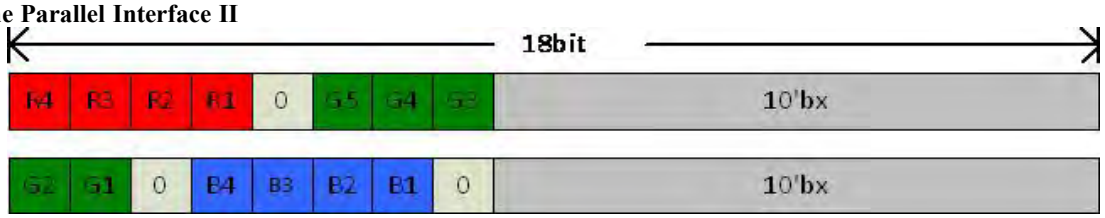
Note 2: 1-times transfer (D17 to D0) is used to transmit 1 pixel data with the 18-bit color depth information.

8.3.4.9 Read Memory Data Color Coding

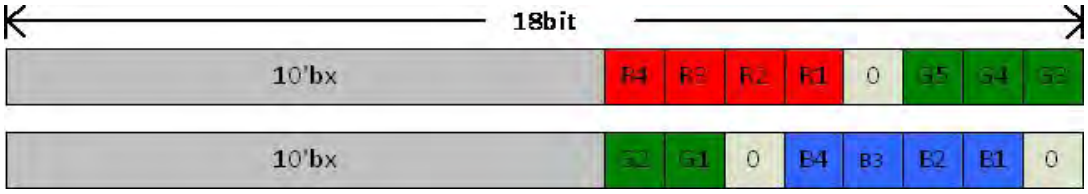
8.3.4.9.1 8 Data Line Parallel Interface I



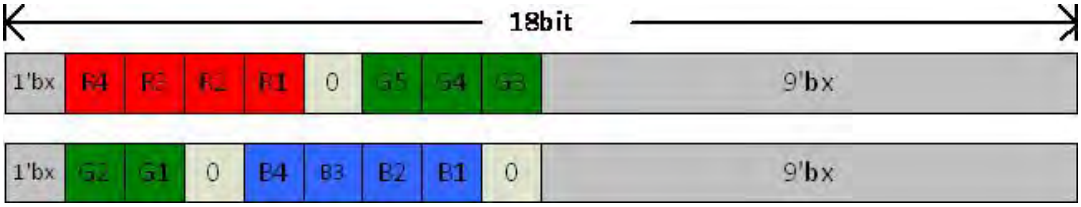
8 Data Line Parallel Interface II



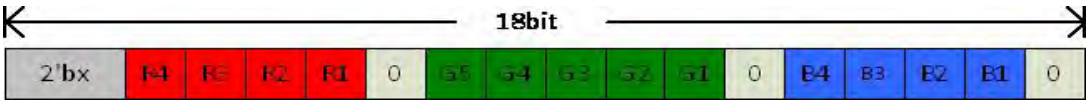
8.3.4.9.2 9 Data Line Parallel Interface I



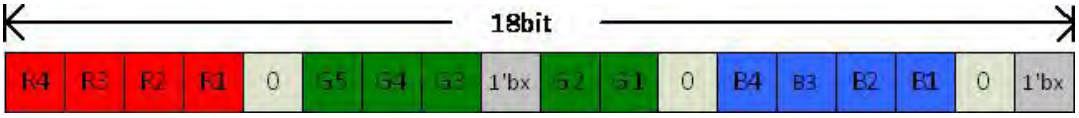
9 Data Line Parallel Interface II



8.3.4.9.3 16 Data Line Parallel Interface I



16 Data Line Parallel Interface II



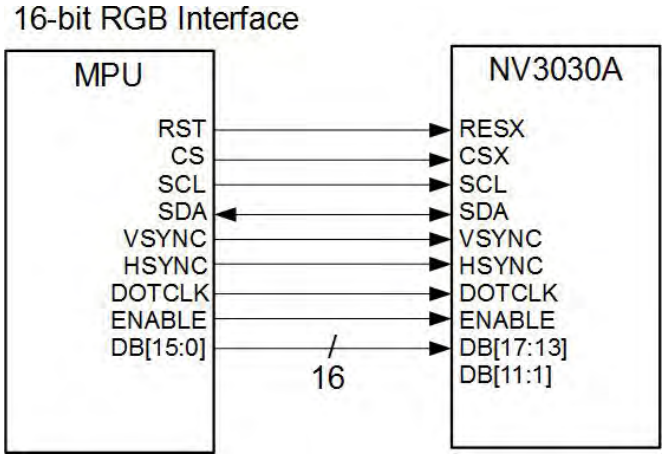
8.3.4.9.4 18 Data Line Parallel Interface I & II

Note:‘bx’means these bits are not usable.

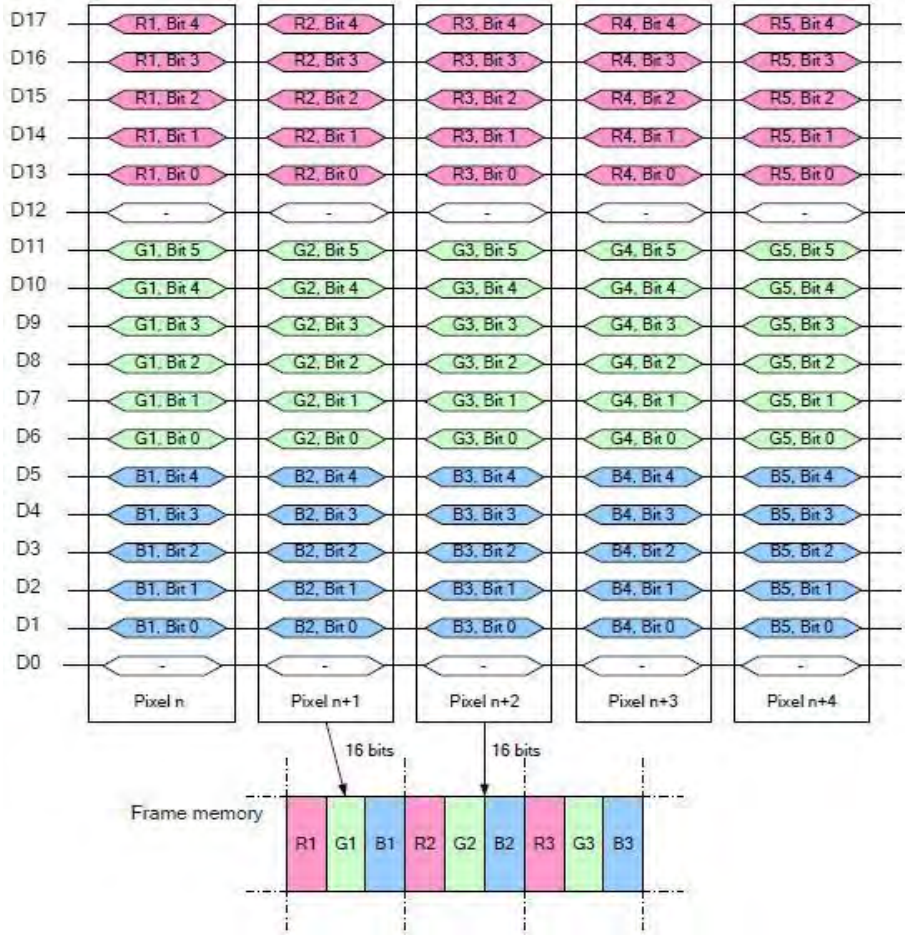
8.3.5 RGB Interface

NV3030B supports two kinds of RGB interface, DE mode and SYNC mode, and 16bit/18bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0] pins can be used; when SYNC mode is selected and the VSYNC, HSYNC, DOTCLK, DB[17:0] pins can be used. When using RGB interface, only serial interface can be selected.

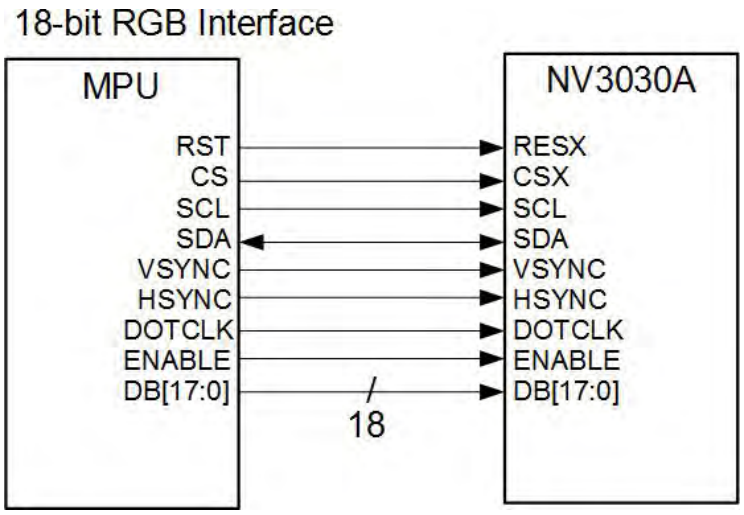
8.3.5.1 16-bit RGB interface



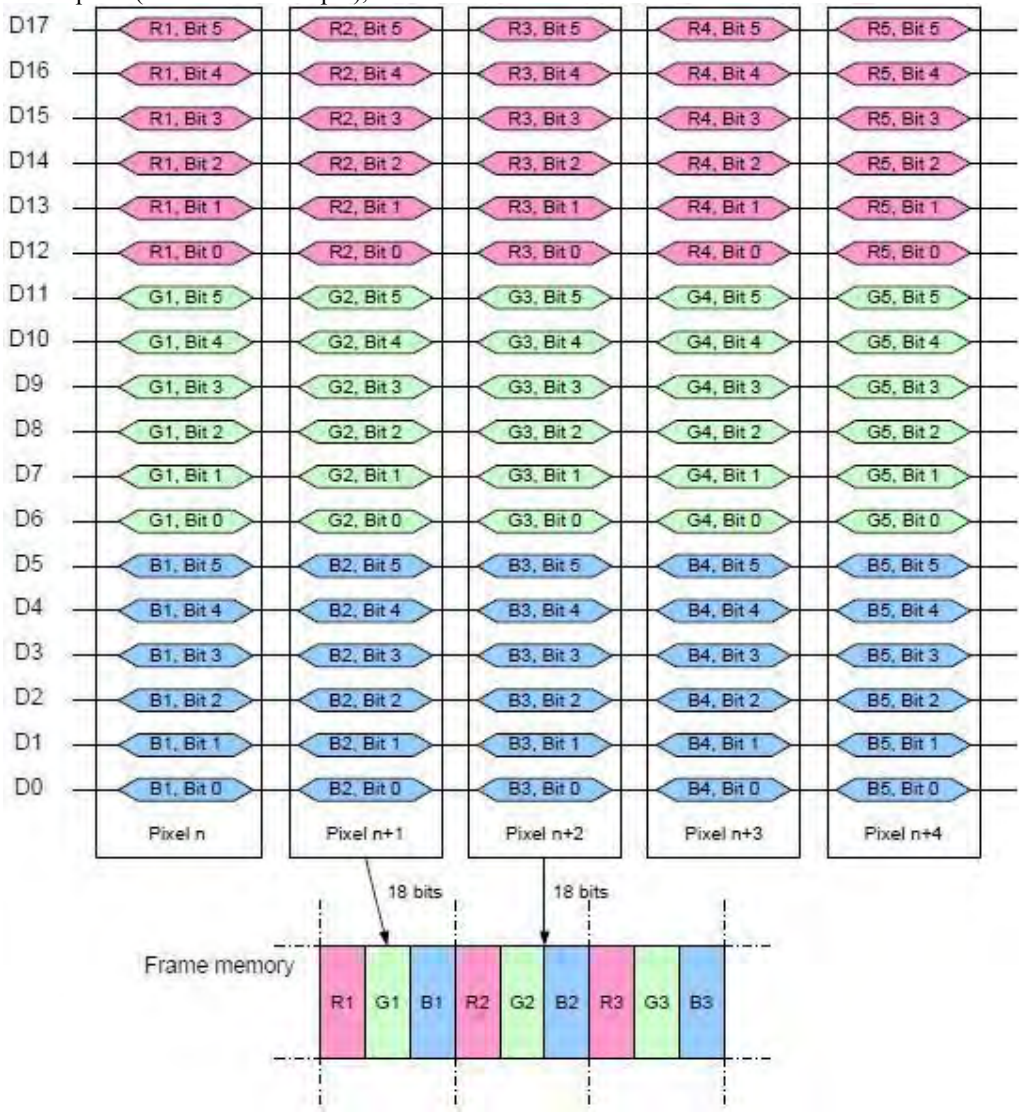
Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



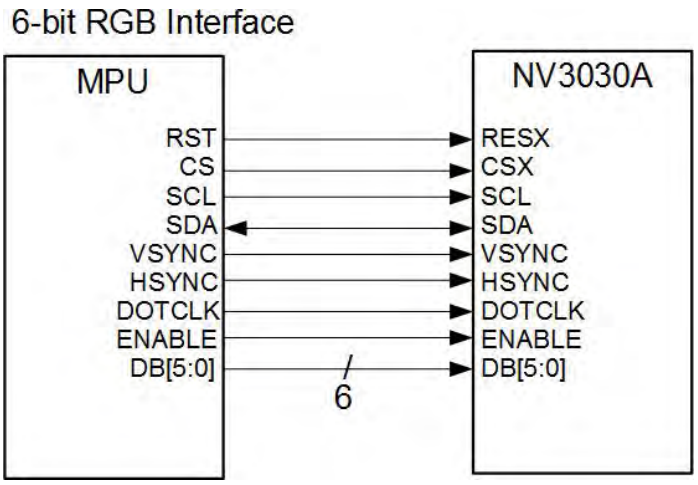
8.3.5.2 18-bit RGB interface



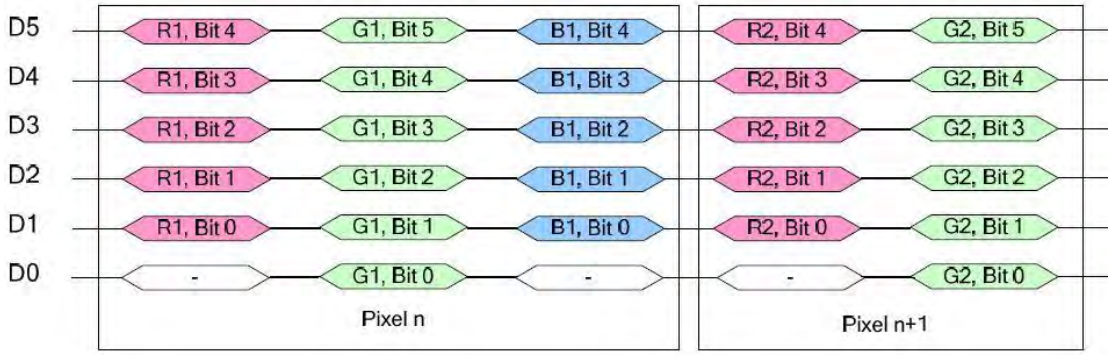
Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors

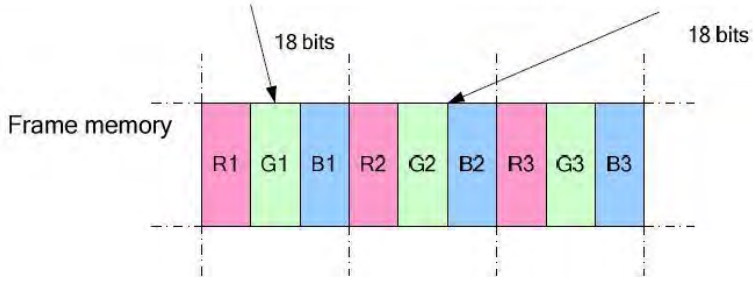


8.3.5.3 6-bit RGB interface

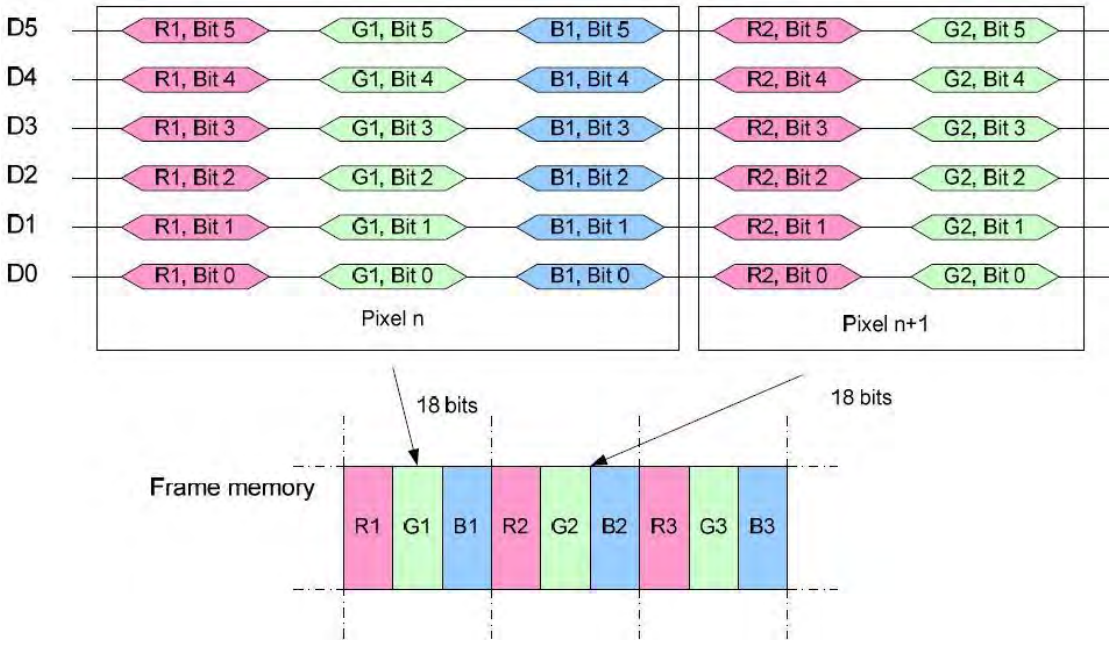


8.3.5.3.1 16-bit/pixel





8.3.5.3.2 18-bit/pixel

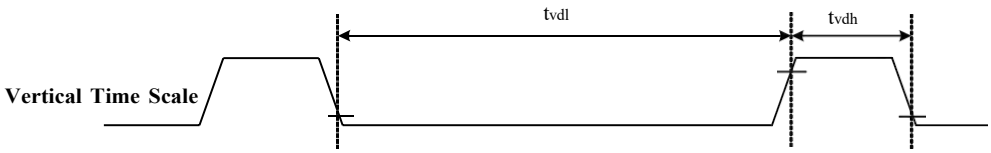


8.4 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

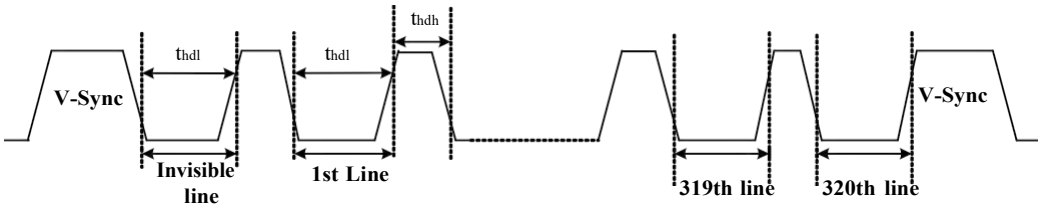
8.4.1 Tearing Effect line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync Information only:

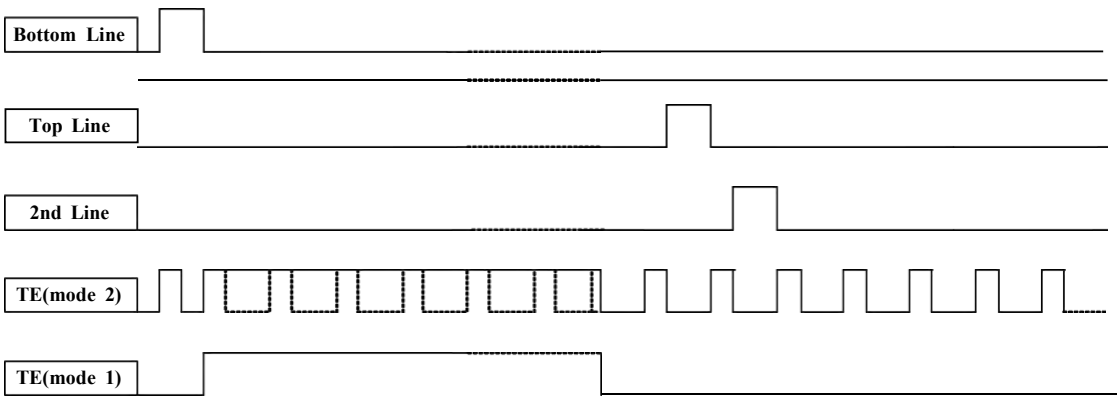


tvdh = The LCD display is not updated from the Frame Memory;
tvdl = The LCD display is updated from the Frame Memory(except Invisible Line – see below).

Mode 2, the Tearing Effect Output signal consists of V-Sync and H-Sync Information, there is one V-sync and 320 H- sync pulses per field:



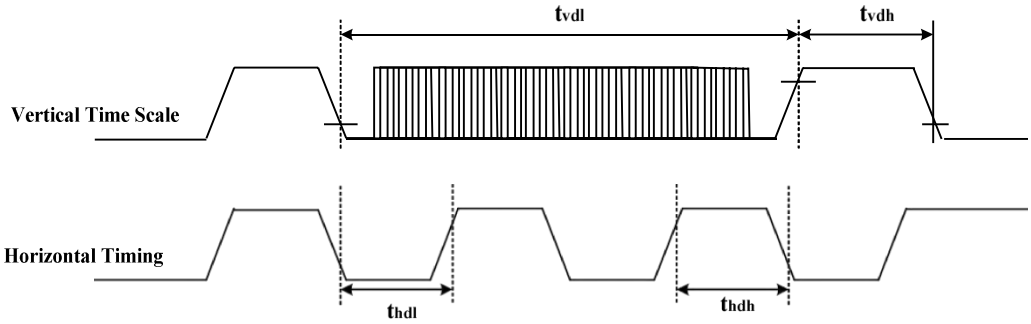
thdh = The LCD display is not updated from the Frame Memory;
thdl = The LCD display is updated from the Frame Memory(except Invisible Line – see below).



Note: During sleep in Mode,the tearing effect Output pin is active low.

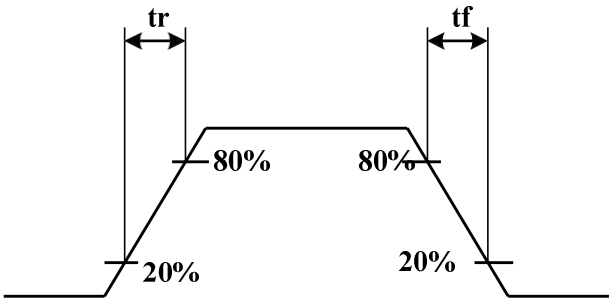
8.4.2 Tearing Effect line Timings

The Tearing Effect signal is described below:



Symbol	Parameter	Min.	Max	Unit
tvdl	Vertical Timing Low Duration	13	17	ms
tvdh	Vertical Timing High Duration	1000	1300	us
thdl	Horizontal Timing Low Duration	20	-	us
thdh	Horizontal Timing High Duration	10	500	us

Notes:
The timings in this table apply when MADCTL B4=0 and B4=1.
The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns.



The tearing effect output line is fed back to the MPU and should be used to avoid tearing effect.

8.5 Power On/Off Sequence

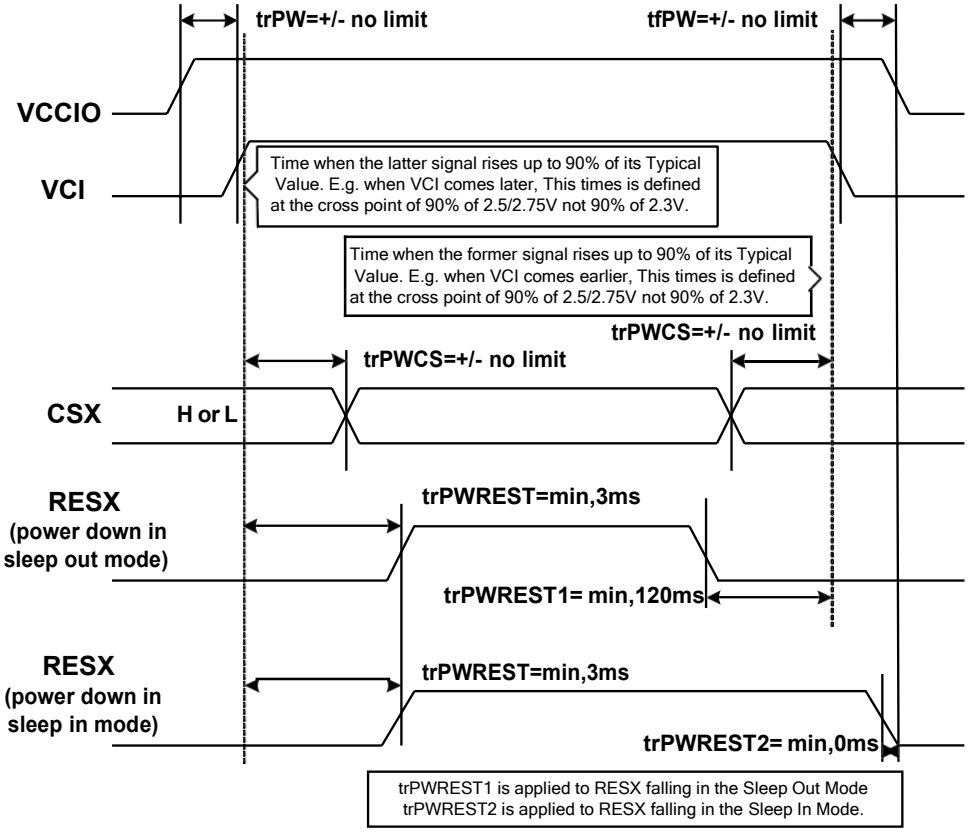
8.5.1 Power On/Off Sequence

VDDI and VCI can be applied in any order.
VCI and VDDI can be powered down in any order.
During power off, if LCD is in the Sleep Out Mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Notes:
1. There will be no damage to the display module if the above power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power off sequence.
4. If RESX line is not held stable by MPU during Power On Sequence ,it will be necessary to apply a Hardware Reset (RESX) after MPU Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

8.5.1.1 Case 1 – RESX line is held high or Unstable by MPU at Power On

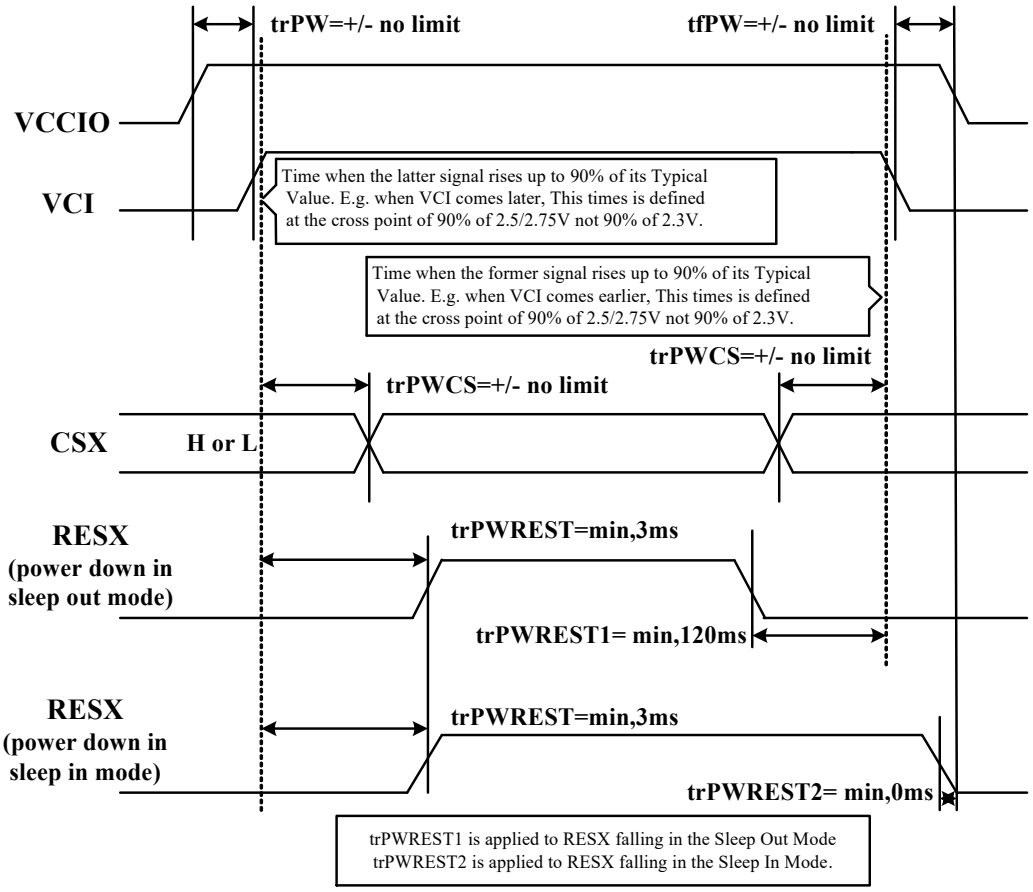
If RESX line is held High or unstable by the MPU during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timing here in show cross point at 50% of signal/power level.

8.5.1.2 Case 2 – RESX line is held low by MPU at Power On

If RESX line is held Low (and stable) by the MPU during Power On, then the RESX must be held low for minimum 3msec after both VCI and VDDI have been applied.



Note: Unless otherwise specilied, timing here in show cross point at 50% of signal/power level.

8.6 Power Level Definition

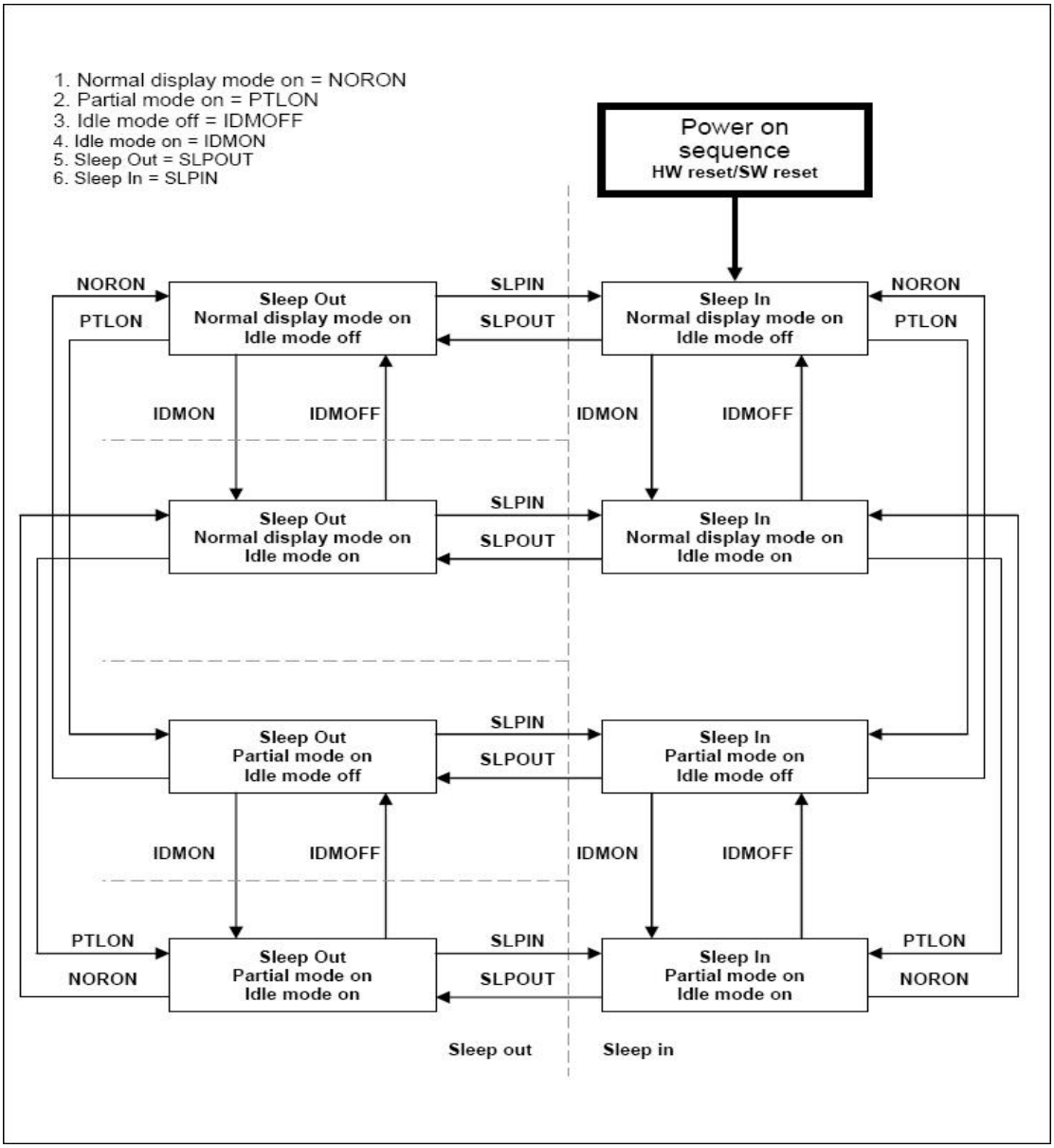
8.6.1 Power levels

6 level modes are defined they are in order of Maximum power consumption to Minimum power consumption.

1. Normal Mode On (full display), Idle Mode Off, Sleep Out
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
   In this mode, part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out
   In this mode, part of the display is used but with 8 colors
5. Sleep In Mode
   In this mode, the DC/DC converter, Internal oscillator and panel driver circuit are stopped. Only the interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and VDDI are removed

Note:
Transition between modes 1-5 is controllable by commands. Mode 6 is entered only when both Power supplies are removed.

8.6.2 Power flow chart



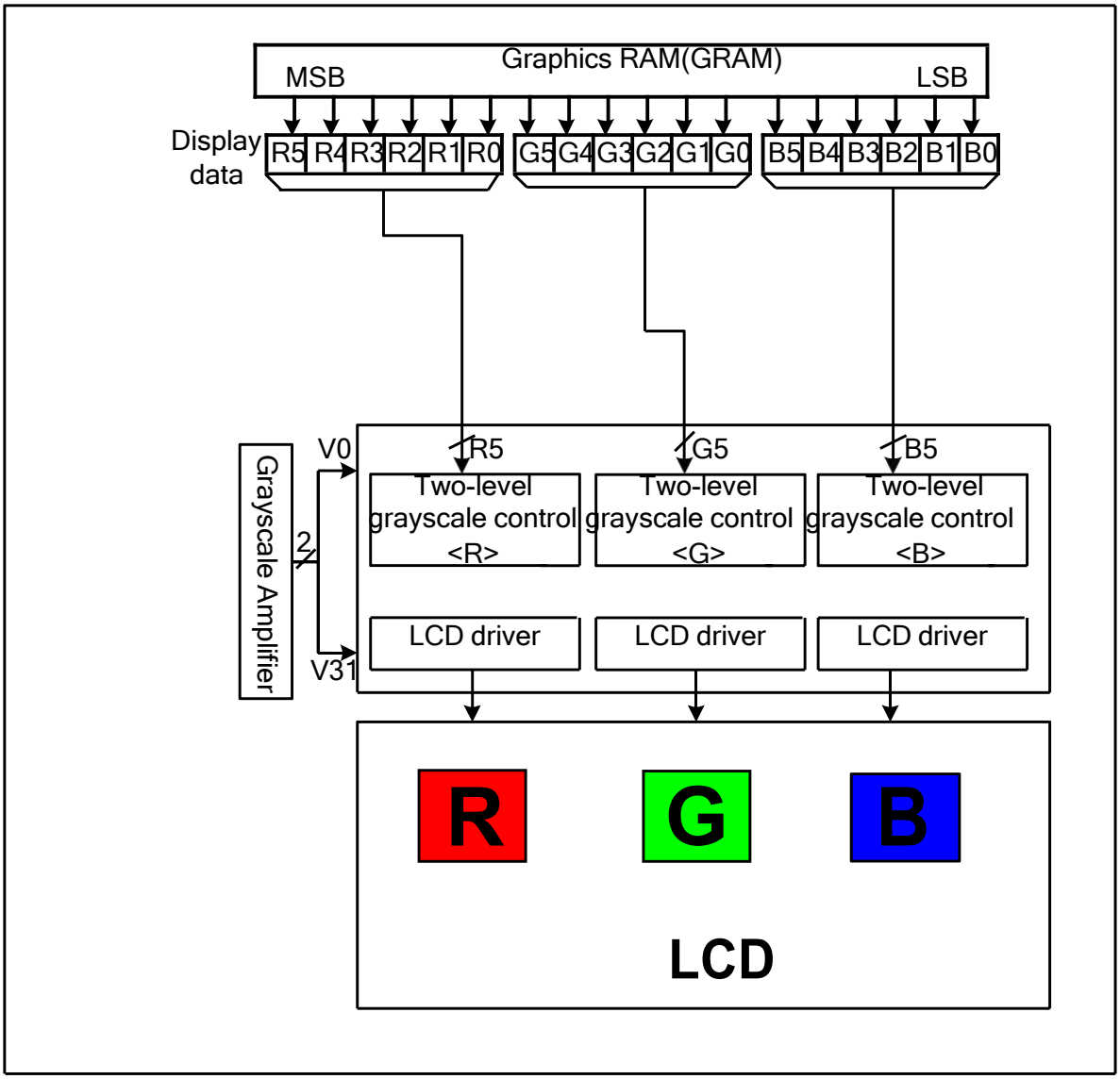
Notes:

1. There is not any abnormal visual effect when there is changing from one power mode to anther power mode.
2. There is not any limitation, which is not specified by Nokia, when there is changing from one power mode to another power mode.

8.7 8-color Display Mode

The NV3030B has a function to display in eight colors. In 8-color mode, the available grayscales are only V0 andV31, and the power supplies for other grayscales (V1 to V30) are cut off to reduce power consumption.

The γ-correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.
In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.



8.8 Gamma Correction

The NV3030B incorporates gamma adjustment function for the 32,768-color display (32 grayscale for each R, G and B color). Gamma adjustment operation is implemented by deciding the 15 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

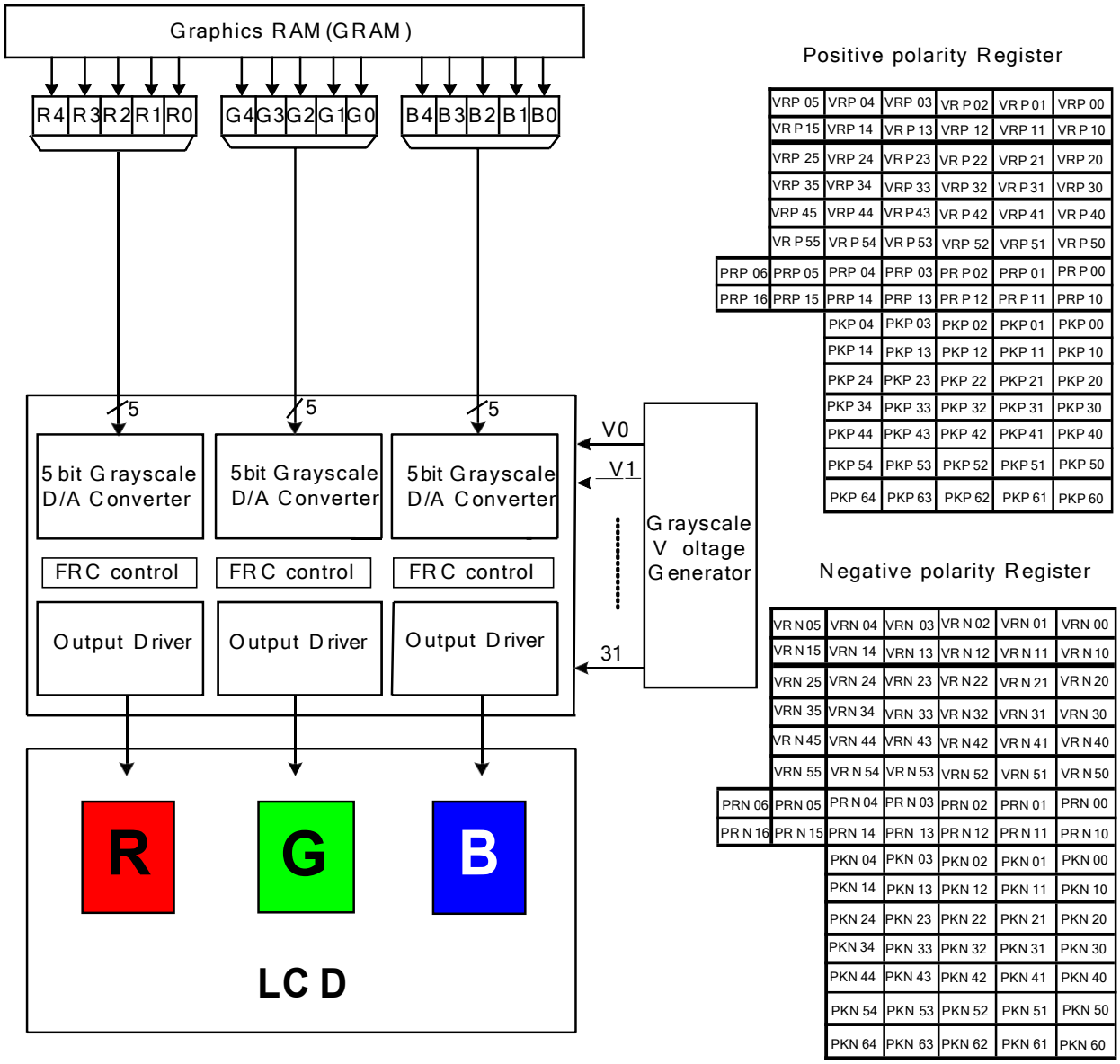


Figure 1: Grayscale control

8.8.1 Gamma-characteristics adjustment registers

This NV3030B has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into three groups, which correspond to the gradient, amplitude, and Micro Adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

0- Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

0- Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 128-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

0- Gamma Micro Adjustment registers

The gamma Micro Adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~6), each of which has 5 inputs and generates one reference voltage output (VgP/N (3,4,10,15,21,27,28)).

Gamma-adjustment registers			
Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor （PRP/N0） for center adjustment
	PRP1 6-0	PRN1 6-0	Variable resistor （PRP/N1） for center adjustment
Micro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 4)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 10)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 21)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 27)
	PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 28)
	PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 15)
Offset Adjustment	VRP0 5-0	VRN0 5-0	Variable resistor （VRP/N0） for offset adjustment
	VRP1 5-0	VRN1 5-0	Variable resistor （VRP/N1） for offset adjustment
	VRP2 5-0	VRN2 5-0	Variable resistor （VRP/N2） for offset adjustment
	VRP3 5-0	VRN3 5-0	Variable resistor （VRP/N3） for offset adjustment
	VRP4 5-0	VRN4 5-0	Variable resistor （VRP/N4） for offset adjustment
	VRP5 5-0	VRN5 5-0	Variable resistor （VRP/N5） for offset adjustment

8.8.2 Gamma resister stream

The block consists of one gamma resister stream. Use different register setting for positive or negative polarity. Each polarity includes sixteen gamma reference voltages. V(P/N)0, V(P/N)1, V(P/N)2, V(P/N)3, V(P/N)4, V(P/N)5, V(P/N)6, V(P/N)7, V(P/N)8, V(P/N)9, V(P/N)10, V(P/N)11, V(P/N)12, V(P/N)13, V(P/N)14, V(P/N)15

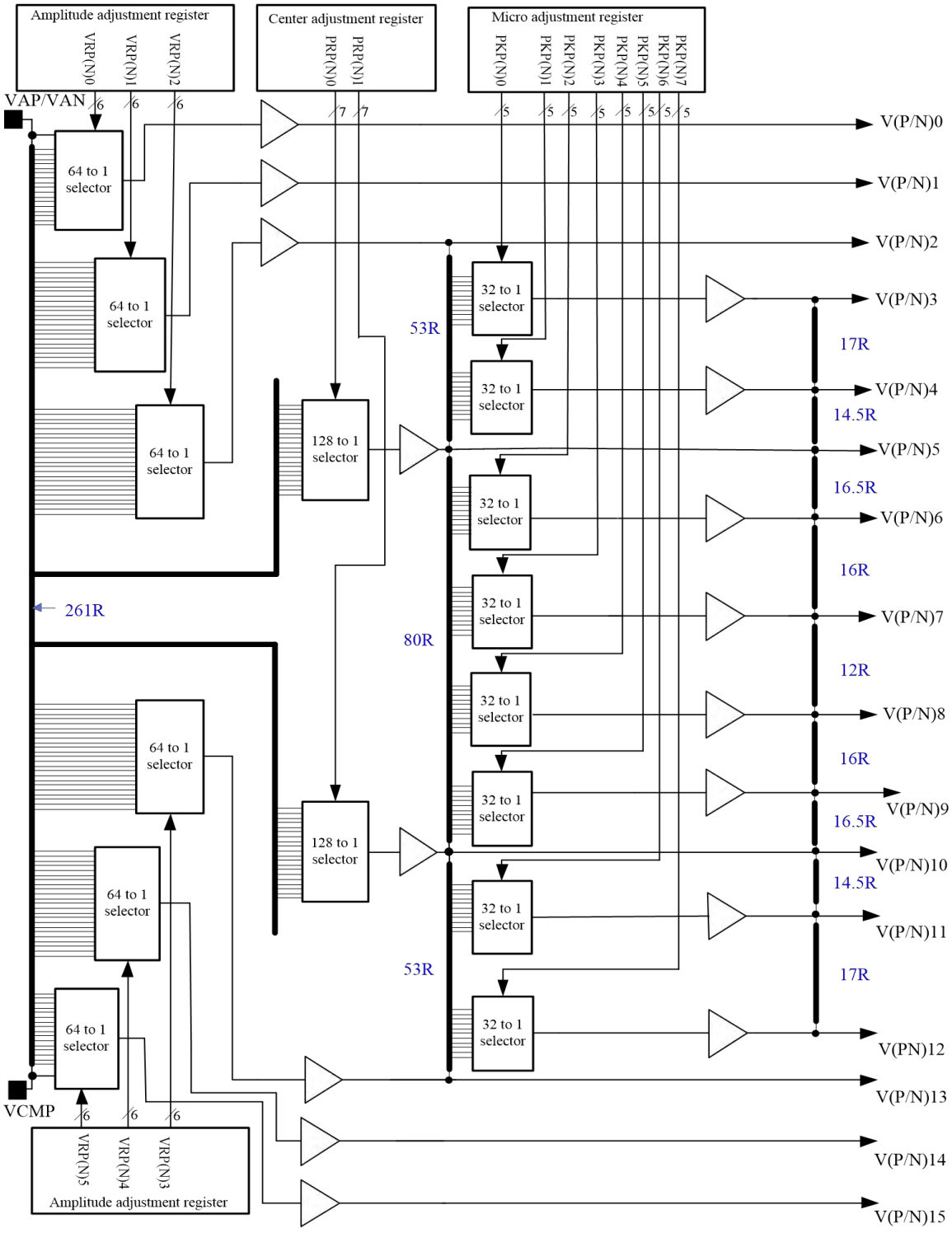


Figure 2 : Gamma resister stream and gamma reference voltage

8.8.3 Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below:

- Table 1: Offset adjustment 0 ~ 5

Register VR(P/N)0[5:0]	Resistance VR(P/N)0
000000	0R
000001	1R
000010	2R
000011	3R
…	…
011101	29R
011110	30R
011111	31R
100000	34R
100001	37R
100010	40R
100011	43R
…	…
111101	121R
111110	124R
111111	127R

Register VR(P/N)1[5:0]	Resistance VR(P/N)1
000000	10R
000001	11R
000010	12R
000011	13R
…	…
011011	37R
011100	38R
011101	39R
011110	42R
011111	45R
100000	48R
100001	51R
…	…
111101	135R
111110	138R
111111	141R

Register VR(P/N)2[5:0]	Resistance VR(P/N)2
000000	20R
000001	21R
000010	22R
000011	23R
…	…
011010	46R
011011	47R
011100	48R
011101	51R
011110	54R
011111	57R
100000	60R
…	…
111101	147R
111110	150R
111111	153R

Register VR(P/N)3[5:0]	Resistance VR(P/N)3
000000	108R
000001	111R
000010	114R
…	…
011111	201R
100000	204R
100001	207R
100010	210R
100011	211R
100100	212R
…	…
111100	236R
111101	237R
111110	238R
111111	239R

Register VR(P/N)4[5:0]	Resistance VR(P/N)4
000000	120R
000001	123R
000010	126R
…	…
011110	210R
011111	213R
100000	216R
100001	219R
100010	220R
100011	221R
…	…
111100	246R
111101	247R
111110	248R
111111	249R

Register VR(P/N)5[5:0]	Resistance VR(P/N)5
000000	135R
000001	138R
000010	141R
…	…
011101	222R
011110	225R
011111	228R
100000	229R
100001	230R
100010	231R
…	…
111100	257R
111101	258R
111110	259R
111111	260R

- Table 2 : Center adjustment

Register PR (P/N)0[6:0]	Resistance PR(P/N)0
0000000	67R
0000001	68R
0000010	69R
…	…
1111101	192R
1111110	193R
1111111	194R

Register PR(P/N)1[6:0]	Resistance PR(P/N)1
0000000	67R
0000001	68R
0000010	69R
…	…
1111101	192R
1111110	193R
1111111	194R

8.8.4 The grayscale levels are determined by the following formulas.

Table 3 : V(P/N)0

Reference Voltage	Micro Adjustment value	V(P/N)0 formula
V(P/N)0	VRP/N0 5-0 = 000000	VAP/VAN
	VRP/N0 5-0 = 000001	((261R -1R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 000010	((261R -2R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 000011	((261R -3R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 000100	((261R -4R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 000101	((261R -5R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 000110	((261R -6R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 000111	((261R -7R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 001000	((261R -8R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 001001	((261R -9R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 001010	((261R -10R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 001011	((261R -11R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 001100	((261R -12R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 001101	((261R -13R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 001110	((261R -14R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 001111	((261R -15R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 010000	((261R -16R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 010001	((261R -17R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 010010	((261R -18R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 010011	((261R -19R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 010100	((261R -20R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 010101	((261R -21R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 010110	((261R -22R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 010111	((261R -23R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 011000	((261R -24R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 011001	((261R -25R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 011010	((261R -26R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 011011	((261R -27R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 011100	((261R -28R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 011101	((261R -29R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 011110	((261R -30R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 011111	((261R -31R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 100000	((261R -34R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 100001	((261R -37R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 100010	((261R -40R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 100011	((261R -43R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 100100	((261R -46R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 100101	((261R -49R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 100110	((261R -52R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 100111	((261R -55R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 101000	((261R -58R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 101001	((261R -61R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 101010	((261R -64R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 101011	((261R -67R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 101100	((261R -70R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 101101	((261R -73R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 101110	((261R -76R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 101111	((261R -79R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 110000	((261R -82R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 110001	((261R -85R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 110010	((261R -88R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 110011	((261R -91R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 110100	((261R -94R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 110101	((261R -97R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 110110	((261R -100R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 110111	((261R -103R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 111000	((261R -106R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 111001	((261R -109R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 111010	((261R -112R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 111011	((261R -115R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 111100	((261R -118R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 111101	((261R -121R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 111110	((261R -124R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N0 5-0 = 111111	((261R -127R) / 261R) * (VAP/VAN–VCMP) + VCMP

Table 4 : V(P/N)1

Reference Voltage	Micro Adjustment value	V(P/N)1 formula
V(P/N)1	VRP/N1 5-0 = 000000	((261R -10R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 000001	((261R -11R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 000010	((261R -12R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 000011	((261R -13R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 000100	((261R -14R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 000101	((261R -15R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 000110	((261R -16R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 000111	((261R -17R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 001000	((261R -18R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 001001	((261R -19R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 001010	((261R -20R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 001011	((261R -21R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 001100	((261R -22R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 001101	((261R -23R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 001110	((261R -24R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 001111	((261R -25R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 010000	((261R -26R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 010001	((261R -27R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 010010	((261R -28R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 010011	((261R -29R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 010100	((261R -30R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 010101	((261R -31R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 010110	((261R -32R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 010111	((261R -33R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 011000	((261R -34R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 011001	((261R -35R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 011010	((261R -36R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 011011	((261R -37R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 011100	((261R -38R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 011101	((261R -39R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 011110	((261R -42R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 011111	((261R -45R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 100000	((261R -48R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 100001	((261R -51R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 100010	((261R -54R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 100011	((261R -57R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 100100	((261R -60R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 100101	((261R -63R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 100110	((261R -66R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 100111	((261R -69R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 101000	((261R -72R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 101001	((261R -75R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 101010	((261R -78R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 101011	((261R -81R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 101100	((261R -84R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 101101	((261R -87R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 101110	((261R -90R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 101111	((261R -93R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 110000	((261R -96R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 110001	((261R -99R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 110010	((261R -102R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 110011	((261R -105R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 110100	((261R -108R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 110101	((261R -111R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 110110	((261R -114R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 110111	((261R -117R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 111000	((261R -120R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 111001	((261R -123R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 111010	((261R -126R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 111011	((261R -129R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 111100	((261R -132R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 111101	((261R -135R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 111110	((261R -138R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N1 5-0 = 111111	((261R -141R) / 261R) * (VAP/VAN–VCMP) + VCMP

Table 5: V(P/N)2

Reference Voltage	Micro Adjustment value	V(P/N)2 formula
V(P/N)2	VRP/N2 5-0 = 000000	((261R -20R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 000001	((261R -21R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 000010	((261R -22R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 000011	((261R -23R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 000100	((261R -24R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 000101	((261R -25R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 000110	((261R -26R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 000111	((261R -27R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 001000	((261R -28R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 001001	((261R -29R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 001010	((261R -30R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 001011	((261R -31R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 001100	((261R -32R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 001101	((261R -33R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 001110	((261R -34R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 001111	((261R -35R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 010000	((261R -36R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 010001	((261R -37R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 010010	((261R -38R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 010011	((261R -39R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 010100	((261R -40R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 010101	((261R -41R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 010110	((261R -42R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 010111	((261R -43R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 011000	((261R -44R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 011001	((261R -45R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 011010	((261R -46R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 011011	((261R -47R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 011100	((261R -48R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 011101	((261R -51R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 011110	((261R -54R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 011111	((261R -57R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 100000	((261R -60R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 100001	((261R -63R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 100010	((261R -66R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 100011	((261R -69R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 100100	((261R -72R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 100101	((261R -75R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 100110	((261R -78R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 100111	((261R -81R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 101000	((261R -84R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 101001	((261R -87R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 101010	((261R -90R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 101011	((261R -93R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 101100	((261R -96R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 101101	((261R -99R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 101110	((261R -102R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 101111	((261R -105R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 110000	((261R -108R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 110001	((261R -111R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 110010	((261R -114R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 110011	((261R -117R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 110100	((261R -120R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 110101	((261R -123R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 110110	((261R -126R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 110111	((261R -129R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 111000	((261R -132R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 111001	((261R -135R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 111010	((261R -138R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 111011	((261R -141R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 111100	((261R -144R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 111101	((261R -147R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 111110	((261R -150R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N2 5-0 = 111111	((261R -153R) / 261R) * (VAP/VAN–VCMP) + VCMP

Table 6 : V(P/N)13

Reference Voltage	Micro Adjustment value	V(P/N)13 formula
V(P/N)13	VRP/N3 5-0 = 000000	((261R -108R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 000001	((261R -111R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 000010	((261R -114R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 000011	((261R -117R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 000100	((261R -120R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 000101	((261R -123R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 000110	((261R -126R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 000111	((261R -129R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 001000	((261R -132R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 001001	((261R -135R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 001010	((261R -138R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 001011	((261R -141R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 001100	((261R -144R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 001101	((261R -147R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 001110	((261R -150R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 001111	((261R -153R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 010000	((261R -156R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 010001	((261R -159R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 010010	((261R -162R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 010011	((261R -165R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 010100	((261R -168R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 010101	((261R -171R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 010110	((261R -174R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 010111	((261R -177R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 011000	((261R -180R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 011001	((261R -183R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 011010	((261R -186R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 011011	((261R -189R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 011100	((261R -192R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 011101	((261R -195R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 011110	((261R -198R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 011111	((261R -201R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 100000	((261R -204R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 100001	((261R -207R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 100010	((261R -210R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 100011	((261R -211R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 100100	((261R -212R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 100101	((261R -213R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 100110	((261R -214R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 100111	((261R -215R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 101000	((261R -216R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 101001	((261R -217R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 101010	((261R -218R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 101011	((261R -219R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 101100	((261R -220R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 101101	((261R -221R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 101110	((261R -222R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 101111	((261R -223R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 110000	((261R -224R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 110001	((261R -225R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 110010	((261R -226R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 110011	((261R -227R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 110100	((261R -228R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 110101	((261R -229R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 110110	((261R -230R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 110111	((261R -231R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 111000	((261R -232R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 111001	((261R -233R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 111010	((261R -234R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 111011	((261R -235R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 111100	((261R -236R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 111101	((261R -237R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 111110	((261R -238R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N3 5-0 = 111111	((261R -239R) / 261R) * (VAP/VAN–VCMP) + VCMP

Table 7 : V(P/N)14

Reference Voltage	Micro Adjustment value	V(P/N)14 formula
V(P/N)14	VRP/N4 5-0 = 000000	((261R -120R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 000001	((261R -123R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 000010	((261R -126R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 000011	((261R -129R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 000100	((261R -132R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 000101	((261R -135R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 000110	((261R -138R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 000111	((261R -141R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 001000	((261R -144R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 001001	((261R -147R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 001010	((261R -150R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 001011	((261R -153R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 001100	((261R -156R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 001101	((261R -159R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 001110	((261R -162R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 001111	((261R -165R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 010000	((261R -168R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 010001	((261R -171R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 010010	((261R -174R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 010011	((261R -177R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 010100	((261R -180R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 010101	((261R -183R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 010110	((261R -186R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 010111	((261R -189R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 011000	((261R -192R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 011001	((261R -195R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 011010	((261R -198R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 011011	((261R -201R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 011100	((261R -204R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 011101	((261R -207R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 011110	((261R -210R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 011111	((261R -213R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 100000	((261R -216R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 100001	((261R -219R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 100010	((261R -220R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 100011	((261R -221R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 100100	((261R -222R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 100101	((261R -223R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 100110	((261R -224R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 100111	((261R -225R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 101000	((261R -226R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 101001	((261R -227R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 101010	((261R -228R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 101011	((261R -229R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 101100	((261R -230R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 101101	((261R -231R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 101110	((261R -232R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 101111	((261R -233R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 110000	((261R -234R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 110001	((261R -235R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 110010	((261R -236R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 110011	((261R -237R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 110100	((261R -238R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 110101	((261R -239R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 110110	((261R -240R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 110111	((261R -241R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 111000	((261R -242R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 111001	((261R -243R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 111010	((261R -244R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 111011	((261R -245R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 111100	((261R -246R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 111101	((261R -247R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 111110	((261R -248R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N4 5-0 = 111111	((261R -249R) / 261R) * (VAP/VAN–VCMP) + VCMP

Table 8 : V(P/N)15

Reference Voltage	Micro Adjustment value	V(P/N)15 formula
V(P/N)15	VRP/N5 5-0 = 000000	((261R -135R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 000001	((261R -138R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 000010	((261R -141R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 000011	((261R -144R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 000100	((261R -147R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 000101	((261R -150R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 000110	((261R -153R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 000111	((261R -156R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 001000	((261R -159R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 001001	((261R -162R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 001010	((261R -165R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 001011	((261R -168R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 001100	((261R -171R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 001101	((261R -174R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 001110	((261R -177R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 001111	((261R -180R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 010000	((261R -183R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 010001	((261R -186R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 010010	((261R -189R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 010011	((261R -192R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 010100	((261R -195R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 010101	((261R -198R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 010110	((261R -201R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 010111	((261R -204R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 011000	((261R -207R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 011001	((261R -210R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 011010	((261R -213R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 011011	((261R -216R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 011100	((261R -219R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 011101	((261R -222R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 011110	((261R -225R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 011111	((261R -228R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 100000	((261R -229R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 100001	((261R -230R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 100010	((261R -231R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 100011	((261R -232R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 100100	((261R -233R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 100101	((261R -234R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 100110	((261R -235R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 100111	((261R -236R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 101000	((261R -237R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 101001	((261R -238R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 101010	((261R -239R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 101011	((261R -240R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 101100	((261R -241R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 101101	((261R -242R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 101110	((261R -243R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 101111	((261R -244R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 110000	((261R -245R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 110001	((261R -246R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 110010	((261R -247R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 110011	((261R -248R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 110100	((261R -249R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 110101	((261R -250R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 110110	((261R -251R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 110111	((261R -252R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 111000	((261R -253R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 111001	((261R -254R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 111010	((261R -255R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 111011	((261R -256R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 111100	((261R -257R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 111101	((261R -258R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 111110	((261R -259R) / 261R) * (VAP/VAN–VCMP) + VCMP
	VRP/N5 5-0 = 111111	((261R -260R) / 261R) * (VAP/VAN–VCMP) + VCMP

Table 9 : V(P/N)5

Reference Voltage	Micro Adjustment value	V(P/N)5 formula
V(P/N)5	PRP/N0 6-0 = 0000000	((261R -67R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0000001	((261R -68R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0000010	((261R -69R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0000011	((261R -70R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0000100	((261R -71R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0000101	((261R -72R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0000110	((261R -73R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0000111	((261R -74R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0001000	((261R -75R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0001001	((261R -76R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0001010	((261R -77R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0001011	((261R -78R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0001100	((261R -79R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0001101	((261R -80R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0001110	((261R -81R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0001111	((261R -82R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0010000	((261R -83R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0010001	((261R -84R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0010010	((261R -85R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0010011	((261R -86R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0010100	((261R -87R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0010101	((261R -88R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0010110	((261R -89R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0010111	((261R -90R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0011000	((261R -91R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0011001	((261R -92R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0011010	((261R -93R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0011011	((261R -94R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0011100	((261R -95R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0011101	((261R -96R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0011110	((261R -97R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0011111	((261R -98R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0100000	((261R -99R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0100001	((261R -100R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0100010	((261R -101R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0100011	((261R -102R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0100100	((261R -103R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0100101	((261R -104R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0100110	((261R -105R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0100111	((261R -106R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0101000	((261R -107R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0101001	((261R -108R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0101010	((261R -109R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0101011	((261R -110R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0101100	((261R -111R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0101101	((261R -112R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0101110	((261R -113R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0101111	((261R -114R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0110000	((261R -115R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0110001	((261R -116R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0110010	((261R -117R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0110011	((261R -118R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0110100	((261R -119R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0110101	((261R -120R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0110110	((261R -121R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0110111	((261R -122R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0111000	((261R -123R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0111001	((261R -124R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0111010	((261R -125R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0111011	((261R -126R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0111100	((261R -127R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0111101	((261R -128R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0111110	((261R -129R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 0111111	((261R -130R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1000000	((261R -131R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1000001	((261R -132R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1000010	((261R -133R) / 261R) * (VAP/VAN–VCMP) + VCMP

	PRP/N0 6-0 = 1000011	((261R -134R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1000100	((261R -135R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1000101	((261R -136R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1000110	((261R -137R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1000111	((261R -138R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1001000	((261R -139R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1001001	((261R -140R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1001010	((261R -141R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1001011	((261R -142R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1001100	((261R -143R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1001101	((261R -144R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1001110	((261R -145R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1001111	((261R -146R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1010000	((261R -147R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1010001	((261R -148R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1010010	((261R -149R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1010011	((261R -150R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1010100	((261R -151R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1010101	((261R -152R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1010110	((261R -153R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1010111	((261R -154R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1011000	((261R -155R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1011001	((261R -156R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1011010	((261R -157R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1011011	((261R -158R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1011100	((261R -159R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1011101	((261R -160R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1011110	((261R -161R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1011111	((261R -162R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1100000	((261R -163R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1100001	((261R -164R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1100010	((261R -165R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1100011	((261R -166R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1100100	((261R -167R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1100101	((261R -168R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1100110	((261R -169R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1100111	((261R -170R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1101000	((261R -171R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1101001	((261R -172R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1101010	((261R -173R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1101011	((261R -174R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1101100	((261R -175R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1101101	((261R -176R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1101110	((261R -177R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1101111	((261R -178R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1110000	((261R -179R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1110001	((261R -180R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1110010	((261R -181R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1110011	((261R -182R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1110100	((261R -183R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1110101	((261R -184R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1110110	((261R -185R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1110111	((261R -186R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1111000	((261R -187R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1111001	((261R -188R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1111010	((261R -189R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1111011	((261R -190R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1111100	((261R -191R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1111101	((261R -192R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1111110	((261R -193R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N0 6-0 = 1111111	((261R -194R) / 261R) * (VAP/VAN–VCMP) + VCMP

Table 10 : V(P/N)10

Reference Voltage	Micro Adjustment value	V(P/N)10 formula
V(P/N)10	PRP/N1 6-0 = 0000000	((261R -67R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0000001	((261R -68R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0000010	((261R -69R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0000011	((261R -70R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0000100	((261R -71R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0000101	((261R -72R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0000110	((261R -73R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0000111	((261R -74R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0001000	((261R -75R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0001001	((261R -76R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0001010	((261R -77R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0001011	((261R -78R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0001100	((261R -79R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0001101	((261R -80R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0001110	((261R -81R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0001111	((261R -82R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0010000	((261R -83R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0010001	((261R -84R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0010010	((261R -85R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0010011	((261R -86R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0010100	((261R -87R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0010101	((261R -88R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0010110	((261R -89R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0010111	((261R -90R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0011000	((261R -91R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0011001	((261R -92R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0011010	((261R -93R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0011011	((261R -94R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0011100	((261R -95R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0011101	((261R -96R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0011110	((261R -97R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0011111	((261R -98R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0100000	((261R -99R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0100001	((261R -100R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0100010	((261R -101R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0100011	((261R -102R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0100100	((261R -103R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0100101	((261R -104R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0100110	((261R -105R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0100111	((261R -106R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0101000	((261R -107R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0101001	((261R -108R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0101010	((261R -109R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0101011	((261R -110R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0101100	((261R -111R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0101101	((261R -112R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0101110	((261R -113R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0101111	((261R -114R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0110000	((261R -115R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0110001	((261R -116R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0110010	((261R -117R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0110011	((261R -118R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0110100	((261R -119R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0110101	((261R -120R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0110110	((261R -121R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0110111	((261R -122R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0111000	((261R -123R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0111001	((261R -124R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0111010	((261R -125R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0111011	((261R -126R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0111100	((261R -127R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0111101	((261R -128R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0111110	((261R -129R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 0111111	((261R -130R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1000000	((261R -131R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1000001	((261R -132R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1000010	((261R -133R) / 261R) * (VAP/VAN–VCMP) + VCMP

Reference Voltage	Micro Adjustment value	V(P/N)10 formula
V(P/N)10	PRP/N1 6-0 = 1000011	((261R -134R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1000100	((261R -135R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1000101	((261R -136R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1000110	((261R -137R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1000111	((261R -138R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1001000	((261R -139R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1001001	((261R -140R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1001010	((261R -141R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1001011	((261R -142R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1001100	((261R -143R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1001101	((261R -144R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1001110	((261R -145R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1001111	((261R -146R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1010000	((261R -147R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1010001	((261R -148R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1010010	((261R -149R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1010011	((261R -150R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1010100	((261R -151R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1010101	((261R -152R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1010110	((261R -153R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1010111	((261R -154R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1011000	((261R -155R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1011001	((261R -156R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1011010	((261R -157R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1011011	((261R -158R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1011100	((261R -159R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1011101	((261R -160R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1011110	((261R -161R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1011111	((261R -162R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1100000	((261R -163R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1100001	((261R -164R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1100010	((261R -165R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1100011	((261R -166R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1100100	((261R -167R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1100101	((261R -168R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1100110	((261R -169R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1100111	((261R -170R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1101000	((261R -171R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1101001	((261R -172R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1101010	((261R -173R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1101011	((261R -174R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1101100	((261R -175R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1101101	((261R -176R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1101110	((261R -177R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1101111	((261R -178R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1110000	((261R -179R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1110001	((261R -180R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1110010	((261R -181R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1110011	((261R -182R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1110100	((261R -183R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1110101	((261R -184R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1110110	((261R -185R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1110111	((261R -186R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1111000	((261R -187R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1111001	((261R -188R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1111010	((261R -189R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1111011	((261R -190R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1111100	((261R -191R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1111101	((261R -192R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1111110	((261R -193R) / 261R) * (VAP/VAN–VCMP) + VCMP
	PRP/N1 6-0 = 1111111	((261R -194R) / 261R) * (VAP/VAN–VCMP) + VCMP

Table 11a: V(P/N)3

Reference Voltage	Micro Adjustment value	V(P/N)3 formula
V(P/N)3	PKP/N0 4-0 = 00000	((53R / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 00001	((53R -1R) / 53R) *(VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 00010	((53R -2R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 00011	((53R -3R) / 53R) *(VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 00100	((53R -4R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 00101	((53R -5R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 00110	((53R -6R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 00111	((53R -7R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 01000	((53R -8R) / 53R) *(VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 01001	((53R -9R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 01010	((53R -10R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 01011	((53R -11R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 01100	((53R -12R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 01101	((53R -13R) / 53R) *(VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 01110	((53R -14R) / 53R) *(VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 01111	((53R -15R) / 53R) *(VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 10000	((53R -16R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 10001	((53R -17R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 10010	((53R -18R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 10011	((53R -19R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 10100	((53R -20R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 10101	((53R -21R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 10110	((53R -22R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 10111	((53R -23R) / 53R) *(VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 11000	((53R -24R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 11001	((53R -25R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 11010	((53R -26R) / 53R) *(VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 11011	((53R -27R) / 53R) *(VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 11100	((53R -28R) / 53R) *(VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 11101	((53R -29R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 11110	((53R -30R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N0 4-0 = 11111	((53R -31R) / 53R) * (VP/N2-VP/N5) + VP/N5

Table 11b: V(P/N)4

Reference Voltage	Micro Adjustment value	V(P/N)4 formula
V(P/N)4	PKP/N1 4-0 = 00000	((53R -20R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 00001	((53R -21R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 00010	((53R -22R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 00011	((53R -23R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 00100	((53R -24R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 00101	((53R -25R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 00110	((53R -26R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 00111	((53R -27R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 01000	((53R -28R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 01001	((53R -29R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 01010	((53R -30R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 01011	((53R -31R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 01100	((53R -32R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 01101	((53R -33R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 01110	((53R -34R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 01111	((53R -35R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 10000	((53R -36R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 10001	((53R -37R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 10010	((53R -38R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 10011	((53R -39R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 10100	((53R -40R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 10101	((53R -41R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 10110	((53R -42R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 10111	((53R -43R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 11000	((53R -44R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 11001	((53R -45R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 11010	((53R -46R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 11011	((53R -47R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 11100	((53R -48R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 11101	((53R -49R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 11110	((53R -50R) / 53R) * (VP/N2-VP/N5) + VP/N5
	PKP/N1 4-0 = 11111	((53R -51R) / 53R) * (VP/N2-VP/N5) + VP/N5

Table 12a: V(P/N)6

Reference Voltage	Micro Adjustment value	V(P/N)6 formula
V(P/N)6	PKP/N2 4-0 = 00000	((80R/ 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 00001	((80R -1R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 00010	((80R -2R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 00011	((80R -3R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 00100	((80R -4R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 00101	((80R -5R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 00110	((80R -6R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 00111	((80R -7R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 01000	((80R -8R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 01001	((80R -9R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 01010	((80R -10R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 01011	((80R -11R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 01100	((80R -12R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 01101	((80R -13R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 01110	((80R -14R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 01111	((80R -15R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 10000	((80R -16R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 10001	((80R -17R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 10010	((80R -18R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 10011	((80R -19R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 10100	((80R -20R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 10101	((80R -21R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 10110	((80R -22R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 10111	((80R -23R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 11000	((80R -24R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 11001	((80R -25R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 11010	((80R -26R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 11011	((80R -27R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 11100	((80R -28R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 11101	((80R -29R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 11110	((80R -30R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N2 4-0 = 11111	((80R -31R) / 80R) * (VP/N5-VP/N10) + VP/N10

Table 12b: V(P/N)7

Reference Voltage	Micro Adjustment value	V(P/N)7 formula
V(P/N)7	PKP/N3 4-0 = 00000	((80R -16R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 00001	((80R -17R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 00010	((80R -18R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 00011	((80R -19R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 00100	((80R -20R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 00101	((80R -21R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 00110	((80R -22R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 00111	((80R -23R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 01000	((80R -24R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 01001	((80R -25R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 01010	((80R -26R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 01011	((80R -27R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 01100	((80R -28R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 01101	((80R -29R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 01110	((80R -30R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 01111	((80R -31R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 10000	((80R -32R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 10001	((80R -33R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 10010	((80R -34R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 10011	((80R -35R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 10100	((80R -36R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 10101	((80R -37R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 10110	((80R -38R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 10111	((80R -39R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 11000	((80R -40R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 11001	((80R -41R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 11010	((80R -42R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 11011	((80R -43R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 11100	((80R -44R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 11101	((80R -45R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 11110	((80R -46R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N3 4-0 = 11111	((80R -47R) / 80R) * (VP/N5-VP/N10) + VP/N10

Table 12c: V(P/N)8

Reference Voltage	Micro Adjustment value	V(P/N)8 formula
V(P/N)8	PKP/N4 4-0 = 00000	((80R -31R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 00001	((80R -32R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 00010	((80R -33R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 00011	((80R -34R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 00100	((80R -35R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 00101	((80R -36R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 00110	((80R -37R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 00111	((80R -38R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 01000	((80R -39R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 01001	((80R -40R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 01010	((80R -41R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 01011	((80R -42R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 01100	((80R -43R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 01101	((80R -44R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 01110	((80R -45R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 01111	((80R -46R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 10000	((80R -47R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 10001	((80R -48R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 10010	((80R -49R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 10011	((80R -50R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 10100	((80R -51R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 10101	((80R -52R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 10110	((80R -53R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 10111	((80R -54R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 11000	((80R -55R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 11001	((80R -56R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 11010	((80R -57R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 11011	((80R -58R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 11100	((80R -59R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 11101	((80R -60R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 11110	((80R -61R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N4 4-0 = 11111	((80R -62R) / 80R) * (VP/N5-VP/N10) + VP/N10

Table 12d: V(P/N)9

Reference Voltage	Micro Adjustment value	V(P/N)9 formula
V(P/N)9	PKP/N5 4-0 = 00000	((80R -47R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 00001	((80R -48R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 00010	((80R -49R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 00011	((80R -50R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 00100	((80R -51R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 00101	((80R -52R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 00110	((80R -53R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 00111	((80R -54R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 01000	((80R -55R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 01001	((80R -56R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 01010	((80R -57R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 01011	((80R -58R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 01100	((80R -59R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 01101	((80R -60R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 01110	((80R -61R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 01111	((80R -62R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 10000	((80R -63R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 10001	((80R -64R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 10010	((80R -65R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 10011	((80R -66R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 10100	((80R -67R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 10101	((80R -68R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 10110	((80R -69R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 10111	((80R -70R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 11000	((80R -71R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 11001	((80R -72R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 11010	((80R -73R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 11011	((80R -74R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 11100	((80R -75R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 11101	((80R -76R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 11110	((80R -77R) / 80R) * (VP/N5-VP/N10) + VP/N10
	PKP/N5 4-0 = 11111	((80R -78R) / 80R) * (VP/N5-VP/N10) + VP/N10

Table 13a: V(P/N)11

Reference Voltage	Micro Adjustment value	V(P/N)11 formula
V(P/N)11	PKP/N6 4-0 = 00000	((53R/ 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 00001	((53R -1R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 00010	((53R -2R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 00011	((53R -3R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 00100	((53R -4R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 00101	((53R -5R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 00110	((53R -6R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 00111	((53R -7R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 01000	((53R -8R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 01001	((53R -9R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 01010	((53R -10R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 01011	((53R -11R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 01100	((53R -12R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 01101	((53R -13R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 01110	((53R -14R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 01111	((53R -15R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 10000	((53R -16R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 10001	((53R -17R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 10010	((53R -18R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 10011	((53R -19R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 10100	((53R -20R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 10101	((53R -21R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 10110	((53R -22R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 10111	((53R -23R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 11000	((53R -24R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 11001	((53R -25R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 11010	((53R -26R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 11011	((53R -27R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 11100	((53R -28R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 11101	((53R -29R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 11110	((53R -30R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N6 4-0 = 11111	((53R -31R) / 53R) * (VP/N10-VP/N13) + VP/N13

Table 13b: V(P/N)12

Reference Voltage	Micro Adjustment value	V(P/N)12 formula
V(P/N)12	PKP/N7 4-0 = 00000	((53R -20R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 00001	((53R -21R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 00010	((53R -22R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 00011	((53R -23R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 00100	((53R -24R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 00101	((53R -25R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 00110	((53R -26R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 00111	((53R -27R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 01000	((53R -28R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 01001	((53R -29R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 01010	((53R -30R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 01011	((53R -31R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 01100	((53R -32R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 01101	((53R -33R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 01110	((53R -34R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 01111	((53R -35R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 10000	((53R -36R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 10001	((53R -37R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 10010	((53R -38R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 10011	((53R -39R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 10100	((53R -40R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 10101	((53R -41R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 10110	((53R -42R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 10111	((53R -43R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 11000	((53R -44R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 11001	((53R -45R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 11010	((53R -46R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 11011	((53R -47R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 11100	((53R -48R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 11101	((53R -49R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 11110	((53R -50R) / 53R) * (VP/N10-VP/N13) + VP/N13
	PKP/N7 4-0 = 11111	((53R -51R) / 53R) * (VP/N10-VP/N13) + VP/N13

Table 14:Positive polarity

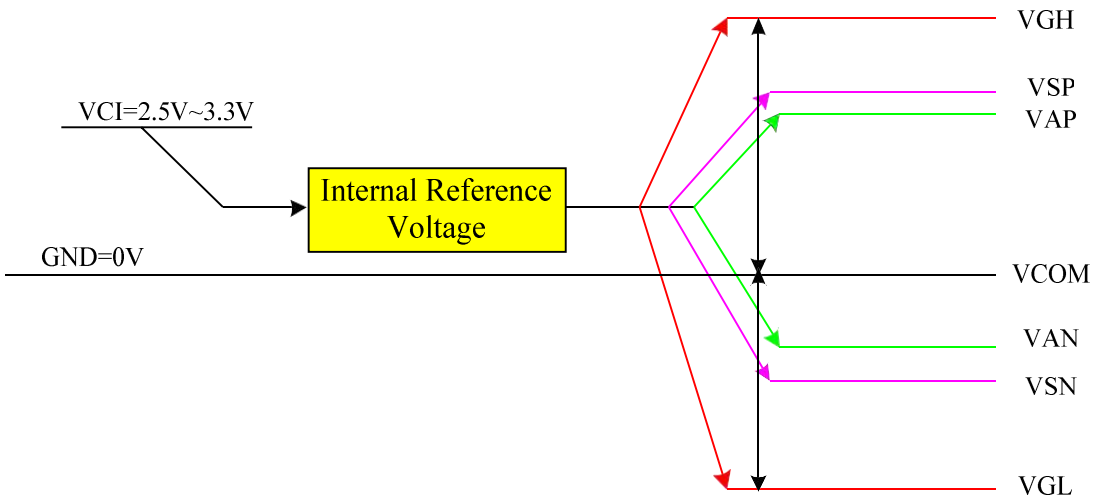
Grayscale voltage	Formula
v0	VP0
v1	VP1
v2	VP2
v3	VP3
v4	VP4+(12.5/17)*(VP3-VP4)
v5	VP4+(8/17)*(VP3-VP4)
v6	VP4+(4/17)*(VP3-VP4)
v7	VP4
v8	VP5+(10.5/14.5)*(VP4-VP5)
v9	VP5+(7/14.5)*(VP4-VP5)
v10	VP5+(3.5/14.5)*(VP4-VP5)
v11	VP5
v12	VP6+(10.5/16.5)*(VP5-VP6)
v13	VP6+(5/16.5)*(VP5-VP6)
v14	VP6
v15	VP7+(12/16)*(VP6-VP7)
v16	VP7+(8/16)*(VP6-VP7)
v17	VP7+(4/16)*(VP6-VP7)
v18	VP7
v19	VP8+(9/12)*(VP7-VP8)
v20	VP8+(6/12)*(VP7-VP8)
v21	VP8+(3/12)*(VP7-VP8)
v22	VP8
v23	VP9+(12/16)*(VP8-VPP9)
v24	VP9+(8/16)*(VP8-V9)
v25	VP9+(4/16)*(VP8-VP9)
v26	VP9
v27	VP10+(11.5/16.5)*(VP9-VP10)
v28	VP10+(6/16.5)*(VP9-VP10)
v29	VP10
v30	VP11+(7.5/14.5)*(VP10-VP11)
v31	VP11+(4/14.5)*(VP10-VP11)
V32	VP11
V33	VP12+(13/17)*(VP11-VP12)
V34	VP12+(9/17)*(VP11-VP12)
V35	VP12+(4.5/17)*(VP11-VP12)
V36	VP12
V37	VP13
V38	VP14
V39	VP15

Table 15: Negative polarity

Grayscale voltage	Formula
V39	VN0
V38	VN1
V37	VN2
V36	VN3
V35	VN4+(12.5/17)*(VN3-VN4)
V34	VN4+(8/17)*(VN3-VN4)
V33	VN4+(4/17)*(VN3-VN4)
V32	VN4
v31	VN5+(10.5/14.5)*(VN4-VN5)
v30	VN5+(7/14.5)*(VN4-VN5)
v29	VN5
v28	VN5+(10.5/14.5)*(VN4-VN5)
v27	VN5+(7/14.5)*(VN4-VN5)
v26	VN6
v25	VN7+(12/16)*(VN6-VN7)
v24	VN7+(8/16)*(VN6-VN7)
v23	VN7+(4/16)*(VN6-VN7)
v22	VN7
v21	VN8+(9/12)*(VN7-VN8)
v20	VN8+(6/12)*(VN7-VN8)
v19	VN8+(3/12)*(VN7-VN8)
v18	VN8
v17	VN9+(12/16)*(VN8-VN9)
v16	VN9+(8/16)*(VN8-VN9)
v15	VN9+(4/16)*(VN8-VN9)
v14	VN9
v13	VN10+(11.5/16.5)*(VN9-VN10)
v12	VN10+(6/16.5)*(VN9-VN10)
v11	VN10
v10	VN11+(11/14.5)*(VN10-VN11)
v9	VN11+(7.5/14.5)*(VN10-VN11)
v8	VN11+(4/14.5)*(VN10-VN11)
v7	VN11
v6	VN12+(13/17)*(VN11-VN12)
v5	VN12+(9/17)*(VN11-VN12)
v4	VN12+(4.5/17)*(VN11-VN12)
V3	VN12
V2	VN13
V1	VN14
V0	VN15

8.9 Voltage Generation

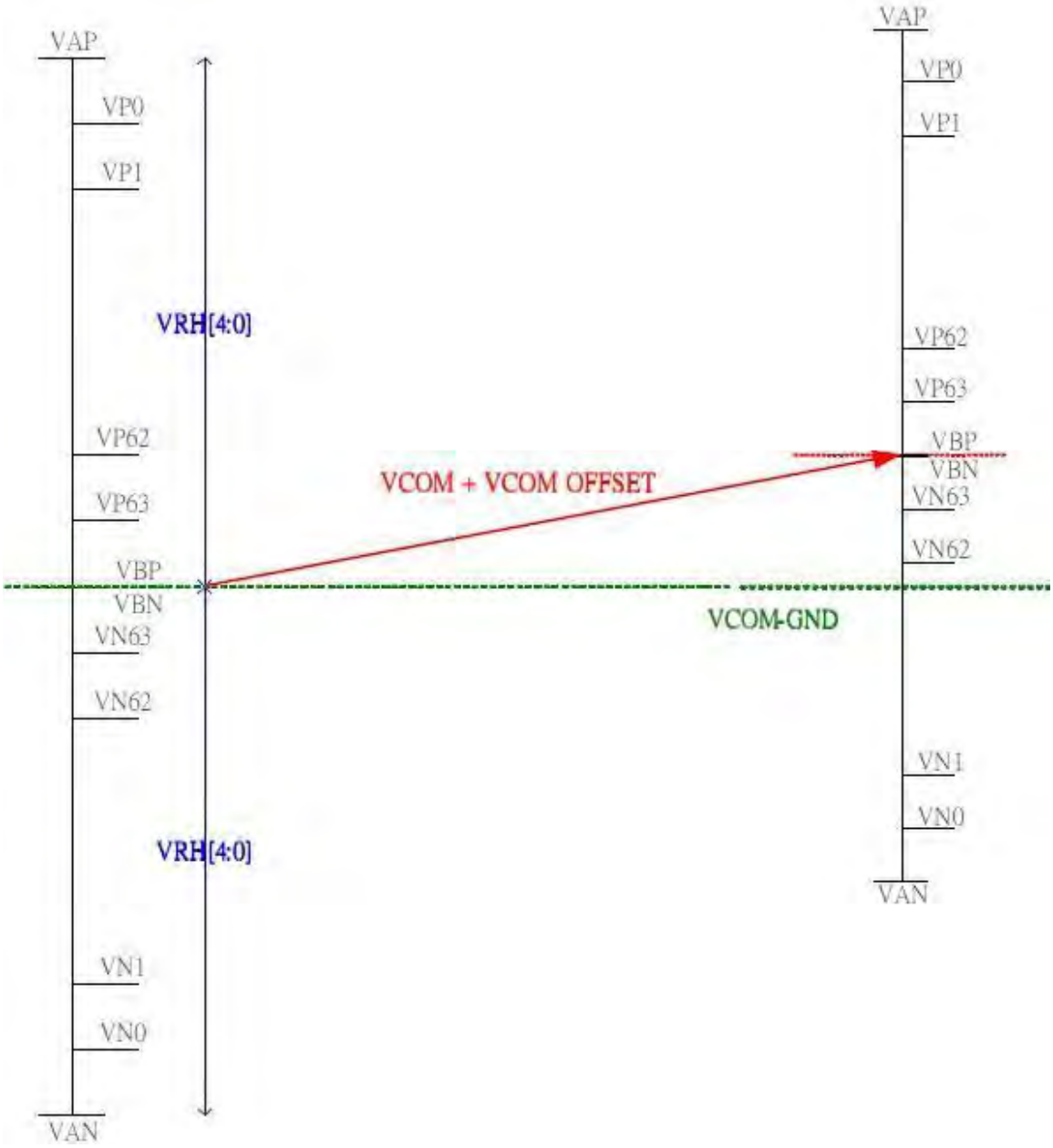
The following is the NV3030B analog voltage pattern diagram:



Power Booster Level

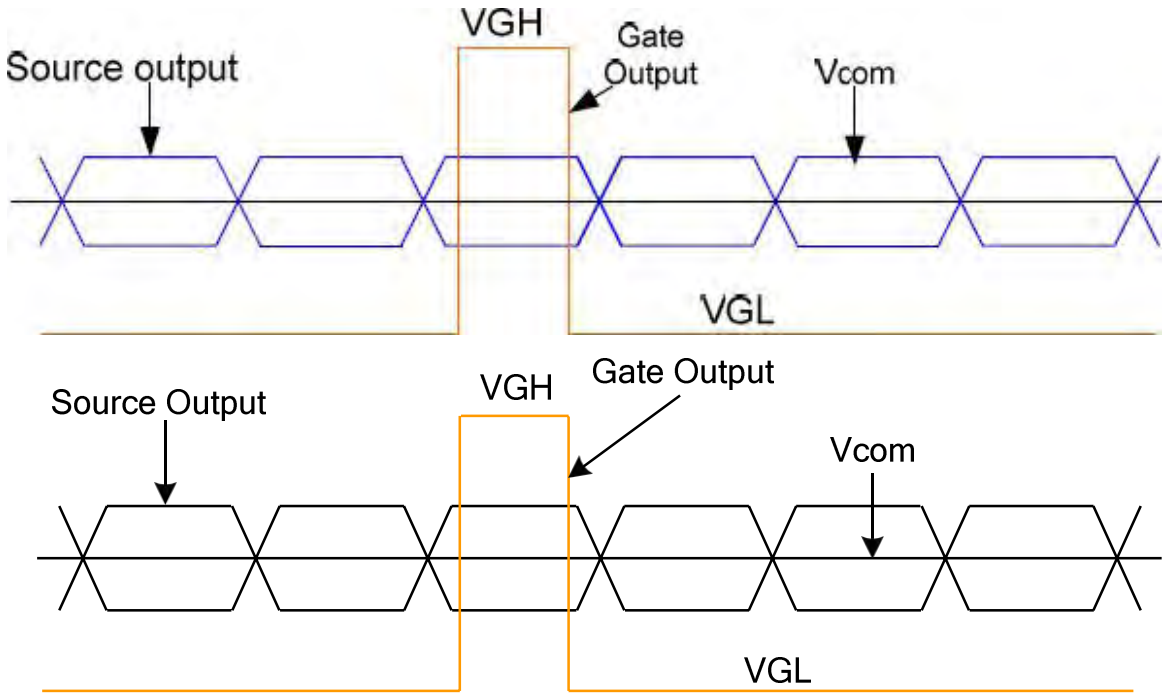
8.10 Relationship about source voltage

The relationship about source voltage is shown as below:



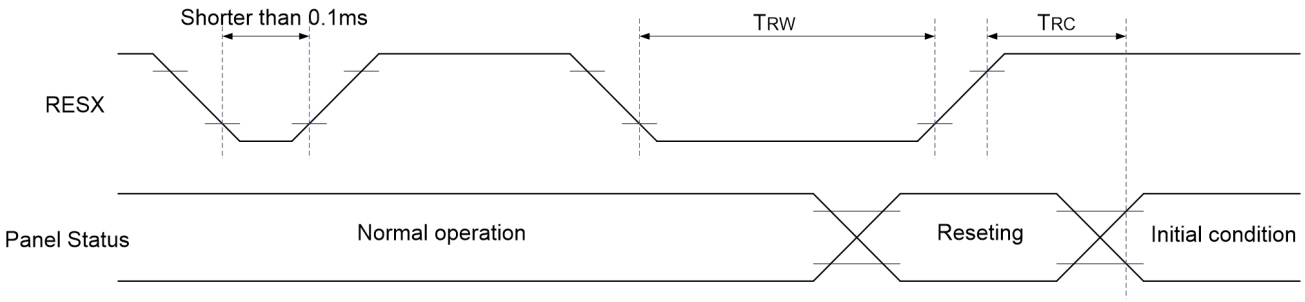
Relationship about source voltage

8.11 Applied Voltage to the TFT panel



Voltage Output to TFT LCD Panel

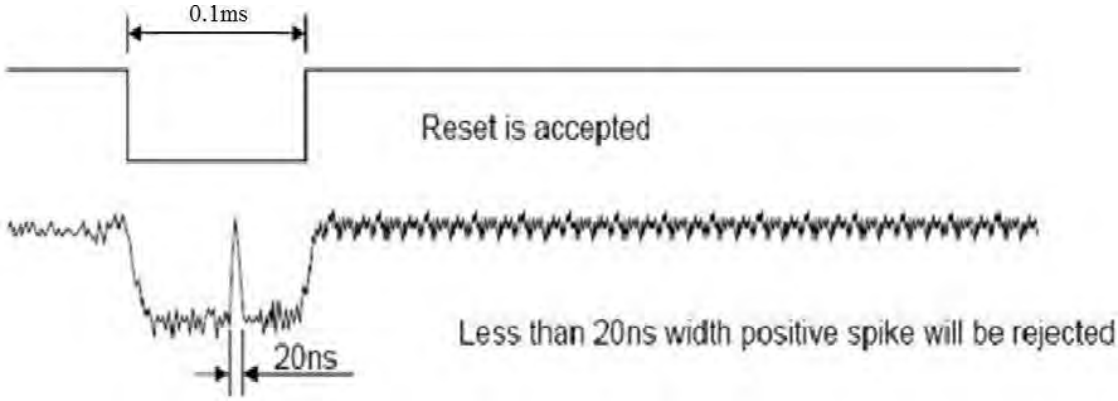
8.12 Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	T_{RW}	RESX low pulse duration	0.1		ms
	T_{RC}	Reset cancel			ms

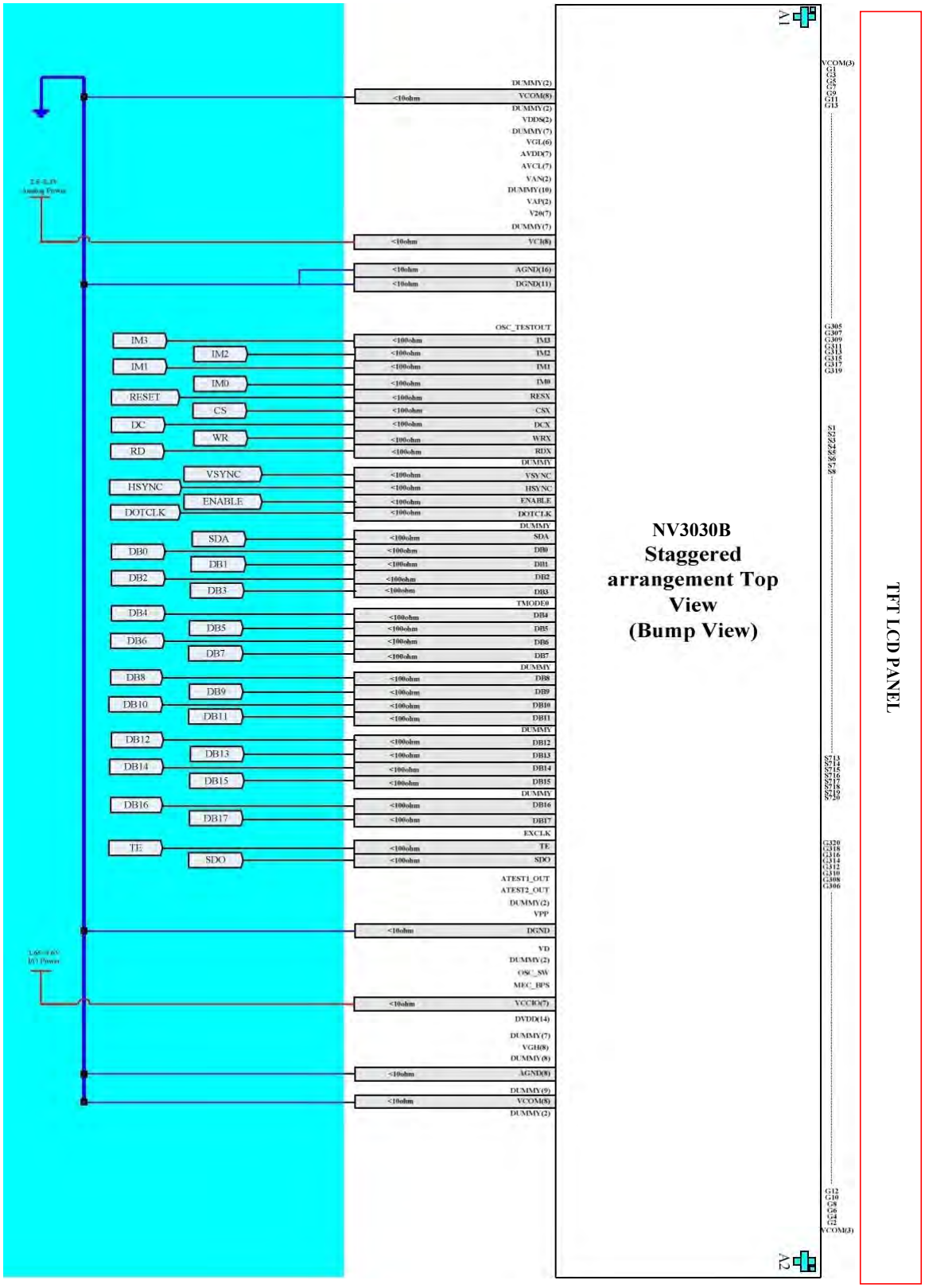
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time(RT) within 5ms after a rising edge of RESX.
2. Spice due to and electrostatic discharge on RESX line does not cause irregular system reset.
   When short than 0.1ms, reset rejected.
3. During the Resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in sleep in-mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

9. Application



10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Item	Symbol	Unit	Ratings	Notes
Power-supply voltage(1)	VCI,VDDI	V	-0.3 to +3.6	1,2
Power-supply voltage(2)	VCI-VSSA	V	-0.3 to +3.6	1,3
Power-supply voltage(3)	VSP-VSSA	V	-0.3 to +6.0	1,4
Power-supply voltage(4)	VGH-VGL	V	-0.3 to +30.0	1,4
Power-supply voltage(5)	VSSA-VGL	V	+3.0 to +13.0	1,7
Power-supply voltage(6)	VSP-VGL	V	+4.0 to +19.0	1,5
Power-supply voltage(7)	VCI-VGL	V	+3.0 to + 16.8	1,7
Input voltage	Vt	V	-0.3 to 3.9	1
Operating temperature	Topr	℃	-40 to +85	1
Storage temperature	Tstg	℃	-55 to +110	1

10.2 DC Characteristic

VCI = 2.5 ~ 3.4V, VDDI = 1.65~3.6V, Ta = -40 ~ 85 °C

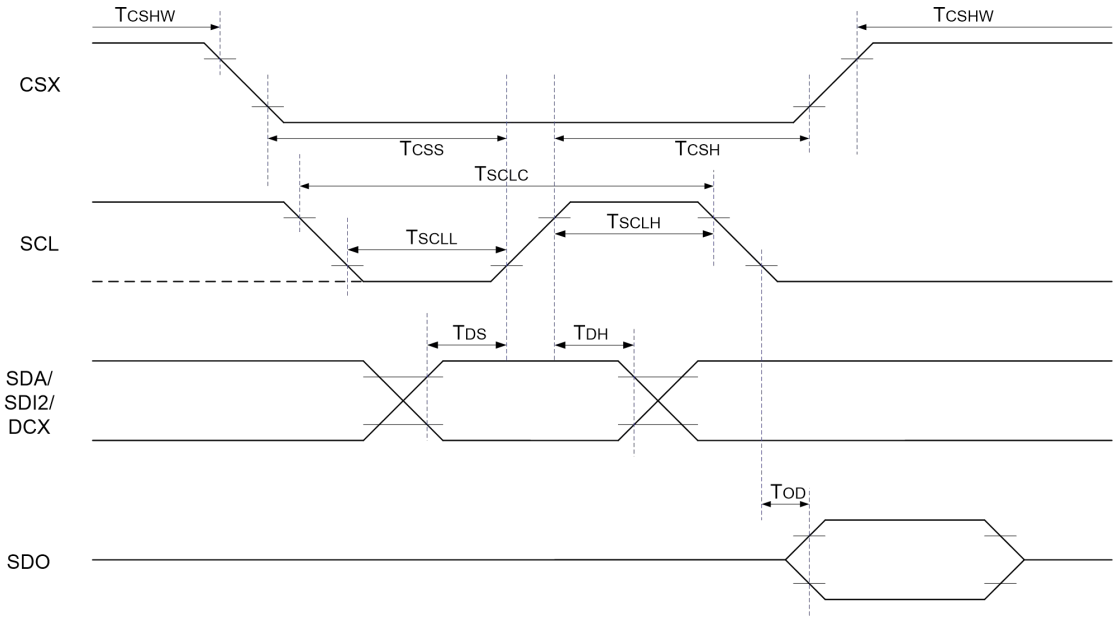
Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	VDDI = 1.65V ~ 3.6 V	0.8* VDDI	-	VDDI	2,3
Input low voltage	V_{IL}	V	VDDI = 1.65V ~ 3.6 V	– 0.3V	-	0.2* VDDI	2,3
Output high voltage (D0-17 pins, FMARK)	V_{OH}	V	IOH = -0.1mA	0.8 * VDDI	-	-	2
Output low voltage (D0-17 pins, FMARK)	V_{OL}	V	VDDI = 1.65 ~ 3.6 V I_{OL} = 0.1mA	-	-	0.2* VDDI	2
I/O leak current	Ili	µA	Vin = 0 ~ VDDI	-1	-	1	4
Current consumption during normal operation (VCI-VSSA)+(VDDI-GND)	IOP(VCI)	mA	VDDI=VCI=2.8V, Ta=25C, Fosc=45MHZ(320 Line)GRAM data =0000h, Frame rate=70HZ, REV=0, SAP=100,AP=100,DC0 =000,DC1=010,B/C=0, VC=001,VRH=0011, VCM=10011,VDV=100 00,VCOMG=1,CL=0, NO panel load	-	TBD	-	
Current consumption during standby operation (VCI-VSSA)+(VDDI-GND)	IOP(VCI)	µA		-	45		5,6

Notes:

1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI within the electrical characteristics conditions in normal operation. Exposure to a condition not within the electrical characteristics may affect reliability of the device.
2. Make sure VCI (high) ≥ GND (low) and VDDI (high) ≥ GND (low).
3. Make sure VCI (high) ≥ VSSA (low).
4. Make sure VSP (high) ≥ VSSA (low).
5. Make sure VSP (high) ≥ VGL (low).
6. Make sure VGH (high) ≥ VSSA (low).
7. Make sure VSSA (high) ≥ VGL (low).
8. The DC/AC characteristics of die and wafer products are guaranteed at 85 ºC.

10.3 AC Characteristics

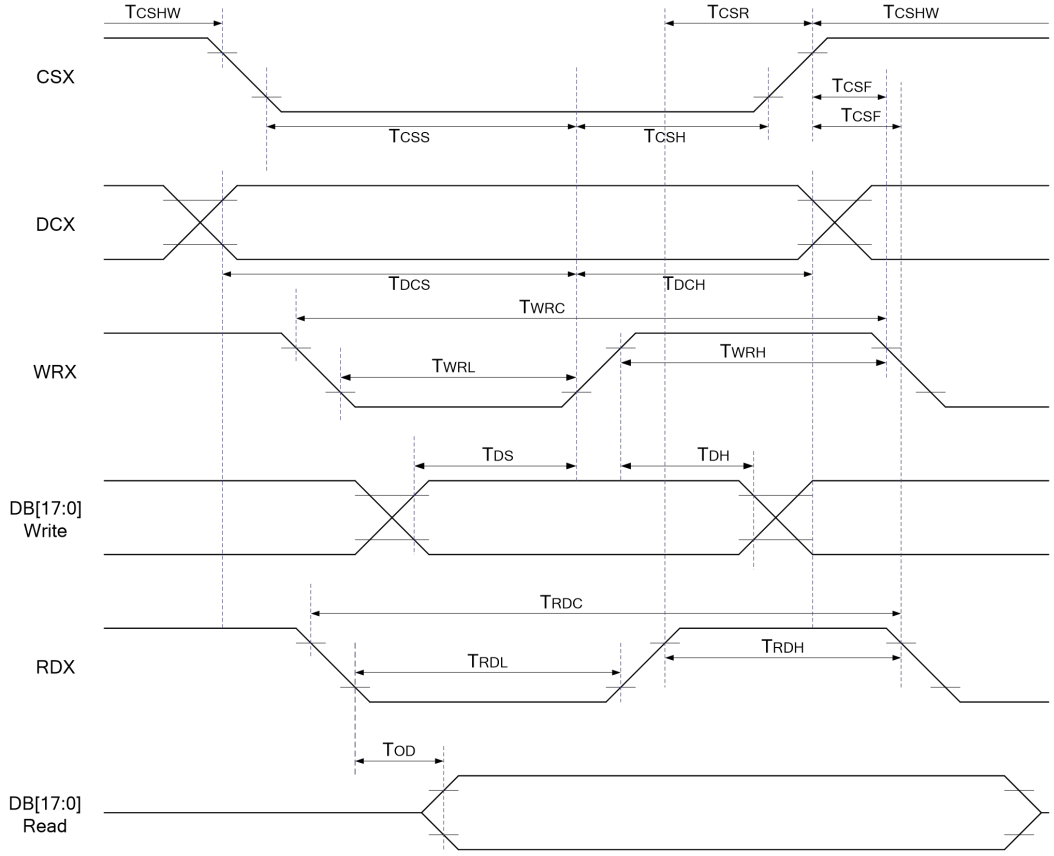
10.3.1 Serial Interface Timing Characteristics (3/4-wire SPI system)



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	CSX setup time	7.7	-	ns	Write
	T_{CSH}	CSX hold time	7.7	-	ns	
	T_{CSHW}	CSX high level width	15.4	-	ns	
	T_{CSS}	CSX setup time	40	-	ns	Read
	T_{CSH}	CSX hold time	40	-	ns	
	T_{CSHW}	CSX high level width	80	-	ns	
SCL	T_{SCLCW}	SCL cycle(Write)	15.4	-	ns	Write
	T_{SCLSW}	SCL low pulse duration(Write)	6.16	-	ns	
	T_{SCLHW}	SCL high pulse duration(Write)	6.16	-	ns	
	T_{SCLCR}	SCL cycle(Read)	80	-	ns	Read
	T_{SCLSR}	SCL low pulse duration(Read)	32	-	ns	
	T_{SCLHR}	SCL high pulse duration(Read)	32	-	ns	
SDA/ SDI2/ DCX	T_{DS}	SDA/SDI2/DCX setup time	6.16	-	ns	Write
	T_{DH}	SDA/SDI2/DCX hold time	6.16	-	ns	
SDO	T_{OD}	Read data output dealy	-	24	ns	Read

Note: Ta=-30℃~70℃, VDDI=1.65V to 3.6V, VCI=2.5V to 3.4V, VSSA=VSSD=0V.

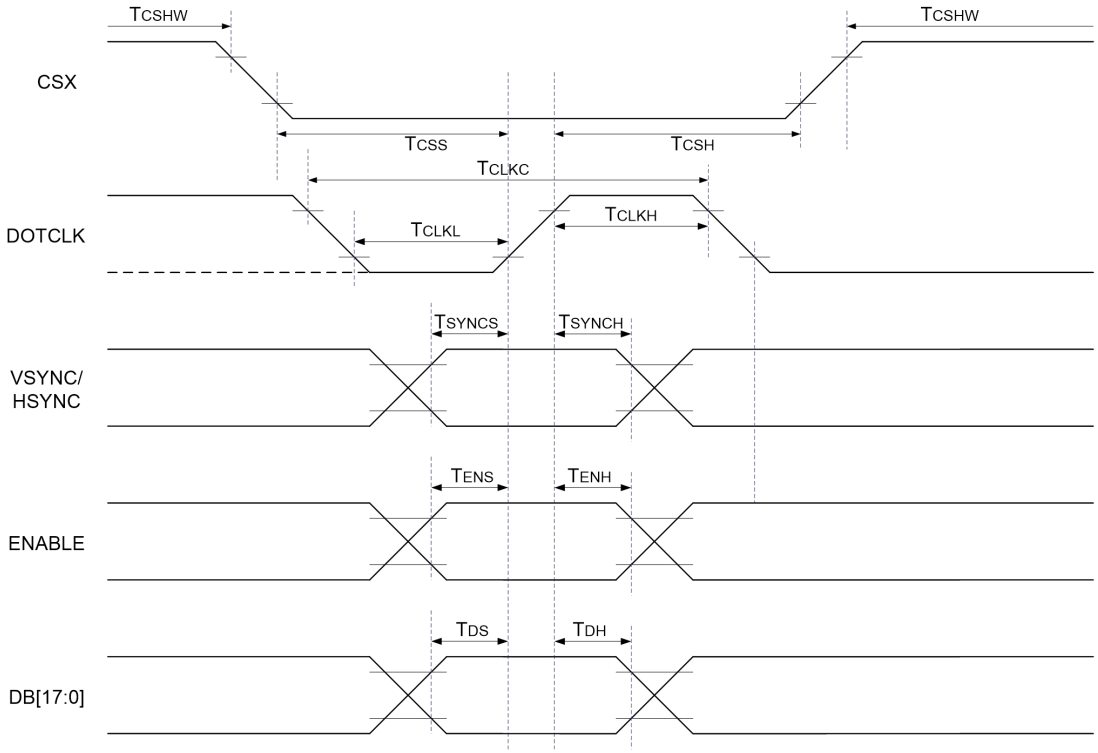
10.3.2 Parallel Interface Timing Characteristics(8080 series 8/9/16/18-Bit Parallel Interface)



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	CSX setup time	15	-	ns	
	T_{CSH}	CSX hold time	15	-	ns	
	T_{CSF}	CSX falling edge before WRX/RDX falling edge	10	-	ns	
	T_{CSHW}	CSX high level width	0	-	ns	
	T_{CSR}	CSX rising edge after RDX rising edge	0	-	ns	
DCX	T_{DCS}	DCX setup time	10	-	ns	
	T_{DCH}	DCX hold time	10	-	ns	
WRX	T_{WRC}	WRX cycle	30	-	ns	
	T_{WRL}	WRX low pulse duration	10	-	ns	
	T_{WRH}	WRX high pulse duration	10	-	ns	
DB[17:0]	T_{DS}	Write data setup time	10	-	ns	Write
	T_{DH}	Write data hold time	10	-	ns	
RDX	T_{RDC}	RDX cycle	160	-	ns	
	T_{RDL}	RDX low pulse duration	48	-	ns	
	T_{RDH}	RDX high pulse duration	48	-	ns	
DB[17:0]	T_{OD}	Read data output delay	-	30	ns	Read

Note: Ta=-30℃~70℃, VDDI=1.65V to 3.6V, VCI=2.5V to 3.4V, VSSA=VSSD=0V.

10.3.3 RGB Interface Timing Characteristics



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	CSX setup time	16	-	ns	
	T_{CSH}	CSX hold time	16	-	ns	
	T_{CSHW}	CSX high level width	0	-	ns	
DOTCLK	T_{CLKC}	DOTCLK cycle	40	-	ns	
	T_{CLKL}	DOTCLK low pulse duration	16	-	ns	
	T_{CLKH}	DOTCLK high pulse duration	16	-	ns	
HSYNC/ VSYNC	T_{SYNCS}	HSYNC/VSYNC setup time	16	-	ns	
	T_{SYNCH}	HSYNC/VSYNC hold time	16	-	ns	
ENABLE	T_{ENS}	ENABLE setup time	16	-	ns	
	T_{ENH}	ENABLE hold time	16	-	ns	
DB[17:0]	T_{DS}	RGB data setup time	16	-	ns	
	T_{DH}	RGB data hold time	16	-	ns	

Note: Ta=-30℃~70℃, VDDI=1.65V to 3.6V, VCI=2.5V to 3.4V, VSSA=VSSD=0V.

Revision history

Version No.	Date	Page	Introduction
0.1	2021-5-24	All	New build.
0.5	2021-08-24	All	Modify VCI range
0.6	2022-01-10	All	NV3030B