DATA SHEET

NV3030A

240RGB x 320dot, 262,144-color

TFT Controller Driver with Internal RAM

Version 0.3

Jan 8, 2021

Contents

1. Introduction

NV3030A is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

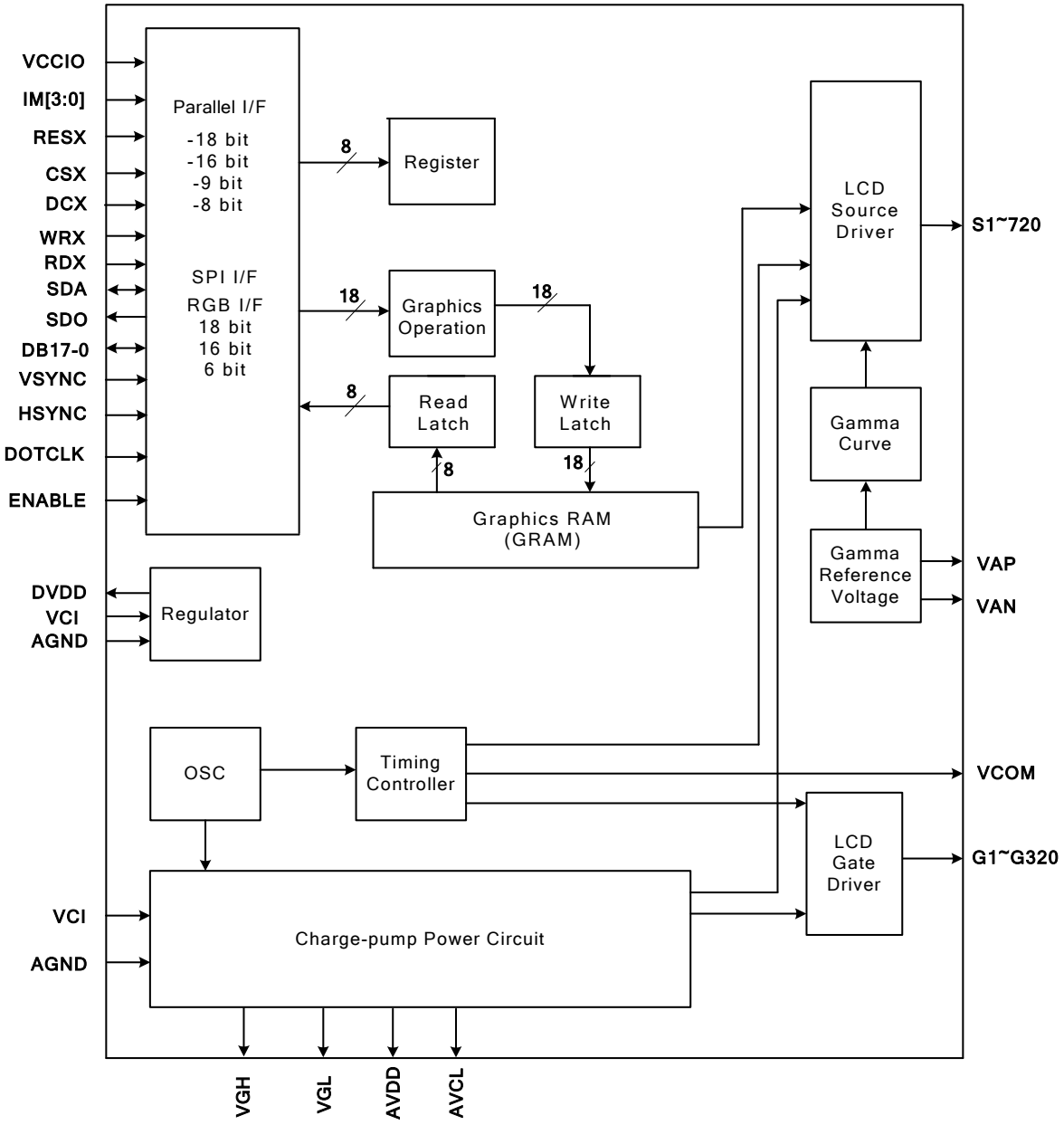
NV3030A supports 8-/9-/16-/18-bit data bus parallel interface, 6-/16-/18-bit data bus RGB interface and 3-/4-wire serial peripheral interface (SPI) and Quad serial peripheral interface (QSPI) . The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

NV3030A can operate with 1.65V ~ 3.6V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. NV3030A supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the NV3030A an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- One-chip controller driver for 240RGB x 320 dot graphics display in 262,144 colors on TFT panel
- One-chip solution for a-Si TFT panel
- System interface
  - 8-, 9-, 16-, 18-bit parallel ports
  - 3-/4-wire serial peripheral interface
  - Quad
- Moving picture display interface
  - RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0) via 6-, 16-, 18-bit ports
- Window address function to specify a rectangular area in the internal RAM to write data
  - Writes data within a rectangular area on the internal RAM via moving picture interface
  - Reduces data transfer by specifying the area on the RAM to rewrite data
  - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
- Display Colors (Color Mode)
  - Full Color:262K, RGB=(666)max.,Idle Mode Off
  - Color Reduce: 8-color, RGB=(111),Idle Mode On
- Low–power consumption architecture (allowing direct input of interface I/O power supply)
  - 8-color display function
  - Input power supply voltages: VDDI = 1.65V ~ 3.6V(interface I/O power supply)
    VCI = 2.5V ~ 3.3 V (liquid crystal analog circuit power supply)
- Driving Algorithm
  - Dot Inversion
  - Column Inversion
- On-Chip Power System
  - Source Voltage (VAP to VAN): +6.4~ -4.6V
  - VCOM level: GND
  - Gate driver HIGH level (VGH to VSSA): +13.3V ~ +16V
  - Gate driver LOW level (VGL to VSSA): -10.2V ~ -7.9V
- Internal liquid crystal drive circuit: 720-channel source output and 320-channel gate output
- Internal oscillator, Hardware and software Reset
- TFT storage capacitor: Cst only
- Don't need any external capacitor
- Optimized layout for COG Assembly

3. Block Diagram



4. Pin Function

4.1 Power Supply Pins

Signal	I/O	Connect to	Function
VDDI	I	I/O voltage	Low voltage power supply for interface logic circuits. (1.65~3.6V).
VCI	I	Analog Power	High voltage power supply for analog circuit blocks. Connect to an external power supply of 2.5V ~ 3.3V.
VSSD	I	Logic Ground	System ground level for logic blocks.
VSSA	I	Analog Ground	System ground level for analog circuit blocks. Connect to GND on the FPC to prevent noise.
VSP_EXT	O	-	Source driver power supply.
VSN_EXT	O	-	Source driver power supply.
VGH	O	-	Gate driver positive power supply.
VGL	O	-	Gate driver negative power supply.
VDD	O	-	Digital circuit power pad.
VAP	O	-	A power output of grayscale voltage generator.
VAN	O	-	A power output (Negative) of grayscale voltage generator.
VCMP	O	-	A power output of grayscale voltage generator.
VDDS_EXT	O	-	Source driver power supply.

4.2 Interface Logic Pins

<table>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>
Select the system interface mode.
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">interface Mode</th><th colspan="2">DB pins</th></tr>
<tr><th>Register</th><th>Gram</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>i80-system
8-bit interface I</td><td>DB[7:0]</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>i80-system
16-bit interface I</td><td>DB[7:0]</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>i80-system
9-bit interface I</td><td>DB[7:0]</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>i80-system
18-bit interface I</td><td>DB[7:0]</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>qspi</td><td colspan="2">DB[7:0]
DB[17:0]</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-wire 9-bit data
Serial interface I</td><td colspan="2" rowspan="2">SDA/WRX/DB[0]/DB[1]:
in/out</td></tr>
<tr><td>2 data lane serial
interface</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data
Serial interface I</td><td colspan="2">SDA: in/out</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>i80-system
16-bit interface
II</td><td>DB[8:1]</td><td>DB[8:1],
DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>i80-system
8-bit interface II</td><td>DB[17:10]</td><td>DB[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>i80-system
18-bit interface
II</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>i80-system
9-bit interface II</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data
Serial interface
II</td><td colspan="2">SDA: in
SDO: out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data
Serial interface
II</td><td colspan="2">SDA: in
SDO: out</td></tr>
</table>
If pad not used, please fix this pin to VDDI or VSSD level.
</td></tr>
</table>

RESX	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
CSX	I	A chip select signal. Low: the NV3030A is selected and accessible. High: the NV3030A is not selected and not accessible.
DCX	I	This pin is used to select “Data or Command” in the parallel interface. When DCX = ’1’, data is selected. When DCX = ’0’, command is selected. This pin is used serial interface clock. If not used, this pin should be connected to VDDI or VSSD.
WRX	I	A write strobe signal and enables an operation to write data when the signal is low. Fix to either VDDI or VSSD level when not in use. SPI 4-wire system: Serves as command or parameter select. 2 data lane serial interface: the second data lane. QSPI interface: the second data pin
RDX	I	A read strobe signal and enables an operation to read out data when the signal is low. Fix to VDDI level in parallel I/F when not in use. And fix to either VDDI or VSSD level in other I/F when not in use.
SDA	I/O	When serial I/F I: it is SPI interface input/output pin. When serial I/F Ⅱ: it is SPI interface input pin. The data is latched on the rising edge of the serial interface clock signal. If not used, please fix this pin at VDDI or VSSD level.
SDO	O	SPI interface output pin. The data is outputted on the falling edge of the serial interface clock signal. If not used, open this pin.
TE	O	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	Pixel clock signal in RGB I/F mode. If not used, fix this pin at VDDI or VSSD.
VSYNC	I	Vertical sync. Signal in RGB I/F mode. If not used, fix this pin at VDDI or VSSD.
HSYNC	I	Horizontal sync. Signal in RGB I/F mode. If not used, fix this pin at VDDI or VSSD.
ENABLE	I	Data enable signal in RGB I/F mode. If not used, fix this pin at VDDI or VSSD.
DB17-DB0	I/O	18-bit parallel bi-directional data bus for system interface and RGB interface mode. DB[0]:the third pin of qspi ; DB[1]:the fourth pin of qspi If not used, fix this pin at VDDI or VSSD.

OSC_SW	I	Input pin only for test.
MEC_BPS	I	Input pin only for test.

4.3 Driver Output Pins

Signal	I/O	Function
S1 to S720	O	Source driver output pads.
G1 to G320	O	Gate driver output pads.
VCOM	O	A power supply for the TFT-LCD common electrode.

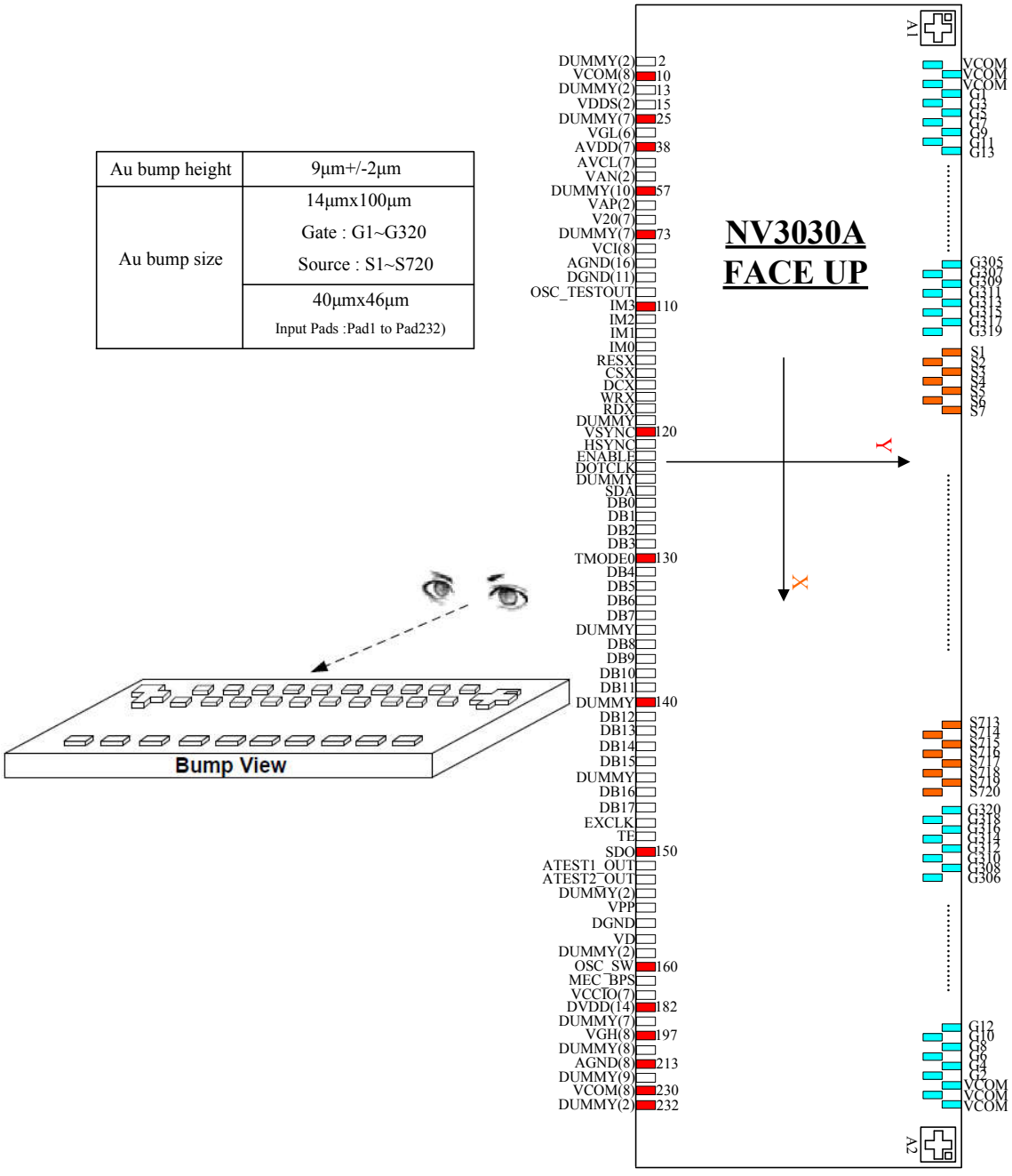
4.4 Test and other pins

Name	I/O	Description
VPP	I	OTP programming power.
BGOUT_TEST/ I_TEST/ VREF_TEST/ OSC_TESTOUT	O	Output pins for testing. Please keep these pins floating.
EXCLK	-	Dummy pin.Leave these pads open.
DMY_GDR/ DMY_GDL	-	These pins are dummy (no electrical characteristic) Can pass signal through these pads on TFT panel. Please open these pins.

5. Pad Arrangement

5.1 Output Bump Dimension

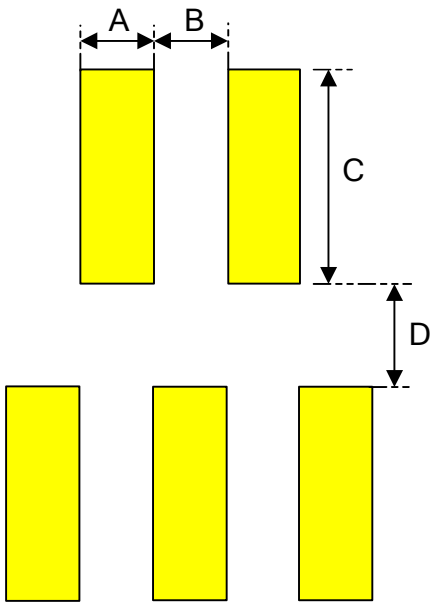
Au bump height	9μm+/-2μm
Au bump size	14μmx100μm Gate : G1~G320 Source : S1~S720
	40μmx46μm Input Pads :Pad1 to Pad232)



5.2 Input Bump Dimension

✧ **Output Pads**S1~S720、G1~G320、VCOM

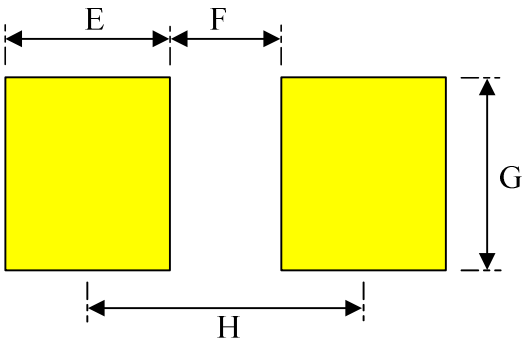
(No.233~1278)



Symbol	Item	Size
A	Bump Width	14um
B	Bump Gap 1 (Horizontal)	14um
C	Bump Height	100um
D	Bump Gap 2 (Vertical)	31um

✧ **Input Pads**

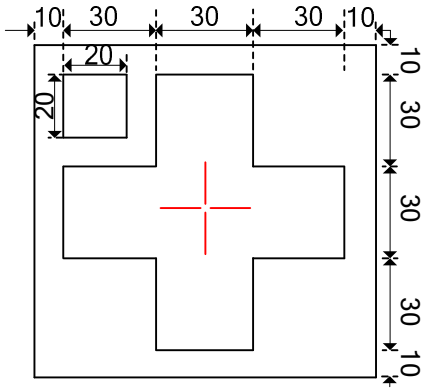
No.1~232



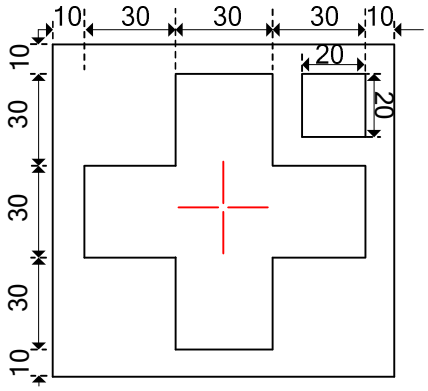
Symbol	Item	Size
E	Bump Width	40 um
F	Bump Gap	20,32.5,45 um
G	Bump Height	46 um
H	Bump Pitch	60,72.5,85 um

5.3 Alignment Mark Dimension

✧ Alignment Mark : A1(X,Y)=(-7480,225)



✧ Alignment Mark : A2(X,Y)=(7480,225)



5.4 Chip Information

Chip size	15300um x 585um
Chip thickness	280um
Pad Location	Pad center
Coordinate Origin	(-40,0)

6 PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	DUMMY	-7291.042	-259.5	38	VSP_EXT	-5071.486	-259.5
2	DUMMY	-7231.054	-259.5	39	VSN_EXT	-5011.498	-259.5
3	VCOM	-7171.066	-259.5	40	VSN_EXT	-4951.51	-259.5
4	VCOM	-7111.078	-259.5	41	VSN_EXT	-4891.522	-259.5
5	VCOM	-7051.09	-259.5	42	VSN_EXT	-4831.534	-259.5
6	VCOM	-6991.102	-259.5	43	VSN_EXT	-4771.546	-259.5
7	VCOM	-6931.114	-259.5	44	VSN_EXT	-4711.558	-259.5
8	VCOM	-6871.126	-259.5	45	VSN_EXT	-4651.57	-259.5
9	VCOM	-6811.138	-259.5	46	VAN	-4591.582	-259.5
10	VCOM	-6751.15	-259.5	47	VAN	-4531.594	-259.5
11	DUMMY	-6691.162	-259.5	48	DUMMY	-4471.606	-259.5
12	DUMMY	-6631.174	-259.5	49	DUMMY	-4411.618	-259.5
13	DUMMY	-6571.186	-259.5	50	BGOUT_TEST	-4351.63	-259.5
14	DUMMY	-6511.198	-259.5	51	BGOUT_TEST	-4291.642	-259.5
15	DUMMY	-6451.21	-259.5	52	DUMMY	-4231.654	-259.5
16	DUMMY	-6391.222	-259.5	53	VCMP	-4171.666	-259.5
17	DUMMY	-6331.234	-259.5	54	VCMP	-4111.678	-259.5
18	DUMMY	-6271.246	-259.5	55	DUMMY	-4051.69	-259.5
19	DUMMY	-6211.258	-259.5	56	DUMMY	-3991.702	-259.5
20	DUMMY	-6151.27	-259.5	57	DUMMY	-3931.714	-259.5
21	DUMMY	-6091.282	-259.5	58	VAP	-3871.726	-259.5
22	DUMMY	-6031.294	-259.5	59	VAP	-3811.738	-259.5
23	DUMMY	-5971.306	-259.5	60	VREF_TEST	-3751.75	-259.5
24	DUMMY	-5911.318	-259.5	61	VREF_TEST	-3691.762	-259.5
25	DUMMY	-5851.33	-259.5	62	DUMMY	-3631.774	-259.5
26	VGL	-5791.342	-259.5	63	DUMMY	-3571.786	-259.5
27	VGL	-5731.354	-259.5	64	VDDS_EXT	-3511.798	-259.5
28	VGL	-5671.366	-259.5	65	VDDS_EXT	-3451.81	-259.5
29	VGL	-5611.378	-259.5	66	DUMMY	-3391.822	-259.5
30	VGL	-5551.39	-259.5	67	DUMMY	-3331.834	-259.5
31	VGL	-5491.402	-259.5	68	VPP	-3271.846	-259.5
32	VSP_EXT	-5431.414	-259.5	69	VPP	-3211.858	-259.5
33	VSP_EXT	-5371.426	-259.5	70	VPP	-3151.87	-259.5
34	VSP_EXT	-5311.438	-259.5	71	VPP	-3091.882	-259.5
35	VSP_EXT	-5251.45	-259.5	72	VPP	-3031.894	-259.5
36	VSP_EXT	-5191.462	-259.5	73	DUMMY	-2971.906	-259.5
37	VSP_EXT	-5131.474	-259.5	74	VCI	-2911.918	-259.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
75	VCI	-2851.93	-259.5	116	DCX	-392.422	-259.5
76	VCI	-2791.942	-259.5	117	WRX	-332.434	-259.5
77	VCI	-2731.954	-259.5	118	RDX	-272.446	-259.5
78	VCI	-2671.966	-259.5	119	DUMMY	-212.458	-259.5
79	VCI	-2611.978	-259.5	120	VSYNC	-152.47	-259.5
80	VCI	-2551.99	-259.5	121	HSYNC	-92.482	-259.5
81	VCI	-2492.002	-259.5	122	ENABLE	-32.494	-259.5
82	VSSA	-2432.014	-259.5	123	DOTCLK	27.495	-259.5
83	VSSA	-2372.026	-259.5	124	DMY<2>	87.483	-259.5
84	VSSA	-2312.038	-259.5	125	SDA	159.968	-259.5
85	VSSA	-2252.05	-259.5	126	DB<0>	244.951	-259.5
86	VSSA	-2192.062	-259.5	127	DB<1>	329.934	-259.5
87	VSSA	-2132.074	-259.5	128	DB<2>	414.917	-259.5
88	VSSA	-2072.086	-259.5	129	DB<3>	499.9	-259.5
89	VSSA	-2012.098	-259.5	130	DUMMY	572.386	-259.5
90	VSSA	-1952.11	-259.5	131	DB<4>	644.871	-259.5
91	VSSA	-1892.122	-259.5	132	DB<5>	729.854	-259.5
92	VSSA	-1832.134	-259.5	133	DB<6>	814.837	-259.5
93	VSSA	-1772.146	-259.5	134	DB<7>	899.82	-259.5
94	VSSA	-1712.158	-259.5	135	DMY<3>	972.306	-259.5
95	VSSA	-1652.17	-259.5	136	DB<8>	1044.791	-259.5
96	VSSA	-1592.182	-259.5	137	DB<9>	1129.774	-259.5
97	VSSA	-1532.194	-259.5	138	DB<10>	1214.757	-259.5
98	VSSD	-1472.206	-259.5	139	DB<11>	1299.74	-259.5
99	VSSD	-1412.218	-259.5	140	DMY<4>	1372.226	-259.5
100	VSSD	-1352.23	-259.5	141	DB<12>	1444.711	-259.5
101	VSSD	-1292.242	-259.5	142	DB<13>	1529.694	-259.5
102	VSSD	-1232.254	-259.5	143	DB<14>	1614.677	-259.5
103	VSSD	-1172.266	-259.5	144	DB<15>	1699.66	-259.5
104	VSSD	-1112.278	-259.5	145	DMY<5>	1772.146	-259.5
105	VSSD	-1052.29	-259.5	146	DB<16>	1844.631	-259.5
106	I_TEST	-992.302	-259.5	147	DB<17>	1929.614	-259.5
107	DMY<0>	-932.314	-259.5	148	EXCLK	2002.1	-259.5
108	DMY<1>	-872.326	-259.5	149	TE	2074.585	-259.5
109	OSC_TESTOUT	-812.338	-259.5	150	SDO	2159.568	-259.5
110	IM<3>	-752.35	-259.5	151	LED_PWM	2244.551	-259.5
111	IM<2>	-692.362	-259.5	152	LED_EN	2329.534	-259.5
112	IM<1>	-632.374	-259.5	153	DUMMY	2402.02	-259.5
113	IM<0>	-572.386	-259.5	154	DUMMY	2462.008	-259.5
114	RESX	-512.398	-259.5	155	DUMMY	2534.493	-259.5
115	CSX	-452.41	-259.5	156	DUMMY	2619.476	-259.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
157	DUMMY	2704.459	-259.5	201	DUMMY	5431.414	-259.5
158	DUMMY	2789.442	-259.5	202	DUMMY	5491.402	-259.5
159	DUMMY	2874.425	-259.5	203	DUMMY	5551.39	-259.5
160	OSC_SW	2959.408	-259.5	204	DUMMY	5611.378	-259.5
161	MEC_BPS	3031.894	-259.5	205	DUMMY	5671.366	-259.5
162	VDDI	3091.882	-259.5	206	VSSA	5731.354	-259.5
163	VDDI	3151.87	-259.5	207	VSSA	5791.342	-259.5
164	VDDI	3211.858	-259.5	208	VSSA	5851.33	-259.5
165	VDDI	3271.846	-259.5	209	VSSA	5911.318	-259.5
166	VDDI	3331.834	-259.5	210	VSSA	5971.306	-259.5
167	VDDI	3391.822	-259.5	211	VSSA	6031.294	-259.5
168	VDDI	3451.81	-259.5	212	VSSA	6091.282	-259.5
169	VDD	3511.798	-259.5	213	VSSA	6151.27	-259.5
170	VDD	3571.786	-259.5	214	DUMMY	6211.258	-259.5
171	VDD	3631.774	-259.5	215	DUMMY	6271.246	-259.5
172	VDD	3691.762	-259.5	216	DUMMY	6331.234	-259.5
173	VDD	3751.75	-259.5	217	DUMMY	6391.222	-259.5
174	VDD	3811.738	-259.5	218	DUMMY	6451.21	-259.5
175	VDD	3871.726	-259.5	219	DUMMY	6511.198	-259.5
176	VDD	3931.714	-259.5	220	DUMMY	6571.186	-259.5
177	VDD	3991.702	-259.5	221	DUMMY	6631.174	-259.5
178	VDD	4051.69	-259.5	222	DUMMY	6691.162	-259.5
179	VDD	4111.678	-259.5	223	VCOM	6751.15	-259.5
180	VDD	4171.666	-259.5	224	VCOM	6811.138	-259.5
181	VDD	4231.654	-259.5	225	VCOM	6871.126	-259.5
182	VDD	4291.642	-259.5	226	VCOM	6931.114	-259.5
183	DUMMY	4351.63	-259.5	227	VCOM	6991.102	-259.5
184	DUMMY	4411.618	-259.5	228	VCOM	7051.09	-259.5
185	DUMMY	4471.606	-259.5	229	VCOM	7111.078	-259.5
186	DUMMY	4531.594	-259.5	230	VCOM	7171.066	-259.5
187	DUMMY	4591.582	-259.5	231	DUMMY	7231.054	-259.5
188	DUMMY	4651.57	-259.5	232	DUMMY	7291.042	-259.5
189	DUMMY	4711.558	-259.5	233	G<18>	7243.464	101.5
190	VGH	4771.546	-259.5	234	G<14>	7271.458	101.5
191	VGH	4831.534	-259.5	235	G<10>	7299.452	101.5
192	VGH	4891.522	-259.5	236	G<6>	7327.446	101.5
193	VGH	4951.51	-259.5	237	G<2>	7355.44	101.5
194	VGH	5011.498	-259.5	238	DMY_GDR	7383.434	101.5
195	VGH	5071.486	-259.5	239	DMY_GDR	7369.437	232.5
196	VGH	5131.474	-259.5	240	DMY_GDR	7397.431	232.5
197	VGH	5191.462	-259.5	241	G<4>	7341.443	232.5
198	DUMMY	5251.45	-259.5	242	G<8>	7313.449	232.5
199	DUMMY	5311.438	-259.5	243	G<12>	7285.455	232.5
200	DUMMY	5371.426	-259.5	244	G<16>	7257.461	232.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
245	G<20>	7229.467	232.5	289	G<108>	6613.599	232.5
246	G<22>	7215.47	101.5	290	G<110>	6599.602	101.5
247	G<24>	7201.473	232.5	291	G<112>	6585.605	232.5
248	G<26>	7187.476	101.5	292	G<114>	6571.608	101.5
249	G<28>	7173.479	232.5	293	G<116>	6557.611	232.5
250	G<30>	7159.482	101.5	294	G<118>	6543.614	101.5
251	G<32>	7145.485	232.5	295	G<120>	6529.617	232.5
252	G<34>	7131.488	101.5	296	G<122>	6515.62	101.5
253	G<36>	7117.491	232.5	297	G<124>	6501.623	232.5
254	G<38>	7103.494	101.5	298	G<126>	6487.626	101.5
255	G<40>	7089.497	232.5	299	G<128>	6473.629	232.5
256	G<42>	7075.5	101.5	300	G<130>	6459.632	101.5
257	G<44>	7061.503	232.5	301	G<132>	6445.635	232.5
258	G<46>	7047.506	101.5	302	G<134>	6431.638	101.5
259	G<48>	7033.509	232.5	303	G<136>	6417.641	232.5
260	G<50>	7019.512	101.5	304	G<138>	6403.644	101.5
261	G<52>	7005.515	232.5	305	G<140>	6389.647	232.5
262	G<54>	6991.518	101.5	306	G<142>	6375.65	101.5
263	G<56>	6977.521	232.5	307	G<144>	6361.653	232.5
264	G<58>	6963.524	101.5	308	G<146>	6347.656	101.5
265	G<60>	6949.527	232.5	309	G<148>	6333.659	232.5
266	G<62>	6935.53	101.5	310	G<150>	6319.662	101.5
267	G<64>	6921.533	232.5	311	G<152>	6305.665	232.5
268	G<66>	6907.536	101.5	312	G<154>	6291.668	101.5
269	G<68>	6893.539	232.5	313	G<156>	6277.671	232.5
270	G<70>	6879.542	101.5	314	G<158>	6263.674	101.5
271	G<72>	6865.545	232.5	315	G<160>	6249.677	232.5
272	G<74>	6851.548	101.5	316	G<162>	6235.68	101.5
273	G<76>	6837.551	232.5	317	G<164>	6221.683	232.5
274	G<78>	6823.554	101.5	318	G<166>	6207.686	101.5
275	G<80>	6809.557	232.5	319	G<168>	6193.689	232.5
276	G<82>	6795.56	101.5	320	G<170>	6179.692	101.5
277	G<84>	6781.563	232.5	321	G<172>	6165.695	232.5
278	G<86>	6767.566	101.5	322	G<174>	6151.698	101.5
279	G<88>	6753.569	232.5	323	G<176>	6137.701	232.5
280	G<90>	6739.572	101.5	324	G<178>	6123.704	101.5
281	G<92>	6725.575	232.5	325	G<180>	6109.707	232.5
282	G<94>	6711.578	101.5	326	G<182>	6095.71	101.5
283	G<96>	6697.581	232.5	327	G<184>	6081.713	232.5
284	G<98>	6683.584	101.5	328	G<186>	6067.716	101.5
285	G<100>	6669.587	232.5	329	G<188>	6053.719	232.5
286	G<102>	6655.59	101.5	330	G<190>	6039.722	101.5
287	G<104>	6641.593	232.5	331	G<192>	6025.725	232.5
288	G<106>	6627.596	101.5	332	G<194>	6011.728	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
333	G<196>	5997.731	232.5	377	G<284>	5381.863	232.5
334	G<198>	5983.734	101.5	378	G<286>	5367.866	101.5
335	G<200>	5969.737	232.5	379	G<288>	5353.869	232.5
336	G<202>	5955.74	101.5	380	G<290>	5339.872	101.5
337	G<204>	5941.743	232.5	381	G<292>	5325.875	232.5
338	G<206>	5927.746	101.5	382	G<294>	5311.878	101.5
339	G<208>	5913.749	232.5	383	G<296>	5297.881	232.5
340	G<210>	5899.752	101.5	384	G<298>	5283.884	101.5
341	G<212>	5885.755	232.5	385	G<300>	5269.887	232.5
342	G<214>	5871.758	101.5	386	G<302>	5255.89	101.5
343	G<216>	5857.761	232.5	387	G<304>	5241.893	232.5
344	G<218>	5843.764	101.5	388	G<306>	5227.896	101.5
345	G<220>	5829.767	232.5	389	G<308>	5213.899	232.5
346	G<222>	5815.77	101.5	390	G<310>	5199.902	101.5
347	G<224>	5801.773	232.5	391	G<312>	5185.905	232.5
348	G<226>	5787.776	101.5	392	G<314>	5171.908	101.5
349	G<228>	5773.779	232.5	393	G<316>	5157.911	232.5
350	G<230>	5759.782	101.5	394	G<318>	5143.914	101.5
351	G<232>	5745.785	232.5	395	G<320>	5129.917	232.5
352	G<234>	5731.788	101.5	396	S<720>	5073.92	101.5
353	G<236>	5717.791	232.5	397	S<719>	5059.923	232.5
354	G<238>	5703.794	101.5	398	S<718>	5045.926	101.5
355	G<240>	5689.797	232.5	399	S<717>	5031.929	232.5
356	G<242>	5675.8	101.5	400	S<716>	5017.932	101.5
357	G<244>	5661.803	232.5	401	S<715>	5003.935	232.5
358	G<246>	5647.806	101.5	402	S<714>	4989.938	101.5
359	G<248>	5633.809	232.5	403	S<713>	4975.941	232.5
360	G<250>	5619.812	101.5	404	S<712>	4961.944	101.5
361	G<252>	5605.815	232.5	405	S<711>	4947.947	232.5
362	G<254>	5591.818	101.5	406	S<710>	4933.95	101.5
363	G<256>	5577.821	232.5	407	S<709>	4919.953	232.5
364	G<258>	5563.824	101.5	408	S<708>	4905.956	101.5
365	G<260>	5549.827	232.5	409	S<707>	4891.959	232.5
366	G<262>	5535.83	101.5	410	S<706>	4877.962	101.5
367	G<264>	5521.833	232.5	411	S<705>	4863.965	232.5
368	G<266>	5507.836	101.5	412	S<704>	4849.968	101.5
369	G<268>	5493.839	232.5	413	S<703>	4835.971	232.5
370	G<270>	5479.842	101.5	414	S<702>	4821.974	101.5
371	G<272>	5465.845	232.5	415	S<701>	4807.977	232.5
372	G<274>	5451.848	101.5	416	S<700>	4793.98	101.5
373	G<276>	5437.851	232.5	417	S<699>	4779.983	232.5
374	G<278>	5423.854	101.5	418	S<698>	4765.986	101.5
375	G<280>	5409.857	232.5	419	S<697>	4751.989	232.5
376	G<282>	5395.86	101.5	420	S<696>	4737.992	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
421	S<695>	4723.995	232.5	465	S<651>	4108.127	232.5
422	S<694>	4709.998	101.5	466	S<650>	4094.13	101.5
423	S<693>	4696.001	232.5	467	S<649>	4080.133	232.5
424	S<692>	4682.004	101.5	468	S<648>	4066.136	101.5
425	S<691>	4668.007	232.5	469	S<647>	4052.139	232.5
426	S<690>	4654.01	101.5	470	S<646>	4038.142	101.5
427	S<689>	4640.013	232.5	471	S<645>	4024.145	232.5
428	S<688>	4626.016	101.5	472	S<644>	4010.148	101.5
429	S<687>	4612.019	232.5	473	S<643>	3996.151	232.5
430	S<686>	4598.022	101.5	474	S<642>	3982.154	101.5
431	S<685>	4584.025	232.5	475	S<641>	3968.157	232.5
432	S<684>	4570.028	101.5	476	S<640>	3954.16	101.5
433	S<683>	4556.031	232.5	477	S<639>	3940.163	232.5
434	S<682>	4542.034	101.5	478	S<638>	3926.166	101.5
435	S<681>	4528.037	232.5	479	S<637>	3912.169	232.5
436	S<680>	4514.04	101.5	480	S<636>	3898.172	101.5
437	S<679>	4500.043	232.5	481	S<635>	3884.175	232.5
438	S<678>	4486.046	101.5	482	S<634>	3870.178	101.5
439	S<677>	4472.049	232.5	483	S<633>	3856.181	232.5
440	S<676>	4458.052	101.5	484	S<632>	3842.184	101.5
441	S<675>	4444.055	232.5	485	S<631>	3828.187	232.5
442	S<674>	4430.058	101.5	486	S<630>	3814.19	101.5
443	S<673>	4416.061	232.5	487	S<629>	3800.193	232.5
444	S<672>	4402.064	101.5	488	S<628>	3786.196	101.5
445	S<671>	4388.067	232.5	489	S<627>	3772.199	232.5
446	S<670>	4374.07	101.5	490	S<626>	3758.202	101.5
447	S<669>	4360.073	232.5	491	S<625>	3744.205	232.5
448	S<668>	4346.076	101.5	492	S<624>	3730.208	101.5
449	S<667>	4332.079	232.5	493	S<623>	3716.211	232.5
450	S<666>	4318.082	101.5	494	S<622>	3702.214	101.5
451	S<665>	4304.085	232.5	495	S<621>	3688.217	232.5
452	S<664>	4290.088	101.5	496	S<620>	3674.22	101.5
453	S<663>	4276.091	232.5	497	S<619>	3660.223	232.5
454	S<662>	4262.094	101.5	498	S<618>	3646.226	101.5
455	S<661>	4248.097	232.5	499	S<617>	3632.229	232.5
456	S<660>	4234.1	101.5	500	S<616>	3618.232	101.5
457	S<659>	4220.103	232.5	501	S<615>	3604.235	232.5
458	S<658>	4206.106	101.5	502	S<614>	3590.238	101.5
459	S<657>	4192.109	232.5	503	S<613>	3576.241	232.5
460	S<656>	4178.112	101.5	504	S<612>	3562.244	101.5
461	S<655>	4164.115	232.5	505	S<611>	3548.247	232.5
462	S<654>	4150.118	101.5	506	S<610>	3534.25	101.5
463	S<653>	4136.121	232.5	507	S<609>	3520.253	232.5
464	S<652>	4122.124	101.5	508	S<608>	3506.256	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
509	S<607>	3492.259	232.5	553	S<563>	2876.391	232.5
510	S<606>	3478.262	101.5	554	S<562>	2862.394	101.5
511	S<605>	3464.265	232.5	555	S<561>	2848.397	232.5
512	S<604>	3450.268	101.5	556	S<560>	2834.4	101.5
513	S<603>	3436.271	232.5	557	S<559>	2820.403	232.5
514	S<602>	3422.274	101.5	558	S<558>	2806.406	101.5
515	S<601>	3408.277	232.5	559	S<557>	2792.409	232.5
516	S<600>	3394.28	101.5	560	S<556>	2778.412	101.5
517	S<599>	3380.283	232.5	561	S<555>	2764.415	232.5
518	S<598>	3366.286	101.5	562	S<554>	2750.418	101.5
519	S<597>	3352.289	232.5	563	S<553>	2736.421	232.5
520	S<596>	3338.292	101.5	564	S<552>	2722.424	101.5
521	S<595>	3324.295	232.5	565	S<551>	2708.427	232.5
522	S<594>	3310.298	101.5	566	S<550>	2694.43	101.5
523	S<593>	3296.301	232.5	567	S<549>	2680.433	232.5
524	S<592>	3282.304	101.5	568	S<548>	2666.436	101.5
525	S<591>	3268.307	232.5	569	S<547>	2652.439	232.5
526	S<590>	3254.31	101.5	570	S<546>	2638.442	101.5
527	S<589>	3240.313	232.5	571	S<545>	2624.445	232.5
528	S<588>	3226.316	101.5	572	S<544>	2610.448	101.5
529	S<587>	3212.319	232.5	573	S<543>	2596.451	232.5
530	S<586>	3198.322	101.5	574	S<542>	2582.454	101.5
531	S<585>	3184.325	232.5	575	S<541>	2568.457	232.5
532	S<584>	3170.328	101.5	576	S<540>	2554.46	101.5
533	S<583>	3156.331	232.5	577	S<539>	2540.463	232.5
534	S<582>	3142.334	101.5	578	S<538>	2526.466	101.5
535	S<581>	3128.337	232.5	579	S<537>	2512.469	232.5
536	S<580>	3114.34	101.5	580	S<536>	2498.472	101.5
537	S<579>	3100.343	232.5	581	S<535>	2484.475	232.5
538	S<578>	3086.346	101.5	582	S<534>	2470.478	101.5
539	S<577>	3072.349	232.5	583	S<533>	2456.481	232.5
540	S<576>	3058.352	101.5	584	S<532>	2442.484	101.5
541	S<575>	3044.355	232.5	585	S<531>	2428.487	232.5
542	S<574>	3030.358	101.5	586	S<530>	2414.49	101.5
543	S<573>	3016.361	232.5	587	S<529>	2400.493	232.5
544	S<572>	3002.364	101.5	588	S<528>	2386.496	101.5
545	S<571>	2988.367	232.5	589	S<527>	2372.499	232.5
546	S<570>	2974.37	101.5	590	S<526>	2358.502	101.5
547	S<569>	2960.373	232.5	591	S<525>	2344.505	232.5
548	S<568>	2946.376	101.5	592	S<524>	2330.508	101.5
549	S<567>	2932.379	232.5	593	S<523>	2316.511	232.5
550	S<566>	2918.382	101.5	594	S<522>	2302.514	101.5
551	S<565>	2904.385	232.5	595	S<521>	2288.517	232.5
552	S<564>	2890.388	101.5	596	S<520>	2274.52	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
597	S<519>	2260.523	232.5	641	S<475>	1644.655	232.5
598	S<518>	2246.526	101.5	642	S<474>	1630.658	101.5
599	S<517>	2232.529	232.5	643	S<473>	1616.661	232.5
600	S<516>	2218.532	101.5	644	S<472>	1602.664	101.5
601	S<515>	2204.535	232.5	645	S<471>	1588.667	232.5
602	S<514>	2190.538	101.5	646	S<470>	1574.67	101.5
603	S<513>	2176.541	232.5	647	S<469>	1560.673	232.5
604	S<512>	2162.544	101.5	648	S<468>	1546.676	101.5
605	S<511>	2148.547	232.5	649	S<467>	1532.679	232.5
606	S<510>	2134.55	101.5	650	S<466>	1518.682	101.5
607	S<509>	2120.553	232.5	651	S<465>	1504.685	232.5
608	S<508>	2106.556	101.5	652	S<464>	1490.688	101.5
609	S<507>	2092.559	232.5	653	S<463>	1476.691	232.5
610	S<506>	2078.562	101.5	654	S<462>	1462.694	101.5
611	S<505>	2064.565	232.5	655	S<461>	1448.697	232.5
612	S<504>	2050.568	101.5	656	S<460>	1434.7	101.5
613	S<503>	2036.571	232.5	657	S<459>	1420.703	232.5
614	S<502>	2022.574	101.5	658	S<458>	1406.706	101.5
615	S<501>	2008.577	232.5	659	S<457>	1392.709	232.5
616	S<500>	1994.58	101.5	660	S<456>	1378.712	101.5
617	S<499>	1980.583	232.5	661	S<455>	1364.715	232.5
618	S<498>	1966.586	101.5	662	S<454>	1350.718	101.5
619	S<497>	1952.589	232.5	663	S<453>	1336.721	232.5
620	S<496>	1938.592	101.5	664	S<452>	1322.724	101.5
621	S<495>	1924.595	232.5	665	S<451>	1308.727	232.5
622	S<494>	1910.598	101.5	666	S<450>	1294.73	101.5
623	S<493>	1896.601	232.5	667	S<449>	1280.733	232.5
624	S<492>	1882.604	101.5	668	S<448>	1266.736	101.5
625	S<491>	1868.607	232.5	669	S<447>	1252.739	232.5
626	S<490>	1854.61	101.5	670	S<446>	1238.742	101.5
627	S<489>	1840.613	232.5	671	S<445>	1224.745	232.5
628	S<488>	1826.616	101.5	672	S<444>	1210.748	101.5
629	S<487>	1812.619	232.5	673	S<443>	1196.751	232.5
630	S<486>	1798.622	101.5	674	S<442>	1182.754	101.5
631	S<485>	1784.625	232.5	675	S<441>	1168.757	232.5
632	S<484>	1770.628	101.5	676	S<440>	1154.76	101.5
633	S<483>	1756.631	232.5	677	S<439>	1140.763	232.5
634	S<482>	1742.634	101.5	678	S<438>	1126.766	101.5
635	S<481>	1728.637	232.5	679	S<437>	1112.769	232.5
636	S<480>	1714.64	101.5	680	S<436>	1098.772	101.5
637	S<479>	1700.643	232.5	681	S<435>	1084.775	232.5
638	S<478>	1686.646	101.5	682	S<434>	1070.778	101.5
639	S<477>	1672.649	232.5	683	S<433>	1056.781	232.5
640	S<476>	1658.652	101.5	684	S<432>	1042.784	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
685	S<431>	1028.787	232.5	729	S<387>	412.917	232.5
686	S<430>	1014.79	101.5	730	S<386>	398.92	101.5
687	S<429>	1000.793	232.5	731	S<385>	384.923	232.5
688	S<428>	986.796	101.5	732	S<384>	370.926	101.5
689	S<427>	972.799	232.5	733	S<383>	356.929	232.5
690	S<426>	958.802	101.5	734	S<382>	342.931	101.5
691	S<425>	944.805	232.5	735	S<381>	328.934	232.5
692	S<424>	930.808	101.5	736	S<380>	314.937	101.5
693	S<423>	916.811	232.5	737	S<379>	300.94	232.5
694	S<422>	902.814	101.5	738	S<378>	286.943	101.5
695	S<421>	888.817	232.5	739	S<377>	272.945	232.5
696	S<420>	874.82	101.5	740	S<376>	258.948	101.5
697	S<419>	860.823	232.5	741	S<375>	244.951	232.5
698	S<418>	846.826	101.5	742	S<374>	230.954	101.5
699	S<417>	832.829	232.5	743	S<373>	216.957	232.5
700	S<416>	818.832	101.5	744	S<372>	202.959	101.5
701	S<415>	804.835	232.5	745	S<371>	188.962	232.5
702	S<414>	790.838	101.5	746	S<370>	174.965	101.5
703	S<413>	776.841	232.5	747	S<369>	160.968	232.5
704	S<412>	762.844	101.5	748	S<368>	146.971	101.5
705	S<411>	748.847	232.5	749	S<367>	132.973	232.5
706	S<410>	734.85	101.5	750	S<366>	118.976	101.5
707	S<409>	720.853	232.5	751	S<365>	104.979	232.5
708	S<408>	706.856	101.5	752	S<364>	90.982	101.5
709	S<407>	692.859	232.5	753	S<363>	76.985	232.5
710	S<406>	678.862	101.5	754	S<362>	62.987	101.5
711	S<405>	664.865	232.5	755	S<361>	48.99	232.5
712	S<404>	650.868	101.5	756	S<360>	-48.99	101.5
713	S<403>	636.871	232.5	757	S<359>	-62.987	232.5
714	S<402>	622.874	101.5	758	S<358>	-76.985	101.5
715	S<401>	608.877	232.5	759	S<357>	-90.982	232.5
716	S<400>	594.88	101.5	760	S<356>	-104.979	101.5
717	S<399>	580.883	232.5	761	S<355>	-118.976	232.5
718	S<398>	566.886	101.5	762	S<354>	-132.973	101.5
719	S<397>	552.889	232.5	763	S<353>	-146.971	232.5
720	S<396>	538.892	101.5	764	S<352>	-160.968	101.5
721	S<395>	524.895	232.5	765	S<351>	-174.965	232.5
722	S<394>	510.898	101.5	766	S<350>	-188.962	101.5
723	S<393>	496.901	232.5	767	S<349>	-202.959	232.5
724	S<392>	482.903	101.5	768	S<348>	-216.957	101.5
725	S<391>	468.906	232.5	769	S<347>	-230.954	232.5
726	S<390>	454.909	101.5	770	S<346>	-244.951	101.5
727	S<389>	440.912	232.5	771	S<345>	-258.948	232.5
728	S<388>	426.915	101.5	772	S<344>	-272.945	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
773	S<343>	-286.943	232.5	817	S<299>	-902.814	232.5
774	S<342>	-300.94	101.5	818	S<298>	-916.811	101.5
775	S<341>	-314.937	232.5	819	S<297>	-930.808	232.5
776	S<340>	-328.934	101.5	820	S<296>	-944.805	101.5
777	S<339>	-342.931	232.5	821	S<295>	-958.802	232.5
778	S<338>	-356.929	101.5	822	S<294>	-972.799	101.5
779	S<337>	-370.926	232.5	823	S<293>	-986.796	232.5
780	S<336>	-384.923	101.5	824	S<292>	-1000.793	101.5
781	S<335>	-398.92	232.5	825	S<291>	-1014.79	232.5
782	S<334>	-412.917	101.5	826	S<290>	-1028.787	101.5
783	S<333>	-426.915	232.5	827	S<289>	-1042.784	232.5
784	S<332>	-440.912	101.5	828	S<288>	-1056.781	101.5
785	S<331>	-454.909	232.5	829	S<287>	-1070.778	232.5
786	S<330>	-468.906	101.5	830	S<286>	-1084.775	101.5
787	S<329>	-482.903	232.5	831	S<285>	-1098.772	232.5
788	S<328>	-496.901	101.5	832	S<284>	-1112.769	101.5
789	S<327>	-510.898	232.5	833	S<283>	-1126.766	232.5
790	S<326>	-524.895	101.5	834	S<282>	-1140.763	101.5
791	S<325>	-538.892	232.5	835	S<281>	-1154.76	232.5
792	S<324>	-552.889	101.5	836	S<280>	-1168.757	101.5
793	S<323>	-566.886	232.5	837	S<279>	-1182.754	232.5
794	S<322>	-580.883	101.5	838	S<278>	-1196.751	101.5
795	S<321>	-594.88	232.5	839	S<277>	-1210.748	232.5
796	S<320>	-608.877	101.5	840	S<276>	-1224.745	101.5
797	S<319>	-622.874	232.5	841	S<275>	-1238.742	232.5
798	S<318>	-636.871	101.5	842	S<274>	-1252.739	101.5
799	S<317>	-650.868	232.5	843	S<273>	-1266.736	232.5
800	S<316>	-664.865	101.5	844	S<272>	-1280.733	101.5
801	S<315>	-678.862	232.5	845	S<271>	-1294.73	232.5
802	S<314>	-692.859	101.5	846	S<270>	-1308.727	101.5
803	S<313>	-706.856	232.5	847	S<269>	-1322.724	232.5
804	S<312>	-720.853	101.5	848	S<268>	-1336.721	101.5
805	S<311>	-734.85	232.5	849	S<267>	-1350.718	232.5
806	S<310>	-748.847	101.5	850	S<266>	-1364.715	101.5
807	S<309>	-762.844	232.5	851	S<265>	-1378.712	232.5
808	S<308>	-776.841	101.5	852	S<264>	-1392.709	101.5
809	S<307>	-790.838	232.5	853	S<263>	-1406.706	232.5
810	S<306>	-804.835	101.5	854	S<262>	-1420.703	101.5
811	S<305>	-818.832	232.5	855	S<261>	-1434.7	232.5
812	S<304>	-832.829	101.5	856	S<260>	-1448.697	101.5
813	S<303>	-846.826	232.5	857	S<259>	-1462.694	232.5
814	S<302>	-860.823	101.5	858	S<258>	-1476.691	101.5
815	S<301>	-874.82	232.5	859	S<257>	-1490.688	232.5
816	S<300>	-888.817	101.5	860	S<256>	-1504.685	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
861	S<255>	-1518.682	232.5	905	S<211>	-2134.55	232.5
862	S<254>	-1532.679	101.5	906	S<210>	-2148.547	101.5
863	S<253>	-1546.676	232.5	907	S<209>	-2162.544	232.5
864	S<252>	-1560.673	101.5	908	S<208>	-2176.541	101.5
865	S<251>	-1574.67	232.5	909	S<207>	-2190.538	232.5
866	S<250>	-1588.667	101.5	910	S<206>	-2204.535	101.5
867	S<249>	-1602.664	232.5	911	S<205>	-2218.532	232.5
868	S<248>	-1616.661	101.5	912	S<204>	-2232.529	101.5
869	S<247>	-1630.658	232.5	913	S<203>	-2246.526	232.5
870	S<246>	-1644.655	101.5	914	S<202>	-2260.523	101.5
871	S<245>	-1658.652	232.5	915	S<201>	-2274.52	232.5
872	S<244>	-1672.649	101.5	916	S<200>	-2288.517	101.5
873	S<243>	-1686.646	232.5	917	S<199>	-2302.514	232.5
874	S<242>	-1700.643	101.5	918	S<198>	-2316.511	101.5
875	S<241>	-1714.64	232.5	919	S<197>	-2330.508	232.5
876	S<240>	-1728.637	101.5	920	S<196>	-2344.505	101.5
877	S<239>	-1742.634	232.5	921	S<195>	-2358.502	232.5
878	S<238>	-1756.631	101.5	922	S<194>	-2372.499	101.5
879	S<237>	-1770.628	232.5	923	S<193>	-2386.496	232.5
880	S<236>	-1784.625	101.5	924	S<192>	-2400.493	101.5
881	S<235>	-1798.622	232.5	925	S<191>	-2414.49	232.5
882	S<234>	-1812.619	101.5	926	S<190>	-2428.487	101.5
883	S<233>	-1826.616	232.5	927	S<189>	-2442.484	232.5
884	S<232>	-1840.613	101.5	928	S<188>	-2456.481	101.5
885	S<231>	-1854.61	232.5	929	S<187>	-2470.478	232.5
886	S<230>	-1868.607	101.5	930	S<186>	-2484.475	101.5
887	S<229>	-1882.604	232.5	931	S<185>	-2498.472	232.5
888	S<228>	-1896.601	101.5	932	S<184>	-2512.469	101.5
889	S<227>	-1910.598	232.5	933	S<183>	-2526.466	232.5
890	S<226>	-1924.595	101.5	934	S<182>	-2540.463	101.5
891	S<225>	-1938.592	232.5	935	S<181>	-2554.46	232.5
892	S<224>	-1952.589	101.5	936	S<180>	-2568.457	101.5
893	S<223>	-1966.586	232.5	937	S<179>	-2582.454	232.5
894	S<222>	-1980.583	101.5	938	S<178>	-2596.451	101.5
895	S<221>	-1994.58	232.5	939	S<177>	-2610.448	232.5
896	S<220>	-2008.577	101.5	940	S<176>	-2624.445	101.5
897	S<219>	-2022.574	232.5	941	S<175>	-2638.442	232.5
898	S<218>	-2036.571	101.5	942	S<174>	-2652.439	101.5
899	S<217>	-2050.568	232.5	943	S<173>	-2666.436	232.5
900	S<216>	-2064.565	101.5	944	S<172>	-2680.433	101.5
901	S<215>	-2078.562	232.5	945	S<171>	-2694.43	232.5
902	S<214>	-2092.559	101.5	946	S<170>	-2708.427	101.5
903	S<213>	-2106.556	232.5	947	S<169>	-2722.424	232.5
904	S<212>	-2120.553	101.5	948	S<168>	-2736.421	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
949	S<167>	-2750.418	232.5	993	S<123>	-3366.286	232.5
950	S<166>	-2764.415	101.5	994	S<122>	-3380.283	101.5
951	S<165>	-2778.412	232.5	995	S<121>	-3394.28	232.5
952	S<164>	-2792.409	101.5	996	S<120>	-3408.277	101.5
953	S<163>	-2806.406	232.5	997	S<119>	-3422.274	232.5
954	S<162>	-2820.403	101.5	998	S<118>	-3436.271	101.5
955	S<161>	-2834.4	232.5	999	S<117>	-3450.268	232.5
956	S<160>	-2848.397	101.5	1000	S<116>	-3464.265	101.5
957	S<159>	-2862.394	232.5	1001	S<115>	-3478.262	232.5
958	S<158>	-2876.391	101.5	1002	S<114>	-3492.259	101.5
959	S<157>	-2890.388	232.5	1003	S<113>	-3506.256	232.5
960	S<156>	-2904.385	101.5	1004	S<112>	-3520.253	101.5
961	S<155>	-2918.382	232.5	1005	S<111>	-3534.25	232.5
962	S<154>	-2932.379	101.5	1006	S<110>	-3548.247	101.5
963	S<153>	-2946.376	232.5	1007	S<109>	-3562.244	232.5
964	S<152>	-2960.373	101.5	1008	S<108>	-3576.241	101.5
965	S<151>	-2974.37	232.5	1009	S<107>	-3590.238	232.5
966	S<150>	-2988.367	101.5	1010	S<106>	-3604.235	101.5
967	S<149>	-3002.364	232.5	1011	S<105>	-3618.232	232.5
968	S<148>	-3016.361	101.5	1012	S<104>	-3632.229	101.5
969	S<147>	-3030.358	232.5	1013	S<103>	-3646.226	232.5
970	S<146>	-3044.355	101.5	1014	S<102>	-3660.223	101.5
971	S<145>	-3058.352	232.5	1015	S<101>	-3674.22	232.5
972	S<144>	-3072.349	101.5	1016	S<100>	-3688.217	101.5
973	S<143>	-3086.346	232.5	1017	S<99>	-3702.214	232.5
974	S<142>	-3100.343	101.5	1018	S<98>	-3716.211	101.5
975	S<141>	-3114.34	232.5	1019	S<97>	-3730.208	232.5
976	S<140>	-3128.337	101.5	1020	S<96>	-3744.205	101.5
977	S<139>	-3142.334	232.5	1021	S<95>	-3758.202	232.5
978	S<138>	-3156.331	101.5	1022	S<94>	-3772.199	101.5
979	S<137>	-3170.328	232.5	1023	S<93>	-3786.196	232.5
980	S<136>	-3184.325	101.5	1024	S<92>	-3800.193	101.5
981	S<135>	-3198.322	232.5	1025	S<91>	-3814.19	232.5
982	S<134>	-3212.319	101.5	1026	S<90>	-3828.187	101.5
983	S<133>	-3226.316	232.5	1027	S<89>	-3842.184	232.5
984	S<132>	-3240.313	101.5	1028	S<88>	-3856.181	101.5
985	S<131>	-3254.31	232.5	1029	S<87>	-3870.178	232.5
986	S<130>	-3268.307	101.5	1030	S<86>	-3884.175	101.5
987	S<129>	-3282.304	232.5	1031	S<85>	-3898.172	232.5
988	S<128>	-3296.301	101.5	1032	S<84>	-3912.169	101.5
989	S<127>	-3310.298	232.5	1033	S<83>	-3926.166	232.5
990	S<126>	-3324.295	101.5	1034	S<82>	-3940.163	101.5
991	S<125>	-3338.292	232.5	1035	S<81>	-3954.16	232.5
992	S<124>	-3352.289	101.5	1036	S<80>	-3968.157	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1037	S<79>	-3982.154	232.5	1081	S<35>	-4598.022	232.5
1038	S<78>	-3996.151	101.5	1082	S<34>	-4612.019	101.5
1039	S<77>	-4010.148	232.5	1083	S<33>	-4626.016	232.5
1040	S<76>	-4024.145	101.5	1084	S<32>	-4640.013	101.5
1041	S<75>	-4038.142	232.5	1085	S<31>	-4654.01	232.5
1042	S<74>	-4052.139	101.5	1086	S<30>	-4668.007	101.5
1043	S<73>	-4066.136	232.5	1087	S<29>	-4682.004	232.5
1044	S<72>	-4080.133	101.5	1088	S<28>	-4696.001	101.5
1045	S<71>	-4094.13	232.5	1089	S<27>	-4709.998	232.5
1046	S<70>	-4108.127	101.5	1090	S<26>	-4723.995	101.5
1047	S<69>	-4122.124	232.5	1091	S<25>	-4737.992	232.5
1048	S<68>	-4136.121	101.5	1092	S<24>	-4751.989	101.5
1049	S<67>	-4150.118	232.5	1093	S<23>	-4765.986	232.5
1050	S<66>	-4164.115	101.5	1094	S<22>	-4779.983	101.5
1051	S<65>	-4178.112	232.5	1095	S<21>	-4793.98	232.5
1052	S<64>	-4192.109	101.5	1096	S<20>	-4807.977	101.5
1053	S<63>	-4206.106	232.5	1097	S<19>	-4821.974	232.5
1054	S<62>	-4220.103	101.5	1098	S<18>	-4835.971	101.5
1055	S<61>	-4234.1	232.5	1099	S<17>	-4849.968	232.5
1056	S<60>	-4248.097	101.5	1100	S<16>	-4863.965	101.5
1057	S<59>	-4262.094	232.5	1101	S<15>	-4877.962	232.5
1058	S<58>	-4276.091	101.5	1102	S<14>	-4891.959	101.5
1059	S<57>	-4290.088	232.5	1103	S<13>	-4905.956	232.5
1060	S<56>	-4304.085	101.5	1104	S<12>	-4919.953	101.5
1061	S<55>	-4318.082	232.5	1105	S<11>	-4933.95	232.5
1062	S<54>	-4332.079	101.5	1106	S<10>	-4947.947	101.5
1063	S<53>	-4346.076	232.5	1107	S<9>	-4961.944	232.5
1064	S<52>	-4360.073	101.5	1108	S<8>	-4975.941	101.5
1065	S<51>	-4374.07	232.5	1109	S<7>	-4989.938	232.5
1066	S<50>	-4388.067	101.5	1110	S<6>	-5003.935	101.5
1067	S<49>	-4402.064	232.5	1111	S<5>	-5017.932	232.5
1068	S<48>	-4416.061	101.5	1112	S<4>	-5031.929	101.5
1069	S<47>	-4430.058	232.5	1113	S<3>	-5045.926	232.5
1070	S<46>	-4444.055	101.5	1114	S<2>	-5059.923	101.5
1071	S<45>	-4458.052	232.5	1115	S<1>	-5073.92	232.5
1072	S<44>	-4472.049	101.5	1116	G<319>	-5129.917	101.5
1073	S<43>	-4486.046	232.5	1117	G<317>	-5143.914	232.5
1074	S<42>	-4500.043	101.5	1118	G<315>	-5157.911	101.5
1075	S<41>	-4514.04	232.5	1119	G<313>	-5171.908	232.5
1076	S<40>	-4528.037	101.5	1120	G<311>	-5185.905	101.5
1077	S<39>	-4542.034	232.5	1121	G<309>	-5199.902	232.5
1078	S<38>	-4556.031	101.5	1122	G<307>	-5213.899	101.5
1079	S<37>	-4570.028	232.5	1123	G<305>	-5227.896	232.5
1080	S<36>	-4584.025	101.5	1124	G<303>	-5241.893	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1125	G<301>	-5255.89	232.5	1168	G<215>	-5857.761	101.5
1126	G<299>	-5269.887	101.5	1169	G<213>	-5871.758	232.5
1127	G<297>	-5283.884	232.5	1170	G<211>	-5885.755	101.5
1128	G<295>	-5297.881	101.5	1171	G<209>	-5899.752	232.5
1129	G<293>	-5311.878	232.5	1172	G<207>	-5913.749	101.5
1130	G<291>	-5325.875	101.5	1173	G<205>	-5927.746	232.5
1131	G<289>	-5339.872	232.5	1174	G<203>	-5941.743	101.5
1132	G<287>	-5353.869	101.5	1175	G<201>	-5955.74	232.5
1133	G<285>	-5367.866	232.5	1176	G<199>	-5969.737	101.5
1134	G<283>	-5381.863	101.5	1177	G<197>	-5983.734	232.5
1135	G<281>	-5395.86	232.5	1178	G<195>	-5997.731	101.5
1136	G<279>	-5409.857	101.5	1179	G<193>	-6011.728	232.5
1137	G<277>	-5423.854	232.5	1180	G<191>	-6025.725	101.5
1138	G<275>	-5437.851	101.5	1181	G<189>	-6039.722	232.5
1139	G<273>	-5451.848	232.5	1182	G<187>	-6053.719	101.5
1140	G<271>	-5465.845	101.5	1183	G<185>	-6067.716	232.5
1141	G<269>	-5479.842	232.5	1184	G<183>	-6081.713	101.5
1142	G<267>	-5493.839	101.5	1185	G<181>	-6095.71	232.5
1143	G<265>	-5507.836	232.5	1186	G<179>	-6109.707	101.5
1144	G<263>	-5521.833	101.5	1187	G<177>	-6123.704	232.5
1145	G<261>	-5535.83	232.5	1188	G<175>	-6137.701	101.5
1146	G<259>	-5549.827	101.5	1189	G<173>	-6151.698	232.5
1147	G<257>	-5563.824	232.5	1190	G<171>	-6165.695	101.5
1148	G<255>	-5577.821	101.5	1191	G<169>	-6179.692	232.5
1149	G<253>	-5591.818	232.5	1192	G<167>	-6193.689	101.5
1150	G<251>	-5605.815	101.5	1193	G<165>	-6207.686	232.5
1151	G<249>	-5619.812	232.5	1194	G<163>	-6221.683	101.5
1152	G<247>	-5633.809	101.5	1195	G<161>	-6235.68	232.5
1153	G<245>	-5647.806	232.5	1196	G<159>	-6249.677	101.5
1154	G<243>	-5661.803	101.5	1197	G<157>	-6263.674	232.5
1155	G<241>	-5675.8	232.5	1198	G<155>	-6277.671	101.5
1156	G<239>	-5689.797	101.5	1199	G<153>	-6291.668	232.5
1157	G<237>	-5703.794	232.5	1200	G<151>	-6305.665	101.5
1158	G<235>	-5717.791	101.5	1201	G<149>	-6319.662	232.5
1159	G<233>	-5731.788	232.5	1202	G<147>	-6333.659	101.5
1160	G<231>	-5745.785	101.5	1203	G<145>	-6347.656	232.5
1161	G<229>	-5759.782	232.5	1204	G<143>	-6361.653	101.5
1162	G<227>	-5773.779	101.5	1205	G<141>	-6375.65	232.5
1163	G<225>	-5787.776	232.5	1206	G<139>	-6389.647	101.5
1164	G<223>	-5801.773	101.5	1207	G<137>	-6403.644	232.5
1165	G<221>	-5815.77	232.5	1208	G<135>	-6417.641	101.5
1166	G<219>	-5829.767	101.5	1209	G<133>	-6431.638	232.5
1167	G<217>	-5843.764	232.5	1210	G<131>	-6445.635	101.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1211	G<129>	-6459.632	232.5	1255	G<41>	-7075.5	232.5
1212	G<127>	-6473.629	101.5	1256	G<39>	-7089.497	101.5
1213	G<125>	-6487.626	232.5	1257	G<37>	-7103.494	232.5
1214	G<123>	-6501.623	101.5	1258	G<35>	-7117.491	101.5
1215	G<121>	-6515.62	232.5	1259	G<33>	-7131.488	232.5
1216	G<119>	-6529.617	101.5	1260	G<31>	-7145.485	101.5
1217	G<117>	-6543.614	232.5	1261	G<29>	-7159.482	232.5
1218	G<115>	-6557.611	101.5	1262	G<27>	-7173.479	101.5
1219	G<113>	-6571.608	232.5	1263	G<25>	-7187.476	232.5
1220	G<111>	-6585.605	101.5	1264	G<23>	-7201.473	101.5
1221	G<109>	-6599.602	232.5	1265	G<21>	-7215.47	232.5
1222	G<107>	-6613.599	101.5	1266	G<17>	-7243.464	232.5
1223	G<105>	-6627.596	232.5	1267	G<13>	-7271.458	232.5
1224	G<103>	-6641.593	101.5	1268	G<9>	-7299.452	232.5
1225	G<101>	-6655.59	232.5	1269	G<5>	-7327.446	232.5
1226	G<99>	-6669.587	101.5	1270	DMY_GDL	-7383.434	232.5
1227	G<97>	-6683.584	232.5	1271	G<1>	-7355.44	232.5
1228	G<95>	-6697.581	101.5	1272	DMY_GDL	-7397.431	101.5
1229	G<93>	-6711.578	232.5	1273	DMY_GDL	-7369.437	101.5
1230	G<91>	-6725.575	101.5	1274	G<3>	-7341.443	101.5
1231	G<89>	-6739.572	232.5	1275	G<7>	-7313.449	101.5
1232	G<87>	-6753.569	101.5	1276	G<11>	-7285.455	101.5
1233	G<85>	-6767.566	232.5	1277	G<15>	-7257.461	101.5
1234	G<83>	-6781.563	101.5	1278	G<19>	-7229.467	101.5
1235	G<81>	-6795.56	232.5				
1236	G<79>	-6809.557	101.5				
1237	G<77>	-6823.554	232.5				
1238	G<75>	-6837.551	101.5				
1239	G<73>	-6851.548	232.5				
1240	G<71>	-6865.545	101.5				
1241	G<69>	-6879.542	232.5				
1242	G<67>	-6893.539	101.5				
1243	G<65>	-6907.536	232.5				
1244	G<63>	-6921.533	101.5				
1245	G<61>	-6935.53	232.5				
1246	G<59>	-6949.527	101.5				
1247	G<57>	-6963.524	232.5				
1248	G<55>	-6977.521	101.5				
1249	G<53>	-6991.518	232.5				
1250	G<51>	-7005.515	101.5				
1251	G<49>	-7019.512	232.5				
1252	G<47>	-7033.509	101.5				
1253	G<45>	-7047.506	232.5				
1254	G<43>	-7061.503	101.5				

7. Command

7.1 Public command

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
No operation	W	0	0	0	0	0	0	0	0	(00h)
Software reset	W	0	0	0	0	0	0	0	1	(01h)
Read display ID	W	0	0	0	0	0	1	0	0	(04h)
	R	id[23:16]								30h
	R	id[15:8]								31h
	R	id[7:0]								FFh
Read display status	W	0	0	0	0	1	0	0	1	(09h)
	R	boost_ status	madctl[7:2]						X	00h
	R	X	color_mode[2:0]			idle	partial_ mode	sleep	normal_ mode	61h
	R	scroll_ mode	X	inv_en	X	X	display_ en	tear_en	X	00h
	R	tear_mode	X	X	X	X	X	X	X	00h
Read display Power mode	W	0	0	0	0	1	0	1	0	(0Ah)
	R	boost_ status	idle	partial_ mode	sleep	normal_ mode	display_ en	X	X	08h
Read display MADCTL	W	0	0	0	0	1	0	1	1	(0Bh)
	R	madctl[7:0]								00h
Read display Pixel format	W	0	0	0	0	1	1	0	0	(0Ch)
	R	rim	dpi[2:0]			X	dbi[2:0]			66h
Read display Image mode	W	0	0	0	0	1	1	0	1	(0Dh)
	R	0	0	0	0	0	0	0	0	00h
Read display Signal mode	W	0	0	0	0	1	1	1	0	(0Eh)
	R	te_on_ off	tear_ mode	rcm[2:0]			de_ mode	X	X	3Ch
Read display self-diagnostic result	W	0	0	0	0	1	1	1	1	(0Fh)
	R	reg_load_ det	func_ det	X	X	X	X	X	X	00h
Sleep in	W	0	0	0	1	0	0	0	0	(10h)
Sleep out	W	0	0	0	1	0	0	0	1	(11h)
Partial mode on	W	0	0	0	1	0	0	1	0	(12h)

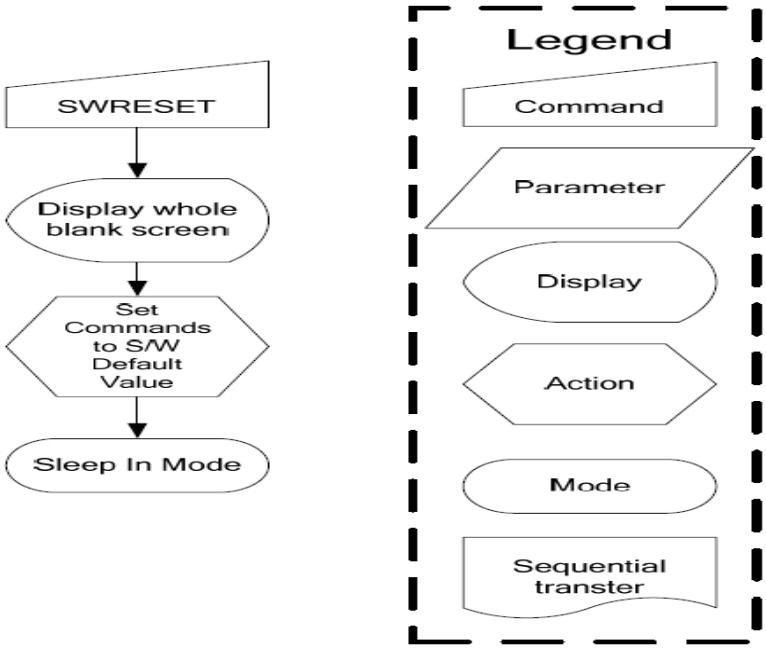
Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
normal mode on and partial mode off	W	0	0	0	1	0	0	1	1	(13h)
Display inversion off	W	0	0	1	0	0	0	0	0	(20h)
Display inversion on	W	0	0	1	0	0	0	0	1	(21h)
Display off	W	0	0	1	0	1	0	0	0	(28h)
Display on	W	0	0	1	0	1	0	0	1	(29h)
Column address	W	0	0	1	0	1	0	1	0	(2Ah)
	W	caset_sc[15:8]								00h
	W	caset_sc[7:0]								00h
	W	caset_ec[15:8]								00h
	W	caset_ec[7:0]								EFh
page address	W	0	0	1	0	1	0	1	1	(2Bh)
	W	paset_sp[15:8]								00h
	W	paset_sp[7:0]								00h
	W	paset_ep[15:8]								01h
	W	paset_ep[7:0]								3Fh
memory write	W	0	0	1	0	1	1	0	0	(2Ch)
memory read	R	0	0	1	0	1	1	1	0	(2Eh)
partial area	W	0	0	1	1	0	0	0	0	(30h)
	W	paset_sr[15:8]								00h
	W	paset_sr[7:0]								00h
	W	paset_er[15:8]								01h
	W	paset_er[7:0]								3Fh
Vertical scrolling	W	0	0	1	1	0	0	1	1	(33h)
	W	vscrdef_tfa[15:8]								00h
	W	vscrdef_tfa[7:0]								00h
	W	vscrdef_vsa[15:8]								01h
	W	vscrdef_vsa[7:0]								40h
	W	vscrdef_bfa[15:8]								00h
	W	vscrdef_bfa[7:0]								00h
Tearing effect line off	W	0	0	1	1	0	1	0	0	(34h)
Tearing effect line on	W	0	0	1	1	0	1	0	1	(35h)
	W	X	X	X	X	X	X	X	tem	00h
MADCTL (memory data access control)	W	0	0	1	1	0	1	1	0	(36h)
	W	my	mx	mv	ml	bgr	mh	X	X	00h
Vertical scrolling start address	W	0	0	1	1	0	1	1	1	(37h)
	W	vscrdef_vsp[15:8]								00h
	W	vscrdef_vsp[7:0]								00h
Idle mode off	W	0	0	1	1	1	0	0	0	(38h)
idle mode on and other mode off	W	0	0	1	1	1	0	0	1	(39h)

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
Interface pixel format	W	0	0	1	1	1	0	1	0	(3Ah)
	W	X	dpi[2:0]			X	dbi[2:0]			66h
write memory continue	W	0	0	1	1	1	1	0	0	(3Ch)
read memory continue	W	0	0	1	1	1	1	1	0	(3Eh)
Get tear scan line	W	0	1	0	0	0	1	0	1	(45h)
	R	X	X	X	X	X	X	gts[9:8]		00h
	R	gts[7:0]								00h
read idd3	W	1	1	0	1	0	0	1	1	(D3h)
	R	id[23:16]								30h
	R	id[15:8]								31h
	R	id[7:0]								FFh
read display id 1	W	1	1	0	1	1	0	1	0	(DAh)
	R	id[23:16]								FFh
read display id 2	W	1	1	0	1	1	0	1	1	(DBh)
	R	id[15:8]								FFh
read display id 3	W	1	1	0	1	1	1	0	0	(DCh)
	R	id[7:0]								FFh

7.1.1 no operation (00h)

<table>
<tr><th>00h</th><th colspan="9">no operation</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>no operation</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(00h)</td></tr>
<tr><td>Parameter</td><td colspan="9">No Parameter.</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is empty command.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.2 software reset (01h)

<table>
<tr><th>01h</th><th colspan="10">software reset</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>software reset</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(01h)</td></tr>
<tr><td>Parameter</td><td colspan="9">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">The display module performs a software reset, registers are written with their SW reset default values.Frame memory contents are unaffected by this command.“-“ Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">It will be necessary to wait 5msec before sending new command following software reset.
The display module loads all display suppliers’ factory default values to the registers during this 5msec.If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command.Software reset command cannot be sent during sleep out sequence.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.1.3 read display ID (04h)

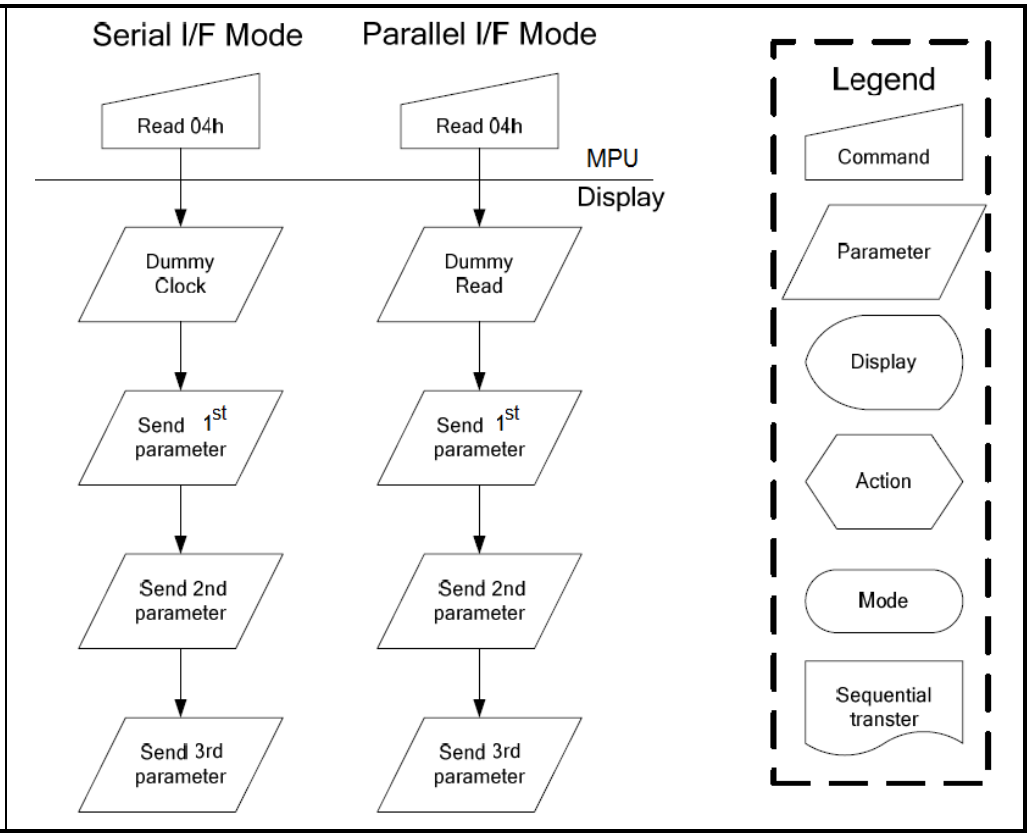
04h	read display ID									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display ID	W	0	0	0	0	0	1	0	0	(04h)
1st parameter	R	id[23:16]								30h
2nd parameter	R	id[15:8]								31h
3rd parameter	R	id[7:0]								ffh
Description	This read byte returns 24-bit display identification information. id[23:0]:LCD module/driver ID. Commands RDID1/2/3(Dah, DBh, DCh) read data correspond to the parameters 1,2,3 of the command 04h,respectively.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	id[23:16]	id[15:8]	id[7:0]
Power On Sequence	00h	31h	35h
S/W Reset	00h	31h	35h
H/W Reset	00h	31h	35h

Flow Chart



7.1.4 read display status (09h)

09h	read display status									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display status	W	0	0	0	0	1	0	0	1	(09h)
1st parameter	R	boost_status	madctl[7:2]						X	00h
2nd parameter	R	X	color_mode[2:0]			idle	partial_mode	sleep	normal_mode	61h
3rd parameter	R	scroll_mode	X	inv_en	X	X	display_en	tear_en	X	00h
4th parameter	R	tear_mode	X	X	X	X	X	X	X	00h

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Comment
boost_status	Booster Voltage Status	0	Booster Off
		1	Booster On
madctl [7...2]	Page Address Order	0	Top to Bottom (When memory data access control D7 = '0')
		1	Bottom to Top (When memory data access control D7 = '1')
	Column Address Order	0	Left to Right (When memory data access control D6 = '0')
		1	Right to Left (When memory data access control D6 = '1')
	Page/Column Order	0	Normal Mode (When memory data access control D5 = '0')
		1	Reverse Mode (When memory data access control D5 = '1')
	Line Address Order	0	LCD Refresh Top to Bottom (When memory data access control D4 = '0')
		1	LCD Refresh Bottom to Top (When memory data access control D4 = '1')
	RGB/BGR Order	0	RGB (When memory data access control D3 = '0')
		1	BGR (When memory data access control D3 = '1')
	mh	-	Reserved
idle	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
partial_mode	Partial Mode On/Off	0	Partial Mode Off
		1	Partial Mode On
sleep	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
normal_mode	Display Normal Mode On/Off	0	Display Normal Mode Off
		1	Display Normal Mode On
scroll_mode	Vertical Scrolling Status	0	Vertical Scrolling is Off
		1	Vertical Scrolling is On
inv_en	Inversion Status	0	Inversion is Off
		1	Inversion is On
display_en	Display On/Off	0	Display is Off
		1	Display is On
tear_en	Tearing Effect Line On/Off	0	Tearing Effect Line Off
		1	Tearing Effect Line On
tear_mode	Tearing Effect Output Line Mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking
D[4…0]	For Future Use	0	Set to '0'
Others	-	0	Set to '0'

Bits color_mode[2:0]: Interface Color Pixel Format Definition.

Interface Format	color_mode[2]	color_mode[1]	color_mode[0]
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

Note:

1. For Bits madctl [7:5], also refer to Section 8.2.3 MPU to memory write/read direction.
2. For Bits madctl [4:2] also refer to 7.1.27 memory data access control (36h).

"-" Don't care.

Restriction

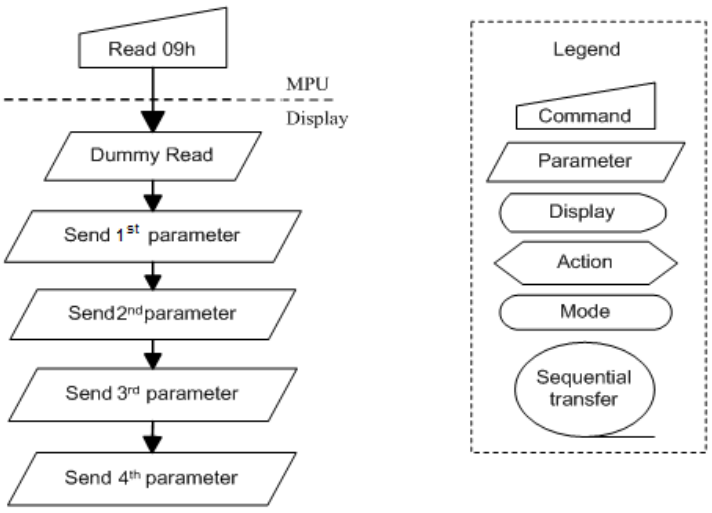
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

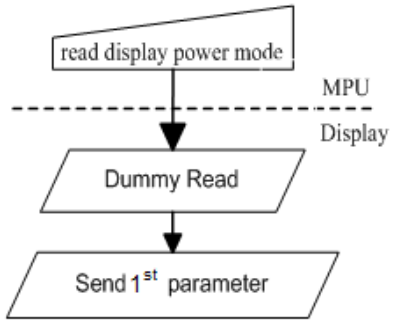
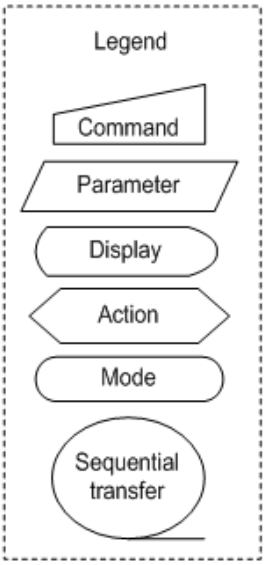
Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart



7.1.5 read display power mode (0Ah)

<table>
<tr><th>0Ah</th><th colspan="10">read display power mode</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display power mode</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>(0Ah)</td></tr>
<tr><td>parameter</td><td>R</td><td>boost_status</td><td>idle</td><td>partial_mode</td><td>sleep</td><td>normal_ mode</td><td>display_ en</td><td>X</td><td>X</td><td>08h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Comment</th></tr>
<tr><td rowspan="2">boost_status</td><td rowspan="2">Booster Voltage Status</td><td>0</td><td>Booster Off or has a fault</td></tr>
<tr><td>1</td><td>Booster On and working OK</td></tr>
<tr><td rowspan="2">idle</td><td rowspan="2">Idle Mode On/Off</td><td>0</td><td>Idle Mode Off</td></tr>
<tr><td>1</td><td>Idle Mode On</td></tr>
<tr><td rowspan="2">partial_mode</td><td rowspan="2">Partial Mode On/Off</td><td>0</td><td>Partial Mode Off</td></tr>
<tr><td>1</td><td>Partial Mode On</td></tr>
<tr><td rowspan="2">sleep</td><td rowspan="2">Sleep In/Out</td><td>0</td><td>Sleep In Mode</td></tr>
<tr><td>1</td><td>Sleep Out Mode</td></tr>
<tr><td rowspan="2">normal_mode</td><td rowspan="2">Display Normal Mode On/Off</td><td>0</td><td>Display Normal Mode Off</td></tr>
<tr><td>1</td><td>Display Normal Mode On</td></tr>
<tr><td rowspan="2">display_en</td><td rowspan="2">Display On/Off</td><td>0</td><td>Display Off</td></tr>
<tr><td>1</td><td>Display On</td></tr>
<tr><td>others</td><td>-</td><td>0</td><td>Set to ‘0’</td></tr>
</table>
“X“ Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>08h</td></tr>
<tr><td>S/W Reset</td><td>08h</td></tr>
<tr><td>H/W Reset</td><td>08h</td></tr>
</table>
</td></tr>
</table>

Flow Chart	 

7.1.6 read display MADCTL (0Bh)

0Bh	read display MADCTL									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display MADCTL	W	0	0	0	0	1	0	1	1	(0Bh)
1st parameter	R	madctl[7:0]								00h

Description

This command indicates the current status of the display as described in the table below:

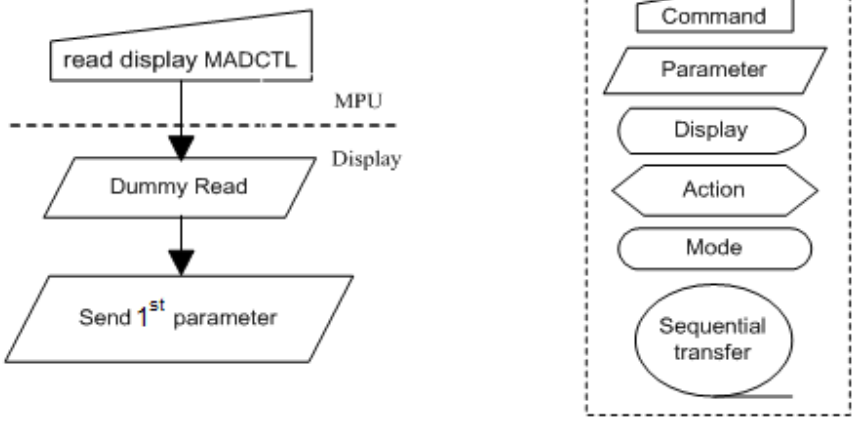
Bit	Description	Value	Comment
Madctl[7]	Page Address Order	0	Top to Bottom (When memory data access control D7='0').
		1	Bottom to Top (When memory data access control D7='1').
Madctl[6]	Column Address Order	0	Left to Right (When memory data access control D6='0')
		1	Right to Left (when memory data access control D6='1'
Madctl[5]	Page/Column Order	0	Normal Mode (When memory data access control D5='0').
		1	Reverse Mode (When memory data access control D5='1')
Madctl[4]	Line Address Order	0	LCD Refresh Top to Bottom (When memory data access control D4='0')
		1	LCD Refresh Bottom to Top (When memory data access control D4='1')
Madctl[3]	RGB/BGR Order	0	RGB (When memory data access control D3='0')
		1	"1": BGR (When memory data access control D3='1')
Madctl[2]	mh	-	Reserved
others	-	0	Set to '0'

Note:

1. For Bits Madctl[7…5], also refer to Section 8.2.3 MPU to memory write/read direction.
2. For Bits Madctl [4:2] also refer to 7.1.27 memory dataaccess control (36h).

"X" Don't care.

Restriction

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

7.1.7 read display pixel format (0Ch)

0Ch	read display pixel format									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display pixel format	W	0	0	0	0	1	1	0	0	(0Ch)
1st parameter	R	rim	dpi[2:0]			X	dbi[2:0]			66h

Description

This command indicates the current status of the display as described in the table below:

rim	dpi[2:0]			RGB interface Format
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	16bit/pixel
0	1	1	0	18bit/pixel
0	1	1	1	Reserved
1	1	0	1	16bit/pixel(6-bit 3 times data transfer)
1	1	1	0	18bit/pixel(6-bit 3 times data transfer)

dbi[2:0]			system Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	12bit/pixel
1	0	0	Reserved
1	0	1	16bit/pixel
1	1	0	18bit/pixel
1	1	1	Reserved

Restriction

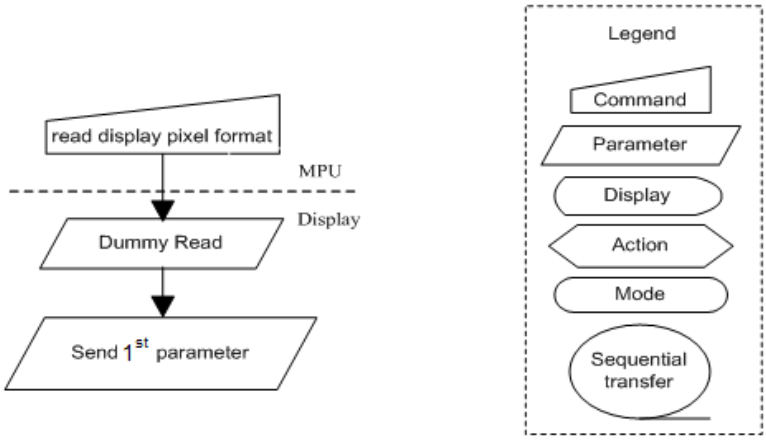
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	66h
S/W Reset	No change
H/W Reset	66h

Flow Chart



7.1.8 read display image mode (0Dh)

0Dh	read display image mode									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display image mode	W	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	R	0	0	0	0	0	0	0	0	00h
Restriction										

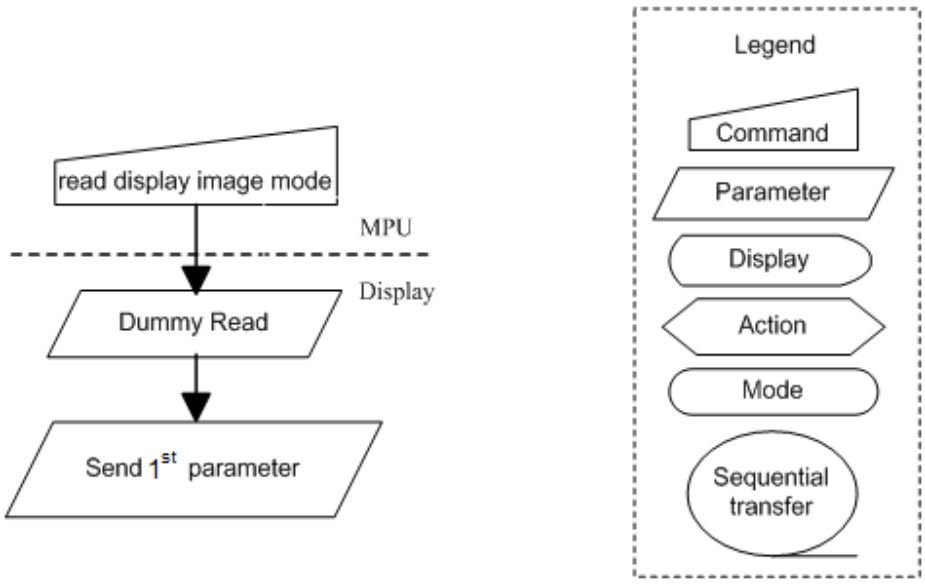
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

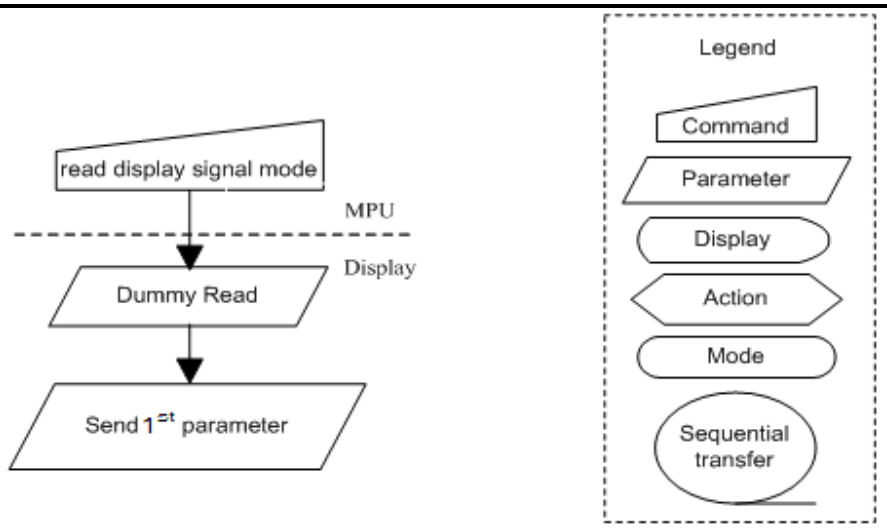
Status	Default Value
Power On Sequence	00h
S/W Reset	no change
H/W Reset	00h

Flow Chart



7.1.9 read display signal mode (0Eh)

<table>
<tr><th>0Eh</th><th colspan="10">read display signal mode</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read display signal mode</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>(0Eh)</td></tr>
<tr><td>1st parameter</td><td>R</td><td>te_on_off</td><td>tear_mode</td><td>rcm[1]</td><td>rcm[1]</td><td>rcm[1]</td><td>de_mode</td><td>X</td><td>X</td><td>3Ch</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="2">te_on_off</td><td>0</td><td>Tearing Effect Line Off</td></tr>
<tr><td>1</td><td>Tearing Effect Line On</td></tr>
<tr><td rowspan="2">tear_mode</td><td>0</td><td>Mode 1（Tearing Effect Line Output Mode, see section 8.4.1）</td></tr>
<tr><td>1</td><td>Mode 2（Tearing Effect Line Output Mode, see section 8.4.1）</td></tr>
<tr><td>de_mode</td><td>-</td><td>RGB DE mode.</td></tr>
</table>
<table>
<tr><th>rcm[1]</th><th>de_mode</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td rowspan="2">MCU interface</td></tr>
<tr><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>DE mode</td></tr>
<tr><td>1</td><td>1</td><td>SYNC mode</td></tr>
</table>
“X” Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>3Ch</td></tr>
<tr><td>S/W Reset</td><td>3Ch</td></tr>
<tr><td>H/W Reset</td><td>3Ch</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>



7.1.10 read display self-diagnostic result (0Fh)

0Fh	read display self-diagnostic result									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display self-diagnostic result	W	0	0	0	0	1	1	1	1	(0Fh)
parameter	R	reg_load_det	func_det	X	X	X	X	X	X	00h

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Action
reg_load_det	Register loading detection	Inverting the D7 bit if registers values loading work properly
func_det	Functionality detection	Inverting the D6 bit if the display is on function
others	-	Set to‘0’

“X”Don’t care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

7.1.11 sleep in (10h)

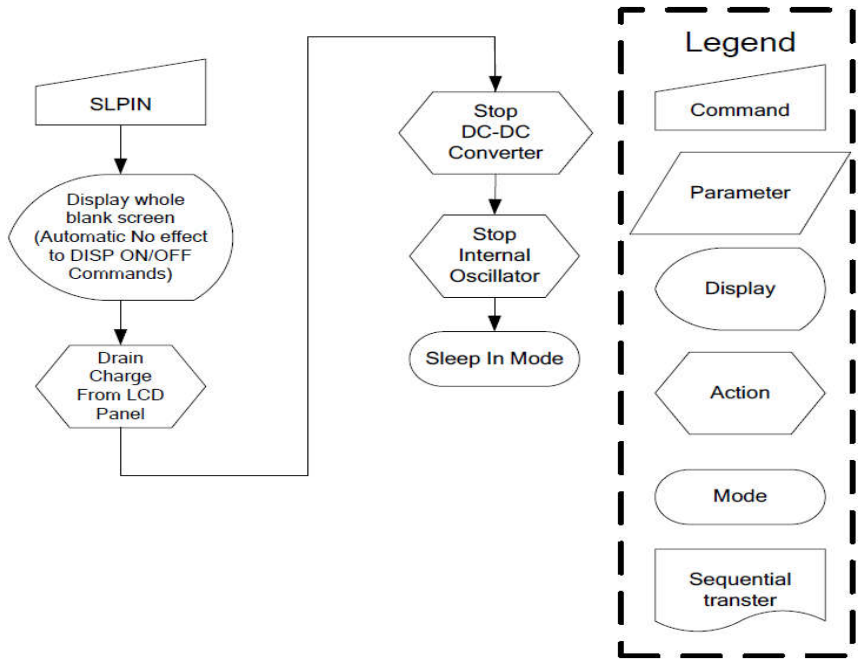
10h	sleep in									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
sleep in	W	0	0	0	1	0	0	0	0	(10h)
parameter	No Parameter									
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC-DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped. Interface and memory are still working and the memory keeps its contents.									
Restriction	This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h). It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

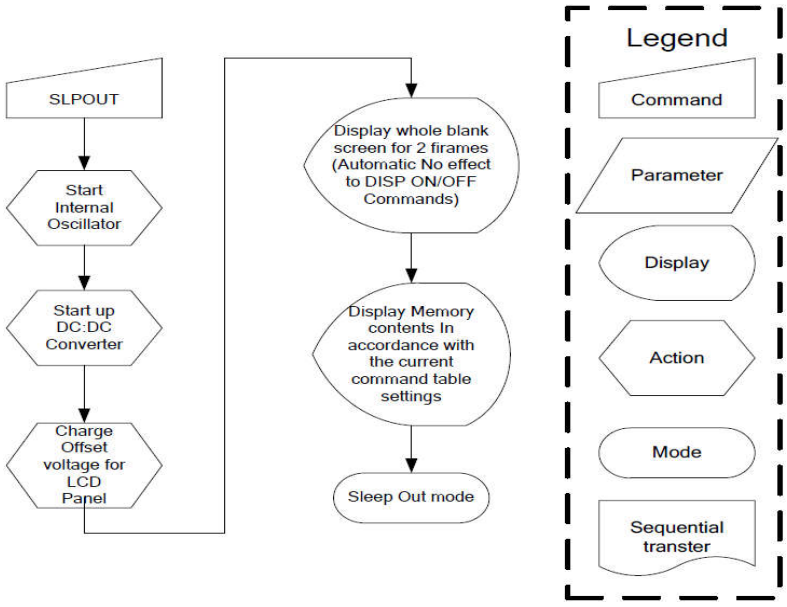
Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart



7.1.12 sleep out (11h)

<table>
<tr><th>11h</th><th colspan="10">sleep out</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>sleep out</td><td>W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(11h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command turn off sleep mode.
In this mode the DC-DC converter is enabled, internal display oscillator is started, and panel scanning is started.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in sleep out mode. Sleep out mode can only be left by the sleep in command (10h).
It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode)before sending an sleep in command.
The display module runs the self-diagnostic functions after this command is received.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep in mode</td></tr><tr><td>S/W Reset</td><td>Sleep in mode</td></tr><tr><td>H/W Reset</td><td>Sleep in mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

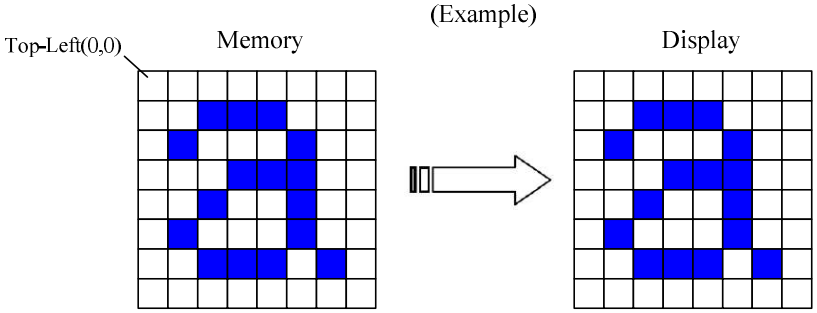
7.1.13 partial mode on (12h)

<table>
<tr><th>12h</th><th colspan="10">partial mode on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>partial mode on</td><td>W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>(12h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h).
To leave Partial mode, the Normal Display Mode On command (13h) should be written.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode on</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode on</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode on</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10">See Partial Area (30h).</td></tr>
</table>

7.1.14 normal mode on and partial mode off (13h)

<table>
<tr><th>13h</th><th colspan="10">normal mode on and partial mode off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>normal mode on and partial mode off</td><td>W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(13h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command turns the display to normal mode.
Normal display mode on means partial mode off.
Exit from normal mode on by the partial mode on command.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when normal display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal display mode on</td></tr><tr><td>S/W Reset</td><td>Normal display mode on</td></tr><tr><td>H/W Reset</td><td>Normal display mode on</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10">See Partial Area (30h).</td></tr>
</table>

7.1.15 display inversion off (20h)

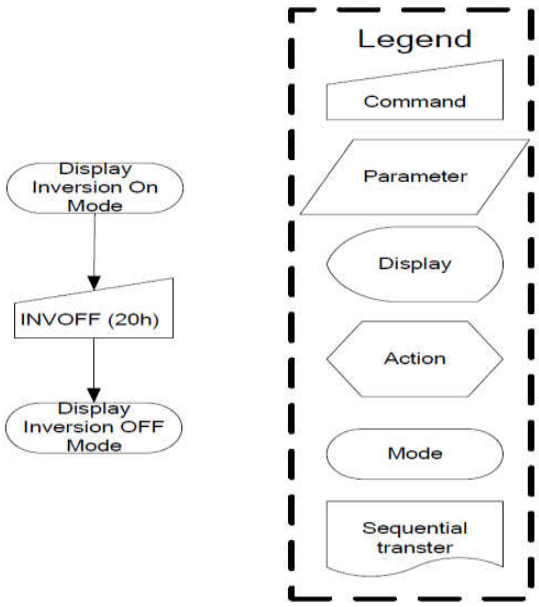
20h	display inversion off									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
display inversion off	W	0	0	1	0	0	0	0	0	(20h)
parameter	No Parameter									
Description	This command is used to recover from display inversion mode. (Example) Top-Left(0,0) Memory Display 									
Restriction	This command has no effect when module is already in inversion off mode.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

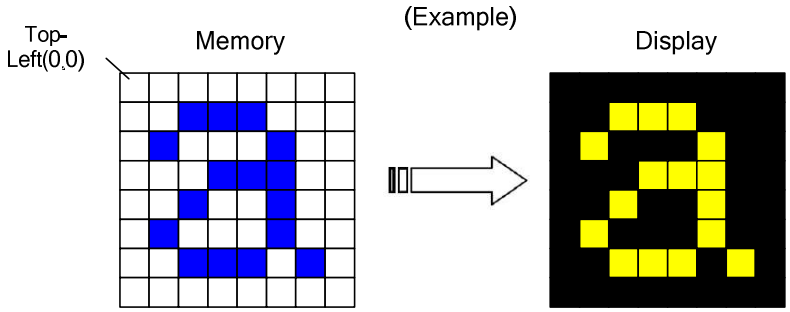
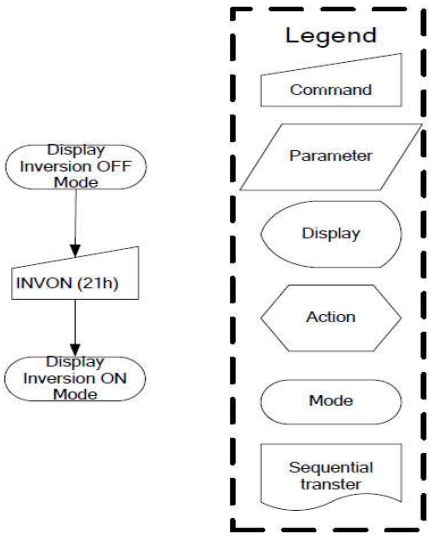
Default

Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

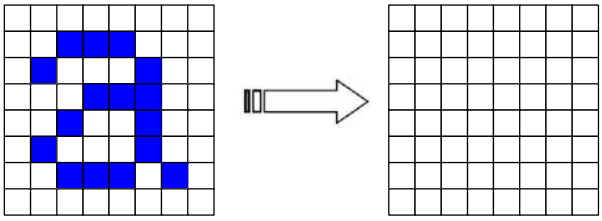
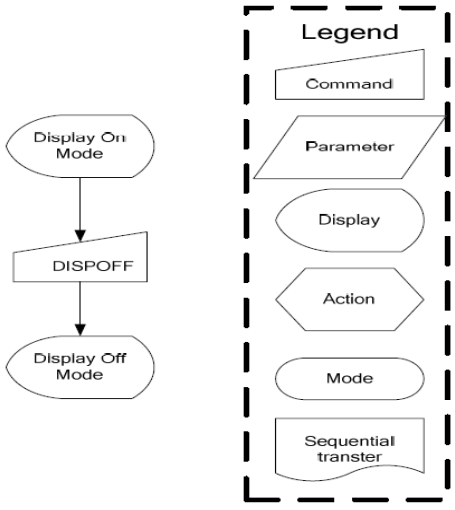
Flow Chart



7.1.16 display inversion on (21h)

<table>
<tr><th>21h</th><th colspan="9">display inversion on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display inversion on</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(21h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into display inversion mode.
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in inversion on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

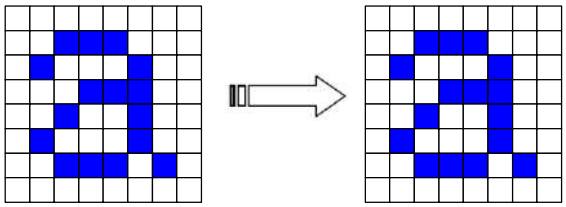
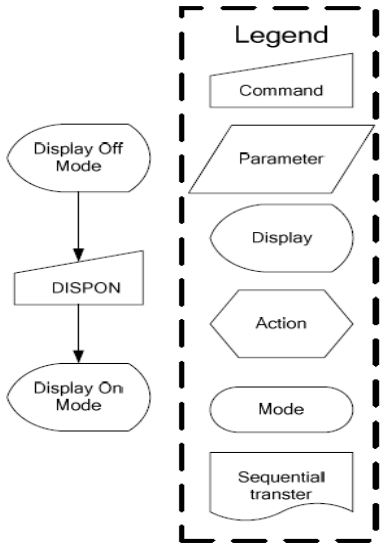
7.1.17 display off (28h)

28h	display off									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
display off	W	0	0	1	0	1	0	0	0	(28h)
parameter	No Parameter									
Description	This command is used to enter into display off mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Exit from this command by Display On (29h) . (Example) Memory Display 									
Restriction	This command has no effect when module is already in display off mode.									
Register Availability										
Default										
Flow Chart										

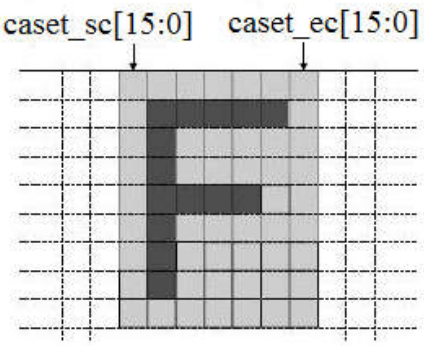
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

7.1.18 display on (29h)

<table>
<tr><th>29h</th><th colspan="9">display on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display on</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>(29h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from display off mode.
Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)
Memory Display
  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>S/W Reset</td><td>Display off</td></tr><tr><td>H/W Reset</td><td>Display off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.1.19 column address (2Ah)

<table>
<tr><th>2Ah</th><th colspan="10">column address</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>column address</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>(2Ah)</td></tr>
<tr><td>1st parameter</td><td>W</td><td colspan="8">caset_sc[15:8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>W</td><td colspan="8">caset_sc[7:0]</td><td>00h</td></tr>
<tr><td>3rd parameter</td><td>W</td><td colspan="8">caset_ec[15:8]</td><td>00h</td></tr>
<tr><td>4th parameter</td><td>W</td><td colspan="8">caset_ec[7:0]</td><td>EFh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to define area of frame memory where system interface can access. This command makes no change on the other driver status.
The values of caset_sc[15:0] and caset_ec[15:0] are referred when memory write command comes. Each value represents one column line in the Frame Memory.
(Example)
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">caset_sc [15:0] always must be equal to or less than caset_ec [15:0].
When caset_sc [15:0] or caset_ec [15:0] is greater than maximum address like below, data of out of range will be ignored.
(Parameter range: 0 < caset_sc [15:0] < caset_ec [15:0] < =239(00EFh)): mv=”0”)
(Parameter range: 0 < caset_sc [15:0] < caset_ec [15:0] < =319(013Fh)): mv=”1”)</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>caset_sc[15:0]</th><th>caset_ec[15:0]</th></tr><tr><td>Power On Sequence</td><td>0000h</td><td>00EFh</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>If MADCTL’s D5=0: caset_ec[15:0]=00EFh
If MADCTL’s D5=1: caset_ec[15:0]=013Fh</td></tr><tr><td>H/W Reset</td><td>0000h</td><td>00EFh</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.20 page address (2Bh)

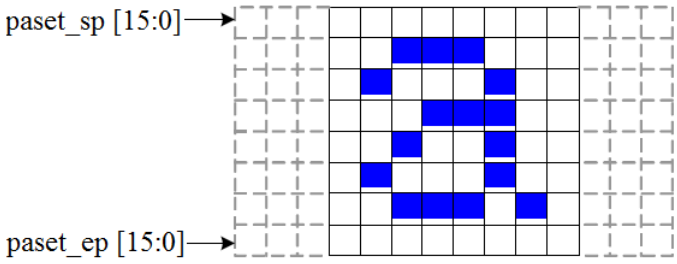
2Bh	page address									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
page address	W	0	0	1	0	1	0	1	1	(2Bh)
1st parameter	W	paset_sp[15:8]								00h
2nd parameter	W	paset_sp[7:0]								00h
3rd parameter	W	paset_ep[15:8]								01h
4th parameter	W	paset_ep[7:0]								3Fh

Description

This command is used to defined area of frame memory where system interface can access.

The value of paset_sp [15:0] and paset_ep [15:0] are referred when memory write command comes.

Each value represents one page line in the Frame Memory.



Restriction

paset_sp[15:0] always must be equal to or less than paset_ep[15:0].

When paset_sp[15:0] or paset_ep[15:0] is greater than maximum address like below, data of out of range will be ignored.

(Parameter range: 0 < paset_sp[15:0] < paset_ep[15:0] <239 (00EFh)): mv="1")

(Parameter range: 0 < paset_sp[15:0] < paset_ep[15:0] <319 (013Fh)): mv="0")

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	paset_sp[15:0]	paset_ep[15:0]
Power On Sequence	0000h	013Fh
S/W Reset	0000h	If MADCTL's D5=0: paset_ep[15:0]=013Fh If MADCTL's D5=1: paset_ep[15:0]=00EFh
H/W Reset	0000h	013Fh

Flow Chart

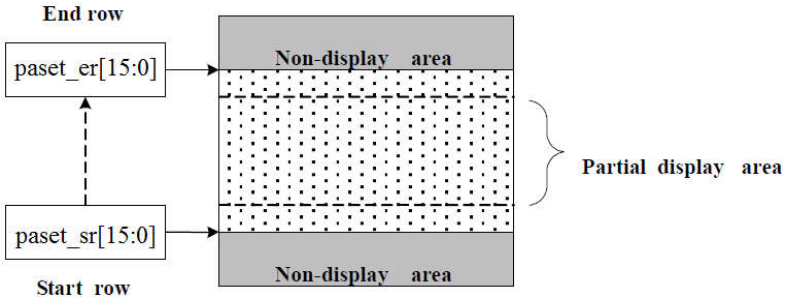
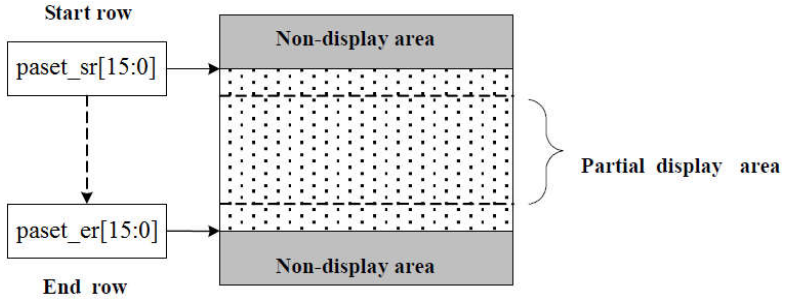
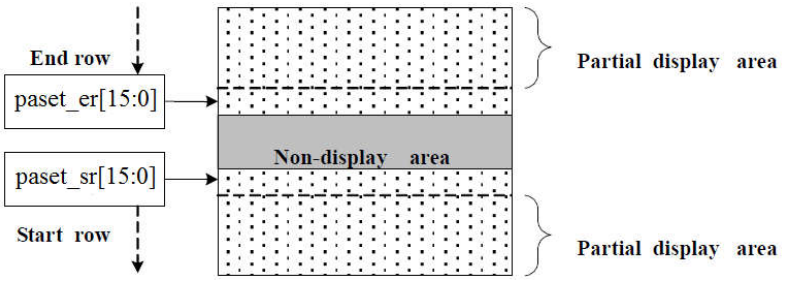
7.1.21 memory write (2Ch)

<table>
<tr><th>2Ch</th><th colspan="10">memory write</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>memory write</td><td>W</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(2Ch)</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to transfer data from MPU to frame memory.
When this command is accepted, the column register and the page register are reset to the start column/start page positions.
The start column/start page positions are different in accordance with MADCTL setting.
Sending any other command can stop frame write.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

7.1.22 memory read (2Eh)

<table>
<tr><th>2Eh</th><th colspan="10">memory read</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>memory read</td><td>R</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>(2Eh)</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to transfer data from frame memory to MPU.
When this command is accepted, the column register and the page register are reset to the Start Column/Start page positions.
The Start Column/Start page positions are different in accordance with MADCTL setting.
Frame Read can be cancelled by sending any other command.
The data color coding is fixed to 18-bit in reading function. Please see section 8.3.4.9 “ Read Memory Data Color Coding” for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

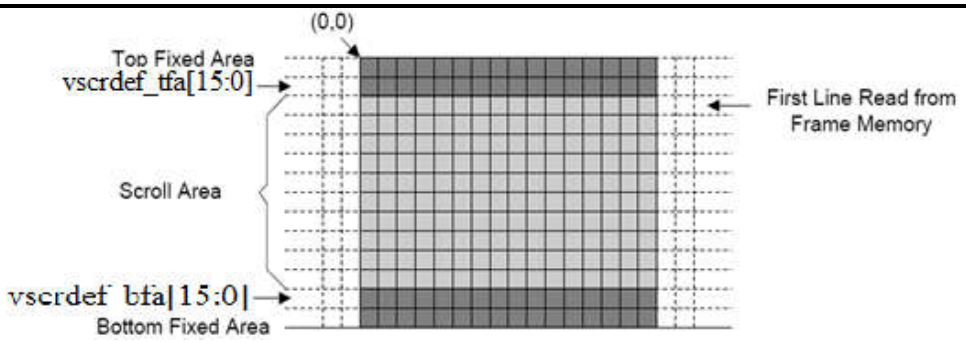
7.1.23 partial area (30h)

30h	partial area									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
partial area	W	0	0	1	1	0	0	0	0	(30h)
1st parameter	W	paset_sr[15:8]								00h
2nd parameter	W	paset_sr[7:0]								00h
3rd parameter	W	paset_er[15:8]								01h
4th parameter	W	paset_er[7:0]								3Fh
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (paset_sr[15:0]) and the second the End Row (paset_er[15:0]), as illustrated in the figures below. paset_sr[15:0] and paset_er[15:0] refer to the Frame Memory row address counter. If End Row > Start Row, when MADCTL ml='1'  If End Row > Start Row, when MADCTL ml='0'  If End Row < Start Row, when MADCTL ml='0'  If End Row = Start Row then the Partial Area will be one row deep.									
Restriction	paset_sr[15:0] and paset_er[15:0] cannot be 0000h nor exceed 013Fh.									

Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>paset_sr[15:0]</th><th>paset_er[15:0]</th></tr><tr><td>Power On Sequence</td><td>0000h</td><td>013Fh</td></tr><tr><td>S/W Reset</td><td>0000h</td><td>013Fh</td></tr><tr><td>H/W Reset</td><td>0000h</td><td>013Fh</td></tr></table>
Flow Chart	

7.1.24 vertical scrolling (33h)

33h	**vertical scrolling**									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
vertical scrolling	W	0	0	1	1	0	0	1	1	(33h)
1st parameter	W	vscrdef_tfa[15:8]								00h
2nd parameter	W	vscrdef_tfa[7:0]								00h
3rd parameter	W	vscrdef_vsa[15:8]								01h
4th parameter	W	vscrdef_vsa[7:0]								40h
5th parameter	W	vscrdef_bfa[15:8]								00h
6th parameter	W	vscrdef_bfa[7:0]								00h
Description	This command defines the Vertical Scrolling Area of the display. **When MADCTL ml = '0'** The 1st &2nd parameter vscrdef_tfa[15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd &4th parameter vscrdef_vsa[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter vscrdef_bfa[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). vscrdef_tfa[15:0], vscrdef_vsa[15:0] and vscrdef_bfa[15:0] refer to the Frame Memory Line Pointer.									

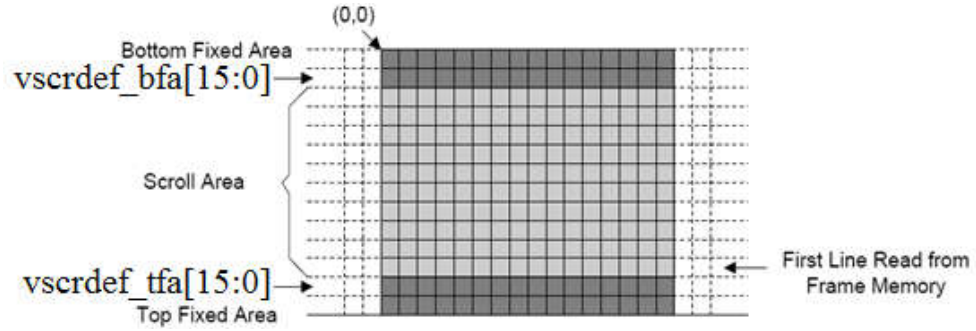


When MADCTL ml = '1'

The 1st &2nd parameter vscrdef_tfa[15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd &4th parameter vscrdef_vsa[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th &6th parameter vscrdef_bfa[15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



See also Section 8.2.2.2 and 8.2.2.3 for details of Vertical Scroll Mode and Vertical Scroll example.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	vscrdef_tfa[15:0]	vscrdef_vsa[15:0]	vscrdef_bfa[15:0]
Power On Sequence	0000h	0140h	0000h
S/W Reset	0000h	0140h	0000h
H/W Reset	0000h	0140h	0000h

Flow Chart

7.1.25 tearing effect line off (34h)

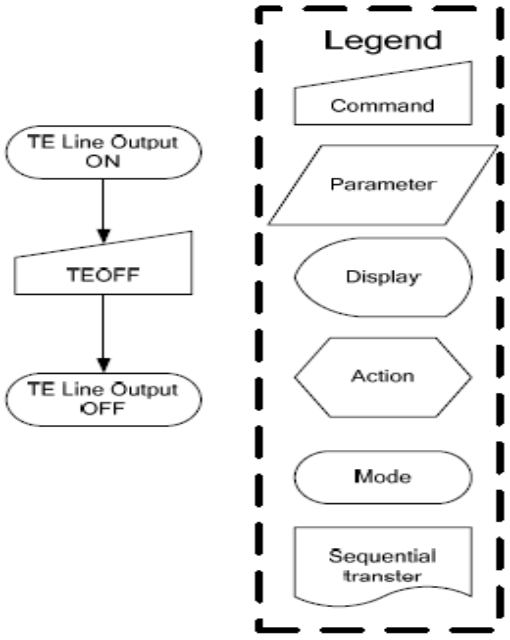
34h	tearing effect line off									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
tearing effect line off	W	0	0	1	1	0	1	0	0	(34h)
parameter	No Parameter									
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when tearing effect output is already off.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

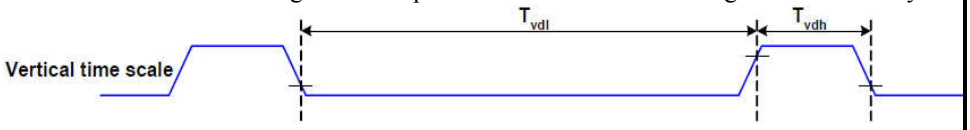
Default

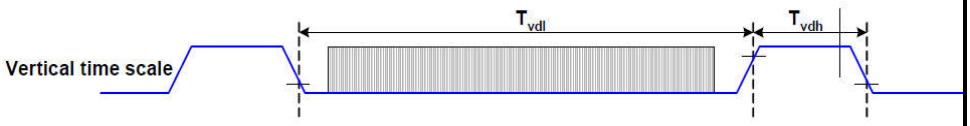
Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



7.1.26 tearing effect line on (35h)

<table>
<tr><th>35h</th><th colspan="9">tearing effect line on</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>tearing effect line on</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(35h)</td></tr>
<tr><td>parameter</td><td>W</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>tem</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to turn on the Tearing Effect output signal from the TE signal line.
This output is not affected by changing MADCTL bit ml.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.
When tem =’0’: The Tearing Effect output line consists of V-Blanking information only:
 

When tem =’1’: The Tearing Effect output Line consists of both V-Blanking and H-Blanking information:
 

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when tearing effect output is already on.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

7.1.27 MADCTL(memory data access control) (36h)

36h	MADCTL(memory data access control)									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
MADCTL(memory data access control)	W	0	0	1	1	0	1	1	0	(36h)
parameter	W	my	mx	mv	ml	bgr	mh	X	X	00h
Description	This command defines read/write scanning direction of frame memory.									

Bit	name	Description
D7	my	Page Address Order
D6	mx	Column Address Order
D5	mv	Page/Column Order
D4	ml	Line Address Order
D3	bgr	RGB/BGR Order
D2	mh	Reserved

-Bit Assignment

Bit D7- Page Address Order

"0" = Top to Bottom (When MADCTL D7="0").

"1" = Bottom to Top (When MADCTL D7="1").

Bit D6- Column Address Order

"0" = Left to Right (When MADCTL D6="0").

"1" = Right to Left (When MADCTL D6="1").

Bit D5- Page/Column Order

"0" = Normal Mode (When MADCTL D5="0").

"1" = Reverse Mode (When MADCTL D5="1")

Bit D4- Line Address Order

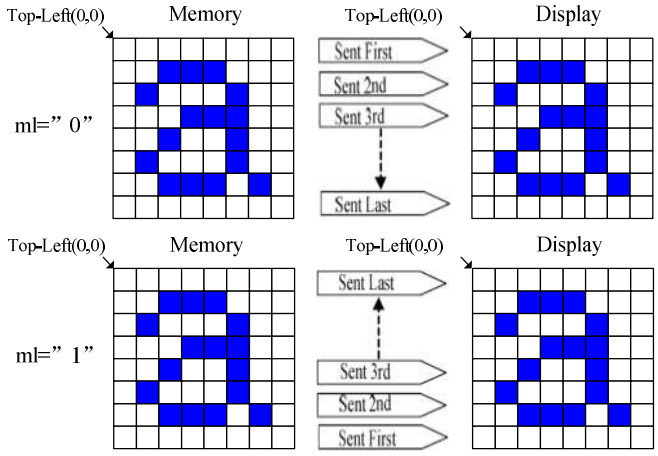
"0" = LCD Refresh Top to Bottom (When MADCTL D4="0")

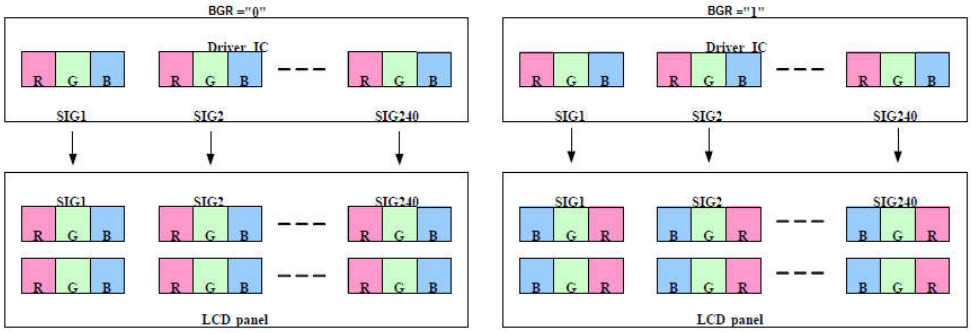
"1" = LCD Refresh Bottom to Top (When MADCTL D4="1")

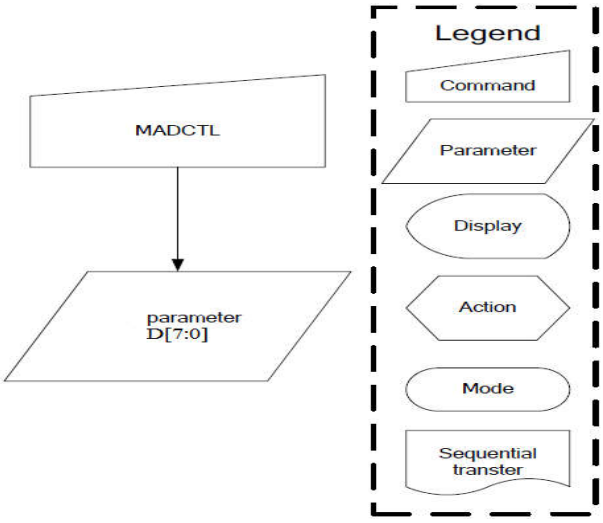
Bit D3- RGB/BGR Order

"0" = RGB (When MADCTL D3="0")

"1" = BGR (When MADCTL D3="1")

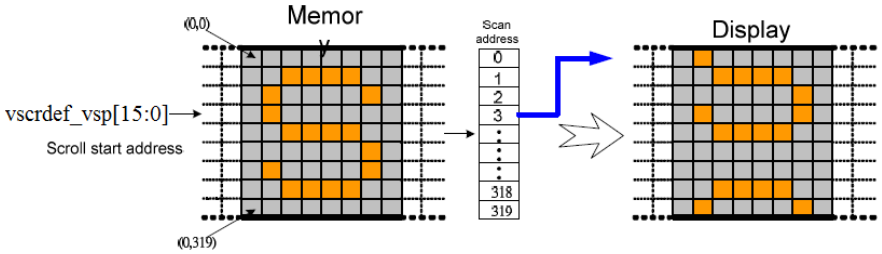


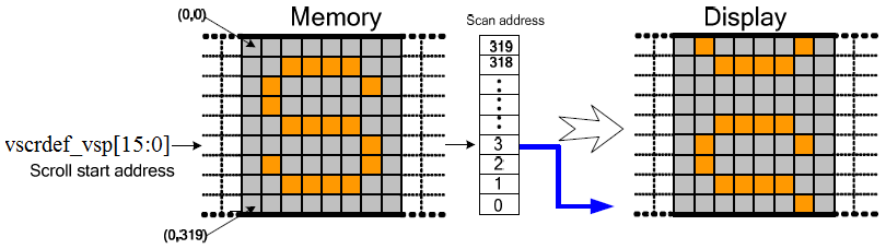


<table>
<tr><td></td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>no change</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

7.1.28 vertical scrolling start address (37h)

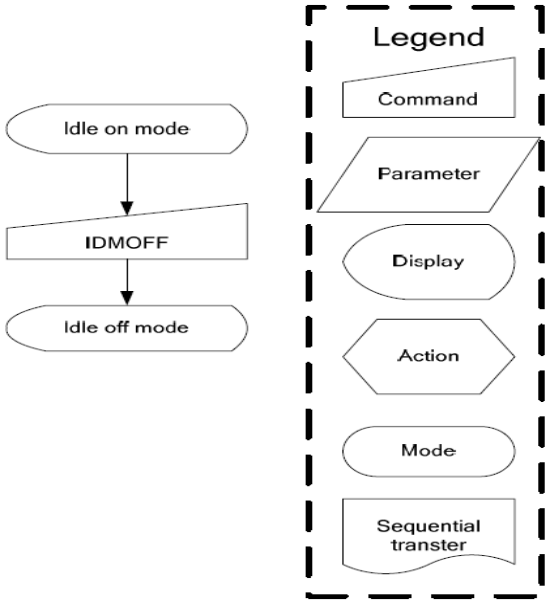
37h	vertical scrolling start address									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
vertical scrolling start address	W	0	0	1	1	0	1	1	1	(37h)
1st parameter	W	vscrdef_vsp[15:8]								00h
2nd parameter	W	vscrdef_vsp[7:0]								00h

<table>
<tr><td>Description</td><td>
This command is used together with Vertical scrolling (33h).
These two commands describe the scrolling area and the scrolling mode.
The Vertical scrolling start address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
When ml='0'
Example:
When Top Fixed Area = Bottom Fixed Area = 00, vertical scrolling area = 320 and vscrdef_vsp = '3'.


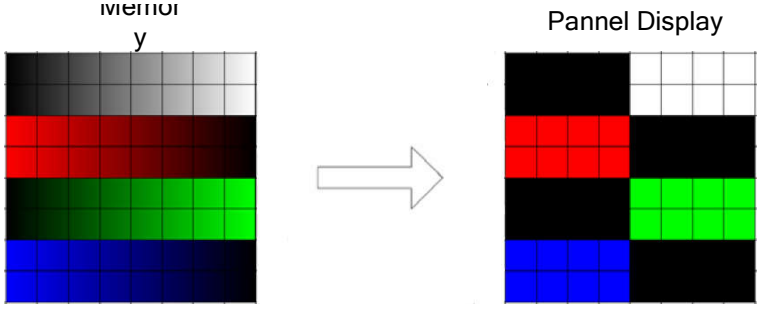
When ml='1'
Example:
When Top Fixed Area = Bottom Fixed Area = 00, vertical scrolling area = 320 and vscrdef_vsp = '3'.


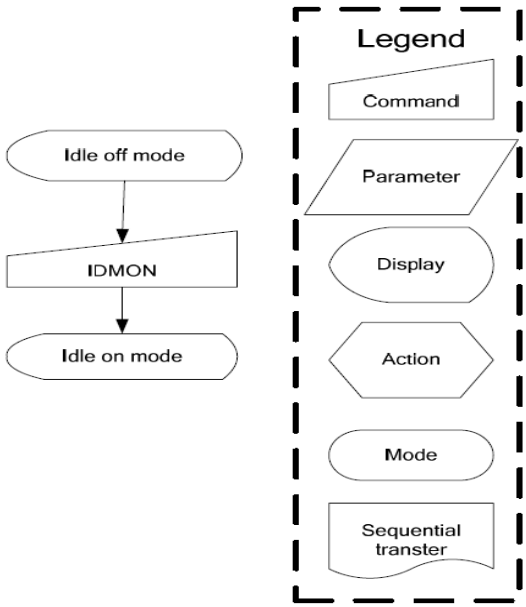
Note: When new pointer position and picture data are sent, the result on the display will happen at the next panel scan to avoid tearing effect.
Vscrdef_vsp refers to the Frame Memory line pointer.
</td></tr>
<tr><td>Restriction</td><td>Since the value of the vertical scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by vertical scrolling (33h)- otherwise undesirable image will be displayed on the panel).</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td></tr>
<tr><td>S/W Reset</td><td>0000h</td></tr>
<tr><td>H/W Reset</td><td>0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

7.1.29 idle mode off (38h)

<table>
<tr><th>38h</th><th colspan="10">idle mode off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>idle mode off</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>(38h)</td></tr>
<tr><td>parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from idle mode on.
In the idle off mode
1. LCD can display 65k or 262k colors.
2. Normal frame frequency is applied.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode off</td></tr><tr><td>S/W Reset</td><td>Idle mode off</td></tr><tr><td>H/W Reset</td><td>Idle mode off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.1.30 idle mode on and other mode off (39h)

<table>
<tr><th>39h</th><th colspan="9">idle mode on and other mode off</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>idle mode on and other mode off</td><td>W</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>(39h)</td></tr>
<tr><td>parameter</td><td colspan="9">No Parameter</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to enter into idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the idle on mode,
1. Color expression is reduced. The colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from idle mode on by idle mode off (38h) command.
 
<table>
<tr><th>Color</th><th>R5 R4 R3 R2 R1 R0</th><th>G5 G4 G3 G2 G1 G0</th><th>B5 B4 B3 B4 B1 B0</th></tr>
<tr><td>Black</td><td>0xxxxx</td><td>0xxxxx</td><td>0xxxxx</td></tr>
<tr><td>Blue</td><td>0xxxxx</td><td>0xxxxx</td><td>1xxxxx</td></tr>
<tr><td>Red</td><td>1xxxxx</td><td>0xxxxx</td><td>0xxxxx</td></tr>
<tr><td>Magenta</td><td>1xxxxx</td><td>0xxxxx</td><td>1xxxxx</td></tr>
<tr><td>Green</td><td>0xxxxx</td><td>1xxxxx</td><td>0xxxxx</td></tr>
<tr><td>Cyan</td><td>0xxxxx</td><td>1xxxxx</td><td>1xxxxx</td></tr>
<tr><td>Yellow</td><td>1xxxxx</td><td>1xxxxx</td><td>0xxxxx</td></tr>
<tr><td>White</td><td>1xxxxx</td><td>1xxxxx</td><td>1xxxxx</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="9">This command has no effect when module is already in idle on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="9"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="9"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle mode off</td></tr>
<tr><td>S/W Reset</td><td>Idle mode off</td></tr>
<tr><td>H/W Reset</td><td>Idle mode off</td></tr>
</table></td></tr>
</table>

Flow Chart	

7.1.31 interface pixel format (3Ah)

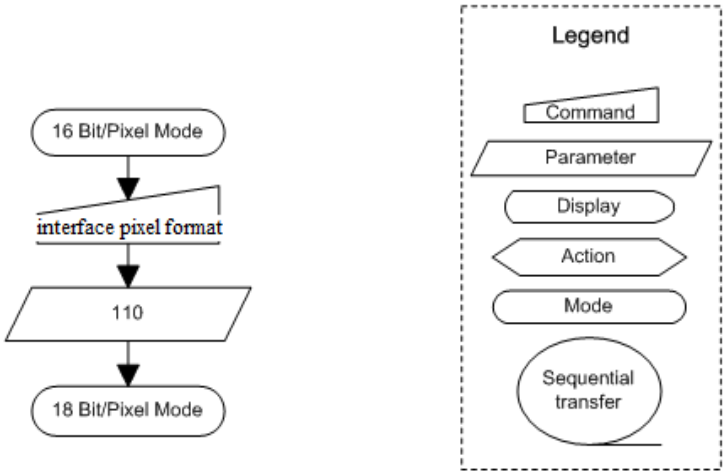
3Ah	interface pixel format									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
interface pixel format	W	0	0	1	1	1	0	1	0	(3Ah)
1st Parameter	W	X	dpi[2:0]			X	dbi[2:0]			66h

Description

dpi[2:0] is the pixel format select of RGB interface.

dbi[2:0] is the pixel format of system interface. If using RGB interface, serial interface must be selected.

dpi[2:0]			RGB interface format	dbi[2:0]			system interface format
0	0	0	reserved	0	0	0	reserved
0	0	1	reserved	0	0	1	reserved
0	1	0	reserved	0	1	0	reserved
0	1	1	reserved	0	1	1	12 bits/pixel
1	0	0	reserved	1	0	0	reserved
1	0	1	16 bits/pixel	1	0	1	16 bits/pixel
1	1	0	18 bits/pixel	1	1	0	18 bits/pixel
1	1	1	reserved	1	1	1	reserved

<table>
<tr><td></td><td>“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td>There is no visible effect until the Frame Memory is written to.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>66h</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>66h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>Example:
 
</td></tr>
</table>

7.1.32 write memory continue (3Ch)

3Ch	write memory continue									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
write memory continue	W	0	0	1	1	1	1	0	0	(3Ch)
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write memory continue or memory write command. If mv= '0': Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (caset_ec) value. The column register is then reset to caset_sc and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (paset_ep) value and the column register equals the caset_ec value, or the host processor sends another command. If the number of pixels exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1) the extra pixels are ignored. If mv= '1': Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (paset_ep) value. The page register is then reset to paset_sp and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (caset_ec) value and the page register equals the paset_ep value, or the host processor sends another command. If the number of pixels exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1) the extra pixels are ignored.									
Restriction	A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

7.1.33 read memory continue (3Eh)

<table>
<tr><th>3Eh</th><th colspan="9">read memory continue</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read memory continue</td><td>R</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>(3Eh)</td></tr>
<tr><td>Description</td><td colspan="10">This command transfers image data from the display module’s frame memory to the MPU. The image data continues from the pixel location following the previous read memory continue or memory read command.
If mv= ’0’:
Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the end column (caset_ec) value. The column register is then reset to caset_sc and the page register is incremented. Pixels are read from the frame memory until the page register equals the end page (paset_ep) value and the column register equals the caset_ec value, or the MPU sends another command.
If mv= ‘1’:
Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the end page (paset_ep) value. The page register is then reset to paset_sp and the column register is incremented. Pixels are read from the frame memory until the column register equals the end column (caset_ec) value and the page register equals the paset_ep value, or the MPU sends another command.</td></tr>
<tr><td>Restriction</td><td colspan="10">Regardless of the color mode set in interface pixel format, the pixel format returned by read memory continue is always 18-bit so there is no restriction on the length of data.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

7.1.35 get tear scan line (45h)

<table>
<tr><th>45h</th><th colspan="10">get tear scan line</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>get tear scan line</td><td>R</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(45h)</td></tr>
<tr><td>1st Parameter</td><td>R</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="2">gts[9:8]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>R</td><td colspan="8">gts[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">The display module returns the current scanline gts, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.When in sleep in mode, the value returned by get scanline is undefined.
“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>S/W Reset</td><td>0000h</td></tr><tr><td>H/W Reset</td><td>0000h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.1.36 read idd3 (D3h)

<table>
<tr><th>D3h</th><th colspan="10">read idd3</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>read idd3</td><td>R</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(D3h)</td></tr>
<tr><td>1st parameter</td><td>R</td><td colspan="8">id[23:16]</td><td>30h</td></tr>
<tr><td>2nd parameter</td><td>R</td><td colspan="8">id[15:8]</td><td>31h</td></tr>
<tr><td>3rd parameter</td><td>R</td><td colspan="8">id[7:0]</td><td>FFh</td></tr>
<tr><td>Description</td><td colspan="11">This read byte returns 24-bits display identification information.
id[23:0]:LCD module/driver ID.</td></tr>
<tr><td>Restriction</td><td colspan="11"></td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="11"></td></tr>
</table>

7.1.37 read display id 1 (DAh)

DAh	read display id 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display id 1	R	1	1	0	1	1	0	1	0	(DAh)
1st parameter	R	id[23:16]								FFh
Description	id[23:16]:LCD module/driver ID.									
Restriction	-									

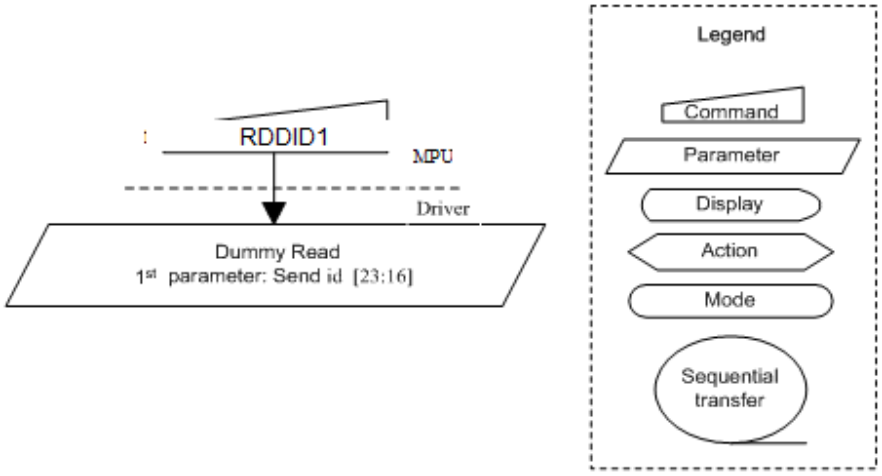
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



7.1.38 read display id 2 (DBh)

DBh	read display id 2									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display id 2	R	1	1	0	1	1	0	1	1	(DBh)
1st parameter	R	id[15:8]								FFh
Description	id[15:8]:LCD module/driver ID.									
Restriction	-									

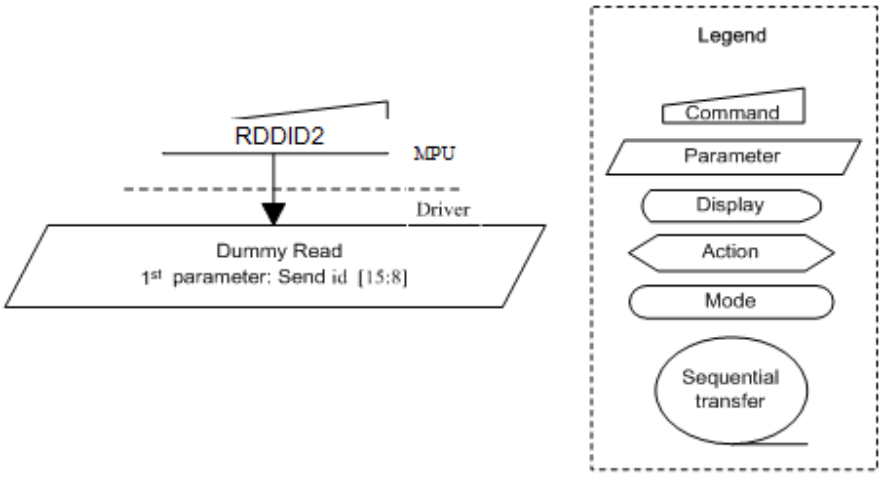
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	31h
S/W Reset	31h
H/W Reset	31h

Flow Chart



7.1.39 read display id 3 (DCh)

DCh	read display id 3									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
read display id 3	R	1	1	0	1	1	1	0	0	(DCh)
1st parameter	R	id[7:0]								FFh
Description	id[7:0]:LCD module/driver ID.									
Restriction	-									

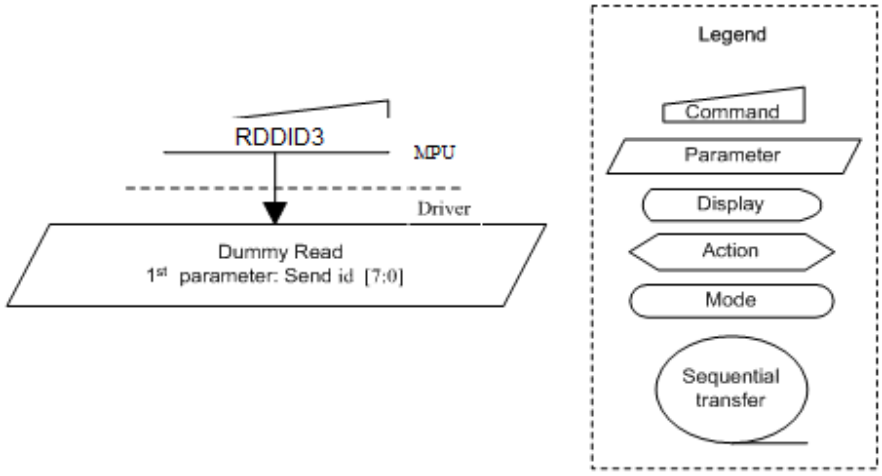
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	35h
S/W Reset	35h
H/W Reset	35h

Flow Chart



7.2 Private command

When enter read/write private register,need send 06h, 08h to FDh register;When exit read/write private register,need send fah, fch to FDh register.

Instruction	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
osc setting	RW	0	1	1	0	0	0	0	0	(60h)
	RW	X	X	0	osc_trim[3:0]					00h
vdd setting	RW	0	1	1	0	0	0	0	1	(61h)
	RW	X	X	X	X	X	vdd_adj[2:0]			07h
vgl setting	RW	0	1	1	0	0	0	1	1	(63h)
	RW	X	Pump5_clamp_en	X	Pump5_sel	X	Pump5_trim[2:0]			43h
	RW	X	X	X	X	Pump5_clamp[3:0]				04h
	RW	X	Pump5_off_frm[2:0]			X	Pump5_on_frm[2:0]			11h
	RW	X	Pump5_pu_off_frm[2:0]			X	Pump5_pu_on_frm[2:0]			20h
vgh setting	RW	0	1	1	0	0	1	0	0	(64h)
	RW	X	X	Pump4_sel[1:0]		X	Pump4_clamp[3:0]			24h
	RW	X	Pump4_trim[2:0]			X	Pump4_clamp_en	X	X	34h
	RW	X	X	X	X	X	X	Pump4_clk[1:0]		02h
	RW	X	Pump4_off_frm[2:0]			0	Pump4_on_frm[2:0]			22h
mv setting (VSP)	RW	0	1	1	0	0	1	0	1	(65h)
	RW	X	Pump1_clk[1:0]		X	Pump1_clamp_en	X	Pump1_clamp[1:0]		2Ah
	RW	X	X	X	Pump1_sel	0	Pump1_trim[2:0]			13h
	RW		Pump1_off_frm[2:0]				Pump1_on_frm[2:0]			20h
	RW	X	X	X	X	X	X	X	X	00h
mv setting (VSN)	RW	0	1	1	0	0	1	1	0	(66h)
	RW	X	X	X	X	Pump2_clamp_en	X	Pump2_clamp[1:0]		0Bh
	RW	X	X	X	pump2_sel	X	pump2_trim[2:0]			13h
	RW	X	pump2_off_frm[2:0]			X	pump4_on_frm[2:0]			20h
gamma ref 1	RW	0	1	1	0	1	0	0	0	(68h)
	RW	VAP[7:0]								00h
	RW	VAN[7:0]								1Ch
	RW	X	VCMP[6:0]							13h
	RW	X	VCOM_OFC[6:0]							13h
gamma ref 2	RW	X	X	VAP_VFB_TRIM[2:0]			VAP _TRIM[2:0]			00h
	RW	X	X	VAN_VFB_TRIM[2:0]			VAN _TRIM[2:0]			00h
	RW	X	X	X	X	X	VCMP_TRIM[2:0]			40h

vdds trim	RW	0	1	1	0	1	0	1	1	(6bh)
	RW	X	X	X	X	X	Vdds_res_trim[2:0]			04h
RGB interface control	RW	1	0	1	1	0	0	0	0	(B0h)
	RW	bypass_mode	rcm[1:0]		X	vspl	hspl	dpl	epl	40h
frame rate1 (normal)	RW	1	0	1	1	0	0	0	1	(B1h)
	RW	X	X	fr1_h[5:0]						24h
	RW	X	X	X	fr1_v[4:0]					06h
	RW	X	X	X	X	X	X	fr1_div[1:0]		03h
frame rate2 (partial)	RW	1	0	1	1	0	0	1	0	(B2h)
	RW	X	X	fr2_h[5:0]						24h
	RW	X	X	X	fr2_v[4:0]					06h
	RW	X	X	X	X	X	X	fr2_div[1:0]		03h
frame rate3 (8-color)	RW	1	0	1	1	0	0	1	1	(B3h)
	RW	X	X	fr3_h[5:0]						24h
	RW	X	X	X	fr3_v[4:0]					06h
	RW	X	X	X	X	X	X	fr3_div[1:0]		03h
display pol control	RW	1	0	1	1	0	1	0	0	(B4h)
	RW	X	X	X	X	X	dinv[2:0]			01h
blanking porch	RW	1	0	1	1	0	1	0	1	(B5h)
	RW	X	vfp[6:0]							02h
	RW	X	vbp[6:0]							02h
	RW	X	hfp[6:0]							0Ah
	RW	X	hbp[6:0]							14h
display function	RW	1	0	1	1	0	1	1	0	(B6h)
	RW	X	rev	X	sm	X	ptg	X	pts	02h
	RW	X	gs	X	ss	X	X	X	normal_black	00h
	RW	X	X	nl[5:0]						27h
	RW	X	X	scn[5:0]						00h
	RW	X	X	X	X	isc[3:0]				02h
entry mode set	RW	1	0	1	1	0	1	1	1	(B7h)
	RW	X	X	X	X	X	gon	dte	X	06h
gamma positive 1	RW	1	1	1	0	0	0	0	0	(E0h)
	RW	X	X	X	pkp0[4:0]					0Bh
	RW	X	X	X	pkp1[4:0]					17h
	RW	X	X	X	pkp2[4:0]					06h
	RW	X	X	X	pkp3[4:0]					10h

	RW	X	X	X	pkp4[4:0]					05h
	RW	X	X	X	pkp5[4:0]					12h
	RW	X	X	X	pkp6[4:0]					0Ah
gamma positive 2	RW	1	1	1	0	0	0	0	1	(E1h)
	RW	X	prp0[6:0]							1Bh
	RW	X	prp1[6:0]							5Ah
gamma positive 3	RW	1	1	1	0	0	0	1	0	(E2h)
	RW	X	X	vrp0[5:0]						0Ah
	RW	X	X	vrp1[5:0]						2Eh
	RW	X	X	vrp2[5:0]						27h
	RW	X	X	vrp3[5:0]						19h
	RW	X	X	vrp4[5:0]						18h
	RW	X	X	vrp5[5:0]						2Bh
gamma negative 1	RW	1	1	1	0	0	0	1	1	(E3h)
	RW	X	X	X	pkn0[4:0]					0Ch
	RW	X	X	X	pkn1[4:0]					19h
	RW	X	X	X	pkn2[4:0]					0Fh
	RW	X	X	X	pkn3[4:0]					19h
	RW	X	X	X	pkn4[4:0]					08h
	RW	X	X	X	pkn5[4:0]					13h
	RW	X	X	X	pkn6[4:0]					13h
gamma negative 2	RW	1	1	1	0	0	1	0	0	(E4h)
	RW	X	prn0[6:0]							1Bh
	RW	X	prn1[6:0]							5Ah
gamma negative 3	RW	1	1	1	0	0	1	0	1	(E5h)
	RW	X	X	vrn0[5:0]						0Ah
	RW	X	X	vrn1[5:0]						22h
	RW	X	X	vrn2[5:0]						20h
	RW	X	X	vrn3[5:0]						13h
	RW	X	X	vrn4[5:0]						0Ch
	RW	X	X	vrn5[5:0]						2Bh
Frame rate 4	RW	1	1	1	1	0	0	0	0	(F0h)
	RW	src_v[3:0]				src_h[3:0]				48h
interface control	RW	1	1	1	1	0	1	1	0	(F6h)
	RW	my_eor	mx_eor	mv_eor	0	bgr_eor	0	0	we_mode	09h
	RW	cs_delay_sel[1:0]		epf[1:0]				mdt[1:0]		10h

	RW		endian			dm[1:0]			rim	00h
	RW		spi_2wire_mode						rm	00h
private access	W	1	1	1	1	1	1	0	1	(FDh)
	W	private_access[15:8]								00h
	W	private_access[7:0]								00h

7.2.1 osc setting (60h)

<table>
<tr><th>60h</th><th colspan="10">osc setting</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>osc setting</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(60h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>0</td><td colspan="5">OSC_TRIM[3:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">osc_fresh[3:0]: Osc clock frequency adjust registers.
<table>
<tr><th>Osc_trim[3:0]</th><th>Freq(MHz)</th><th>Osc_trim[3:0]</th><th>freq(MHz)</th></tr>
<tr><td>0000</td><td>45.64</td><td>1000</td><td>43.31</td></tr>
<tr><td>0001</td><td>47.85</td><td>1001</td><td>41.57</td></tr>
<tr><td>0010</td><td>49.54</td><td>1010</td><td>40.29</td></tr>
<tr><td>0011</td><td>52.41</td><td>1011</td><td>38.84</td></tr>
<tr><td>0100</td><td>54.44</td><td>1100</td><td>37.95</td></tr>
<tr><td>0101</td><td>57.73</td><td>1101</td><td>36.55</td></tr>
<tr><td>0110</td><td>60.3</td><td>1110</td><td>35.54</td></tr>
<tr><td>0111</td><td>64.68</td><td>1111</td><td>34.45</td></tr>
</table></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>1008h</td></tr>
<tr><td>S/W Reset</td><td>no change</td></tr>
<tr><td>H/W Reset</td><td>1008h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.2 vdd setting (61h)

<table>
<tr><th>61h</th><th colspan="10">vdd setting</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>vdd setting</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(61h)</td></tr>
<tr><td>parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="3">vdd_adj[2:0]</td><td>07h</td></tr>
<tr><td>Description</td><td colspan="10">vdd_adj[1:0]:VDD setting is as below:
<table>
<tr><th>vdd_adj[2:0]</th><th>Value(V)</th></tr>
<tr><td>000</td><td>1.53</td></tr>
<tr><td>001</td><td>1.47</td></tr>
<tr><td>010</td><td>1.42</td></tr>
<tr><td>011</td><td>1.38</td></tr>
<tr><td>100</td><td>1.57</td></tr>
<tr><td>101</td><td>1.62</td></tr>
<tr><td>110</td><td>1.68</td></tr>
<tr><td>111</td><td>1.73</td></tr>
</table></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>01h</td></tr>
<tr><td>S/W Reset</td><td>no change</td></tr>
<tr><td>H/W Reset</td><td>01h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.3 vgl setting(63h)

63h	vgl setting									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
vgl setting	RW	0	1	1	0	0	0	1	1	(63h)
1st parameter	RW	X	Pump5_clamp_en	X	Pump5_sel	X	Pump5_trim[1:0]			13h
2nd parameter	RW	X	X	X	X	Pump5_clamp5[3:0]				04h
3rdparameter	RW	X	Pump5_off_frm[2:0]			X	Pump5_on_frm[2:0]			11h
4thparameter	RW	X	Pump5_pu_off_frm[2:0]			X	Pump5_pu_on_frm[2:0]			20h

Description

PUMP5_CLAMP_EN: Enable VGL clamp level.

PUMP5_CLAMP_EN	VGL clamp function
0	Disable
1	Enable

PUMP5_SEL: Sets the factor used in the step-up circuits for VGL.
Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

PUMP5_SEL	VGL OUTPUT
0	VGL Pump to -5*VCI
1	VGL Pump to -6*VCI

Pump5_trim[1:0]: VSN voltage adjustment.

VSN_ADJ	VSN
000	0%
001	-2.5%
010	-5.0%
011	-7.5%
100	+2.5%
101	+5.0%
110	+7.5%
111	0% & OCP Disable

PUMP5_CLAMP: Sets the VGL clamp level.

PUMP5_CLAMP[3:0]	VGL clamp level(V)
0000	-7.1
0001	-7.6
0010	-8.1
0011	-8.6
0100	-9.1
0101	-9.6
0110	-10.1
0111	-10.6
1000	-11.1
1001	-11.6
1010	-11.85
1011	-12.1
1100	-12.35
1101	-12.6
1110	-12.85
1111	-13.1

Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes

<table>
<tr><td></td><td></td><td><table>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td><td></td></tr>
<tr><td>Default</td><td colspan="3"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="3"></td></tr>
</table>

7.2.4 vgh setting (64h)

64h	vgh setting									
Inst / Para	WR	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
vgh setting	RW	0	1	1	0	0	1	0	0	(64h)
1st parameter	RW	X	X	Pump4_sel[1:0]		X	Pump4_clamp[2:0]			24h
2nd parameter	RW	X	Pump4_trim[2:0]			X	Pump4_clamp_en	X	X	34h
3rd parameter	RW	X	X	X	X	X	X	Pump4_clk[1:0]		02h
4th parameter	RW	X	Pump4_off_frm[2:0]			X	Pump4_on_frm[2:0]			22h

Description

PUMP4_SEL: Sets the factor used in the step-up circuits for VGH.
Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

PUMP4_SEL[1:0]	VGH OUTPUT
00	VGH Pump to 5*VCI
01	VGH Pump to 6*VCI
10	VGH Pump to 7*VCI
11	VGH Pump to 8*VCI

PUMP4_CLAMP: Sets the VGH clamp level.

PUMP4_CLAMP[3:0]	VGH clamp level(V)
0000	7.5
0001	9.5
0010	10.0
0011	10.5
0100	11.0
0101	11.5
0110	12.0
0111	12.5
1000	13.0
1001	13.5
1010	14.0
1011	14.5
1100	15.0
1101	15.5
1110	16.0
1111	16.5

Pump4_trim[2:0]: HV-regulator VGH voltage adjustment.

VGH_ADJ	VGH
000	0%
001	-1.3%
010	-2.7%
011	-4%
100	1.3%
101	3.3%
110	4.7%
111	0% & OCP Disable

PUMP4_CLAMP_EN: Enable VGH clamp level.

PUMP4_CLAMP_EN	VGH clamp function
0	Disable
1	Enable

PUMP45_CLK: Selects the operating frequency of the step-up circuit 4/5. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increase the current consumption. Adjust the frequency taking into account the trade-off between the display quality and the current consumption.

PUMP45_CLK [1:0]	Step-up cycle for step-up circuit 4/5
000	8 lines
001	4 lines
010	2 lines
011	1 line
100	1/2 line
101	1/4 line
110	1/8 line
111	Other setting inhibit

Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.5 mv setting (VSP) (65h)

<table>
<tr><th>66h</th><th colspan="10">mv setting (VSP)</th></tr>
<tr><td>Inst / Para</td><td>WR</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>mv setting</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(65h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td colspan="2">Pump1_clk[1:0]</td><td>X</td><td>Pump1_clamp_en</td><td></td><td colspan="2">Pump1_clamp[1:0]</td><td>2Ah</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>Pump1_sel</td><td>X</td><td colspan="3">Pump1_trim[2:0]</td><td>13h</td></tr>
<tr><td>3th parameter</td><td>RW</td><td>X</td><td colspan="3">Pump1_off_frm[2:0]</td><td>X</td><td colspan="3">Pum1_on_frm[2:0]</td><td>20h</td></tr>
<tr><td>Description</td><td colspan="10">
PUMP1_CLK[1:0]: .
<table>
<tr><th colspan="2">PUMP1_CLK</th><th>PUMP1 FREQ.</th></tr>
<tr><td colspan="2">0</td><td>0</td><td>3.33Meg</td></tr>
<tr><td colspan="2">0</td><td>1</td><td>4.7Meg</td></tr>
<tr><td colspan="2">1</td><td>0</td><td>5.5Meg</td></tr>
<tr><td colspan="2">1</td><td>1</td><td>6.67Meg</td></tr>
</table>
PUMP1_CLAMP_EN :
<table>
<tr><th>PUMP1_CLAMP_EN</th><th>Status</th></tr>
<tr><td>0</td><td>Disable VSP pump clamp function</td></tr>
<tr><td>1</td><td>Enable VSP pump clamp function</td></tr>
</table>
PUMP1_CLAMP: Set the VSP clamp level.
<table>
<tr><th colspan="2">PUMP1_CLAMP</th><th>VSP clamp level(V)</th></tr>
<tr><td colspan="2">0</td><td>0</td><td>6.2</td></tr>
<tr><td colspan="2">0</td><td>1</td><td>6.4</td></tr>
<tr><td colspan="2">1</td><td>0</td><td>6.6</td></tr>
<tr><td colspan="2">1</td><td>1</td><td>6.8</td></tr>
</table>
PUMP1_SEL: Select step-up circuit 1 operation mode.
<table>
<tr><th>PUMP1_SEL</th><th>step-up circuit 1 operation mode</th></tr>
<tr><td>0</td><td>VSP Pump to 2*VCI</td></tr>
<tr><td>1</td><td>VSP Pump to 3*VCI</td></tr>
</table>
Pump1_trim[2:0]: VSP voltage adjustment.
<table>
<tr><th>VSP_TRIM</th><th>VSP</th></tr>
<tr><td>000</td><td>0%</td></tr>
<tr><td>001</td><td>-2.5%</td></tr>
<tr><td>010</td><td>-5.0%</td></tr>
<tr><td>011</td><td>-7.5%</td></tr>
<tr><td>100</td><td>+2.5%</td></tr>
<tr><td>101</td><td>+5.0%</td></tr>
<tr><td>110</td><td>+7.5%</td></tr>
<tr><td>111</td><td>0% & OCP Disable</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.6 mv setting (VSN) (66h)

<table>
<tr><th>66h</th><th colspan="10">mv setting (VSN)</th></tr>
<tr><td>Inst / Para</td><td>WR</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>mv setting</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>(66h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>Pump2_clamp_en</td><td colspan="2">Pump2_clamp[1:0]</td><td></td><td>0Bh</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>Pump2_sel</td><td>X</td><td colspan="3">Pump2_trim[2:0]</td><td>13h</td></tr>
<tr><td>3th parameter</td><td>RW</td><td>X</td><td colspan="3">Pump2_off_frm[2:0]</td><td>X</td><td colspan="3">Pum2_on_frm[2:0]</td><td>20h</td></tr>
<tr><td>Description</td><td colspan="10">
PUMP2_CLAMP_EN :
<table>
<tr><th>PUMP2_CLAMP_EN</th><th>Status</th></tr>
<tr><td>0</td><td>Disable VSN pump clamp function</td></tr>
<tr><td>1</td><td>Enable VSN pump clamp function</td></tr>
</table>
PUMP2_CLAMP[1:0]: Set the VSN clamp level.
<table>
<tr><th colspan="2">PUMP2_CLAMP</th><th>VSN clamp level(V)</th></tr>
<tr><td colspan="2">0</td><td>0</td><td>-4.4</td></tr>
<tr><td colspan="2">0</td><td>1</td><td>-4.6</td></tr>
<tr><td colspan="2">1</td><td>0</td><td>-4.8</td></tr>
<tr><td colspan="2">1</td><td>1</td><td>-5.0</td></tr>
</table>
PUMP2_SEL: Select step-up circuit 2 operation mode.
<table>
<tr><th>PUMP2_SEL</th><th>step-up circuit 2 operation mode</th></tr>
<tr><td>0</td><td>VSN Pump to -1*VCI</td></tr>
<tr><td>1</td><td>VSN Pump to -2*VCI</td></tr>
</table>
PUMP2_TRIM[2:0]: VSN voltage adjustment.
<table>
<tr><th>VSN_TRIM</th><th>VSN</th></tr>
<tr><td>000</td><td>0%</td></tr>
<tr><td>001</td><td>-2.5%</td></tr>
<tr><td>010</td><td>-5.0%</td></tr>
<tr><td>011</td><td>-7.5%</td></tr>
<tr><td>100</td><td>+2.5%</td></tr>
<tr><td>101</td><td>+5.0%</td></tr>
<tr><td>110</td><td>+7.5%</td></tr>
<tr><td>111</td><td>0% & OCP Disable</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.6 vdds trim (6bh)

<table>
<tr><th>6bh</th><th colspan="10">vdds trim</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>vdds trim</td><td>RW</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>(66h)</td></tr>
<tr><td>parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="3">vdds_res_trim[2:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">vdds_res_trim[2:0]: VDDS setting is as below:
<table>
<tr><th>vdds_res_trim[2:0]</th><th>Value(V)</th></tr>
<tr><td>000</td><td>1.82</td></tr>
<tr><td>001</td><td>1.69</td></tr>
<tr><td>010</td><td>1.57</td></tr>
<tr><td>011</td><td>1.47</td></tr>
<tr><td>100</td><td>1.98</td></tr>
<tr><td>101</td><td>2.16</td></tr>
<tr><td>110</td><td>2.38</td></tr>
<tr><td>111</td><td>2.62</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>04h</td></tr>
<tr><td>S/W Reset</td><td>no change</td></tr>
<tr><td>H/W Reset</td><td>04h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.7 gamma ref 1 (68h)

68h	gamma ref 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma ref 1	RW	0	1	1	0	1	0	0	0	(68h)
1st parameter	RW	VAP[7:0]								90h
2nd parameter	RW	VAN[7:0]								30h
3rd parameter	RW	X	VCMP[6:0]							27h
4th parameter	RW	X	VCOM_OFC[6:0]							21h

Description

VAP_CTRL value must lower than VSP

VAP	Value(V)
8'B00000000	3.6
:	:
8'B10001110	5.375
8'B10001111	5.3875
8'B10010000	5.4
:	:
8'B01111111	6.7875

VAN_CTRL value must higher than VSN

VAN	Value(V)
8'B00000000	-4.9875
:	:
8'B01101111	-3.6
8'B01110000	-3.5875
8'B01110001	-3.575
:	:
8'B01111111	-1.8

VCMP	Value(V)
7'B0000000	0.0125
:	:
7'B1001110	0.9875
7'B1001111	1
7'B1010000	1.0125
:	:
7'B0111111	1.6

Trim gamma voltage.
VAP = VAP[7:0] + VCOM_OFC[6:0]
VAN = VAN[7:0] + VCOM_OFC[6:0]
VCMP = VCMP[6:0] + VCOM_OFC[6:0]

Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes

		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes
Default			
Flow Chart			

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

7.2.8 RGB interface control (B0h)

B0h	RGB interface control									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
RGB interface control	RW	1	0	1	1	0	0	0	0	(B0h)
parameter	RW	bypass_mode	rcm[1:0]		X	vspl	hspl	dpl	epl	40h

Description

Set the operation status of display interface. The setting becomes effective as soon as the command is seted.

Bit	Description	Value	Comment
bypass_mode	Select the display data bypass	0	through memory
		1	direct to shift register
vspl	VSYNC polarity	0	Low level sync clock
		1	High level sync clock
hspl	HSYNC polarity	0	Low level sync clock
		1	High level sync clock
dpl	Dot clock polarity	0	data fetched at the rising time
		1	data fetched at the falling time
epl	DE polarity	0	High enable for RGB interface
		1	Low enable for RGB interface

rcm[1:0]:RGB interface enable mode selection.

rcm[1:0]	Mode
00	system interface
01	
10	RGB DE mode
11	RGB SYNC mode

"X" = Don't care.

Restriction -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes

		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes
Default			

Status	Default Value
Power On Sequence	40h
S/W Reset	40h
H/W Reset	40h

Flow Chart	

7.2.9 frame rate1 (normal) (B1h)

B1h	frame rate1 (normal)									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
frame rate1	RW	1	0	1	1	0	0	0	1	(B1h)
1st parameter	RW	X	X	fr1_h[5:0]						24h
2nd parameter	RW	X	X	X	fr1_v[4:0]					06h
3rd parameter	RW	X	X	X	X	X	X	fr1_div[1:0]		03h

Description

It is adjustable frame rate in normal mode.

fr1_h[5:0]: Adjustable the number of clocks.

fr1_v[4:0]: Adjustable the number of lines.

fr1_div[1:0]:set the division ratio of the internal oscillation clock, when NV3030A's display operation is synchronized with internal oscillation clock. NV3030A's internal operation is synchronized with the frequency divided internal oscillation clock. When changing the fr1_div[1:0] setting, the width of the reference clock for liquid crystal panel control signals is changed.

fr1_div[1:0]	Division Ratio	Internal Operation Clock Unit
2'h0	1/1 fosc	One OSC clock
2'h1	1/2 fosc	2 OSC clock
2'h2	1/3 fosc	3 OSC clock
2'h3	1/4 fosc	4 OSC clock

Frame Frequency Calculation

$$\text{Frame Frequency} = \frac{\text{Fosc}}{\text{fr1\_div[1:0]} \times (240 + \text{src\_h} + \text{fr1\_h[5:0]}) \times (320 + \text{src\_v} + \text{fr1\_v[4:0]})}$$

1.Fosc:RC oscillation frequency,adjustment by osc_trim and osc_fresh.

2.src_h:row pitch during source normal work.Source current row pitch is clock number.Insure source finished transfer and latched data when adjust the frame frequency.

3.src_v: interval frame during normal work.

4. fr1_h[5:0]: Adjustable the number of clocks. fr1_v[4:0]:Adjustable the number of lines.

5. fr1_div[1:0]: Division Ratio of clocks.

"X" = Don't care.

Restriction	

Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>920Bh</td></tr><tr><td>S/W Reset</td><td>920Bh</td></tr><tr><td>H/W Reset</td><td>920Bh</td></tr></table>
Flow Chart	

7.2.10 frame rate2 (partial) (B2h)

B2h	**frame rate2 (partial)**									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
frame rate2	RW	1	0	1	1	0	0	1	0	(B2h)
1st parameter	RW	X	X	fr2_h[5:0]						24h
2nd parameter	RW	X	X	X	fr2_v[4:0]					06h
3rd parameter	RW	X	X	X	X	X	X	fr2_div[1:0]		03h
Description	It is adjustable frame rate in partial mode. See frame rate1(B1h) for detail description. “X” = Don’t care.									
Restriction	-									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>920Bh</td></tr><tr><td>S/W Reset</td><td>920Bh</td></tr><tr><td>H/W Reset</td><td>920Bh</td></tr></table>									
Flow Chart										

7.2.11 frame rate3 (8-color) (B3h)

<table>
<tr><th>B3h</th><th colspan="10">frame rate3 (8-color)</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>frame rate3</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>(B3h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td>X</td><td colspan="6">fr3_h[5:0]</td><td>24h</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td colspan="5">fr3_v[4:0]</td><td>06h</td></tr>
<tr><td>3rd parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="2">fr2_div[1:0]</td><td>03h</td></tr>
<tr><td>Description</td><td colspan="10">It is adjustable frame rate in idle mode.
See frame rate1(B1h) for detail description.
“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>920Bh</td></tr><tr><td>S/W Reset</td><td>920Bh</td></tr><tr><td>H/W Reset</td><td>920Bh</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.12 display pol control (B4h)

<table>
<tr><th>B4h</th><th colspan="10">display pol control</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>display pol control</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(B4h)</td></tr>
<tr><td>parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="3">dinv[2:0]</td><td>01h</td></tr>
<tr><td>Description</td><td colspan="10">dinv: Inversion setting in full colors normal mode (Normal Mode On).
<table>
<tr><th colspan="3">dinv</th><th>Inversion</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Colum Inversion</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1 dot inversion</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2 dot inversion</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3 dot inversion</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4 dot inversion</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Colum Inversion</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Colum Inversion</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Colum Inversion</td></tr>
</table>
“X” = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>01h</td></tr>
<tr><td>S/W Reset</td><td>01h</td></tr>
<tr><td>H/W Reset</td><td>01h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.13 blanking porch (B5h)

<table>
<tr><th>B5h</th><th colspan="10">blanking porch</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>blanking porch</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(B5h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td colspan="7">vfp[6:0]</td><td>02h</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td colspan="7">vbp[6:0]</td><td>02h</td></tr>
<tr><td>3rd parameter</td><td>RW</td><td>X</td><td colspan="7">hfp[6:0]</td><td>0Ah</td></tr>
<tr><td>4th parameter</td><td>RW</td><td>X</td><td colspan="7">hbp[6:0]</td><td>14h</td></tr>
<tr><td>Description</td><td colspan="10">vfp[6:0]/vbp[6:0]:The vfp[6:0] and vbp[6:0] bits specify the line number of vertical front and back porch period respectively.
hfp[6:0]/ hbp[6:0]:The hfp[6:0] and hbp [6:0] bits specify the dotclk number of horizontal front and back porch period respectively.
Note:when rim == 1， porch size is according to clock counter， isn’t according to pixel counter.
“X”: Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.14 display function (B6h)

B6h	display function									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
display function	RW	1	0	1	1	0	1	1	0	(B6h)
1st parameter	RW	X	rev	X	sm	X	ptg	X	pts	02h
2nd parameter	RW	X	gs	X	ss	X	X	X	normal_black	00h
3rd parameter	RW	X	X	nl[5:0]						27h
4th parameter	RW	X	X	scn[5:0]						00h
5th parameter	RW	X	X	X	X	isc[3:0]				02h

Description

normal_black: Panel selection. normal_black='0',normal white; normal_black='1',normal black.

pts: Determine source output in a non-display area in the partial display mode.

pts	Source output on non-display area
0	V63
1	V0

ptg:Set the scan mode in non-display area.

ptg	Gate outputs in non-display area
0	normal scan
1	Interval scan

rev: xor display inversion setting.

nl[5:0]: Set the number of gate line.

nl[5:0]	The number of gate line
0x00	8 gate line
0x01	16 gate line
0x02	24 gate line
…	…
0x27	320 gate line

gs: Gate scan direction.gs="0": Gate scan direction is 0→319;gs="1": Gate scan direction is 319 →0.

ss: selects the shift direction of outputs of the source driver. 0: Source output S1→S720; 1: Source output S720→S1.

sm: Gate interlace mode selection.sm="0": Gate scan using interlace mode. sm="1": Gate scan using non-interlace mode.

isc[3:0]: Specify the scan cycle of the gate driver when the ptg is seted to "1" in non-display area. The scan cycle can be set in odd number of frames from 0 to 31. In this case, polarity is inverted every scan cycle.

Isc[3:0]	Scan cycle	(Ffrm)=60HZ
0000	0 frame	-
0001	3 frame	50ms
0010	5 frame	84ms
0011	7 frame	117ms
0100	9 frame	150ms
0101	11 frame	184ms

<table>
<tr><td></td><td>
<table>
<tr><td>0110</td><td>13frame</td><td>217ms</td></tr>
<tr><td>0111</td><td>15frame</td><td>251ms</td></tr>
<tr><td>1000</td><td>17frame</td><td>284ms</td></tr>
<tr><td>1001</td><td>19frame</td><td>317ms</td></tr>
<tr><td>1010</td><td>21frame</td><td>351ms</td></tr>
<tr><td>1011</td><td>23 frame</td><td>384ms</td></tr>
<tr><td>1100</td><td>25frame</td><td>418ms</td></tr>
<tr><td>1101</td><td>27frame</td><td>451ms</td></tr>
<tr><td>1110</td><td>29 frame</td><td>484ms</td></tr>
<tr><td>1111</td><td>31frame</td><td>518ms</td></tr>
</table>
“X” = Don’t care.
</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td></td></tr>
<tr><td>S/W Reset</td><td></td></tr>
<tr><td>H/W Reset</td><td></td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td></td></tr>
</table>

7.2.15 entry mode set (B7h)

<table>
<tr><th>B7h</th><th colspan="9">entry mode set</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>entry mode set</td><td>RW</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>(B7h)</td></tr>
<tr><td>parameter</td><td>RW</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>gon</td><td>dte</td><td>X</td><td>06h</td></tr>
<tr><td>Description</td><td colspan="10">gon/dte: Set the output level of gate driver:
<table><tr><th>gon</th><th>dte</th><th>G1~G320 Gate Output</th></tr><tr><td>0</td><td>0</td><td>VGH</td></tr><tr><td>0</td><td>1</td><td>VGH</td></tr><tr><td>1</td><td>0</td><td>VGL</td></tr><tr><td>1</td><td>1</td><td>Normal display</td></tr></table>“X”: Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>06h</td></tr><tr><td>S/W Reset</td><td>06h</td></tr><tr><td>H/W Reset</td><td>06h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.16 gamma positive 1 (E0h)

E0h	gamma positive 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma positive 1	RW	1	1	1	0	0	0	0	0	(E0h)
1st parameter	RW	X	X	X	pkp0[4:0]					0Bh
2ndparameter	RW	X	X	X	pkp1[4:0]					11h
3rdparameter	RW	X	X	X	pkp2[4:0]					11h
4thparameter	RW	X	X	X	pkp3[4:0]					12h
5thparameter	RW	X	X	X	pkp4[4:0]					10h
6thparameter	RW	X	X	X	pkp5[4:0]					0Eh
7thparameter	RW	X	X	X	pkp6[4:0]					07h
8thparameter	RW	X	X	X	pkp7[4:0]					19h
Description	E0h is gamma adjust registers.See gamma correction section for reference. “X”：Don’t care.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.17 gamma positive 2 (E1h)

<table>
<tr><th>E1h</th><th colspan="9">gamma positive 2</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>gamma positive 2</td><td>RW</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(E1h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td colspan="7">prp0[6:0]</td><td>45h</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td colspan="7">prp1[6:0]</td><td>57h</td></tr>
<tr><td>Description</td><td colspan="10">E1h is gamma adjust registers.See gamma correction section for reference.
“X”: Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>1B5Ah</td></tr><tr><td>S/W Reset</td><td>no change</td></tr><tr><td>H/W Reset</td><td>1B5Ah</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.18 gamma positive 3 (E2h)

E2h	gamma positive 3									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma positive 3	RW	1	1	1	0	0	0	1	0	(E2h)
1st parameter	RW	X	X	vrp0[5:0]						00h
2nd parameter	RW	X	X	vrp1[5:0]						1Fh
3rd parameter	RW	X	X	vrp2[5:0]						36h
4th parameter	RW	X	X	vrp3[5:0]						1Ch
5th parameter	RW	X	X	vrp4[5:0]						1Eh
6th parameter	RW	X	X	vrp5[5:0]						3Fh
Description	E2h is gamma adjust registers.See gamma correction section for reference. “X”: Don’t care.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.19 gamma negative 1 (E3h)

E3h	gamma negative 1									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma negative 1	RW	1	1	1	0	0	0	1	1	(E3h)
1st parameter	RW	X	X	X	pkn0[4:0]					03h
2nd parameter	RW	X	X	X	pkn1[4:0]					11h
3rd Parameter	RW	X	X	X	pkn2[4:0]					18h
4th Parameter	RW	X	X	X	pkn3[4:0]					1Ah
5th parameter	RW	X	X	X	pkn4[4:0]					18h
6th Parameter	RW	X	X	X	pkn5[4:0]					13h
7th Parameter	RW	X	X	X	pkn6[4:0]					13h
8th Parameter	RW	X	X	X	Pkn7[4:0]					15h
Description	E3h is gamma adjust registers.See gamma correction section for reference. “X”: Don’t care.									
Restriction	-									
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes									
Default	Status / Default Value: Power On Sequence: S/W Reset: H/W Reset:									
Flow Chart										

7.2.20 gamma negative 2 (E4h)

<table>
<tr><th>E4h</th><th colspan="10">gamma negative 2</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>gamma negative 2</td><td>RW</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>(E4h)</td></tr>
<tr><td>1st parameter</td><td>RW</td><td>X</td><td colspan="7">prn0[6:0]</td><td>5Dh</td></tr>
<tr><td>2nd parameter</td><td>RW</td><td>X</td><td colspan="7">prn1[6:0]</td><td>45h</td></tr>
<tr><td>Description</td><td colspan="10">E4h is gamma adjust registers.See gamma correction section for reference.
“X”: Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>1B5Ah</td></tr><tr><td>S/W Reset</td><td>no change</td></tr><tr><td>H/W Reset</td><td>1B5Ah</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"></td></tr>
</table>

7.2.21 gamma negative 3 (E5h)

E5h	gamma negative 3									
Inst / Para	W//R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
gamma negative 3	RW	1	1	1	0	0	1	0	1	(E5h)
1st parameter	RW	X	X	vrn0[5:0]						3Fh
2nd parameter	RW	X	X	vrn1[5:0]						28h
3rd parameter	RW	X	X	vrn2[5:0]						24h
4th parameter	RW	X	X	vrn3[5:0]						2Ch
5th parameter	RW	X	X	vrn4[5:0]						1Dh
6th parameter	RW	X	X	vrn5[5:0]						00h
Description	E5h is gamma adjust registers.See gamma correction section for reference. “X”: Don’t care.									
Restriction	-									
Register Availability										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	
S/W Reset	
H/W Reset	

Flow Chart

7.2.22 Frame Rate 4 (F0h)

<table>
<tr><th>F0h</th><th colspan="9">Frame Rate 4</th></tr>
<tr><td>Inst / Para</td><td>W/R</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HW RST</td></tr>
<tr><td>Frame Rate4</td><td>RW</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F0h</td></tr>
<tr><td>1st Parameter</td><td>RW</td><td colspan="4">src_v[3:0]</td><td colspan="4">src_h[3:0]</td><td>48h</td></tr>
<tr><td>Description</td><td colspan="10">src_h[3:0]:row pitch during source normal work.Source current row pitch is clock number.Insure source finished transfer and latched data when adjust frame rate.
src_v[3:0]: interval frame during normal work.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>48h</td></tr><tr><td>S/W Reset</td><td>48h</td></tr><tr><td>H/W Reset</td><td>48h</td></tr></table></td></tr>
</table>

7.2.23 Interface control (F6h)

F6h	Interface control									
Inst / Para	W/ R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
Interface control	RW	1	1	1	1	0	1	1	0	F6h
1st parameter	RW	my_eor	mx_eor	mv_eor	X	bgr_eor	X	X	we_mode	09h
2nd parameter	RW	cs_delay_sel[1:0]		epf[1:0]			mdt[1:0]			10h
3rd parameter	RW	X	endian	X	X	dm[1:0]		X	rim	00h
4th parameter	RW	X	spi_2wire_ mode	X	X	X	X	X	rm	00h

Description

my_eor/mx_eor/mv_eor/bgr_eor:the set of value MADCTL is used in the IC is derived as exclusive OR between first parameter of interface control and MADCTL parameter.

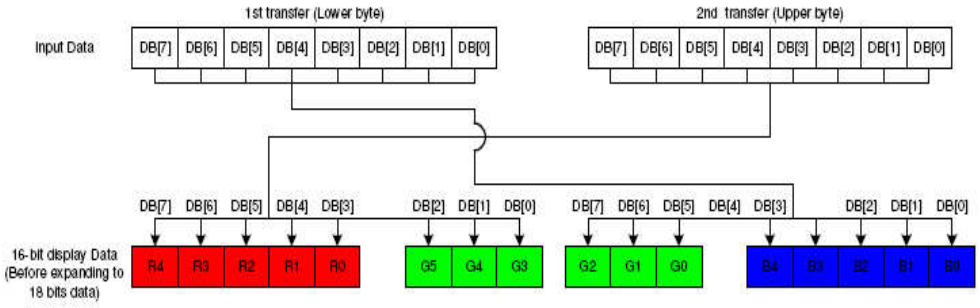
mdt[1:0]:select the method of display data transferring.
we_mode:memory write control.
we_mode=0:when the transfer number of data exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1), the exceeding data will be ignored.
we_mode=1:when the transfer number of data exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

spi_2wire_mode:enable 2 data lane serial interface mode.

endian: select the little endian interface bit. At little endian mode, the MPU sends LSB data first.

endian	Data transfer mode
0	Normal (MSB first)
1	Little endian (LSB first)

Note: the little endian is valid on only 65k 8bit and 9bit parallel interface mode.



dm[1:0]: select the display operation mode.

dm[1]	dm[0]	Display operation mode
0	0	Internal clock operation
0	1	RGB interface mode
1	0	reserved
1	1	reserved

The dm[1:0] setting allows switching between internal clock operation mode and external display interface operation mode.
rm:select the interface to access the GRAM.

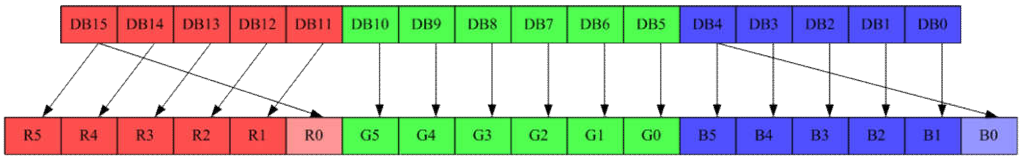
rm	Interface for RAM access
0	system interface
1	RGB interface

rim: specify the RGB interface mode when RGB interface is used. These bits should be set before display operation through RGB interface and should not be set during operation.

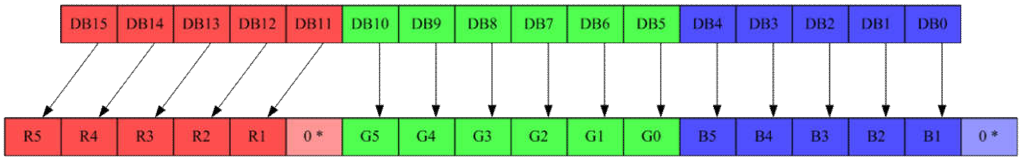
rim	dpi[1:0]	Display operation mode
0	110(262k color)	18 bit RGB interface (1 transfer/pixel)
	101(65k color)	16 bit RGB interface (1 transfer/pixel)
1	110(262k color)	6 bit RGB interface (3 transfer/pixel)
	101(65k color)	6 bit RGB interface (3 transfer/pixel)

epf[1:0]:

epf = 00

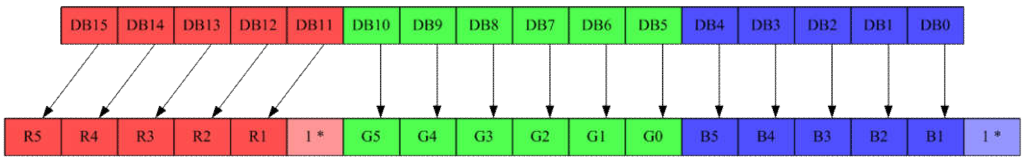


epf = 01



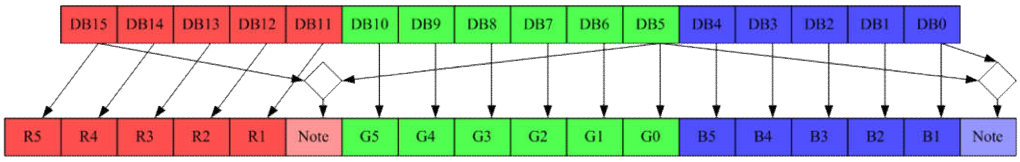
Note: Exception
1. R0 = 1 when R5~R1 = 1111
2. B0 = 1 when B4~B1 = 1111

epf = 10



Note: Exception
1. R0 = 0 when R5~R1 = 0000
2. B0 = 0 when B4~B1 = 0000

epf = 11



Note:
1. If DB15~DB11 = DB10~DB6, R0 = DB5, else R0 = DB15
2. If DB4~DB0 = DB10~DB16, B0 = DB5, else B0 = DB0

"X" = Don't care.

Restriction	

Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out — Yes; Normal Mode On, Idle Mode On, Sleep Out — Yes; Partial Mode On, Idle Mode Off, Sleep Out — Yes; Partial Mode On, Idle Mode On, Sleep Out — Yes; Sleep In — Yes
Default	Status / Default Value: Power On Sequence; S/W Reset; H/W Reset

7.2.24 Private access (FDh)

FDh	Private access									
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	HW RST
Private access	RW	1	1	1	1	1	1	0	1	FDh
1st Parameter	RW	private_access[15:8]								00h
2nd Parameter	RW	private_access[7:0]								00h
Description	private_access[15:0] : private registers access control.									

private access	private_access[15:8]	private_access[7:0]
enter private registers mode	06h	07h
exit private registers mode	FAh	FBh

Restriction	
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out — Yes; Normal Mode On, Idle Mode On, Sleep Out — Yes; Partial Mode On, Idle Mode Off, Sleep Out — Yes; Partial Mode On, Idle Mode On, Sleep Out — Yes; Sleep In — Yes
Default	Status / Default Value: Power On Sequence — 0000h; S/W Reset — 0000h; H/W Reset — 0000h

8. Functional description

8.1 Interface

8.1.1 Serial Interface

PAD Name	Serial Interface Pin Name	Description
CSX	CSX	A chip select signal.Signal is active low.
DCX	SCL	This pin is used serial interface clock.
WRX	DCX/SDI2	SPI 4-wire system: Serves as command or parameter select. 2 data lane serial interface: the second data lane. QSPI interface: the second data pin
SDA	SDA/SDI	SDA(When serial I/F Ⅰ): it is SPI and QSPIinterface input/output pin. SDI(When serial I/F Ⅱ): it is SPI interface input pin.
SDO	SDO	SPI interface output pin.
DB[0]	DB[0]	the third pin of qspi
DB[1]	DB[1]	the fourth pin of qspi

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

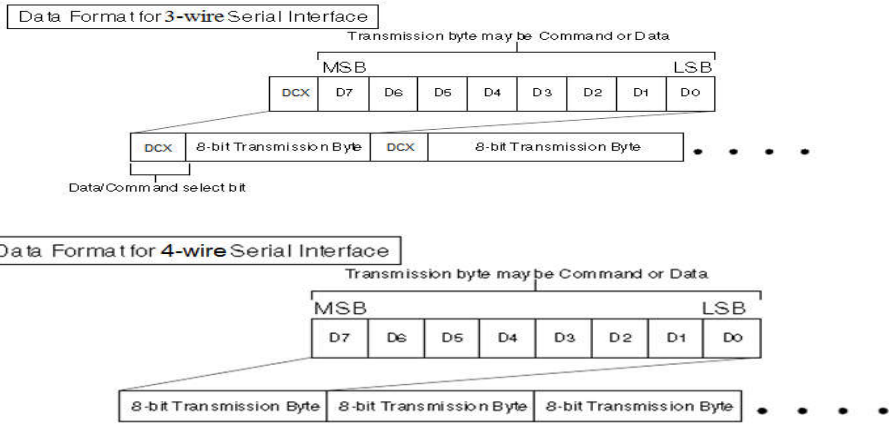
IM3	IM2	IM1	IM0	System Interface Mode	CSX	DCX	SCL	Function
0	1	0	0	qspi	“L”	-		Read/Write command, parameter or display data.
0	1	0	1	3-wire serial interface 2 data lane serial interface	“L”	-		Read/Write command, parameter or display data.
0	1	1	0	4-wire serial interface	“L”	“H/L”		Read/Write command, parameter or display data.
1	1	0	1	3-wire serial interface	“L”	-		Read/Write command, parameter or display data.
1	1	1	0	4-wire serial interface	“L”	“H/L”		Read/Write command, parameter or display data.

NV3030A supplies 3-wire/ 9-bit and 4-wire/8-bit bi-directional serial interfaces for communication between MPU and NV3030A. The 3-wire serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDA/SDO). The 4-wire serial mode consists of the Data/Command selection input (DCX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDA/SDO) for data transmission. The data bus (D[17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary.

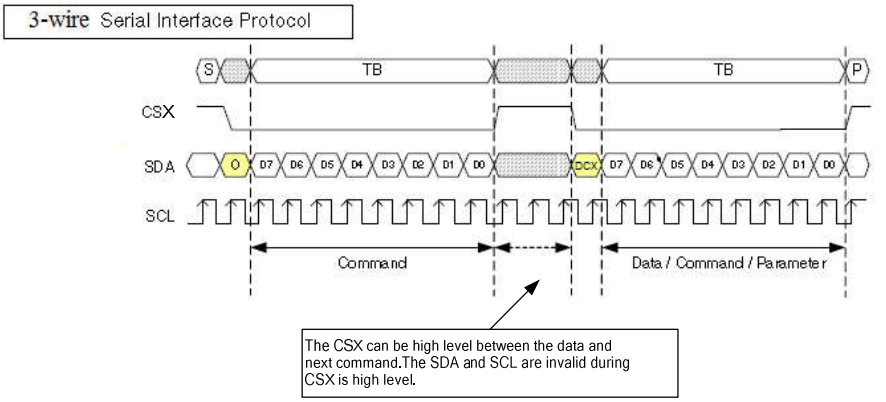
8.1.1.1 Write Cycle Sequence

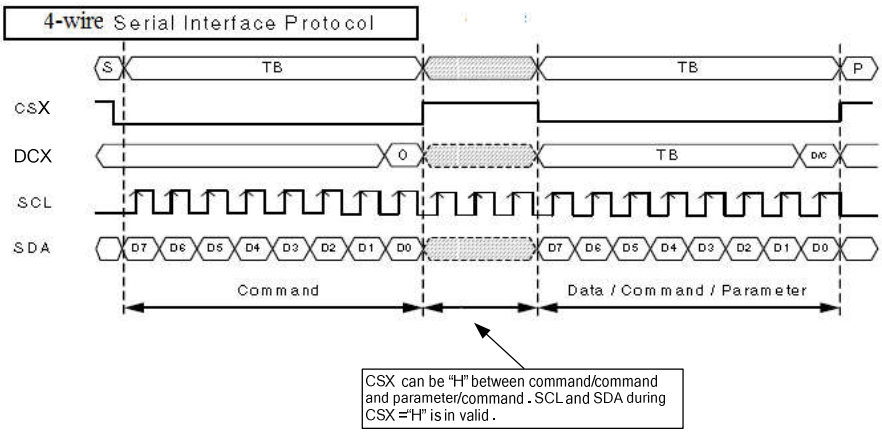
The write mode of the interface means that MPU writes commands or data to NV3030A. The 3-wire serial data packet contains a data/command select bit (DCX) and a transmission byte. If the DCX bit is “low”, the transmission byte is interpreted as a command byte. If the DCX bit is “high”, the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to NV3030A and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-wire serial interface.



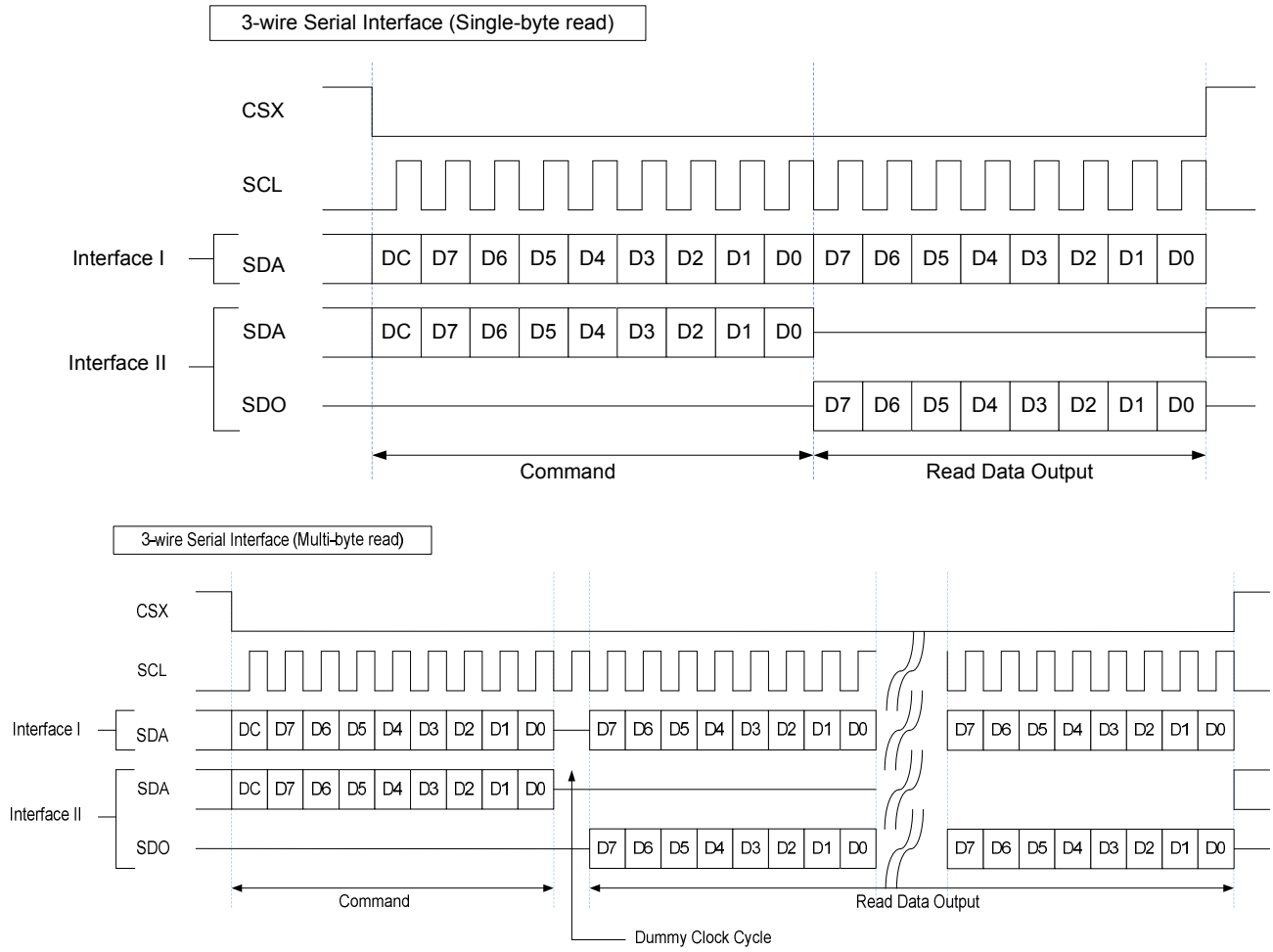
MPU drives the CSX pin to low and starts by setting the DCX bit on SDA. The bit is read by NV3030A on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the MPU. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional DCX signal is used, a byte is eight read cycle width. The 3/4-wire serial interface writes sequence described in the figure as below.



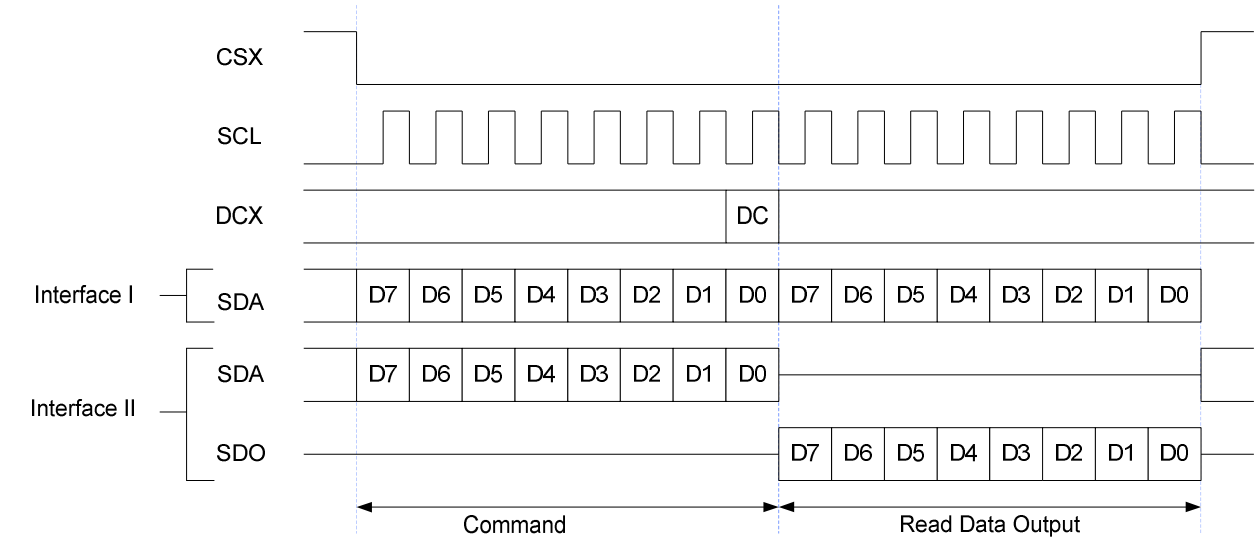


8.1.1.2 Read Cycle Sequence

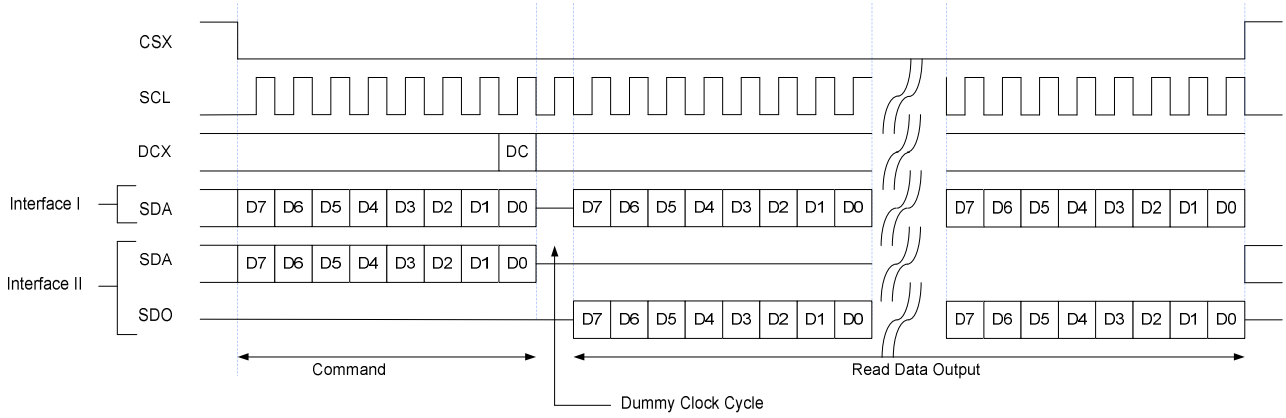
The read mode of interface means that the MPU reads register's parameter from NV3030A. The MPU has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. NV3030A latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has two types of transmitted command data (single/multi-byte) according to command code.



4-wire Serial Interface (Single-byte read)

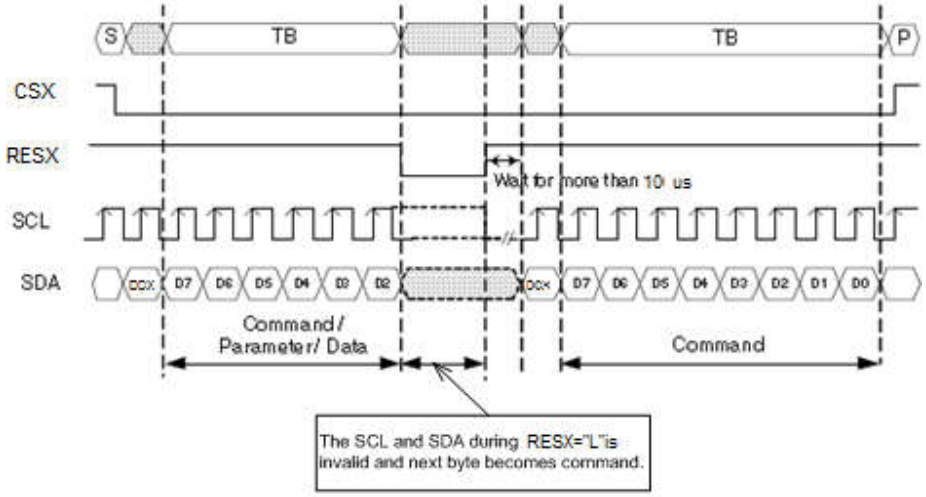


4-wire Serial Interface (Multi-byte read)

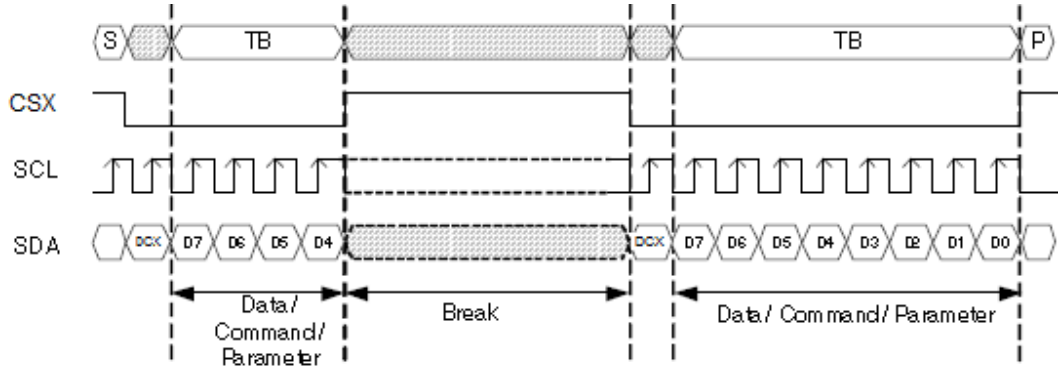


8.1.1.3 Data Transfer Break and Recovery

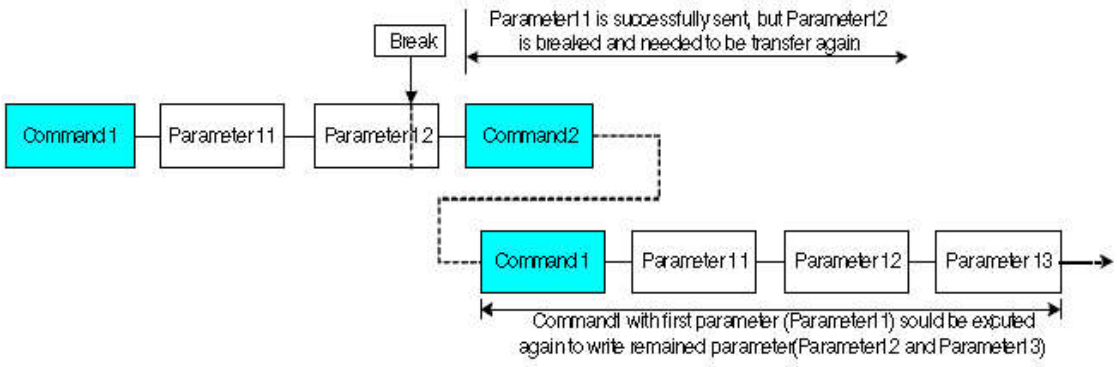
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



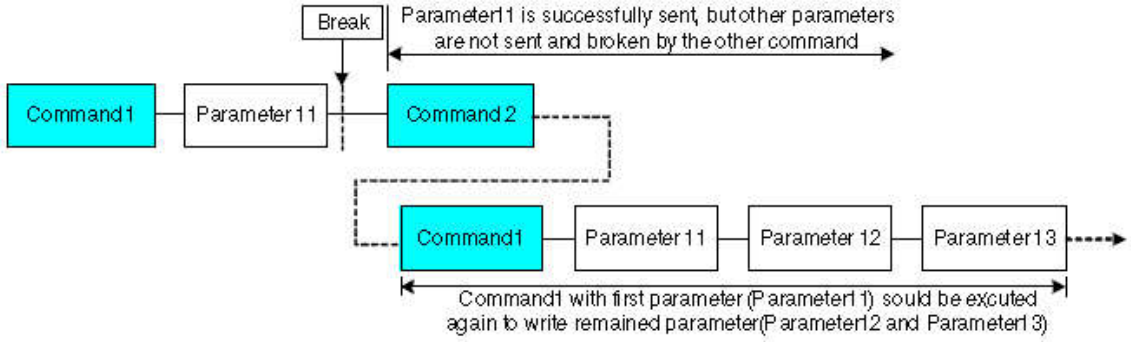
If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the MPU then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

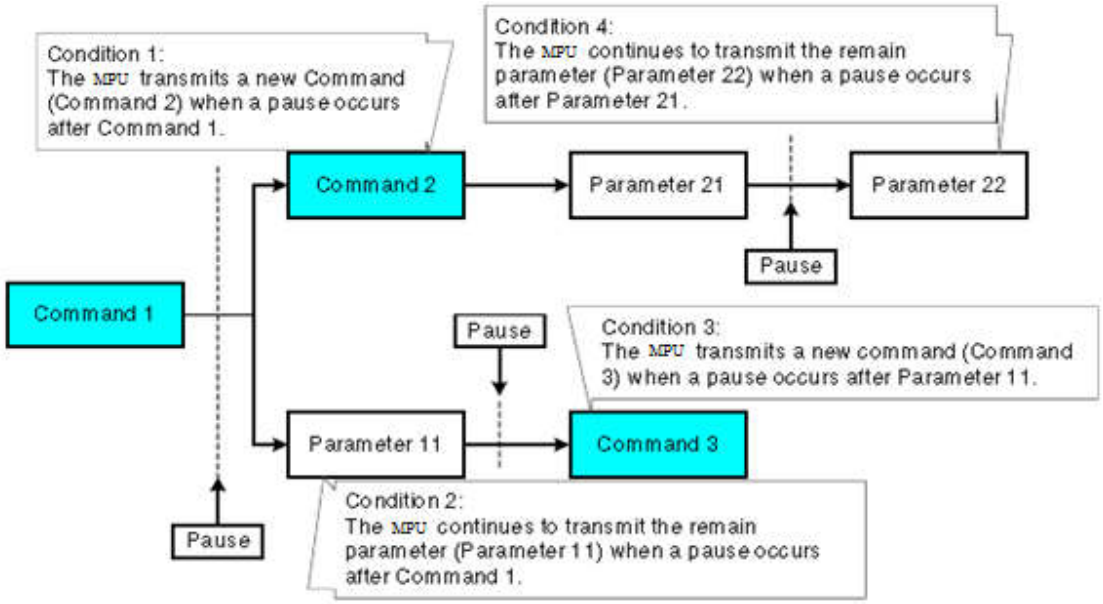
8.1.1.4 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then NV3030A will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.



This applies to the following 4 conditions:

1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter



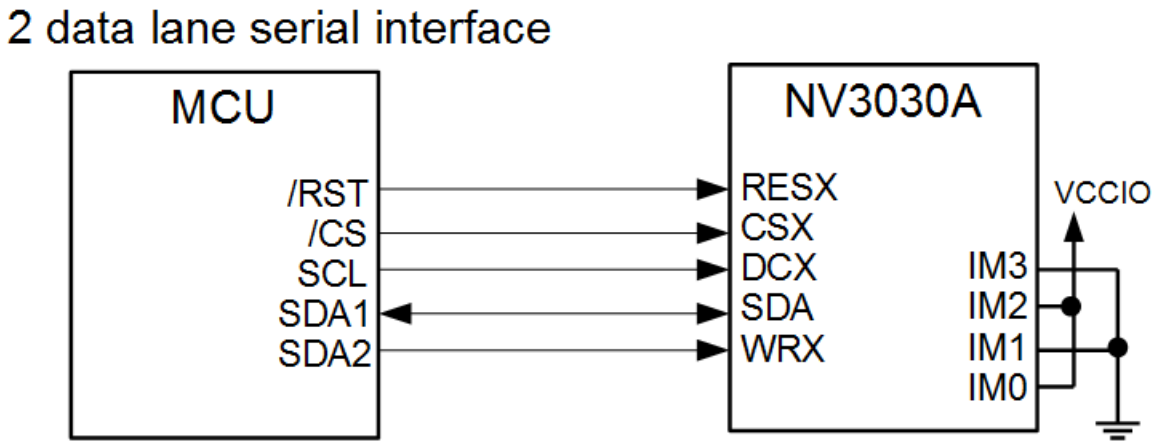
8.1.1.5 2 data lane serial interface

Interface selection:

IM3	IM2	IM1	IM0	Interface
0	1	0	1	2 data lane serial interface

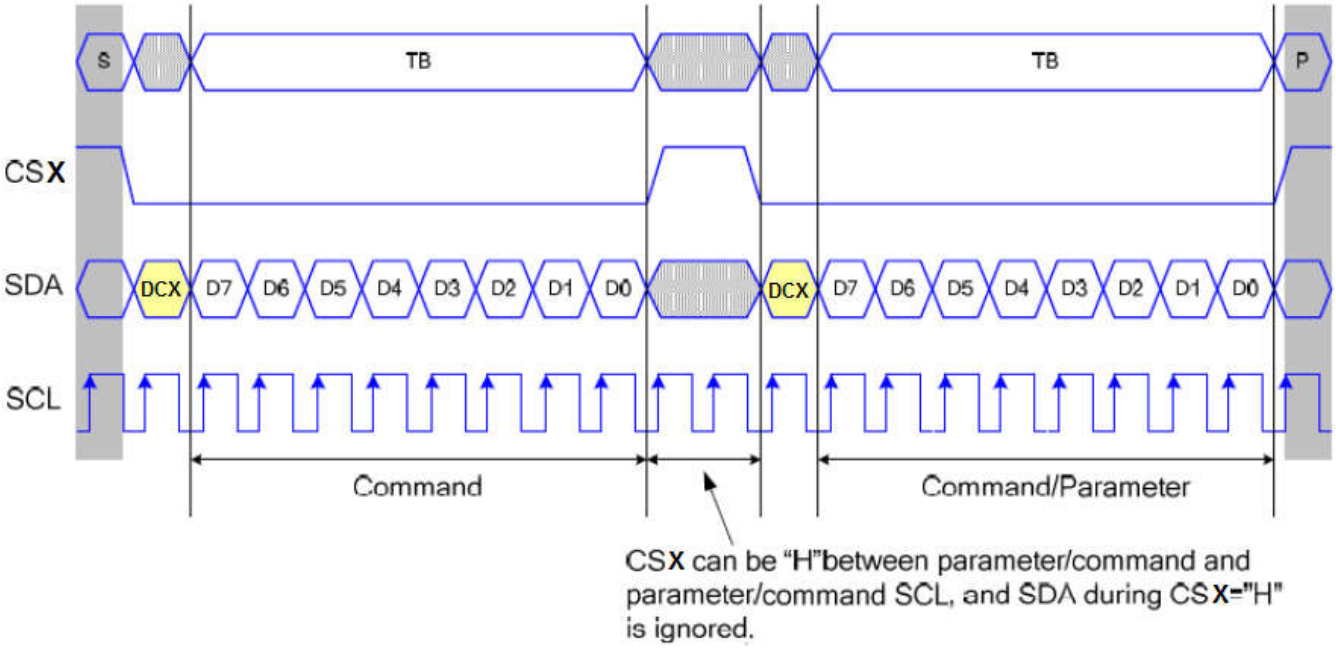
2 data lane serial interface use: CSX (chip enable), DCX (serial clock) and SDA (serial data input/output 1), and WRX (serial data input 2). To enter this interface, register spi_2wire_mode, which is located in the 3rd parameter of command F6h, should be set.

2 data lane hardware suggestion and Pin description:
2 data lane serial interface, IM[3:0]=0101



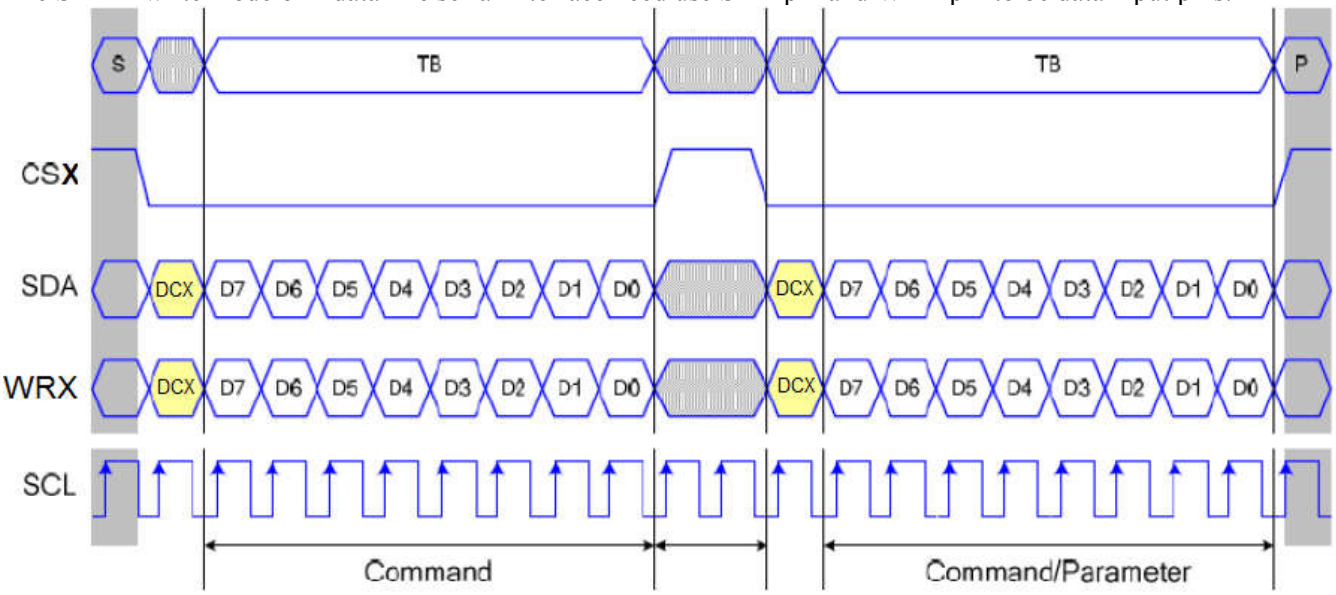
Pin Name	Description
CSX	Chip selection signal
DCX	Clock signal
SDA	Serial data input/output1
WRX	Serial data input2

Command write mode:
The command write protocol of 2 data lane serial interface is the same with the 3-wire serial interface,so users can ignore the input data of WRX.
Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.



SRAM write mode:

The SRAM write mode of 2 data line serial interface need use SDA pin and WRX pin to be data input pins.



Read function:

The read mode of 2 data lane serial interface is the same with the 3-wire serial interface and WRX pin can be ignored.

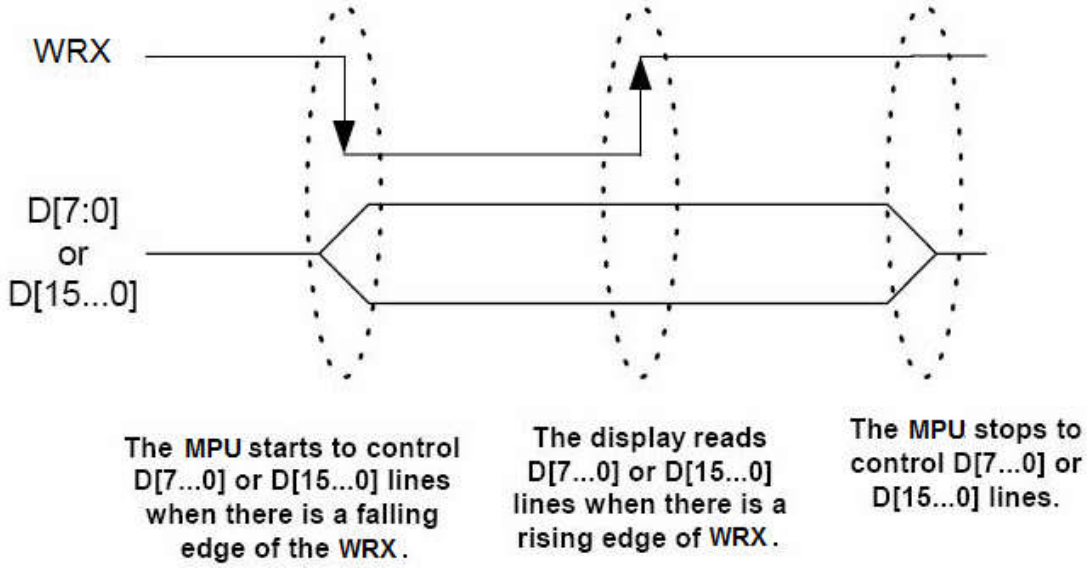
8.1.2 Parallel Interface

The Module uses a 11-wires 8-data parallel interface (IM0 = Low) or 19-wires 16-bit parallel interface (IM0 = High). The chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[7…0] or D[15…0] is parallel data.
The Graphics Controller Chip reads the data at the rising edge of WRX signal. The DCX is data/command flag. When DCX = "1", D15 (or D7) to D0 bits are display RAM data or command parameters. When DCX = "0" D15 (or D7) to D0 bits are commands.

8.1.2.1 Write Cycle/Sequence

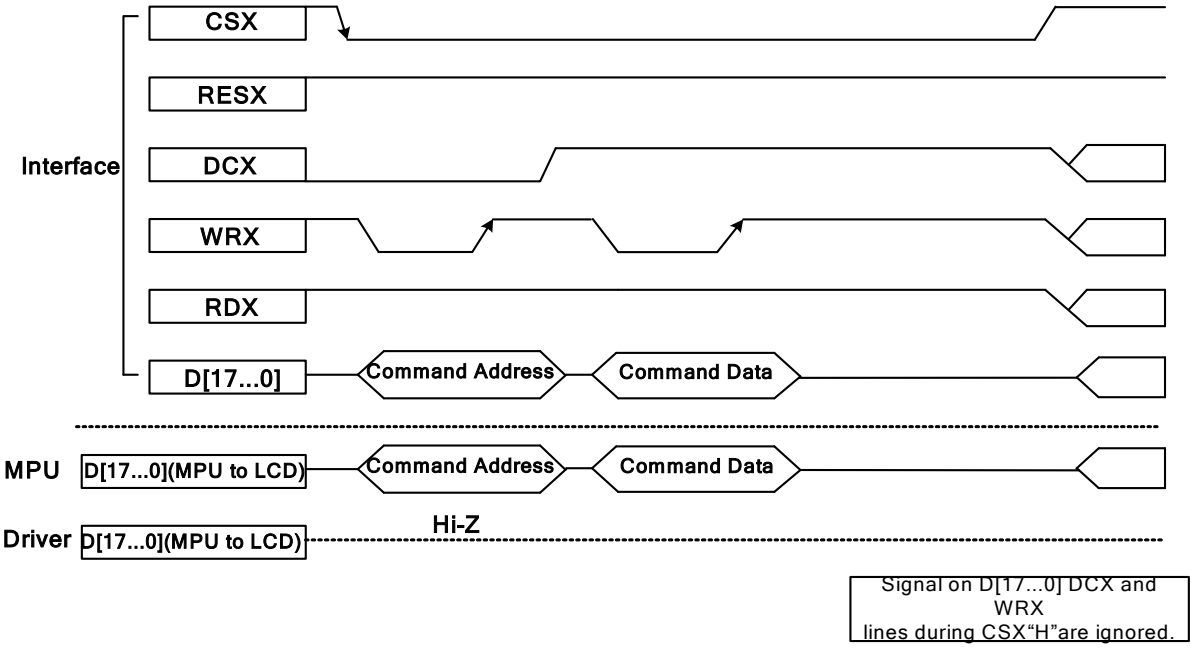
The write cycle means that the MPU writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, WRX) and 8 (D[7..0]) or 16 (D[15…0]) data signals. DCX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (='0') and vice versa it is data ('1').

The write cycle is described in the following figure.



Note: WRX is an unsynchronized signal (it can be stopped).

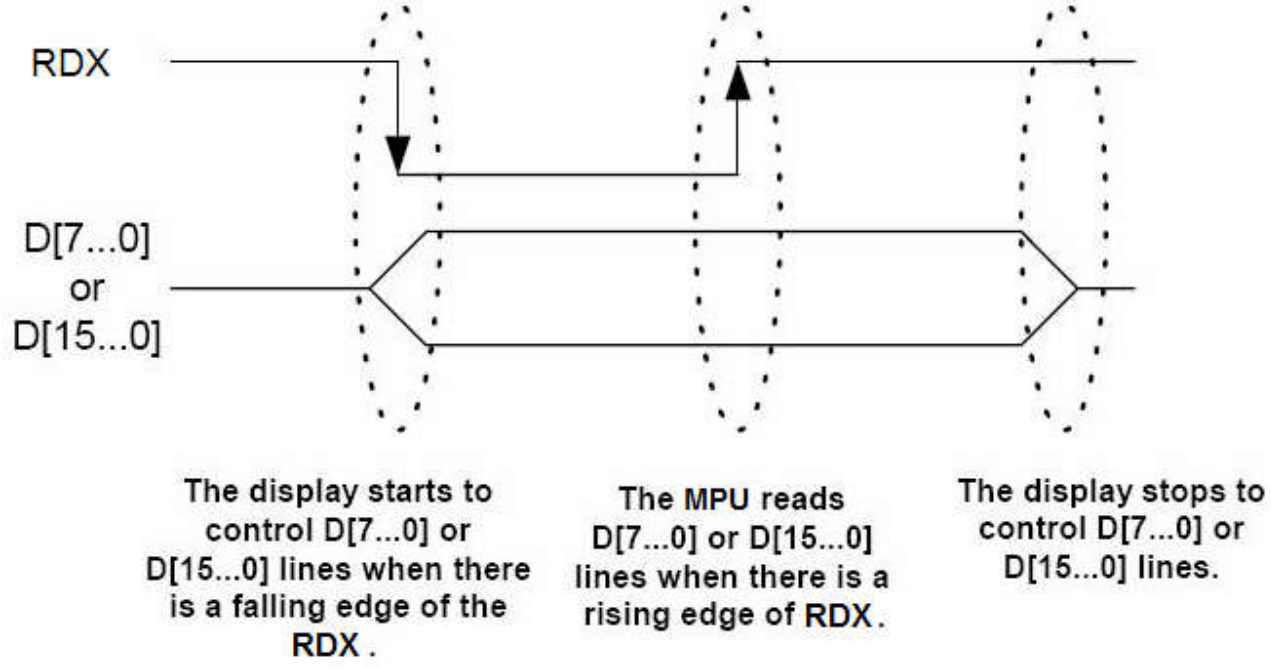
Parallel I/F write Sequence-Example



8.1.2.2 Read Cycle/Sequence

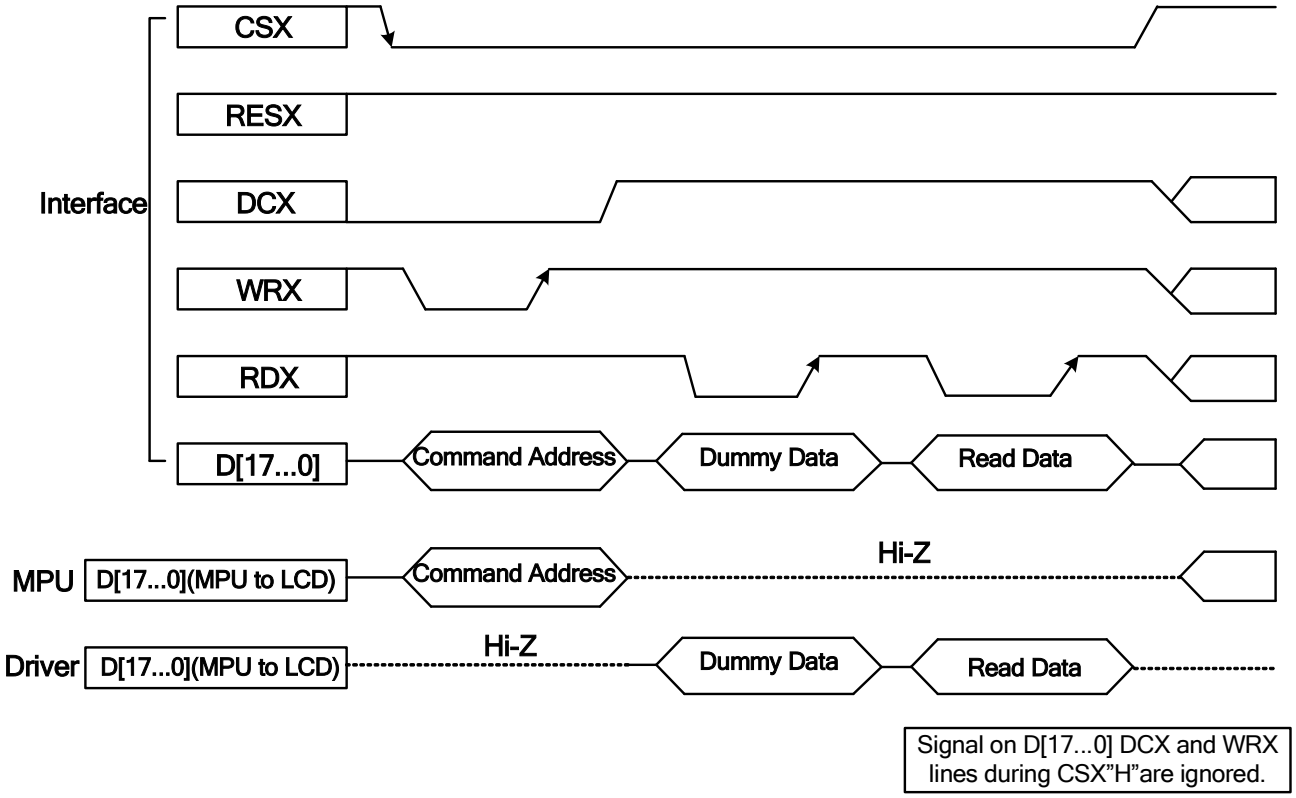
The read cycle (RDX high-low-high sequence) means that the MPU reads information from the display via interface. The display sends data (D[7...0] or D[15…0]) to the MPU when there is a falling edge of RDX and the MPU reads data when there is a rising edge of RDX.

The RDX cycle is described the following figure.



Note: RDX is an unsynchronized signal (it can be stopped).

Parallel I/F Read Sequence-example



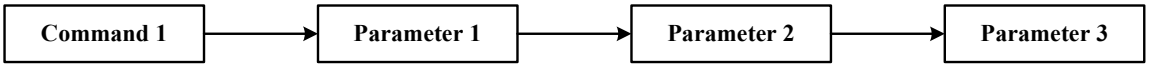
Note:

Read Data is only valid when DCX input is set High, if DCX is set Low during read then Driver Data line will be High Impedance.

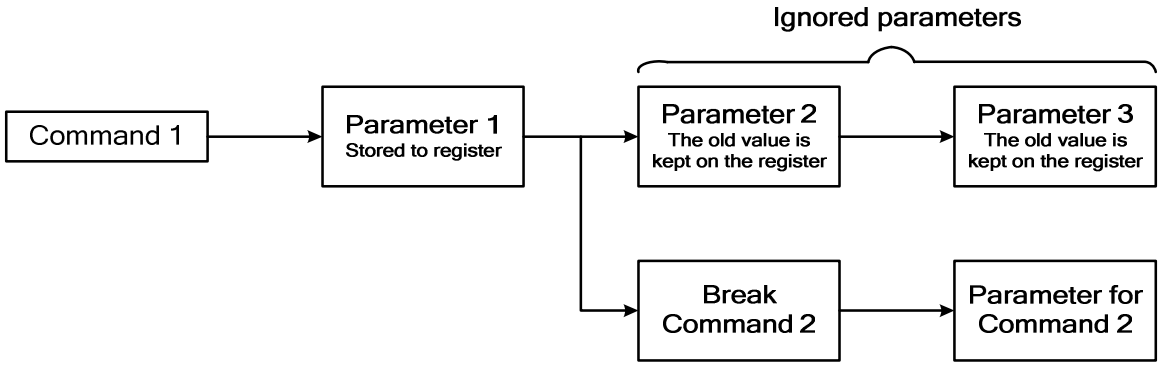
8.1.2.3 Display Module Data Transfer Break

If parameter 1 or more parameter command is being sent and a break occurs sending before the last parameter of the command and if the MPU then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameters after the break occurred is rejected if there is a new command as shown in the following example:

Without break

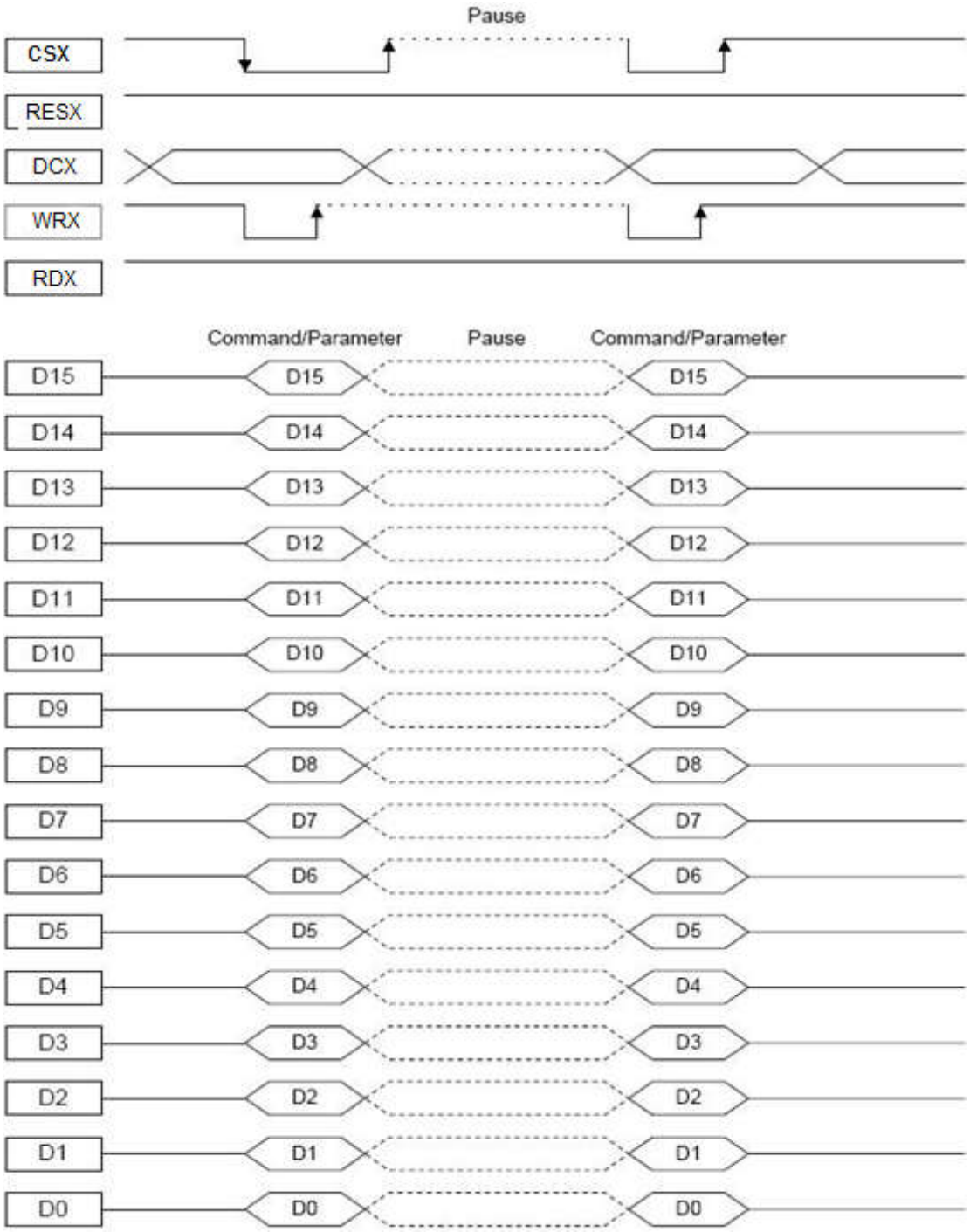


With break



Break can be another command or noise pulse.

8.1.2.4 Display Module Data Transfer Pause



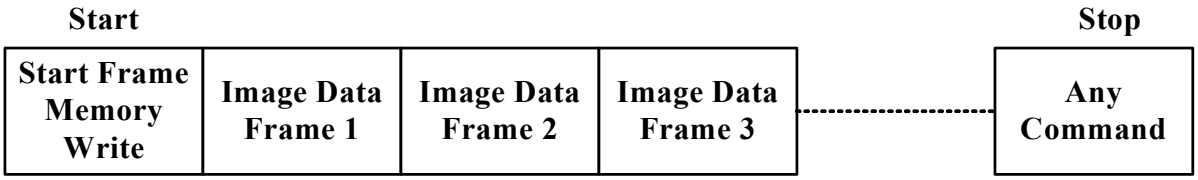
This applies to the following 4 conditions:
1. Command-Pause-Command
2. Command-Pause-Parameter
3. Parameter-Pause-Command
4. Parameter-Pause-Parameter

8.1.2.5 Display Module Data Transfer Modes

The module has four color modes for transferring data to the display data RAM. These are 16-bit color per pixel, 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

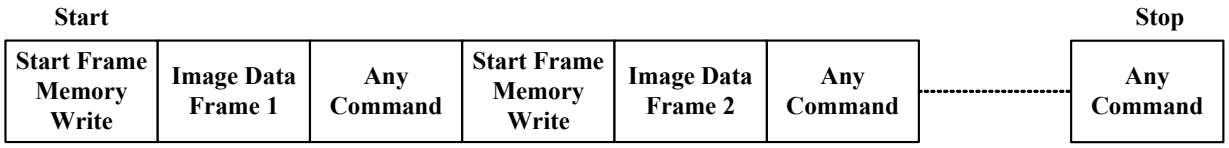
8.1.2.5.1 Method 1

The image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



8.1.2.5.2 Method 2

The image data is sent and at end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame downloaded.



Note:

1. These apply to all Data Transfer Color modes on Parallel interface;
2. The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored to the Frame Memory.

8.1.3 RGB Interface

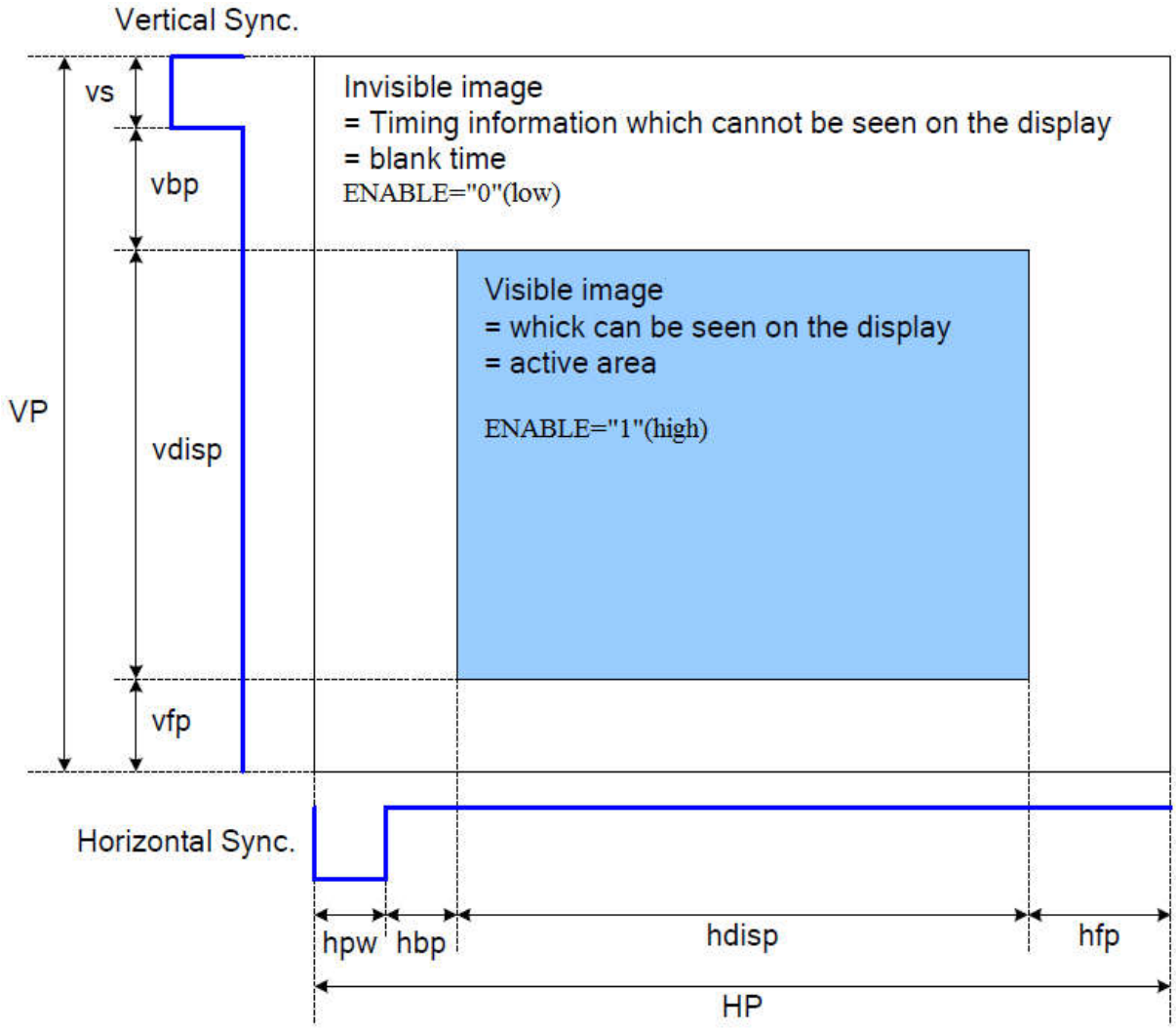
8.1.3.1 RGB interface Selection

The color format selection of RGB Interface for NV3030A is selected by setting the rim and dpi[2:0].

rim	dpi[2:0]	RGB Interface Mode	Data pins
0	110	18-bit 262K RGB Interface	DB[17:0]
0	101	16-bit 65K RGB Interface	DB[17:13], DB[11:1]
1	110	6-bit 262K RGB Interface	DB[5:0]
1	101	6-bit 65K RGB Interface	DB[5:0]

8.1.3.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	4	10	hpw+hbp=31	Clock
Horizontal Sync. Back Porch	hbp	8	10		Clock
Horizontal Sync. Front Porch	hfp	4	38	-	Clock
Vertical Sync. Width	vs	2	4	vs+vbp=127	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

8.1.3.3 RGB Interface Mode Selection

NV3030A supports two kinds of RGB interface, DE mode and SYNC mode. Each mode also can select with ram and without ram. The table shown below uses command B0h to select RGB interface mode.

RCM[1:0]	bypass_mode	Mode	Data Path	Control Signals
10	0	DE mode	without Ram	DOTCLK, ENABLE, VSYNC(optional), HSYNC(optional)
	1		Ram	
11	0	SYNC mode	without Ram	DOTCLK, VSYNC, HSYNC
	1		Ram	

The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Graphics operation function	Not available	Available

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

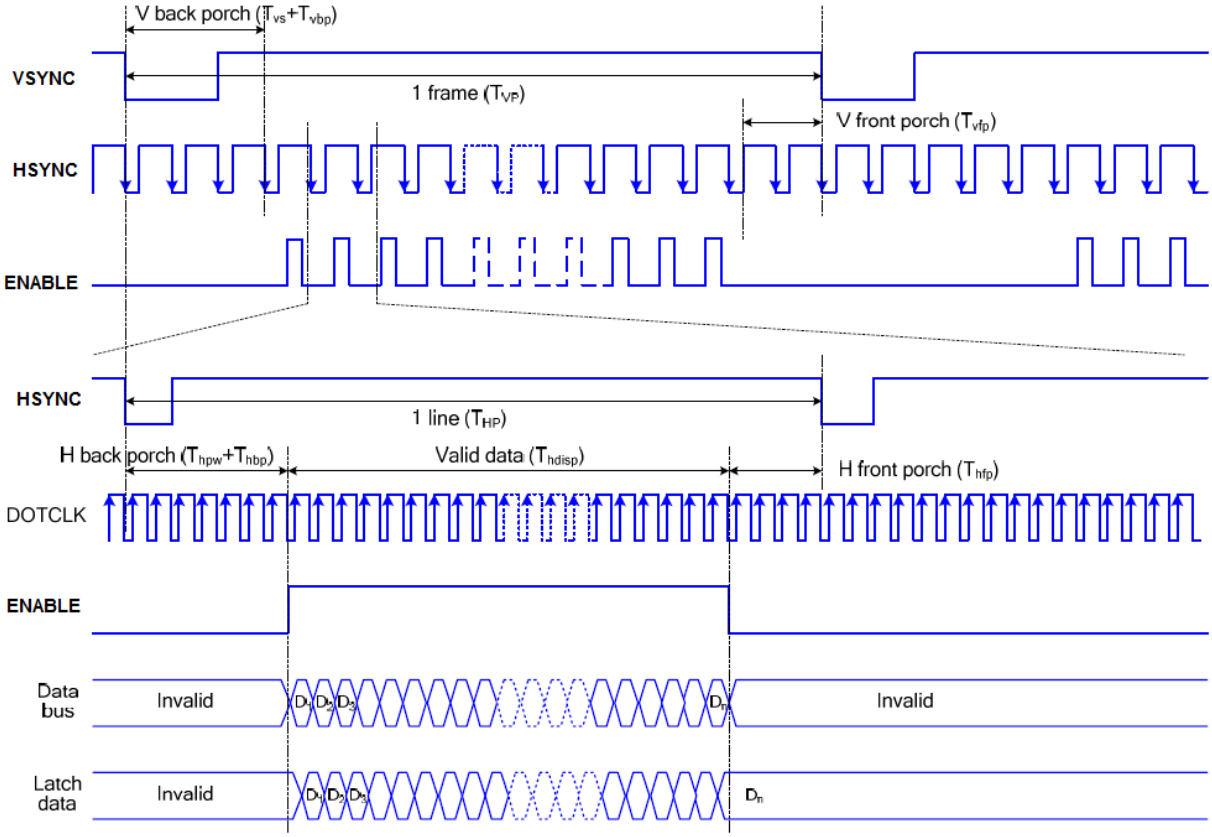
In 6-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

In 6-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

Switching between the internal operation mode and the external RGB interface mode is prohibited.

8.1.3.4 RGB Interface Timing Diagram

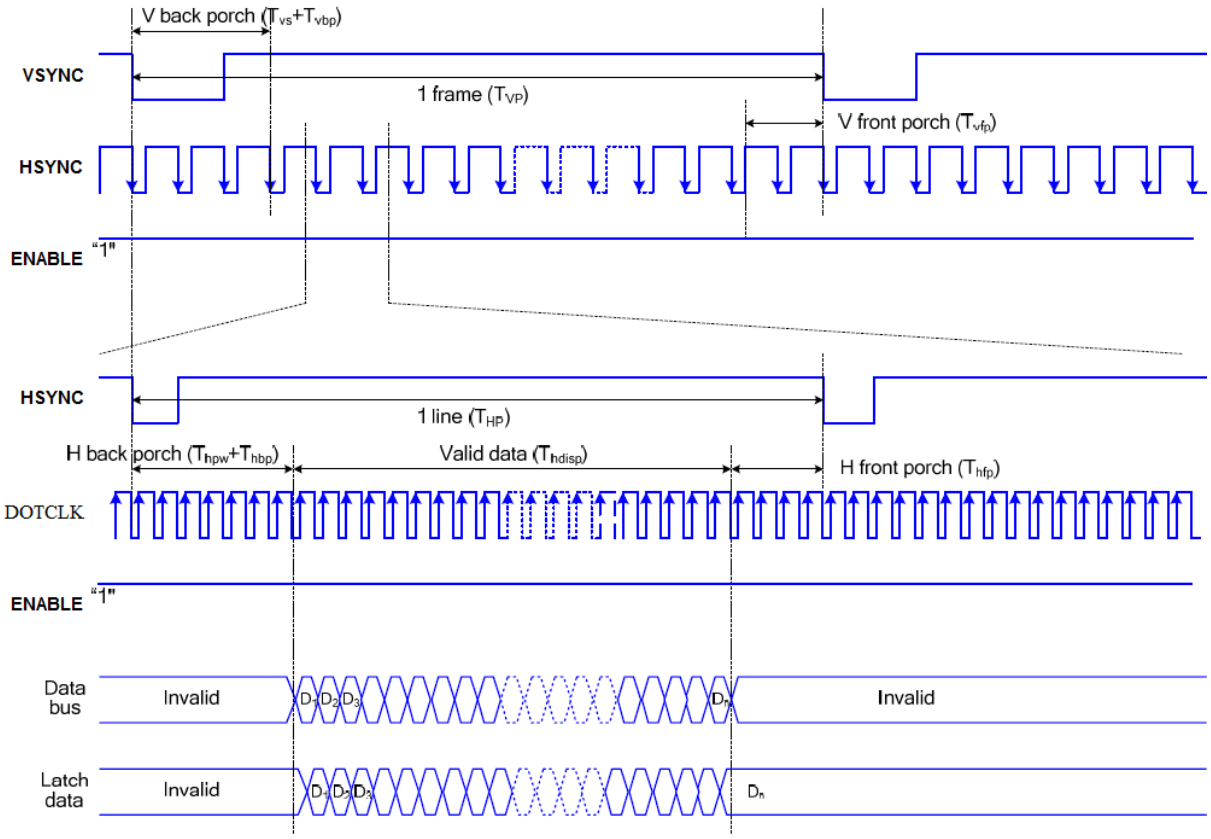
The timing chart of RGB interface DE mode is shown as follows.



Timing Chart of Signals in RGB Interface DE Mode

Note: The setting of front porch and back porch in MPU must match that in IC as this mode.

The timing chart of RGB interface SYNC mode is shown as follows.

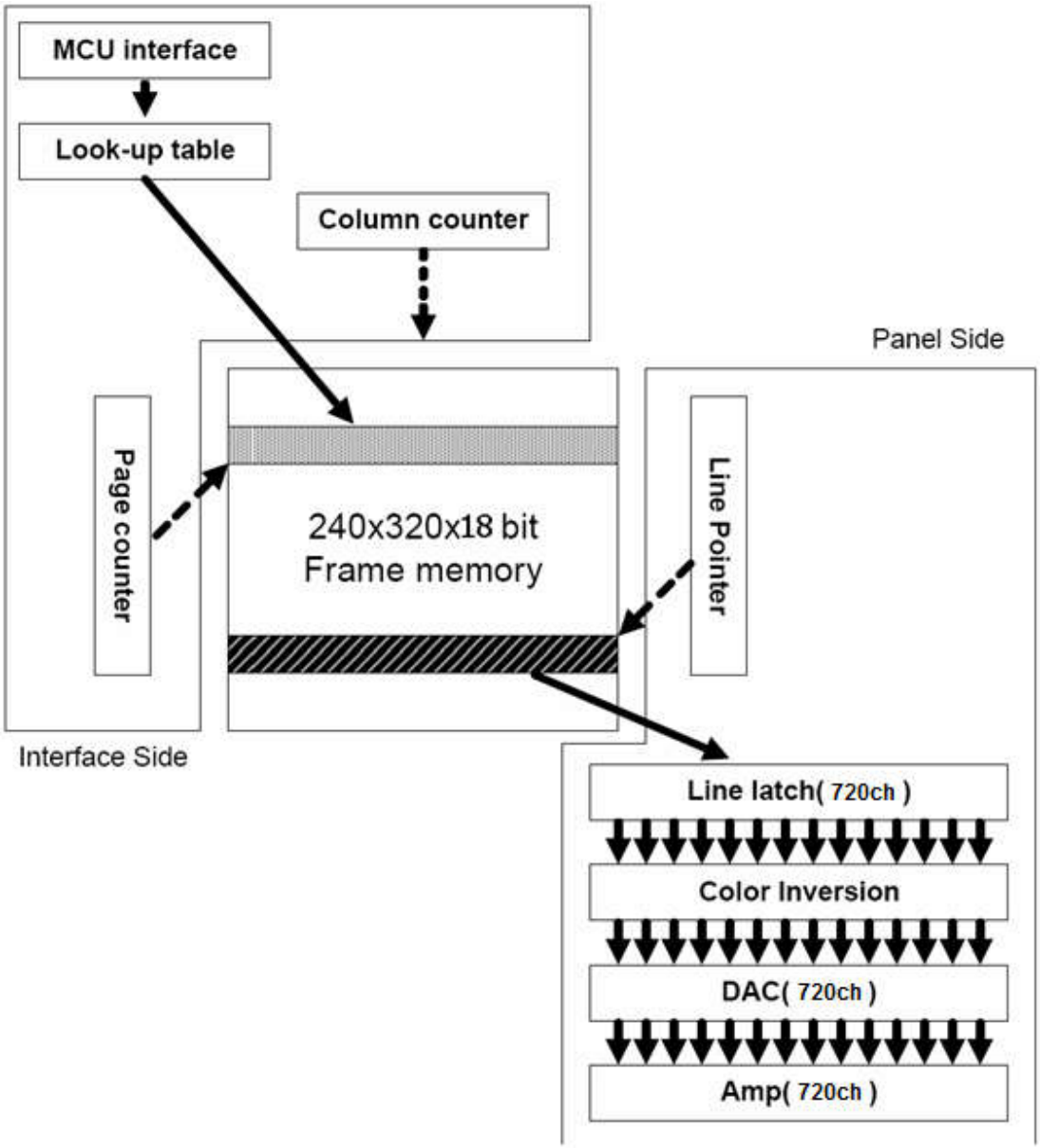


Timing chart of RGB interface SYNC mode

8.2 Display Data RAM

8.2.1 Configuration

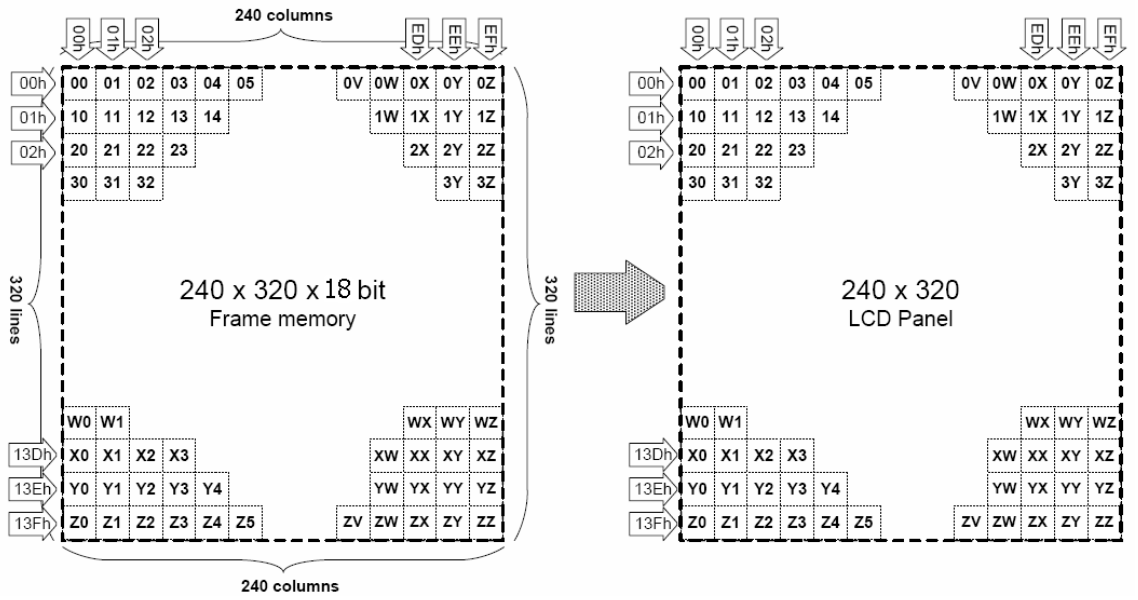
The display data RAM stores display dots and consists of 1,382,400 bits (240×320×18 bits).There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



8.2.2 Memory to Display Address Mapping

8.2.2.1 Normal Display On or Partial Mode On, Vertical Scroll Off

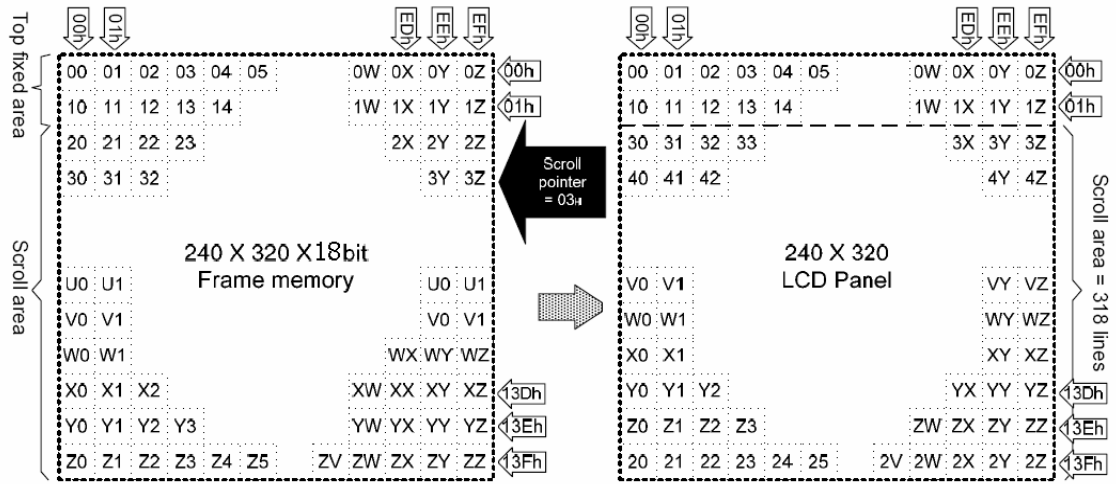
In this mode, contents of the frame memory within an area where column pointer is 0000h to 00Efh and page pointer is 0000h to 013Fh is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0).



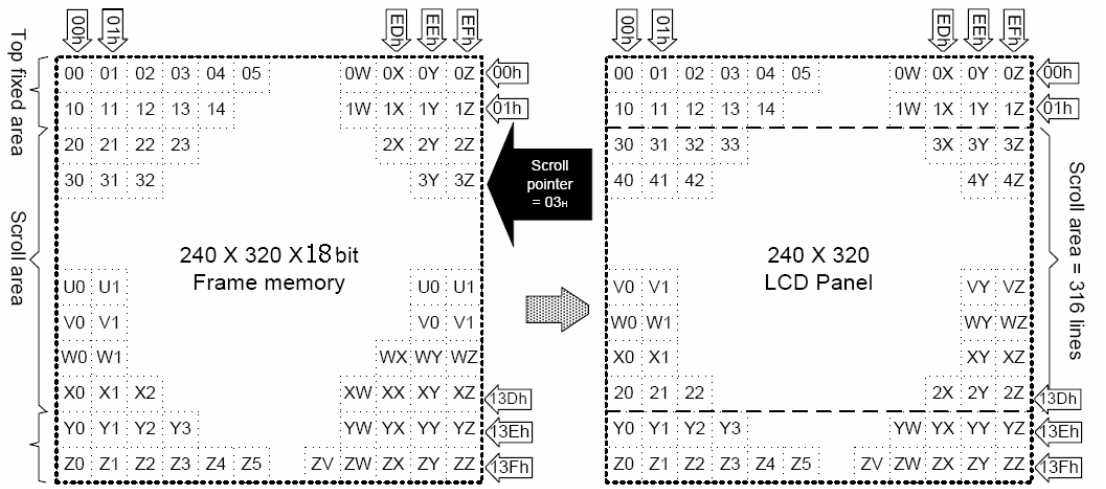
8.2.2.2 Vertical Scroll Mode

There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling” (33h) and “Vertical Scrolling Start Address” (37h).

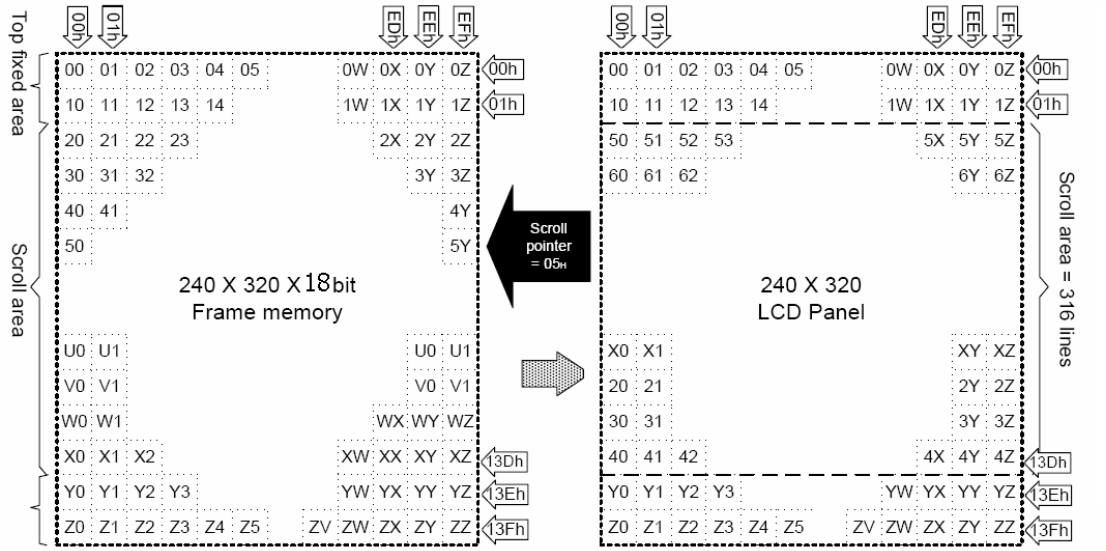
Example 1
TFA= 2, VSA = 318, BFA = 0 when MADCTL Bit B4 = 0



Example 2
TFA=2,VSA=316,BFA=2 when MADCTL bit B4=0



Example 3
TFA=2,VSA=316,BFA=4 when MADCTL bit B4=0



Note:
When Vertical Scrolling Parameters(TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.

8.2.2.3 Vertical Scroll example

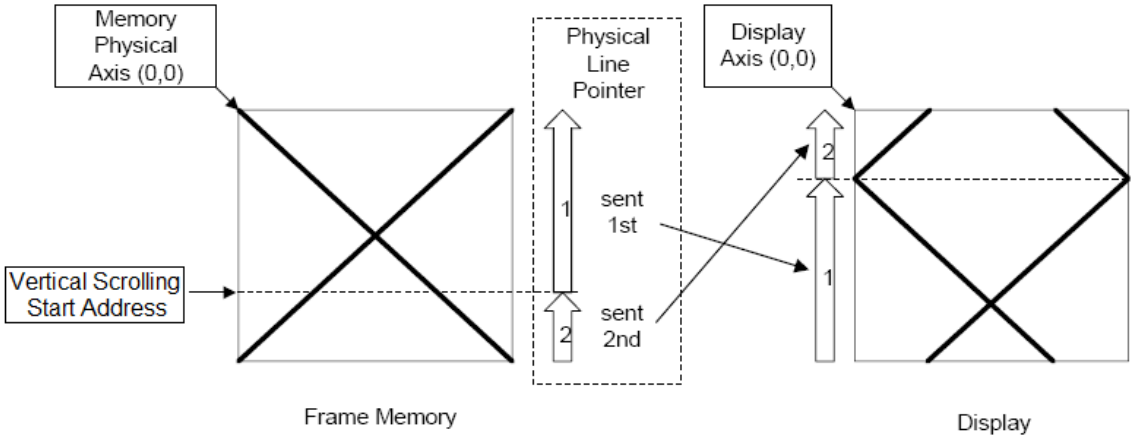
Case 1: TFA + VSA + BFA < 320

N/A. Do not set TFA + VSA + BFA < 320, unless unexpected picture will be shown.

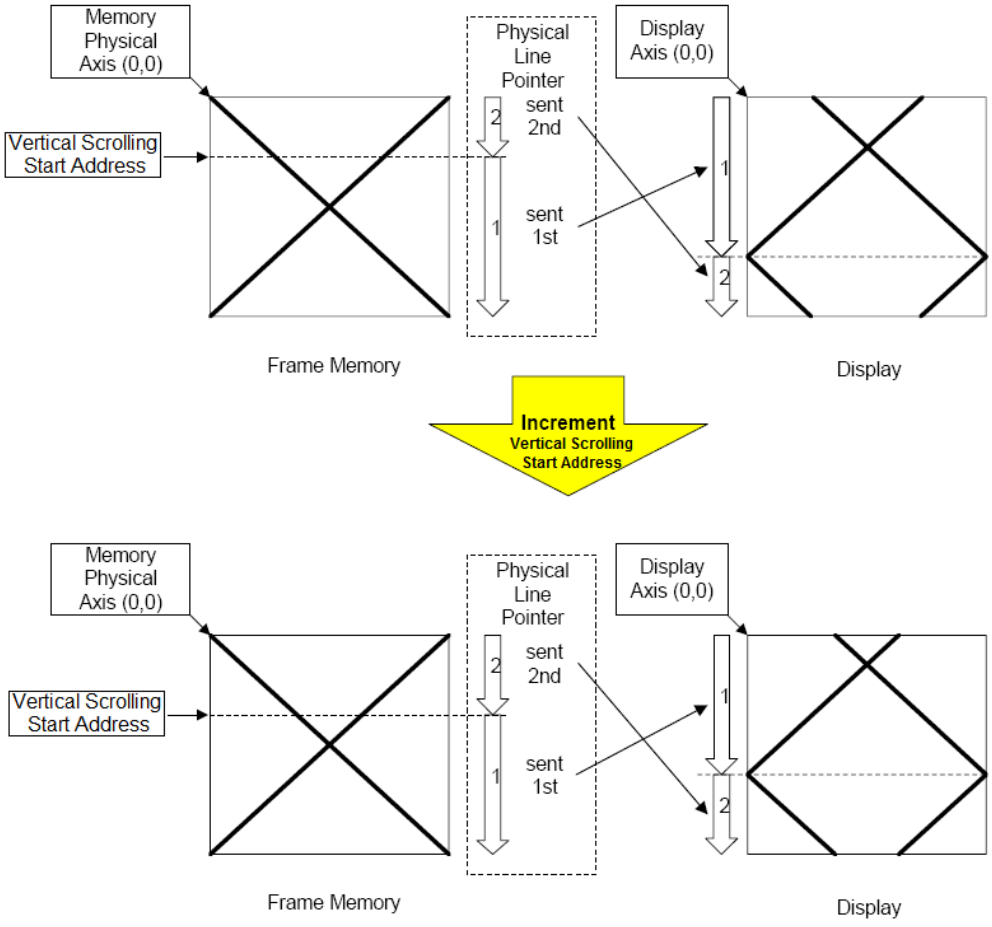
Case 2: TFA + VSA + BFA = 320 (Rolling Scrolling)

Example 2-a. When TFA = 0, VSA = 320, BFA = 0 and Vertical Scrolling Start Address = 40.

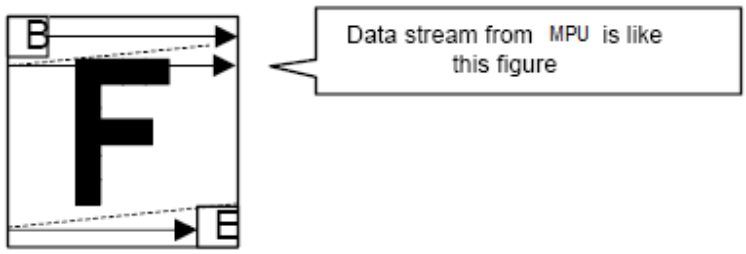
MADCTL parameter B4= “0”



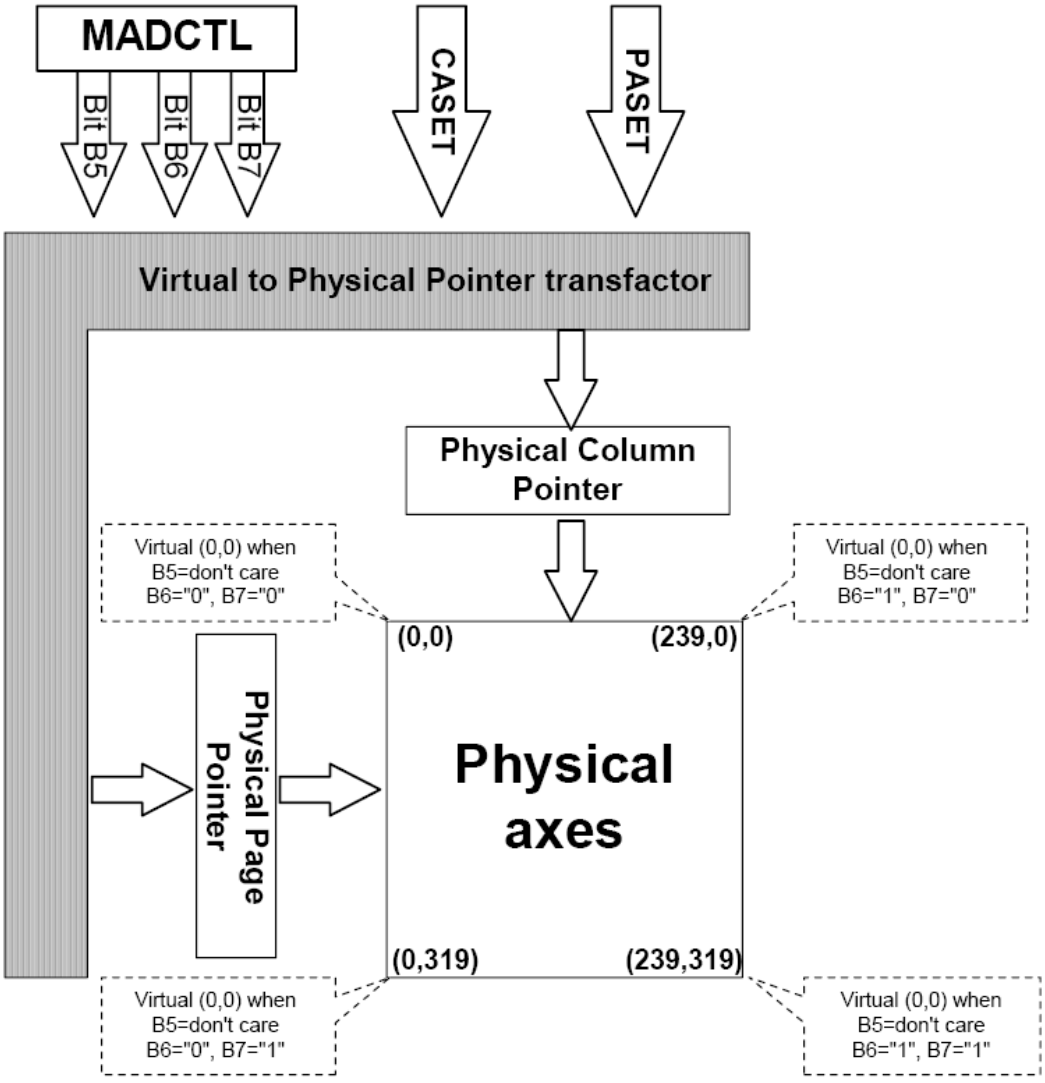
MADCTL parameter B4= “1”



8.2.3 MPU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” command, Bits B5, B6, B7 as described below.



For each image orientation, the controls for the column and page counters apply as below:

B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direc to(239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

For each image orientation, the controls for the column and page counters apply as below:

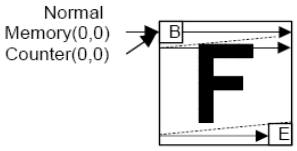
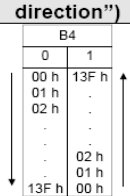
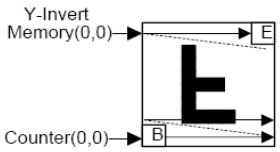
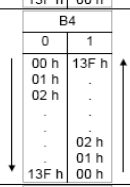
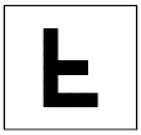
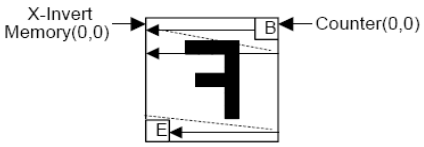
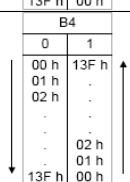
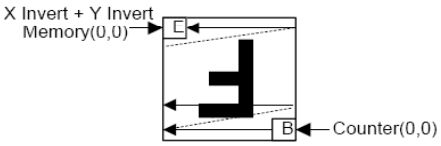
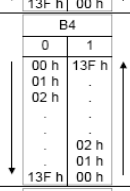
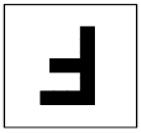
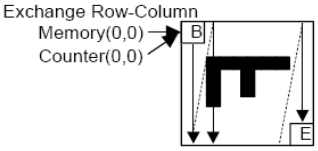
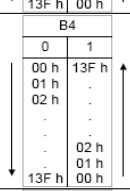
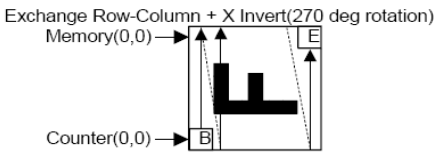
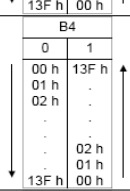
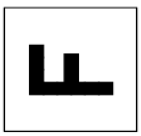
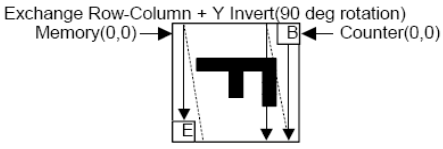
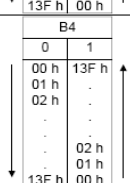
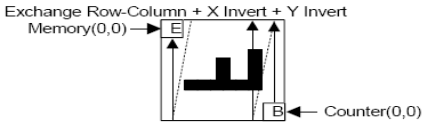
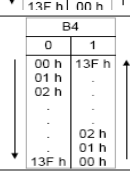
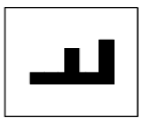
Condition	Column Counter	Page Counter
When memory write/memory read command is accepted	Return to “Start Column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than “End Column”	Return to “Start Column”	Increment by 1
The Column counter value is larger than “End Column” and the Page counter value is larger than “End Page”	Return to “Start Column”	Return to “Start Page”

Note:
Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

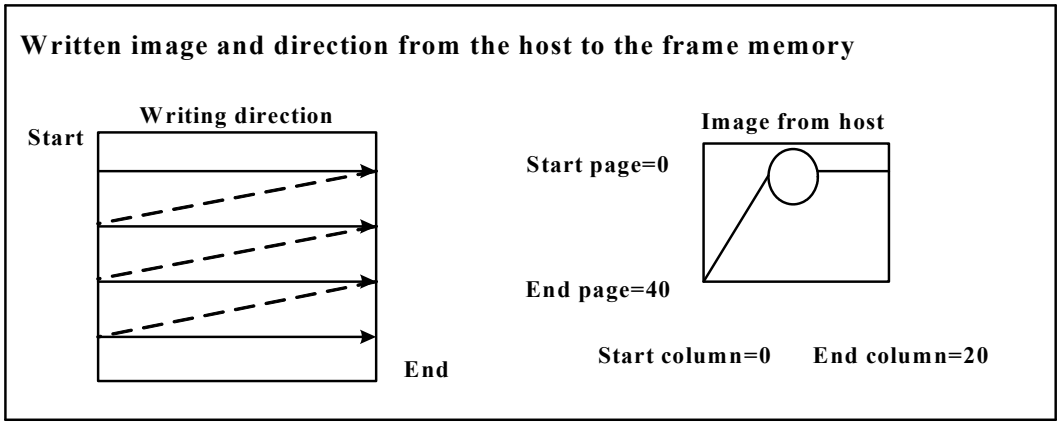
One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

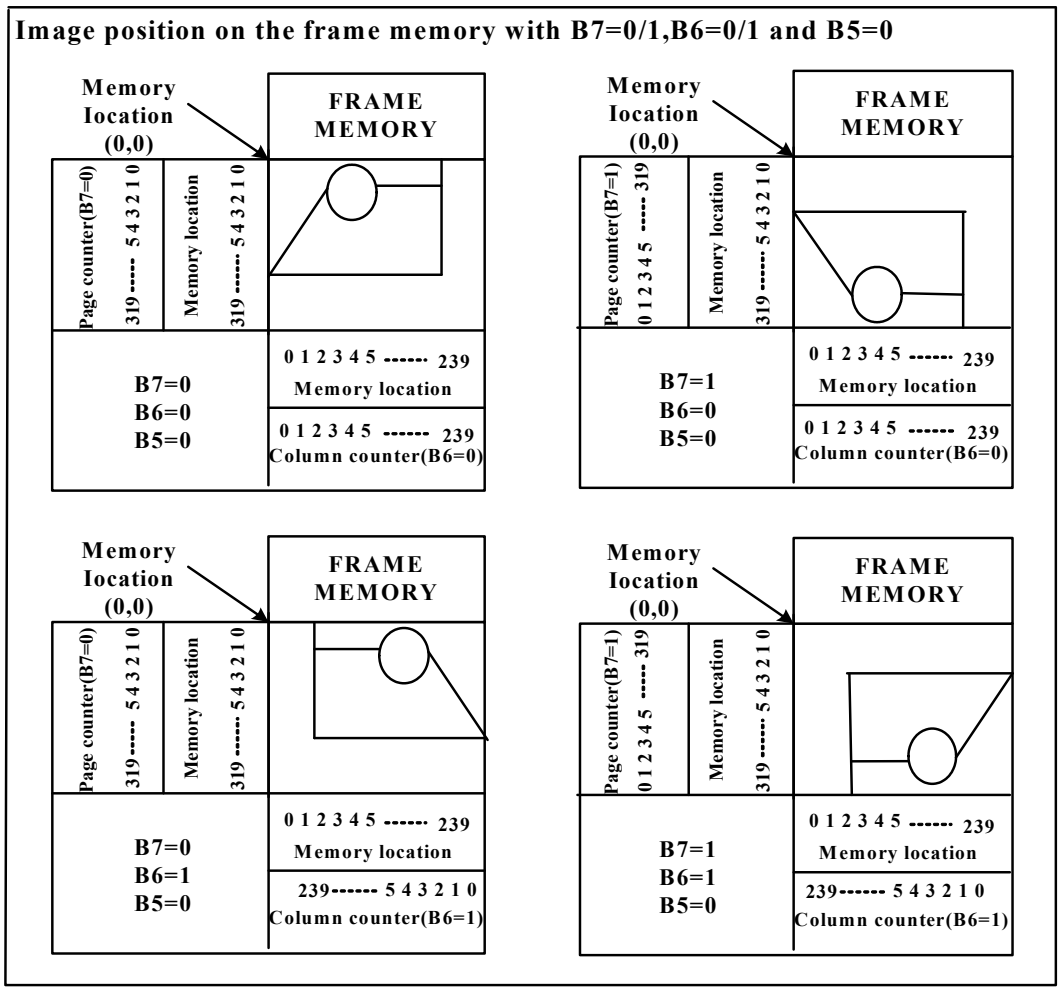
This resultant image for each orientation setting is illustrated below:

B5 B6 B7 (Bits)	Image in the memory ("→" means "MCU to memory read/write direction")	B4 Bit ("→" means "RAM to display scan direction")	Image in the Display
0 0 0			
0 0 1			
0 1 0			
0 1 1			
1 0 0			
1 0 1			
1 1 0			
1 1 1			

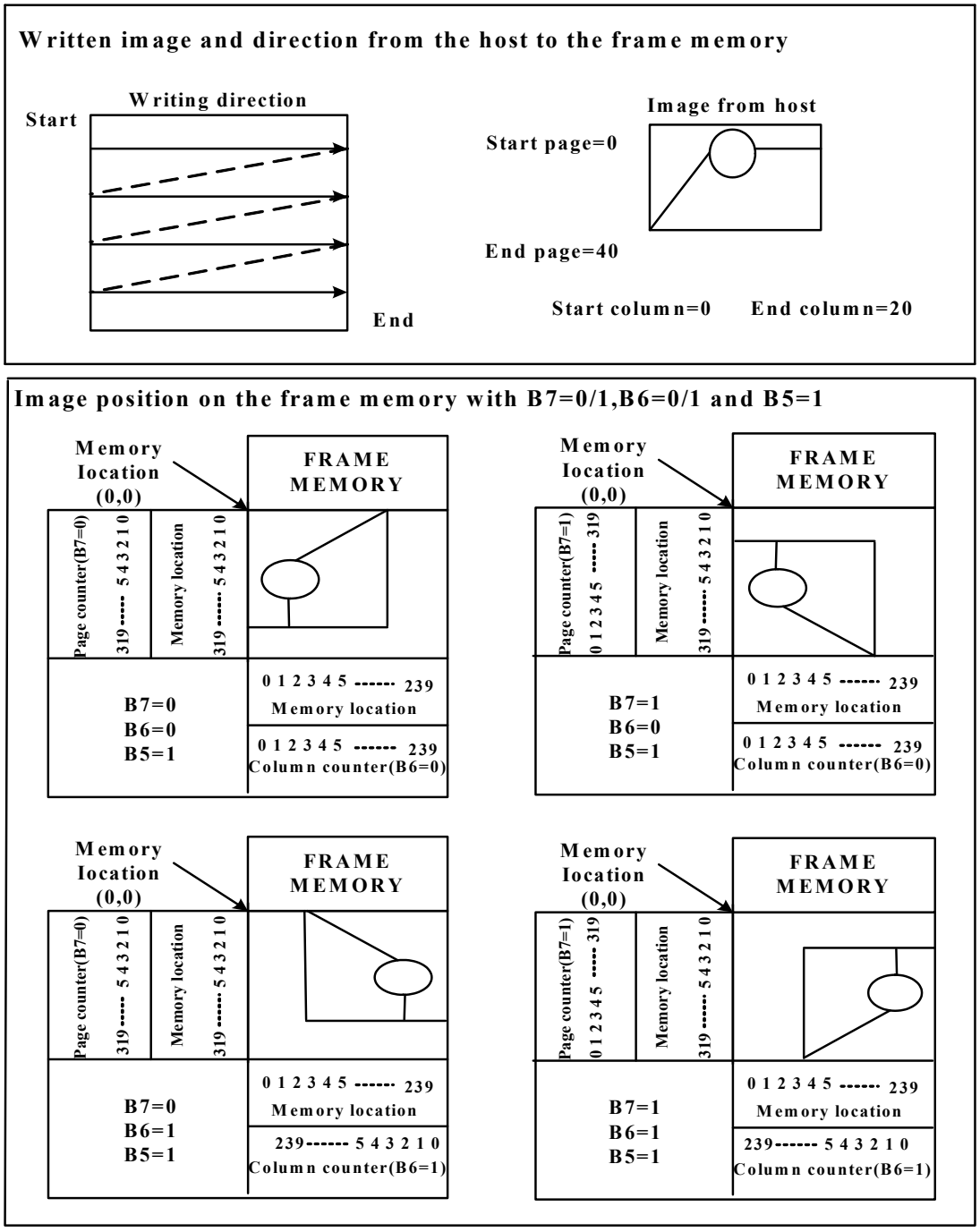
Example for rotation with B7, B6 and B5
This example is using following values:
start page = 0, end page = 40, start column = 0 and end column = 20
= Commands: page address set (0,40) and column address set (0,20).

The sent figure is as follows and its sending order is as follows:





The sent figure is as follows and its sending order is as follows:



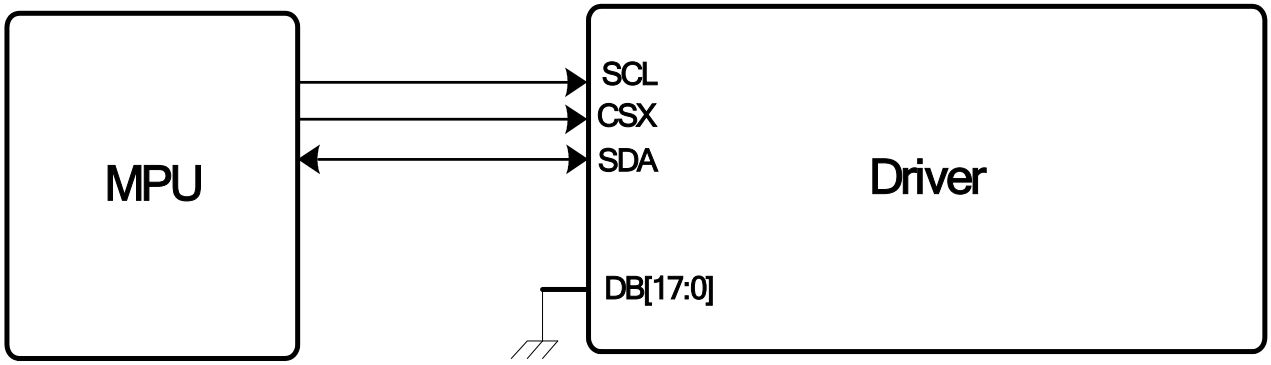
8.3 Display Data Format

NV3030A supplies 18-/16-/9-/8-bit parallel interface with 8080-Ⅰ /8080-Ⅱ series, 3-/4-wire serial interface and 6-/16-18-bit parallel RGB interface. The parallel interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters rcm[1:0].

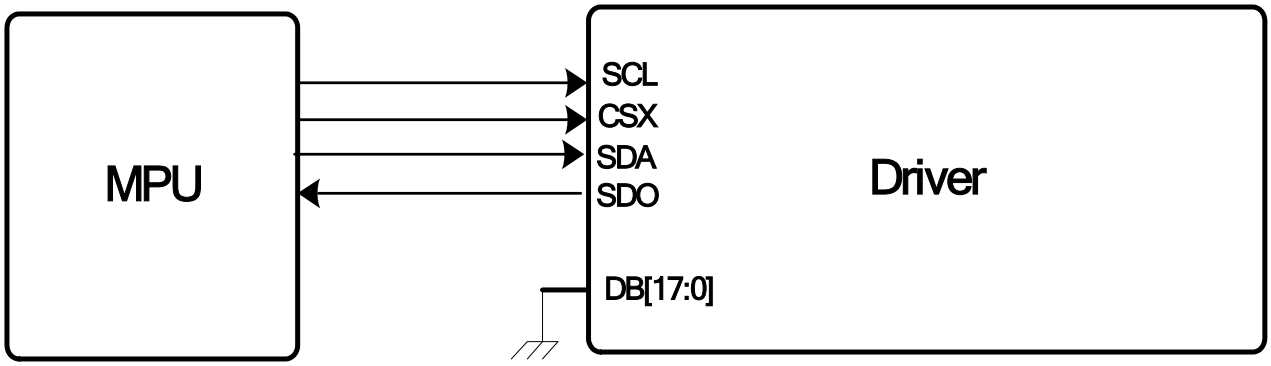
8.3.1 3-wire Serial Interface

The 3-wire/9-bit serial bus interface of NV3030A can be used by setting external pin as IM [3:0] to “0101” for serial interface I or IM [3:0] to “1101” for serial interface II. The shown figure is the example of 3-wire SPI interface.

3-wire Serial interface Ⅰ

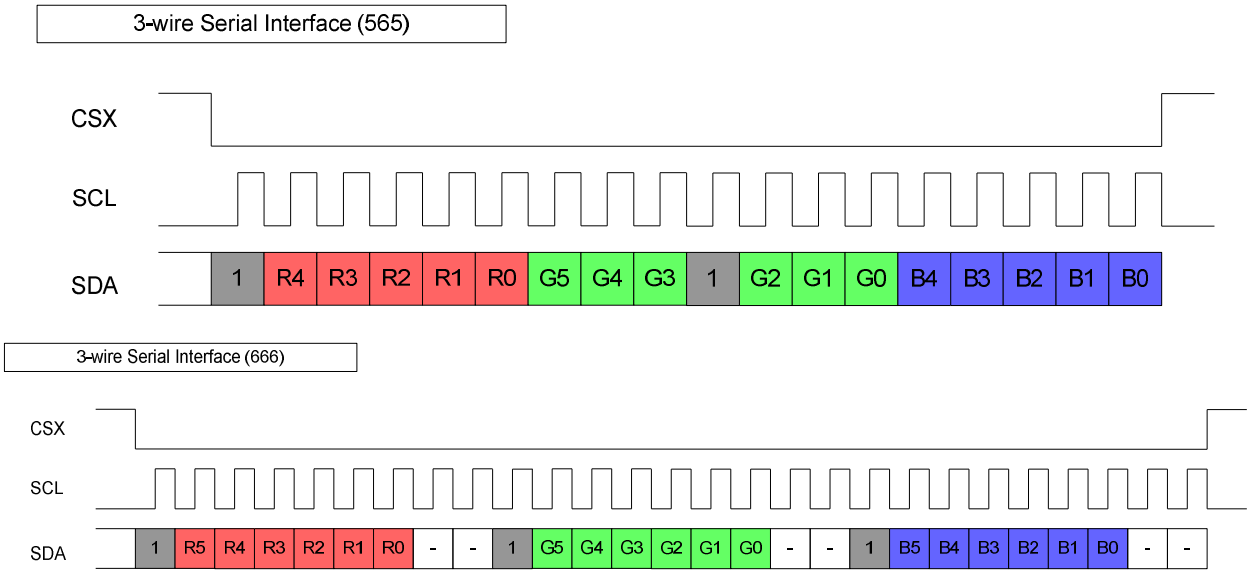


3-wire Serial interface Ⅱ



In 3-wire serial interface, different display data format is available for two color depths supported by the LCM listed below:

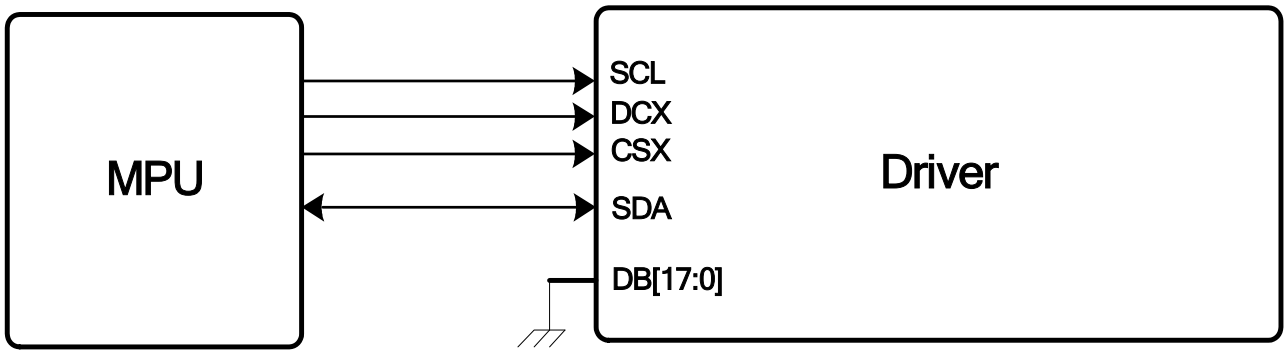
1. -65k colors, RGB 5, 6, 5 –bits input.
2. -262k colors, RGB 6, 6, 6 –bits input.



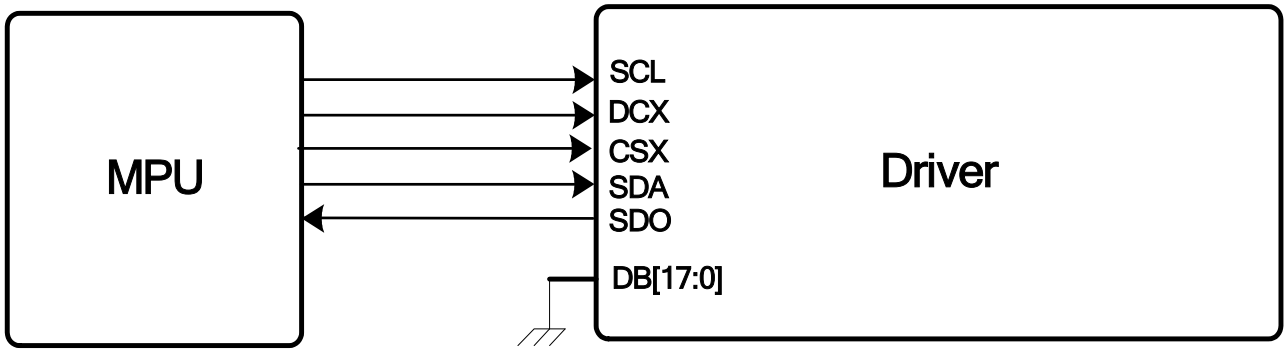
8.3.2 4-wire Serial Interface

The 4-wire/8-bit serial bus interface of NV3030A can be used by setting external pin as IM [3:0] to “0110” for serial interface I or IM [3:0] to “1110” for serial interface II. The shown figure is the example of 4-wire SPI interface.

4-wire Serial interface I



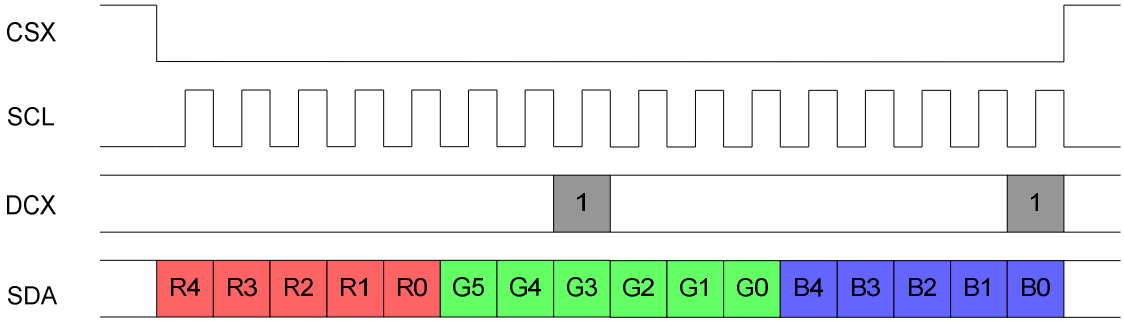
4-wire Serial interface II



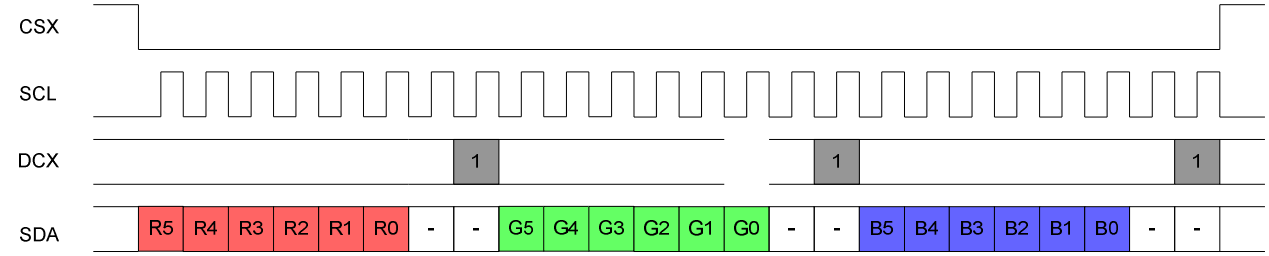
In 4-wire serial interface, different display data format is available for two color depths supported by the LCM listed below:

1. -65k colors, RGB 5, 6, 5 –bits input.
2. -262k colors, RGB 6, 6, 6 –bits input.

4-wire Serial Interface (565)

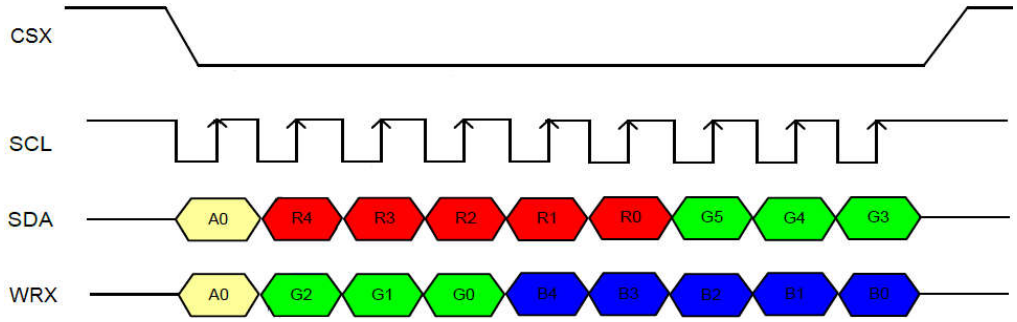


4-wire Serial Interface (666)

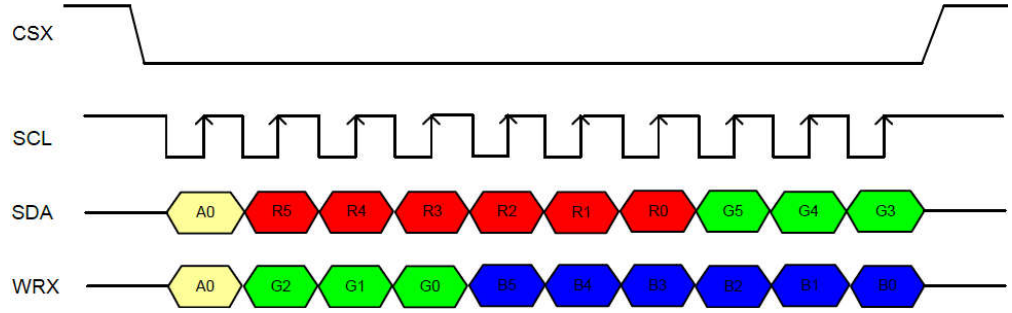


8.3.3 2 data lane serial interface

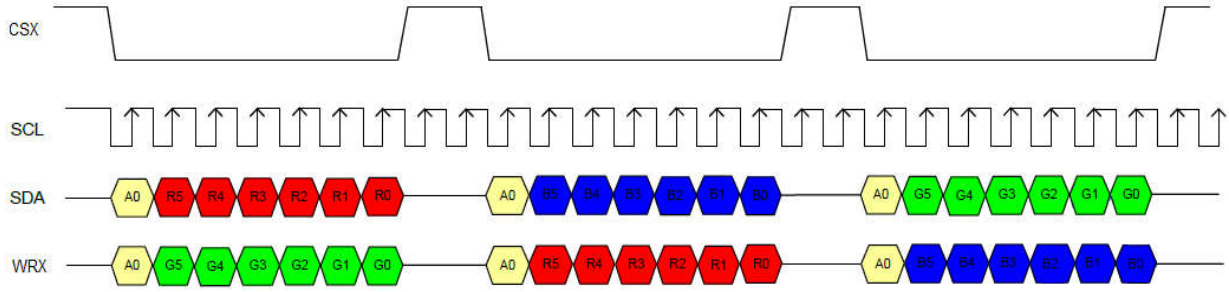
1) RGB565



2) RGB666,mdt=00



3) RGB666,mdt=01



8.3.4 Parallel Interface

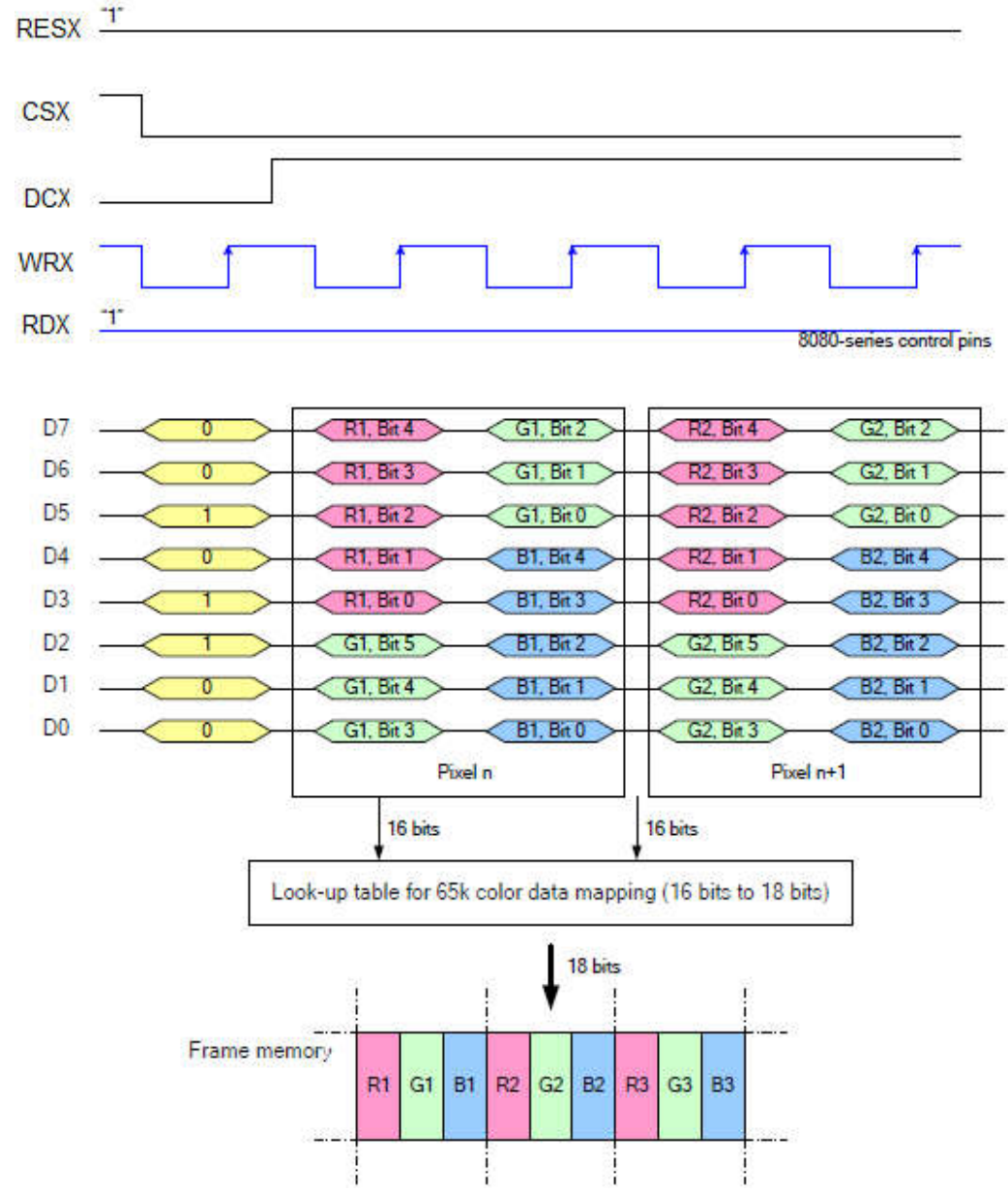
8.3.4.1 8080-Ⅰ series 8-bit Parallel Interface

The 8080-Ⅰ series 8-bit parallel interface of NV3030A can be used by setting IM[3:0]=”0000b”. Different display data formats are available for two Colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

8.3.4.1.1 16-bit/pixel

There is 1pixel (3 sub-pixels) per 2-byte



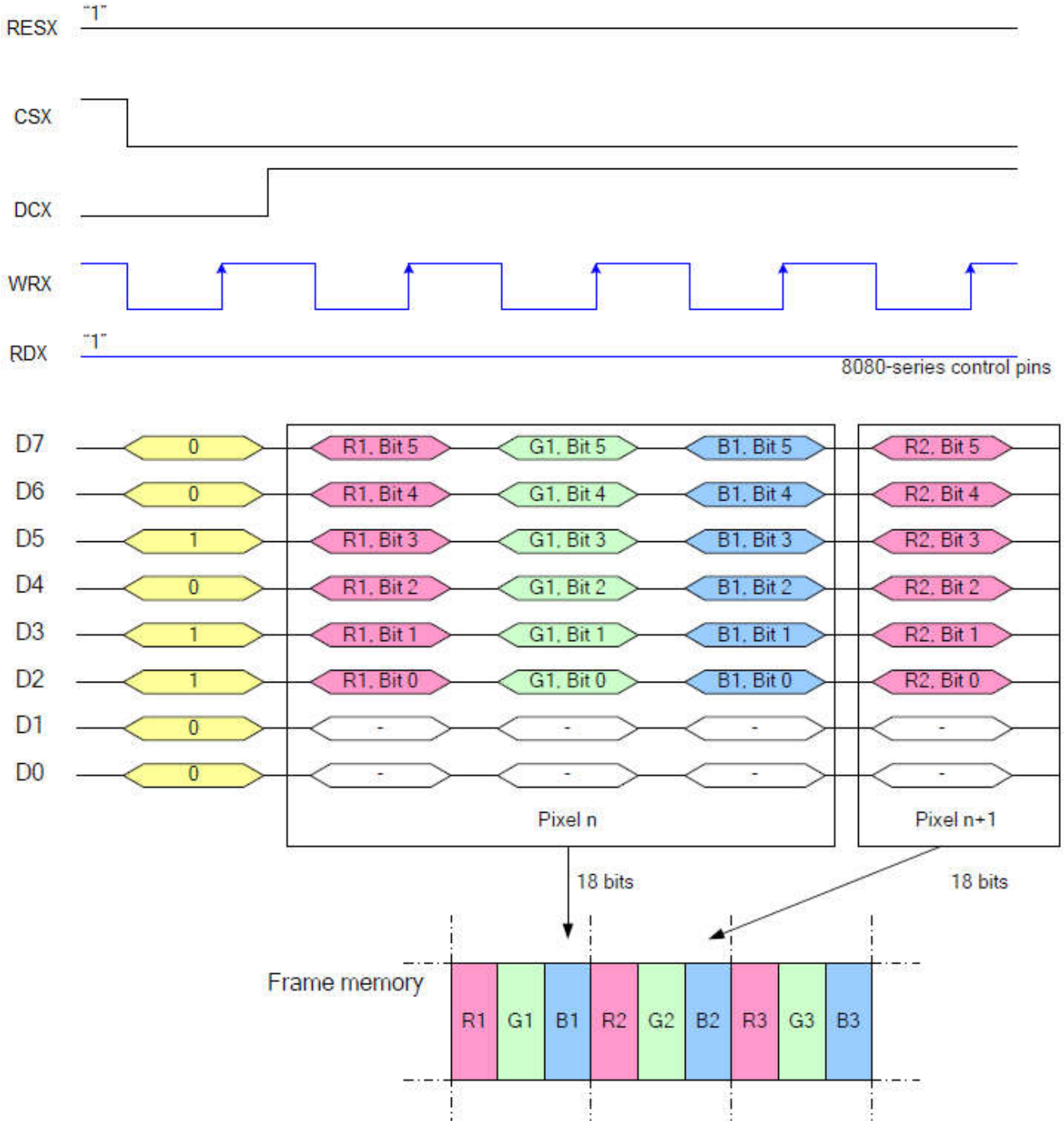
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.1.2 18-bit/pixel

There is 1pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

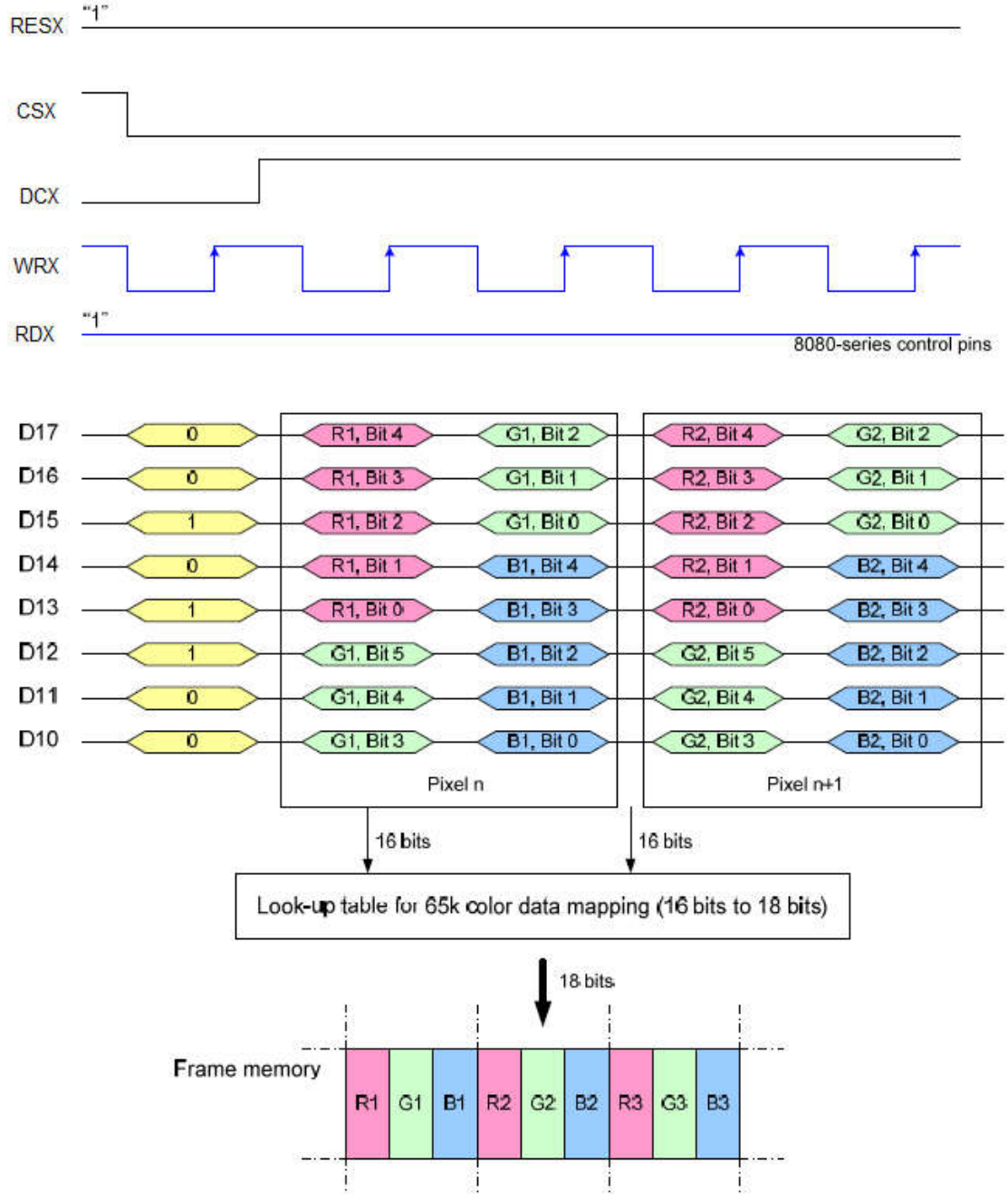
Note 3: '-' = Don't care – Can be set to '0' or '1'.

8.3.4.2 8080-II series 8-bit Parallel Interface

The 8080-Ⅱ series 8-bit parallel interface of NV3030A can be used by setting IM[3:0]=”1001b”. Different display data formats are available for two Colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

8.3.4.2.1 16-bit/pixel

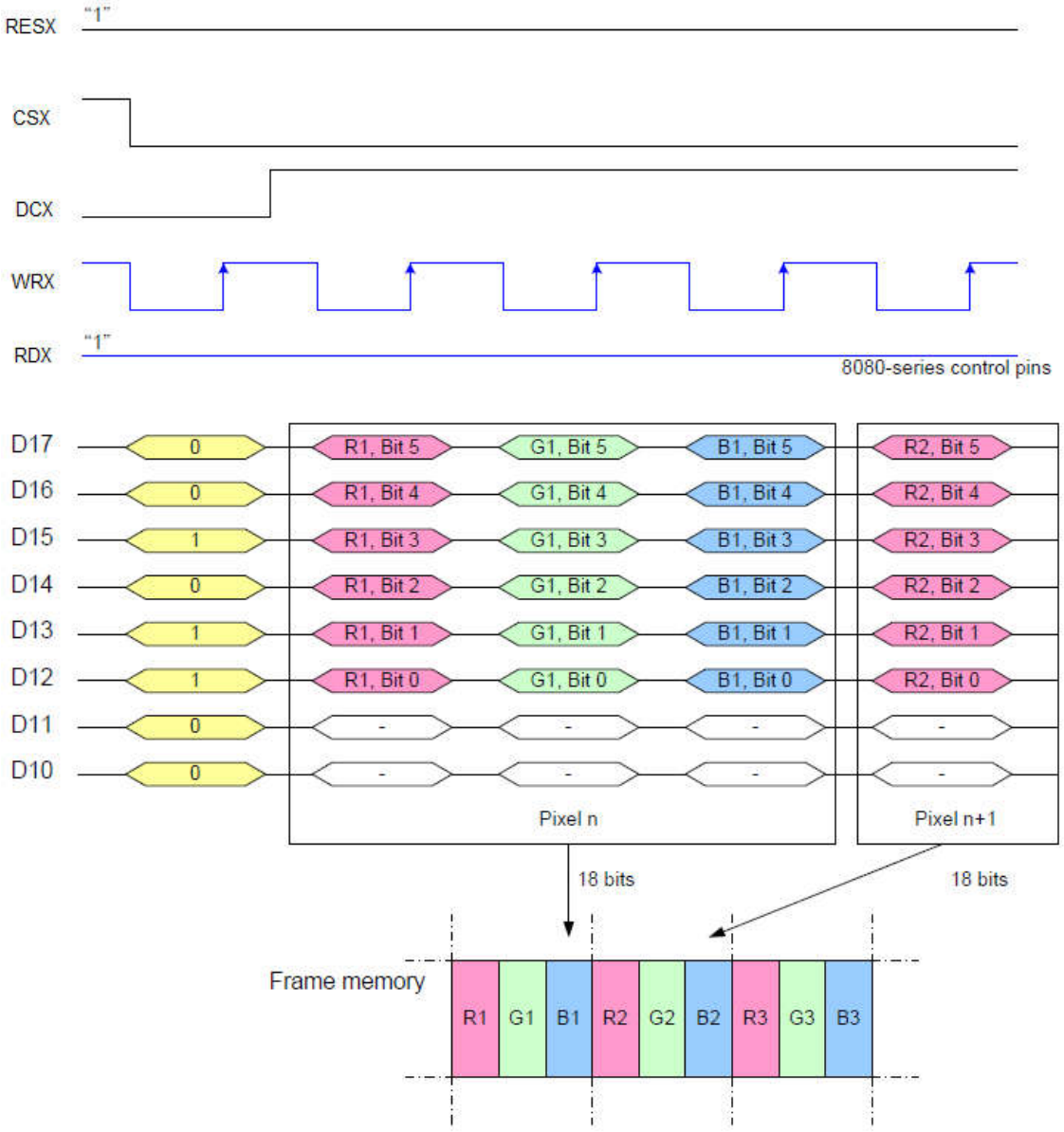


Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.2.2 18-bit/pixel



Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

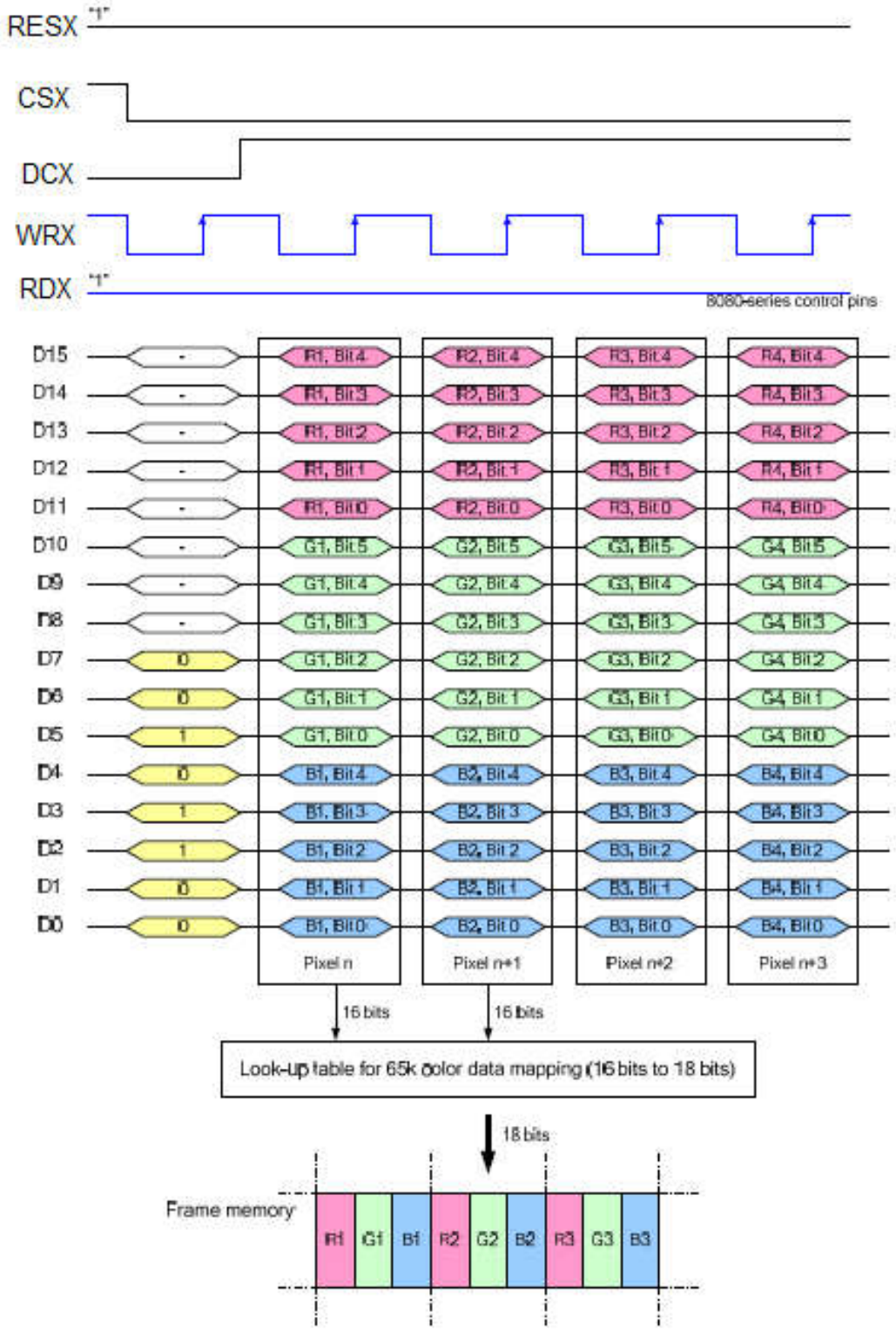
8.3.4.3 8080-I series 16-Bit Parallel Interface

The 8080-Ⅰ series 16-bit parallel interface of NV3030A can be used by setting IM[3:0]="0001b". Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

8.3.4.3.1 16-bit/pixel

There is 1 pixel (3 sub-pixels) per 1 byte



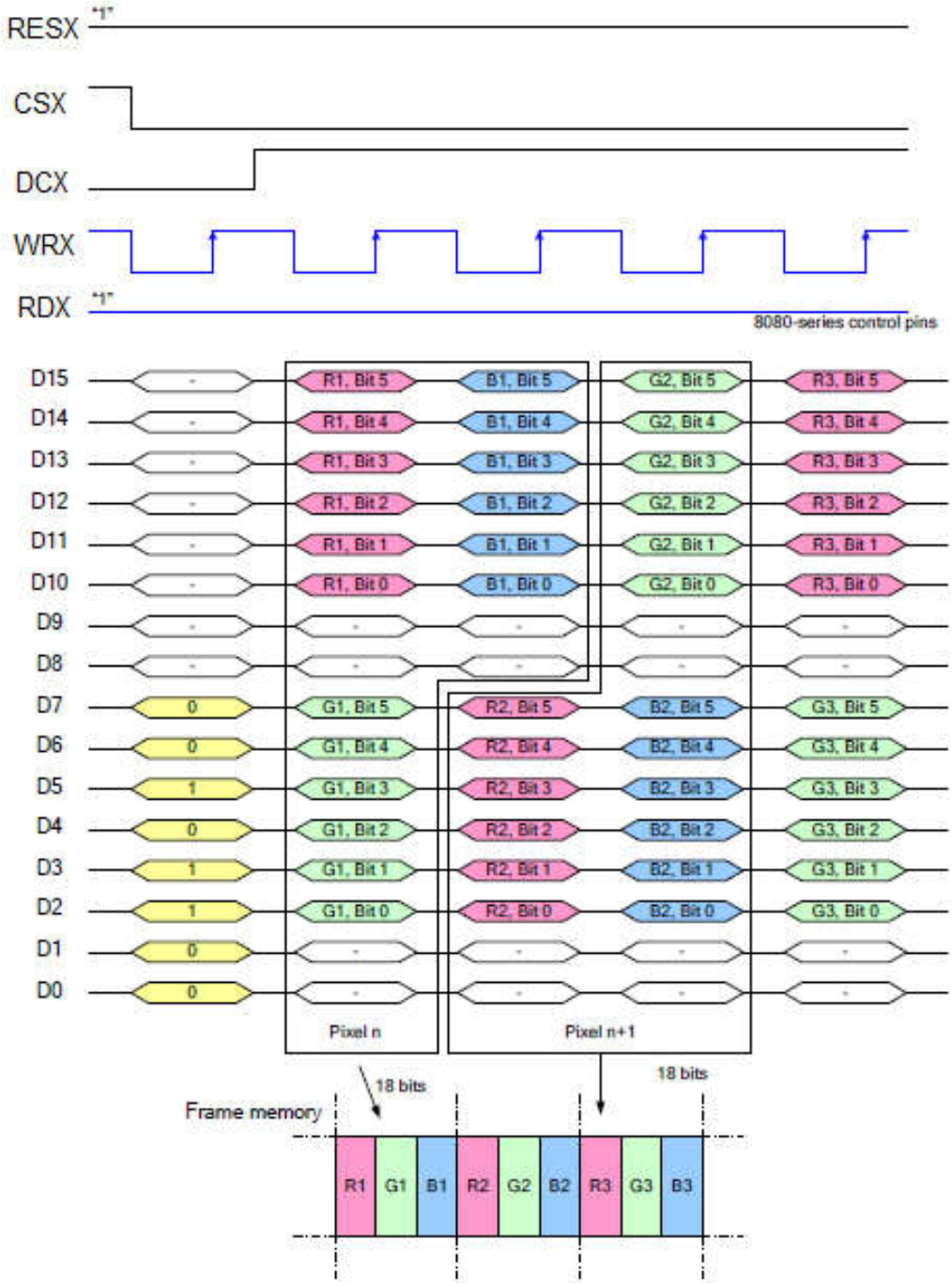
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1' .

8.3.4.3.2 18-bit/pixel(MDT[1:0]=”00b”)

There are 2 pixels (6 sub-pixels) per 3 bytes

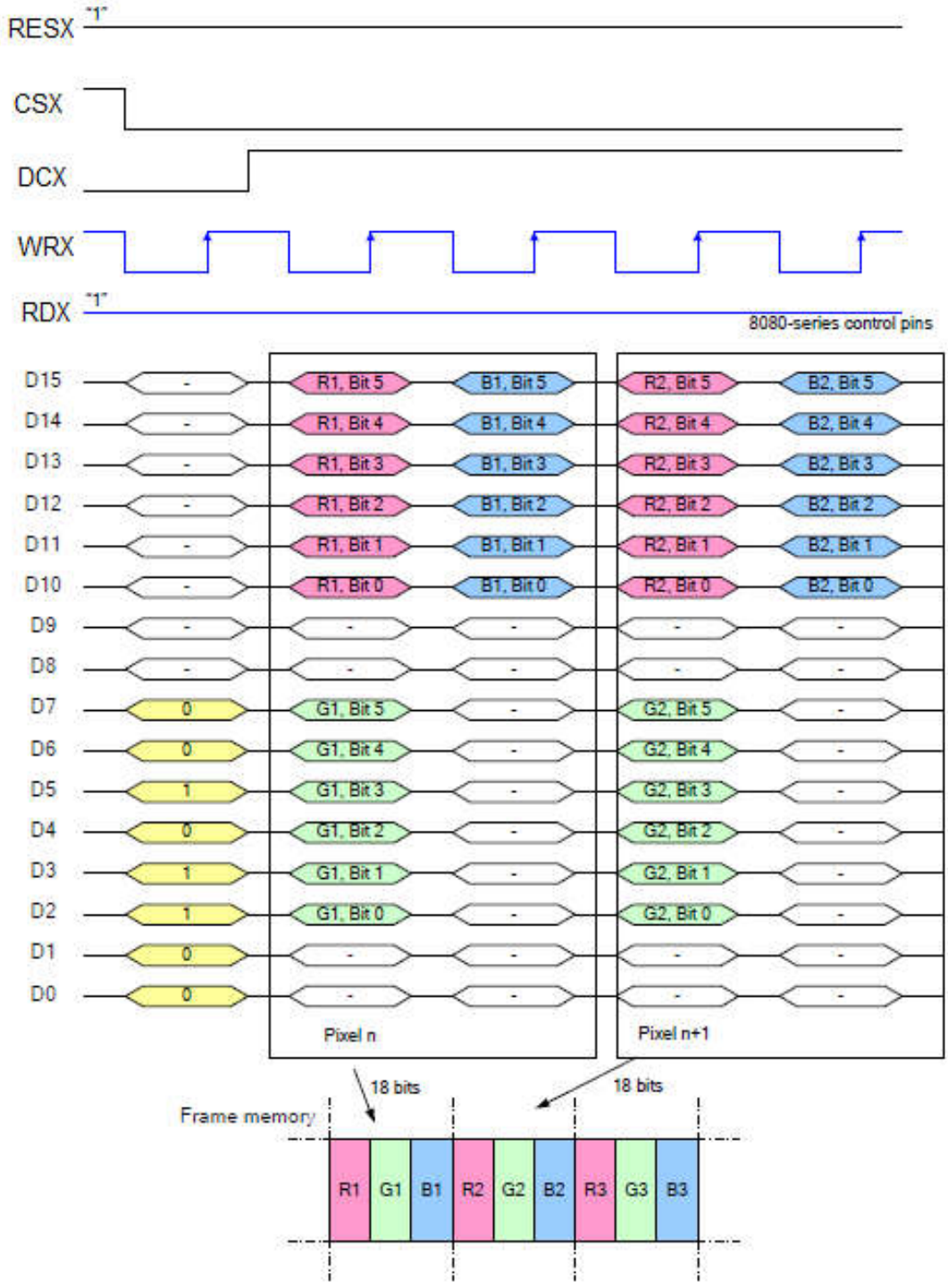


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.3.3 18-bit/pixel(MDT[1:0]=”01b”)

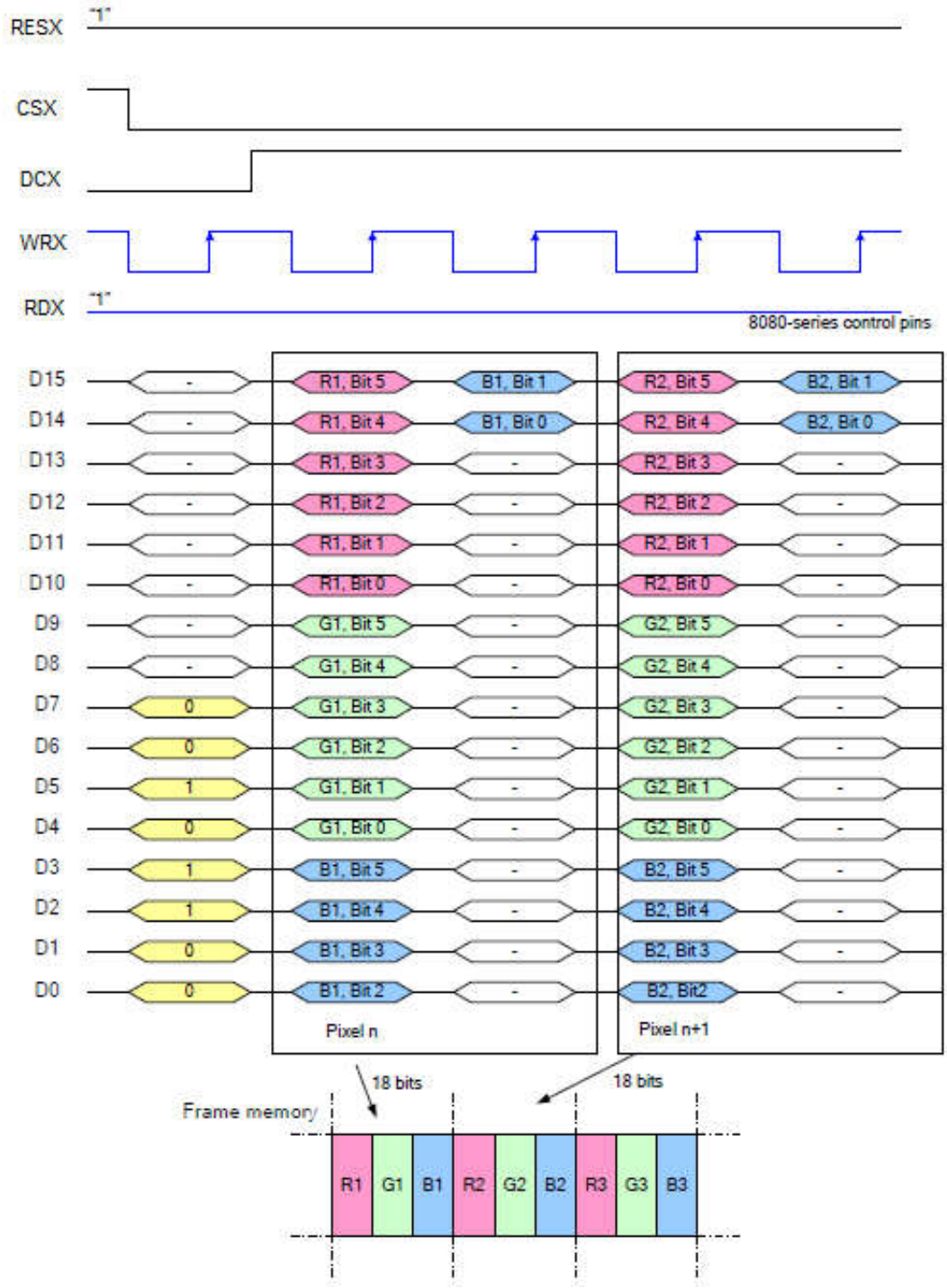


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’= Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.3.4 18-bit/pixel(MDT[1:0]=”10b”)

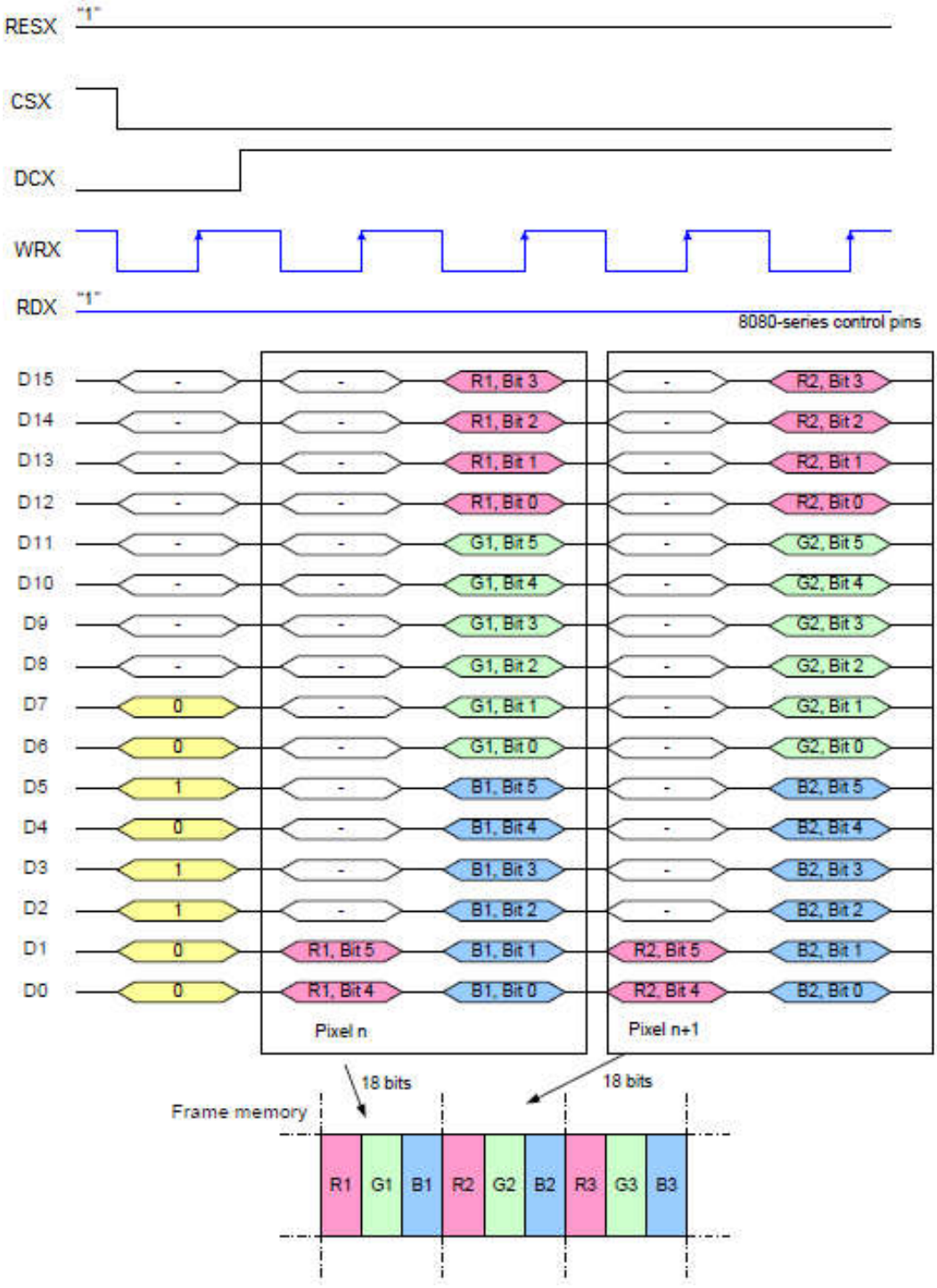


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.3.5 18-bit/pixel (MDT[1:0]=”11b”)



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

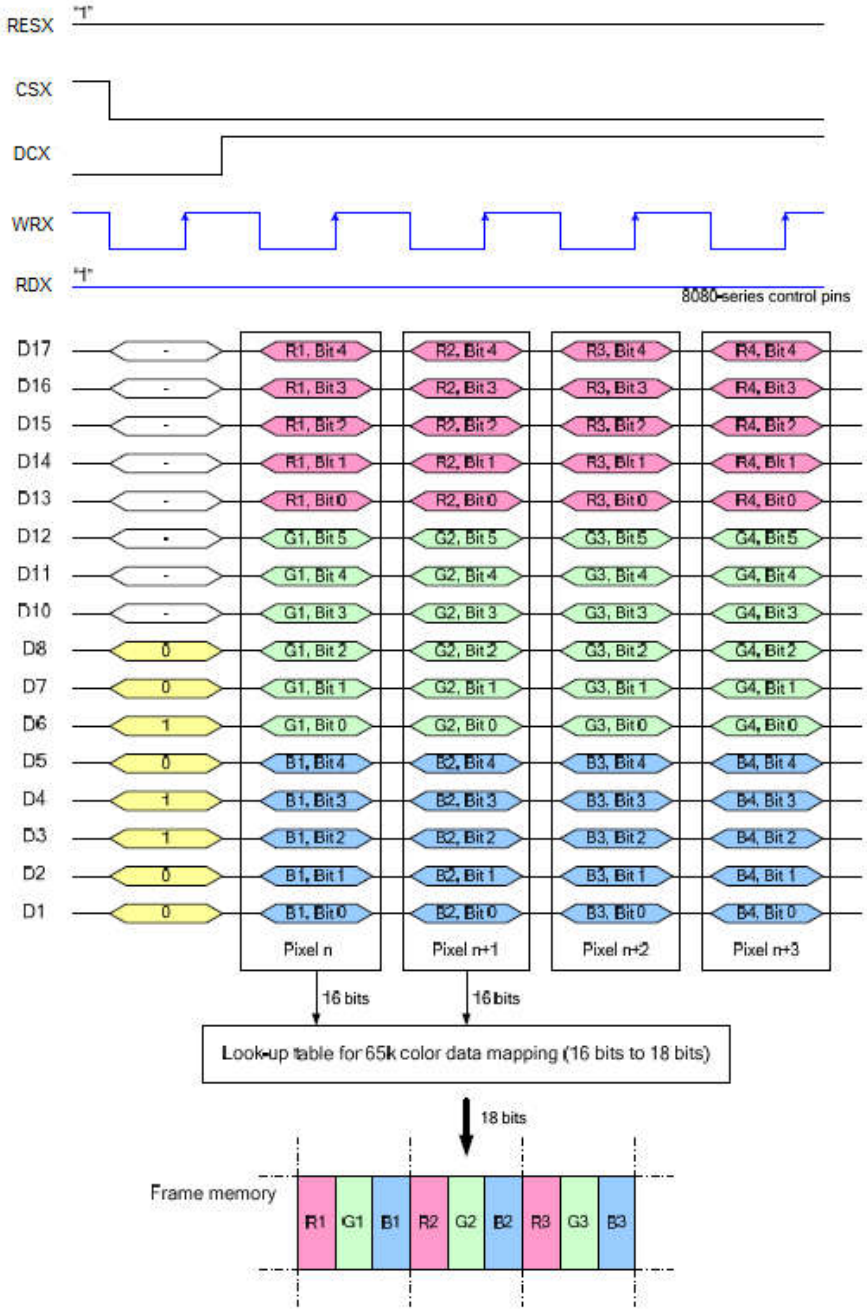
8.3.4.4 8080-Ⅱ series 16-Bit Parallel Interface

The 8080-Ⅱ series 16-bit parallel interface of NV3030A can be used by setting IM[3:0]=”1000b”. Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

8.3.4.4.1 16-bit/pixel

There is 1 pixel (3 sub-pixels) per 1 byte



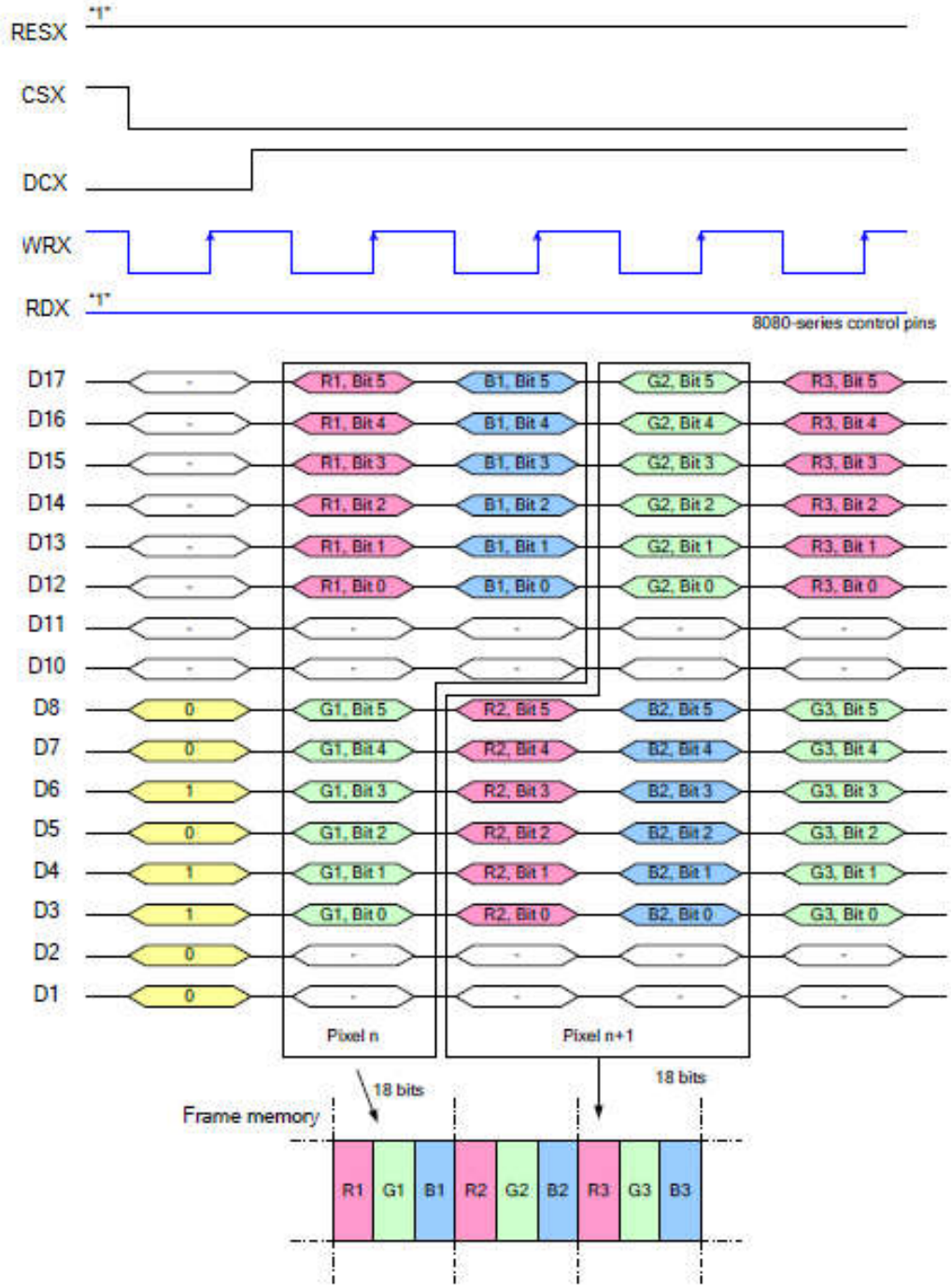
Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D17~D10, D8~D1) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-'= Don't care – Can be set to '0' or '1'.

8.3.4.4.2 18-bit/pixel(MDT[1:0]="00b")

There are 2 pixels (6 sub-pixels) per 3 bytes

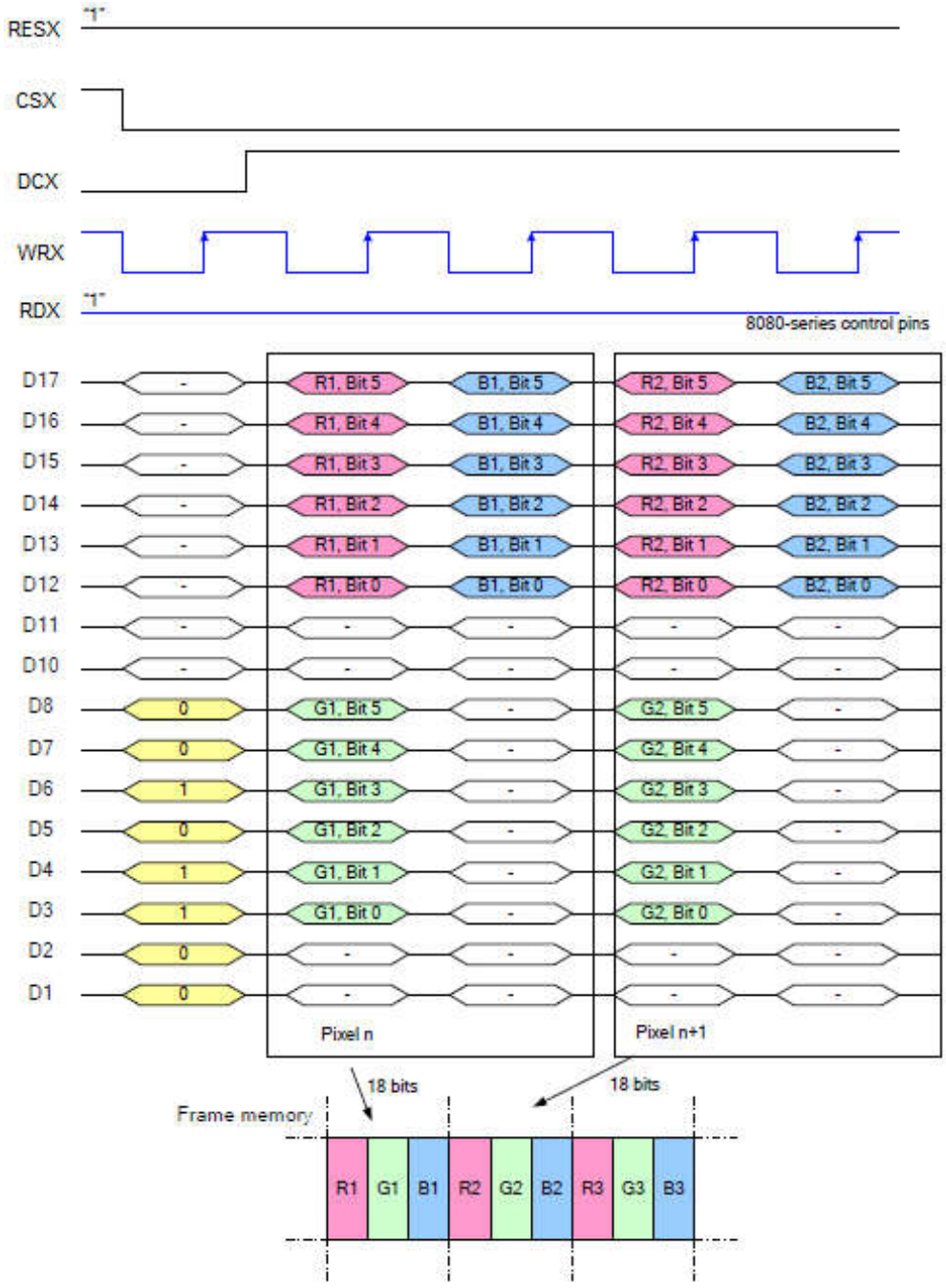


Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'.

8.3.4.4.3 18-bit/pixel(MDT[1:0]=”01b”)

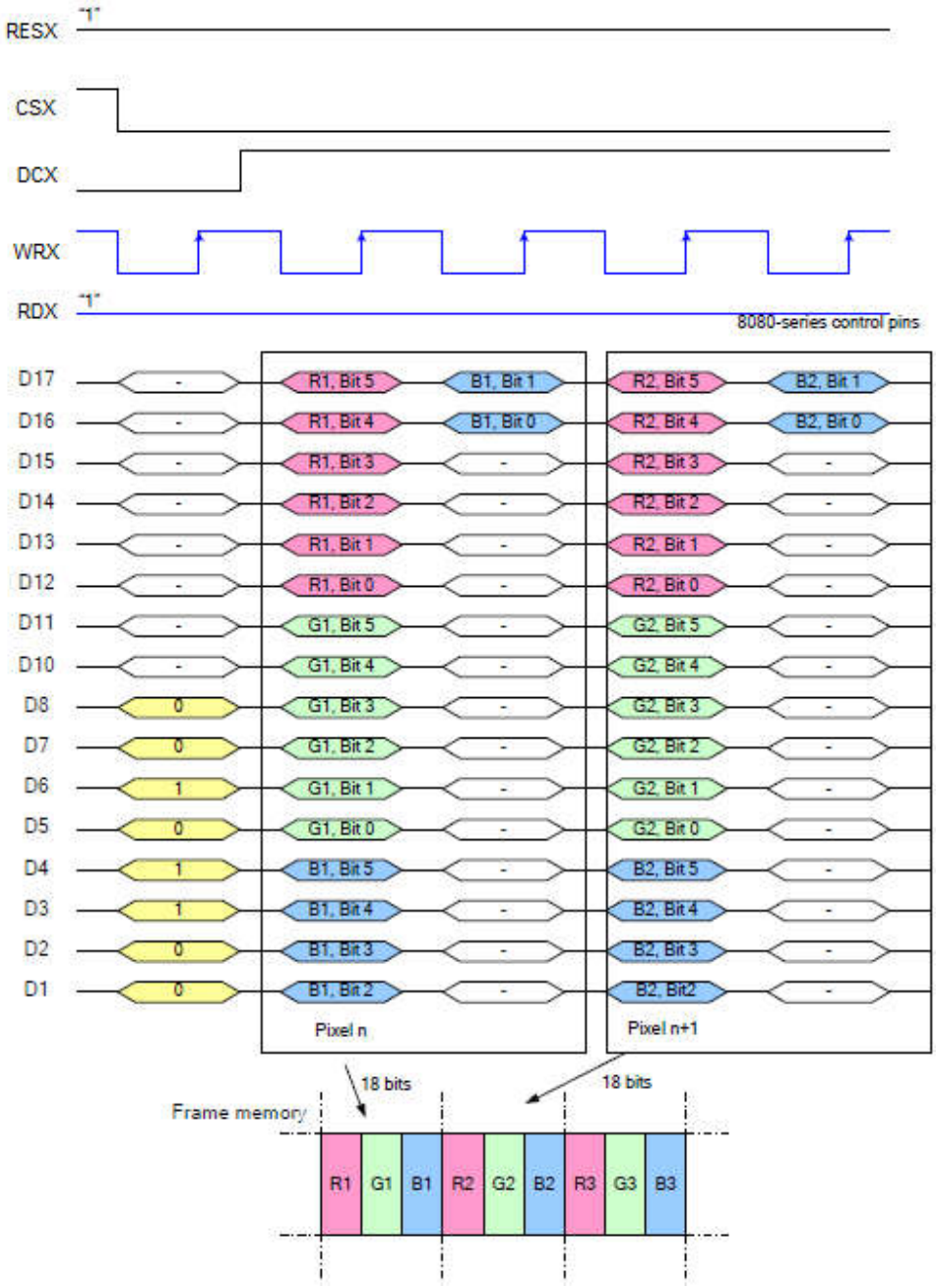


Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.4.4 18-bit/pixel(MDT[1:0]=”10b”)

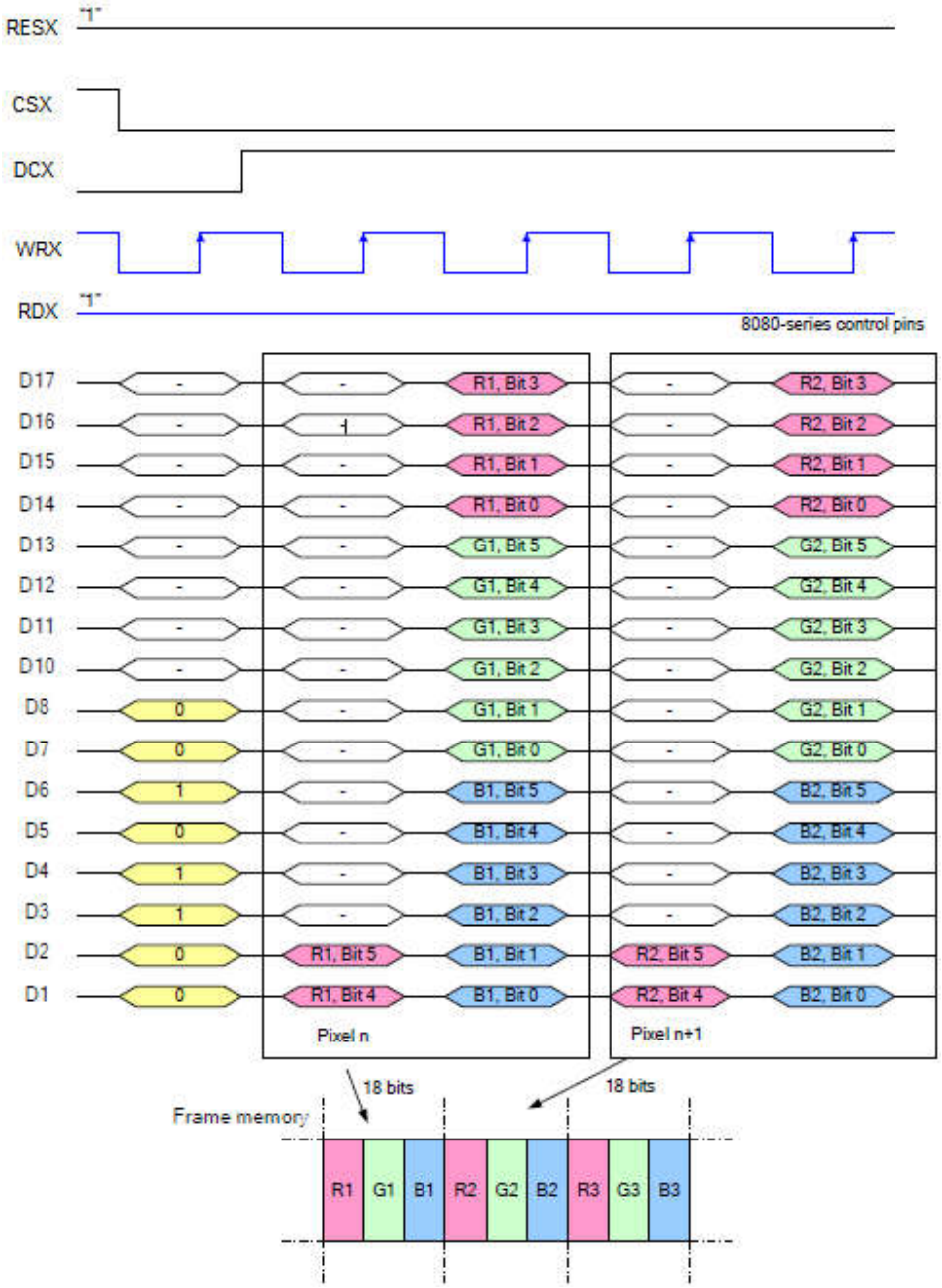


Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.4.5 18-bit/pixel(MDT[1:0]=”11b”)



Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

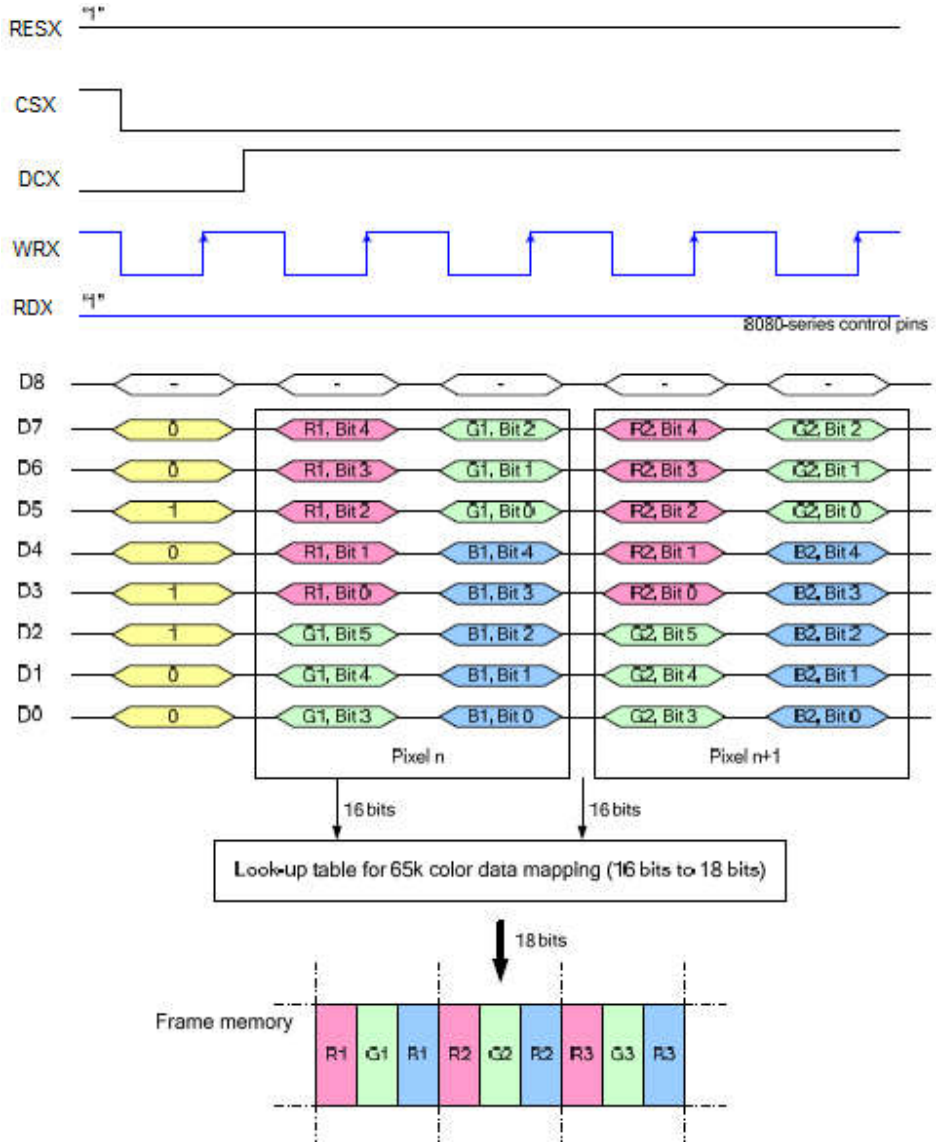
8.3.4.5 8080-I series 9-Bit Parallel Interface

The 8080-Ⅰ series 9-bit parallel interface of NV3030A can be used by setting IM[3:0]=”0010b” Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5,6,5-bit input

-262k colors, RGB 6,6,6-bit input

8.3.4.5.1 16-bit/pixel



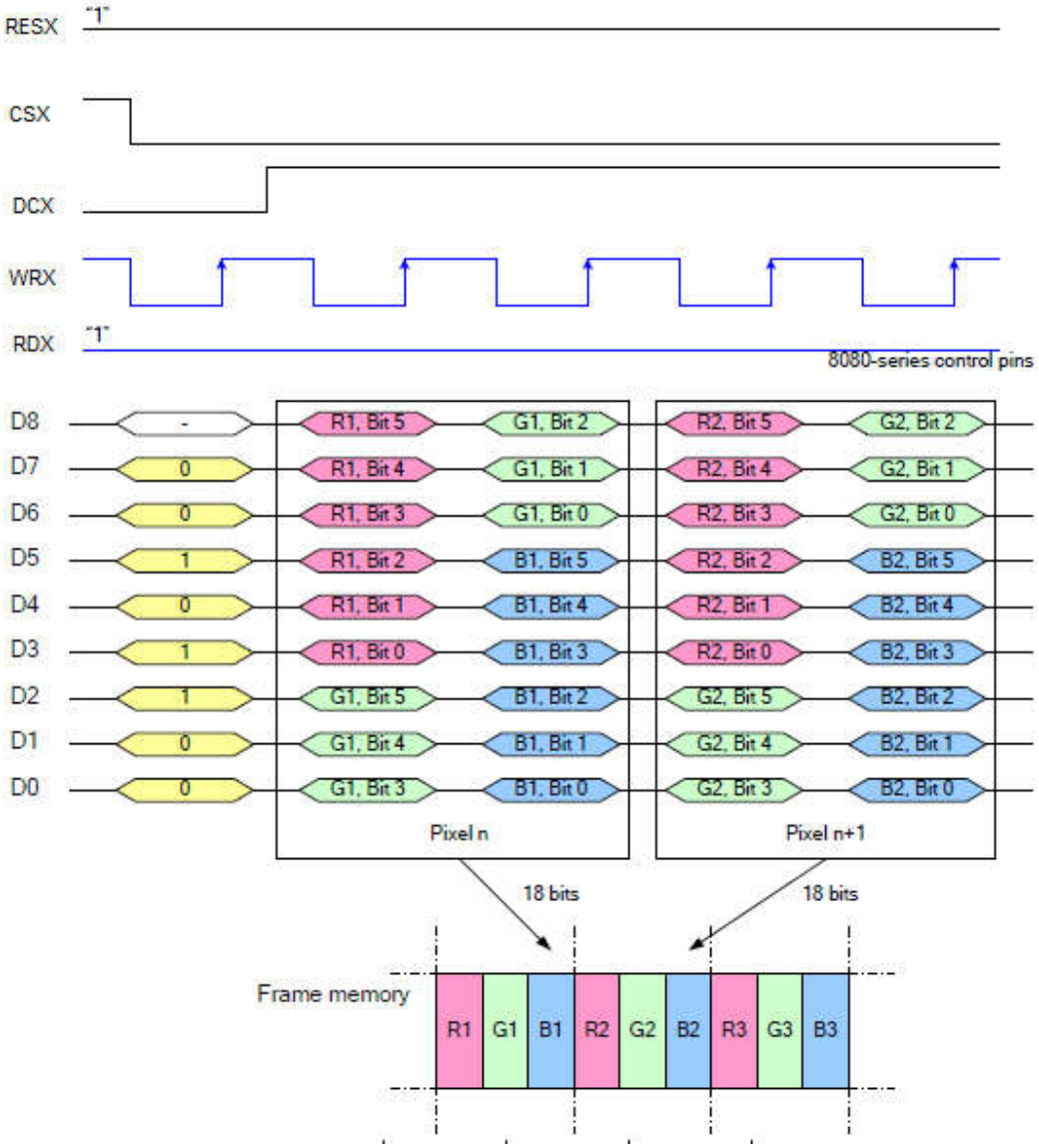
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 4, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.5.2 18-bit/pixel(MDT[1:0]=”00b”)

There is 1 pixel (3 sub-pixels) per 2bytes

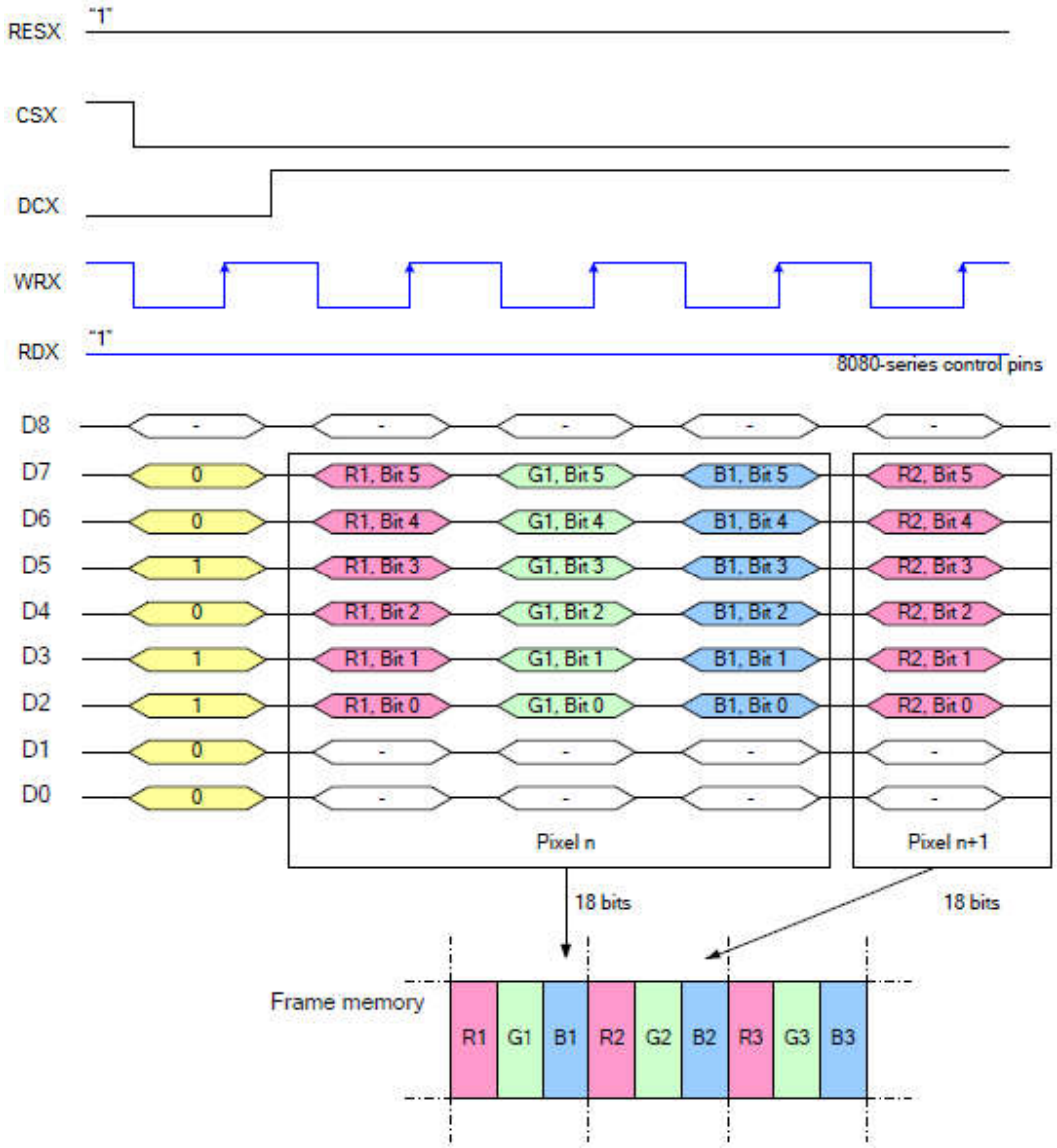


Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Greenand Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.5.3 18-bit/pixel(MDT[1:0]="01b")



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'.

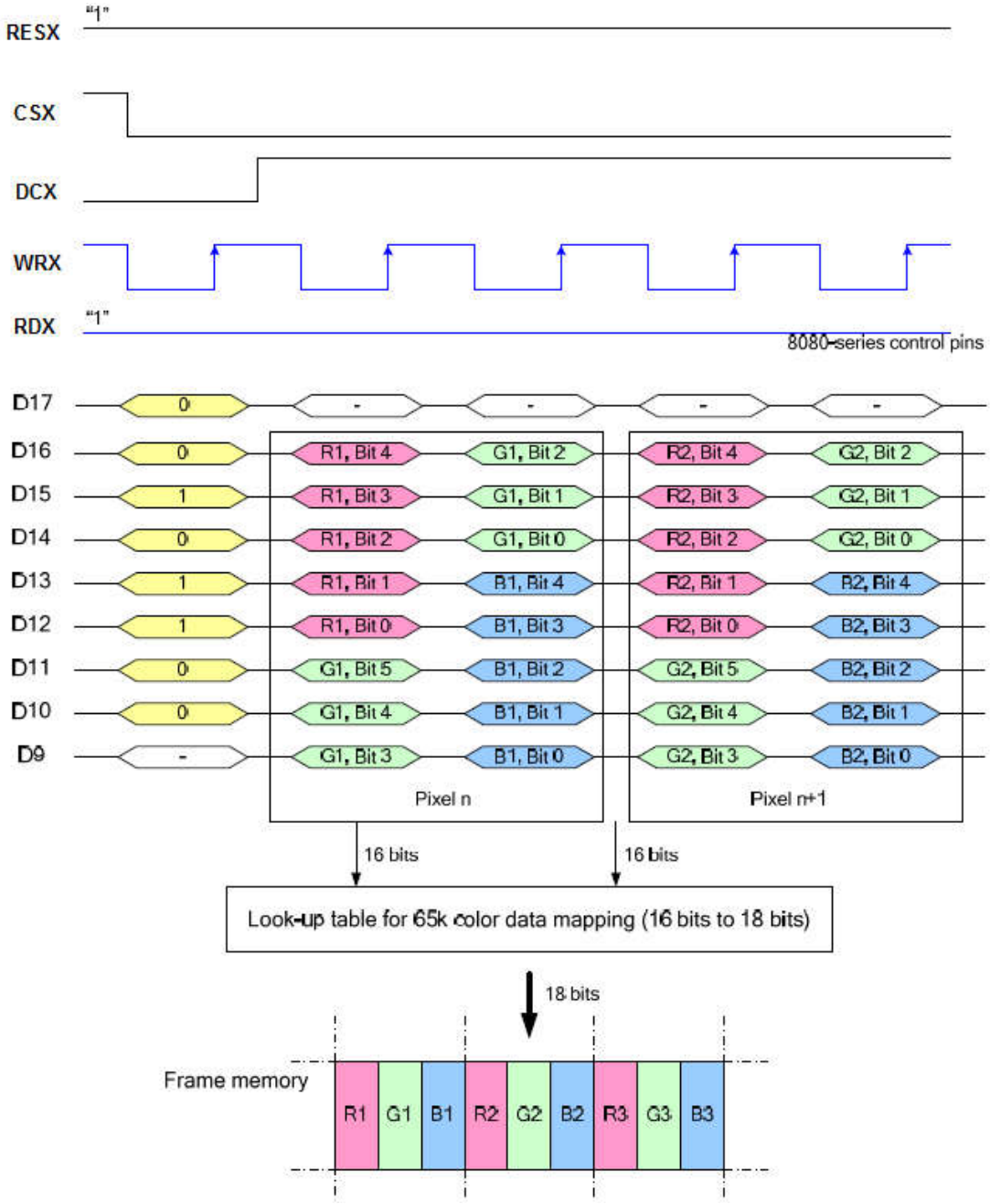
8.3.4.6 8080-II series 9-bit Parallel Interface

The 8080-Ⅱ series 9-bit parallel interface of NV3030A can be used by setting IM[3:0]=”1011b”Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5,6,5-bit input

-262k colors, RGB 6,6,6-bit input

8.3.4.6.1 16-bit/pixel



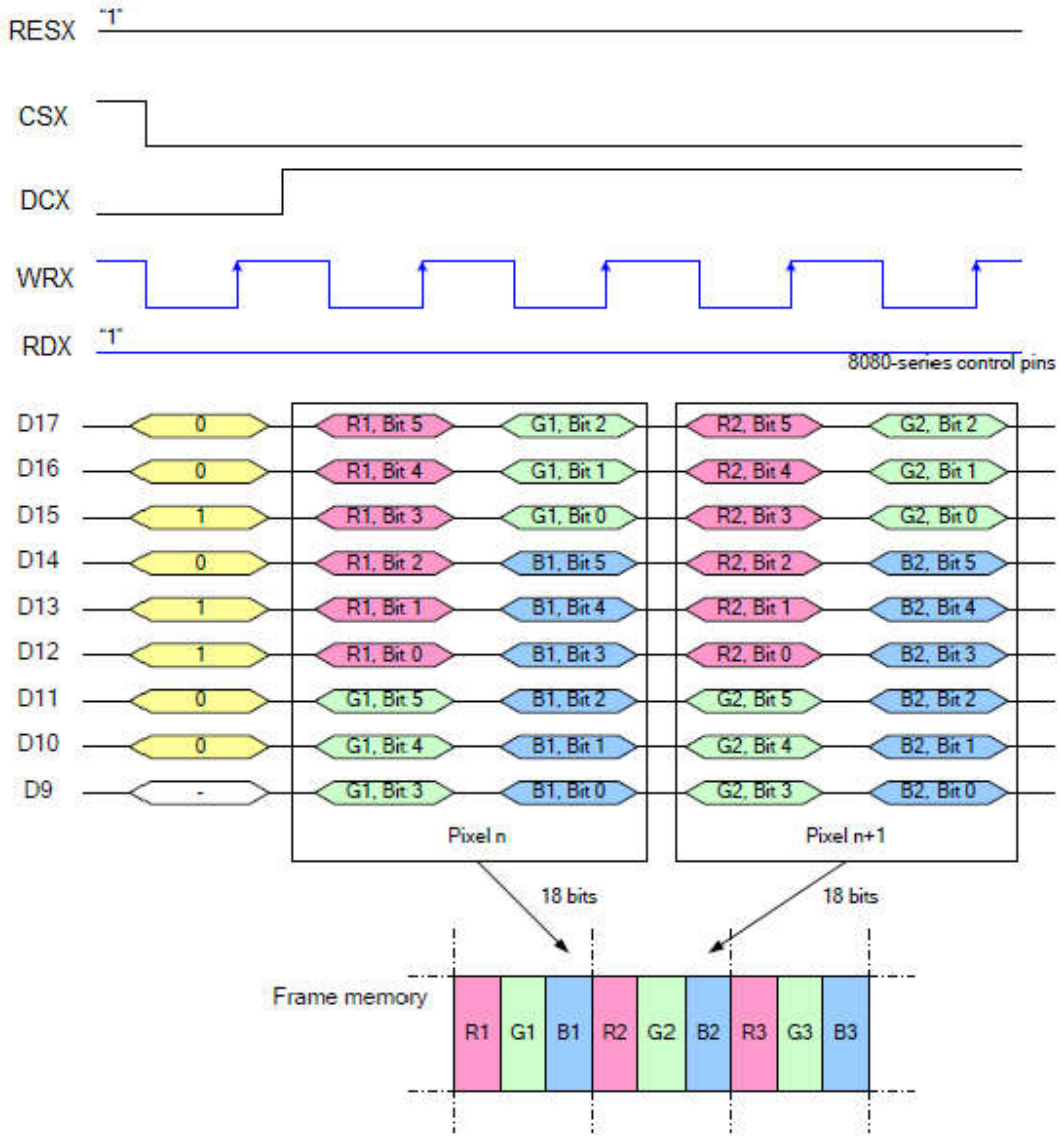
Note 1: The data order is as follows, MSB=D16, LSB=D9 and picture data is MSB=Bit 4, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.6.2 18-bit/pixel(MDT[1:0]=”00b”)

There is 1 pixel (3 sub-pixels) per 2bytes

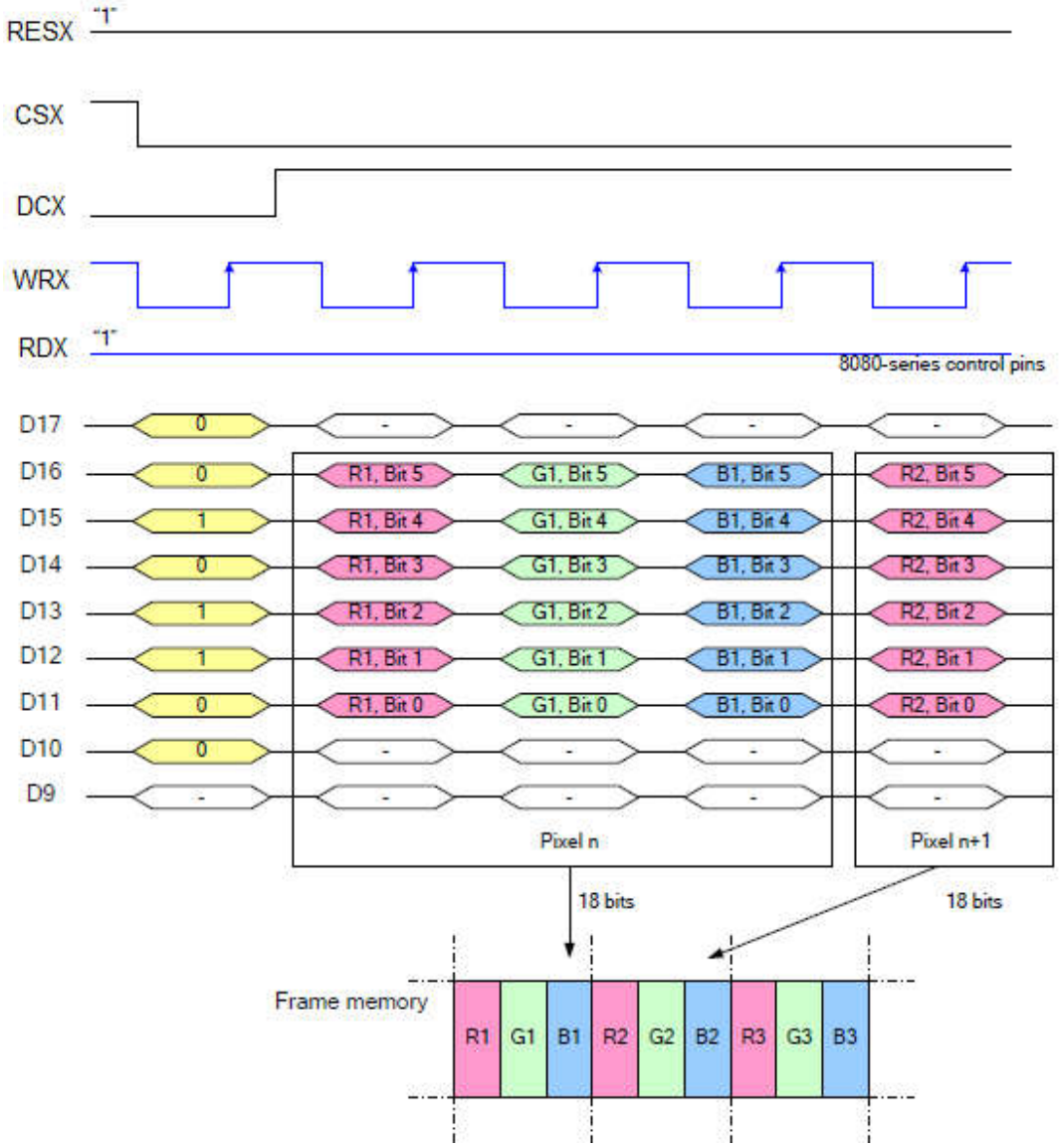


Note 1: The data order is as follows, MSB=D17, LSB=D9 and picture data is MSB=Bit 5, LSB=Bit 0 for Red,Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

8.3.4.6.3 18-bit/pixel(MDT[1:0]=”01b”)



Note 1: The data order is as follows, MSB=D16, LSB=D11 and picture data is MSB=Bit 5, LSB=Bit 0 for Red,Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: ‘-’ = Don’t care – Can be set to ‘0’ or ‘1’.

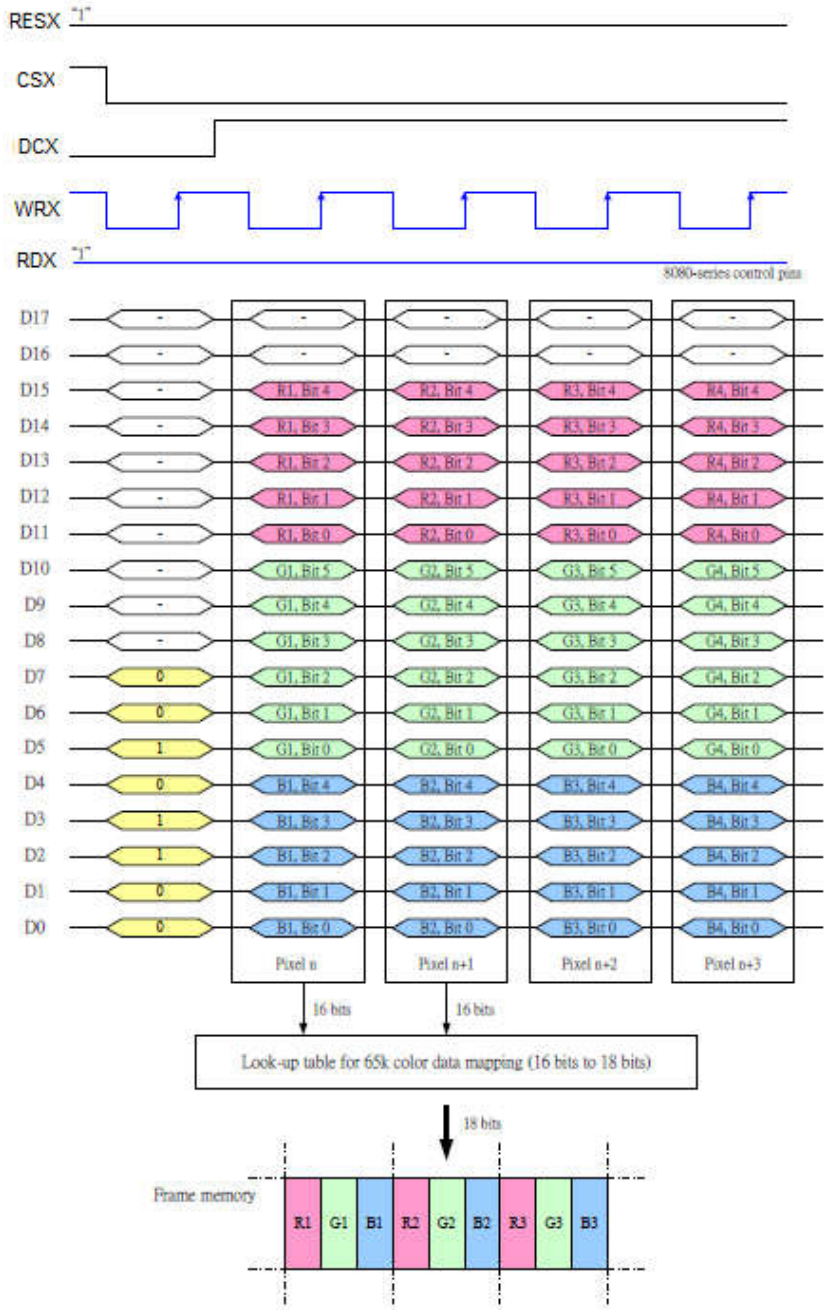
8.3.4.7 8080-I series 18-Bit Parallel Interface

The 8080- Ⅰ series 18-bit parallel interface of NV3030A can be used by setting IM[3:0]=”0011b”. Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

8.3.4.7.1 16-bit/pixel

There is one pixel (3 sub-pixels) per byte

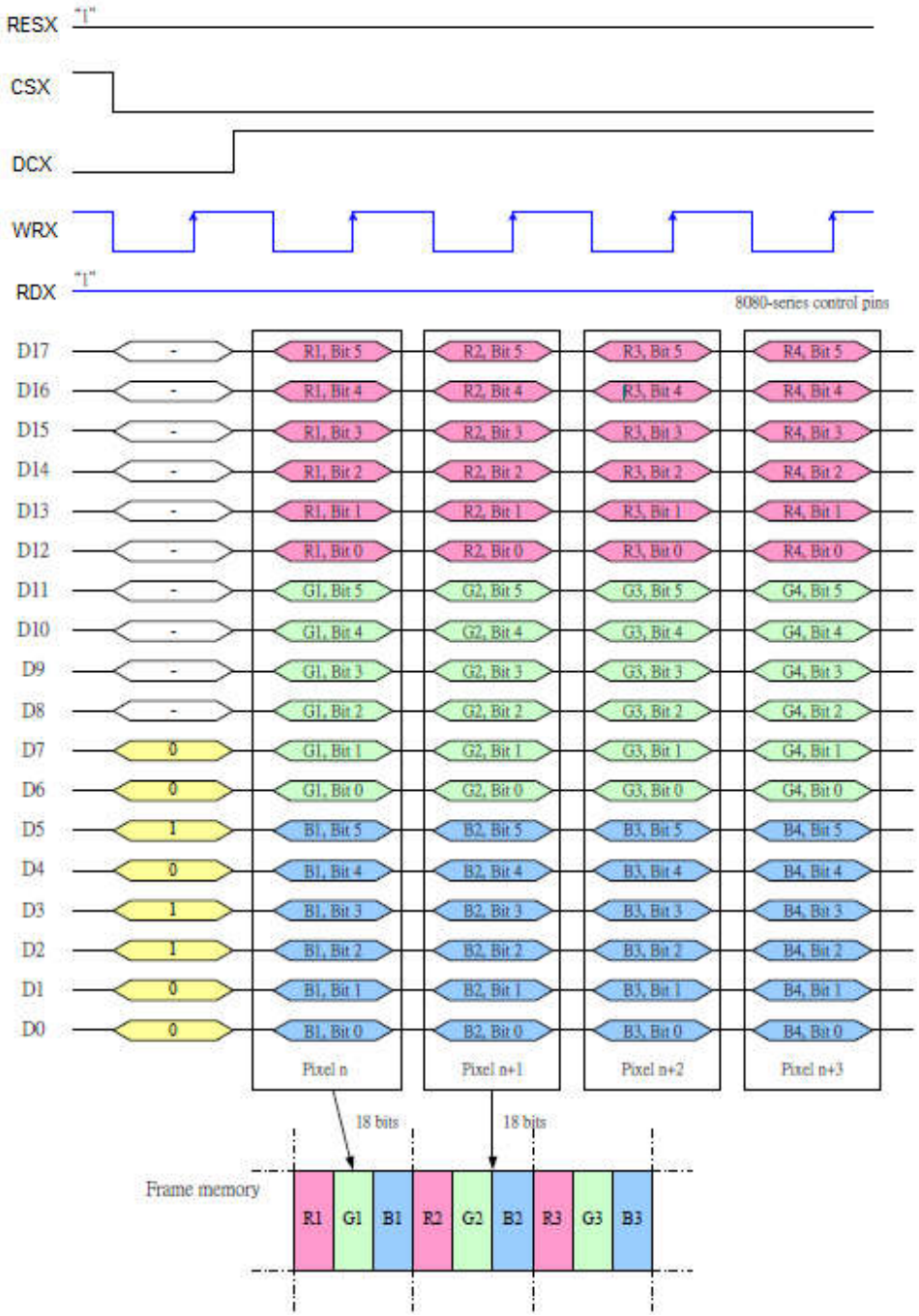


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

8.3.4.7.2 18-bit/pixel

There is 1 pixel (3 sub-pixels) per byte



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read,Green and Blue data.

Note 2: 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

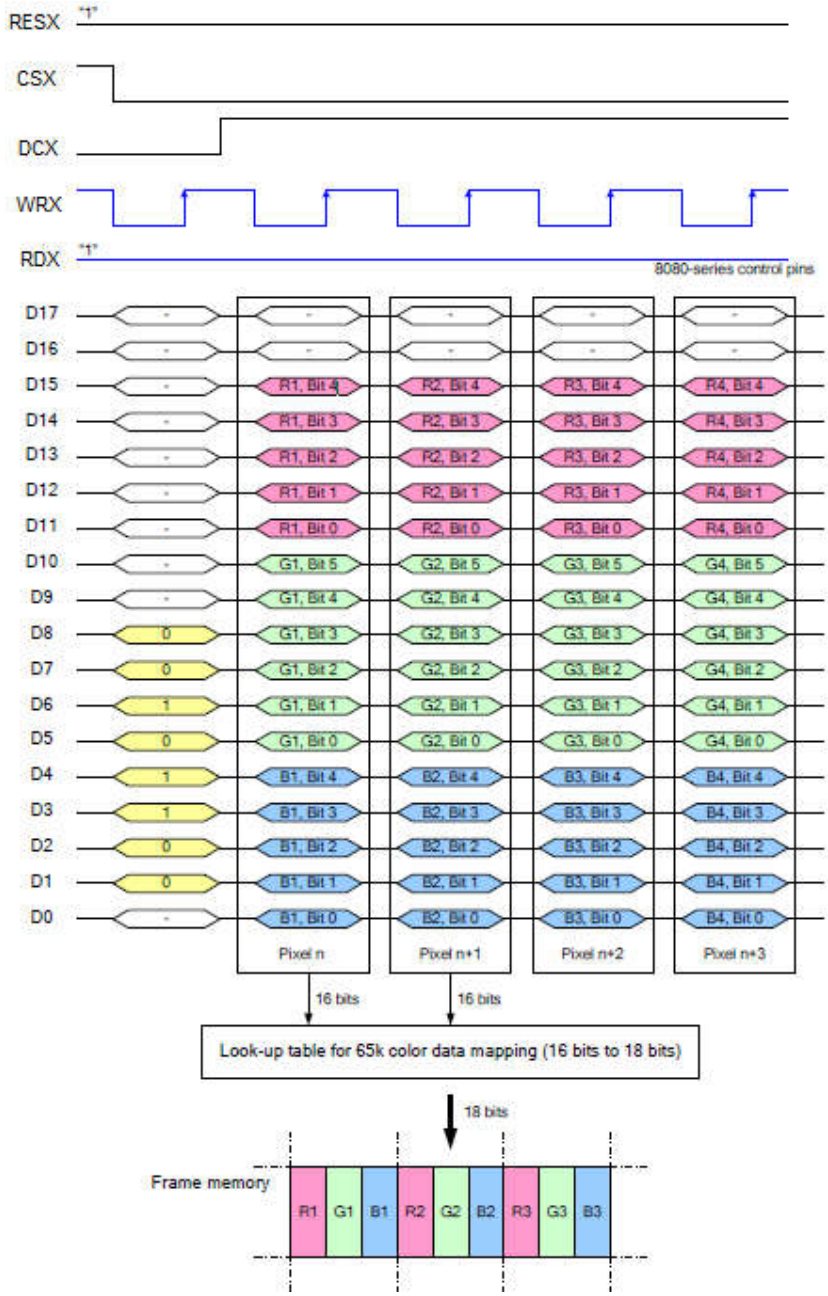
8.3.4.8 8080-Ⅱ series 18-Bit Parallel Interface

The 8080-Ⅱ series 18-bit parallel interface of NV3030A can be used by setting IM[3:0]=”1010b”. Different display data formats are available for two colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

8.3.4.8.1 16-bit/pixel

There is one pixel (3 sub-pixels) per byte

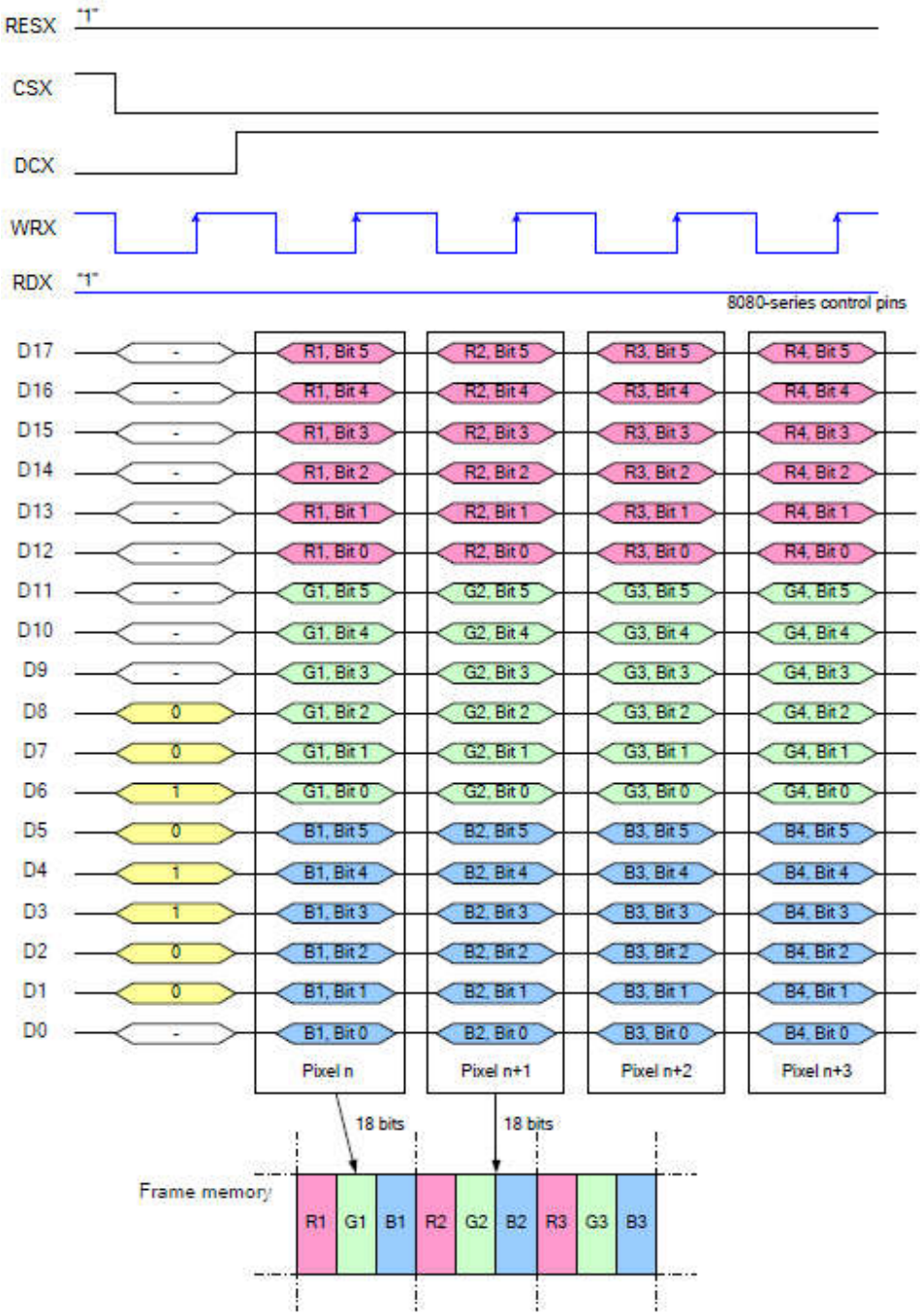


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green,and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

8.3.4.8.2 18-bit/pixel

There is 1 pixel (3 sub-pixels) per byte

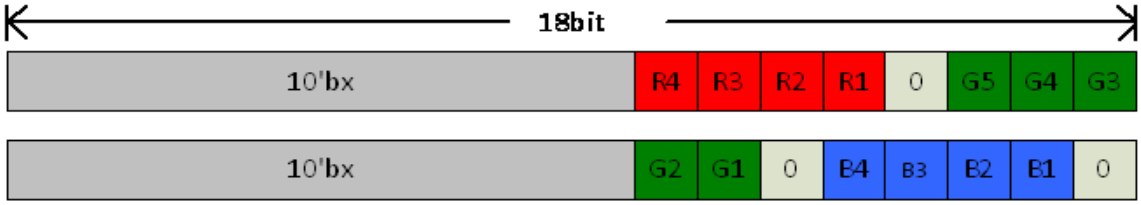


Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

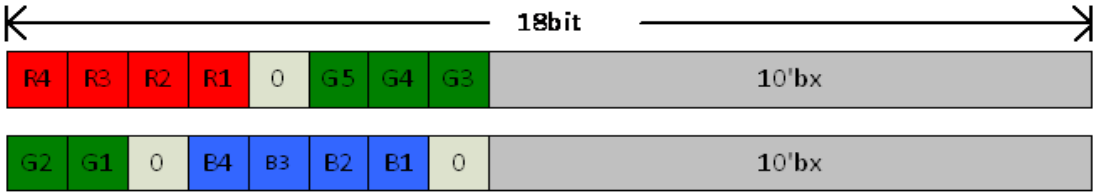
Note 2: 1-times transfer (D17 to D0) is used to transmit 1 pixel data with the 18-bit color depth information.

8.3.4.9 Read Memory Data Color Coding

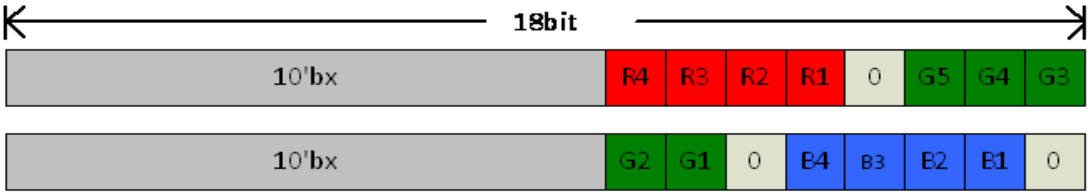
8.3.4.9.1 8 Data Line Parallel Interface I



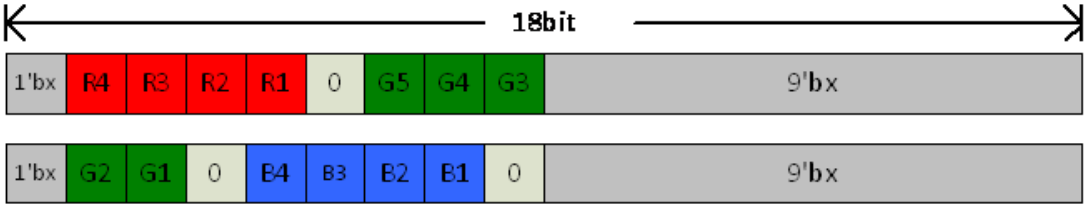
8 Data Line Parallel Interface II



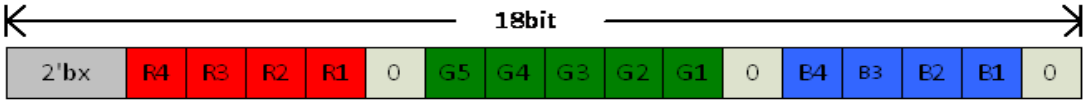
8.3.4.9.2 9 Data Line Parallel Interface I



9 Data Line Parallel Interface II

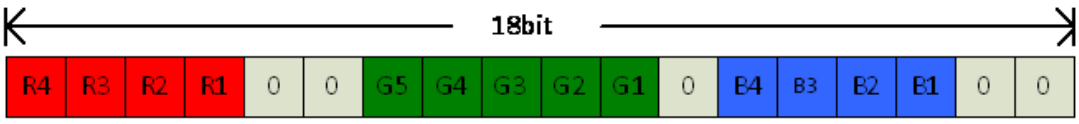


8.3.4.9.3 16 Data Line Parallel Interface I



16 Data Line Parallel Interface II

8.3.4.9.4 18 Data Line Parallel Interface I & II

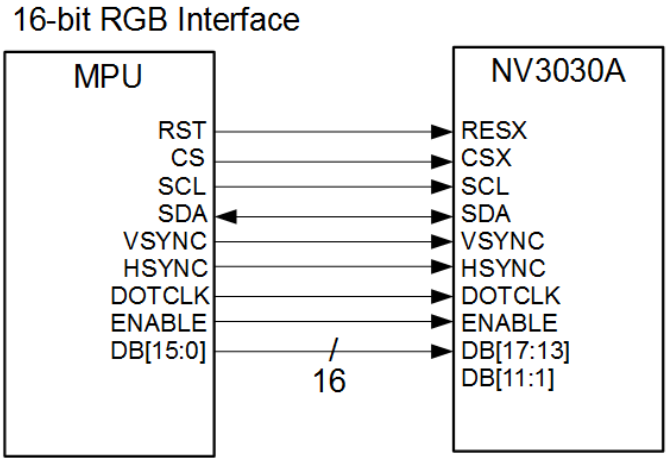


Note:‘bx’means these bits are not usable.

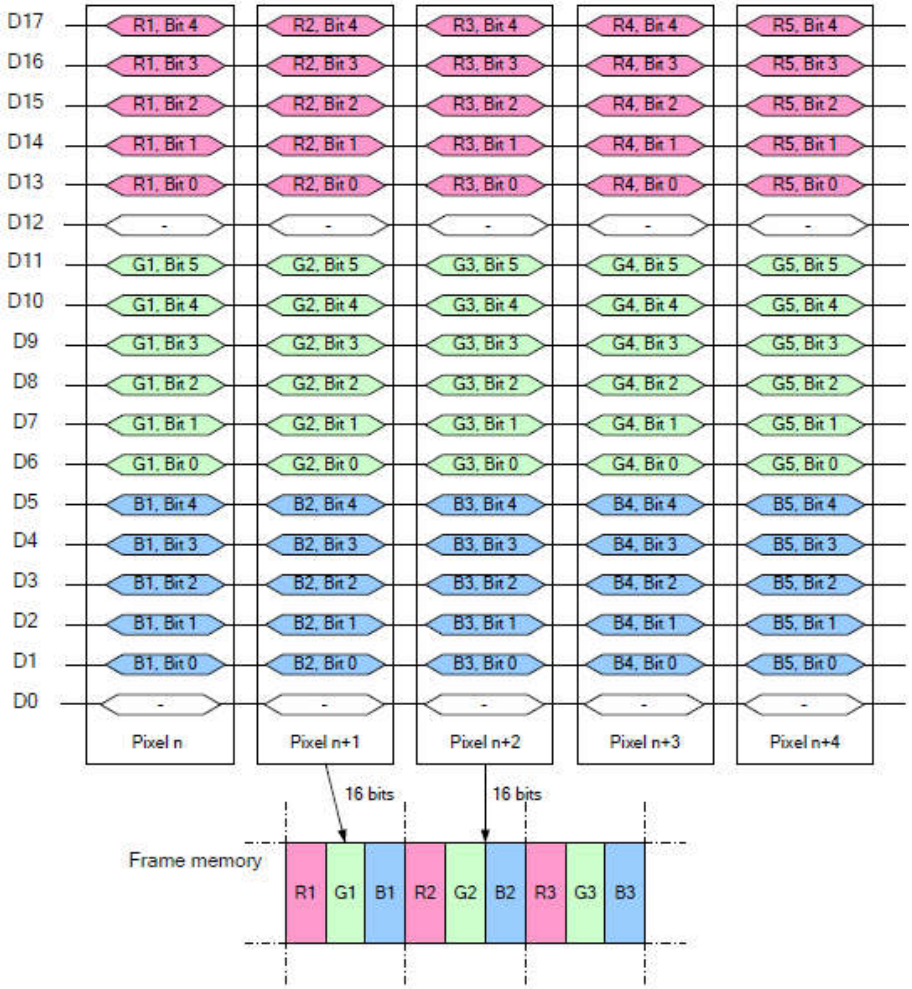
8.3.5 RGB Interface

NV3030A supports two kinds of RGB interface, DE mode and SYNC mode, and 16bit/18bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0] pins can be used; when SYNC mode is selected and the VSYNC, HSYNC, DOTCLK, DB[17:0] pins can be used. When using RGB interface, only serial interface can be selected.

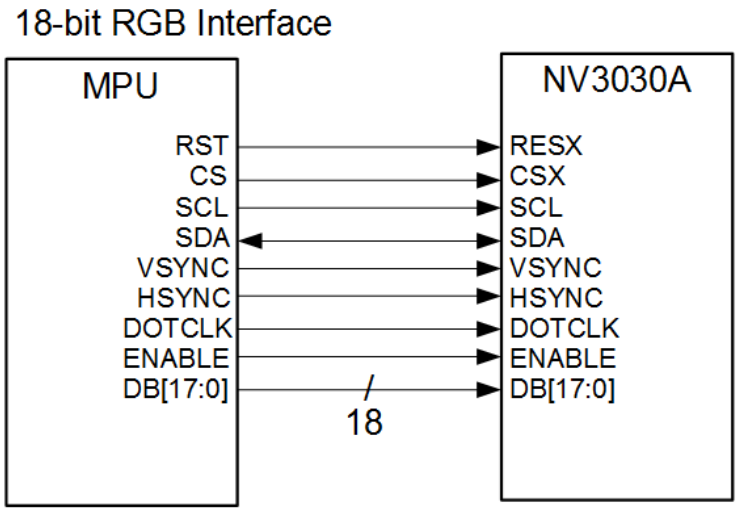
8.3.5.1 16-bit RGB interface



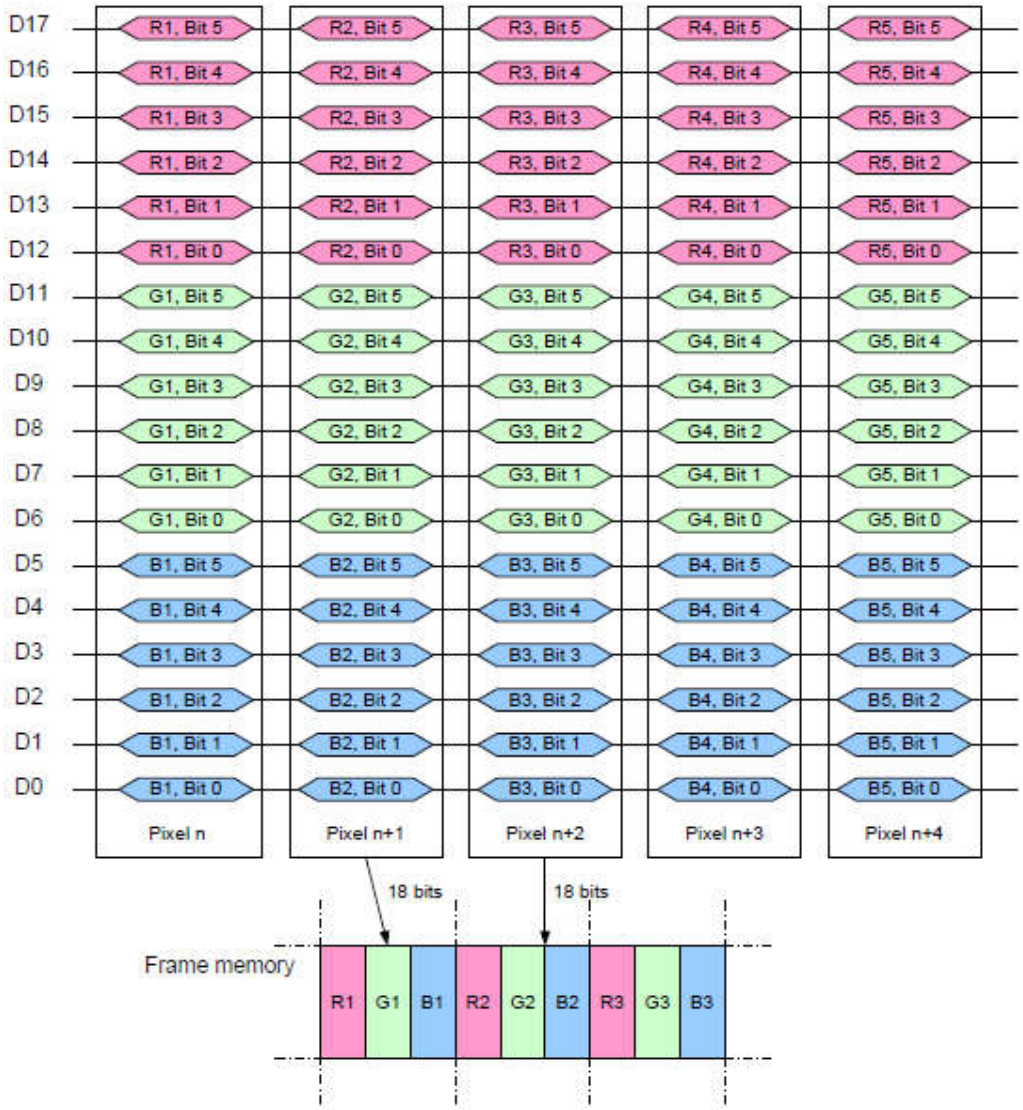
Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



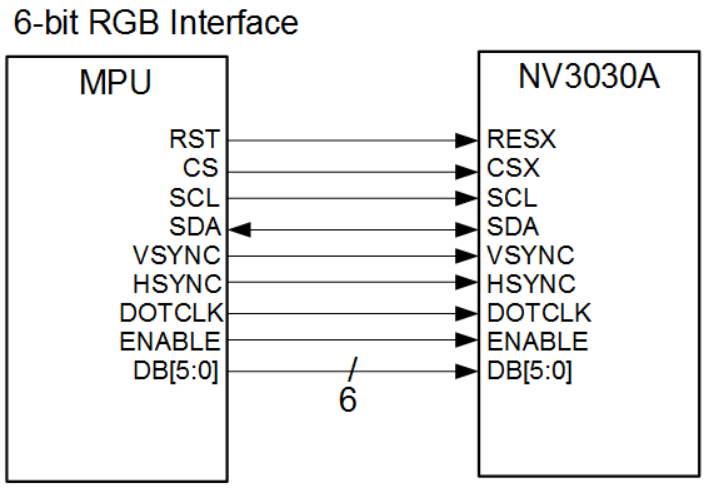
8.3.5.2 18-bit RGB interface



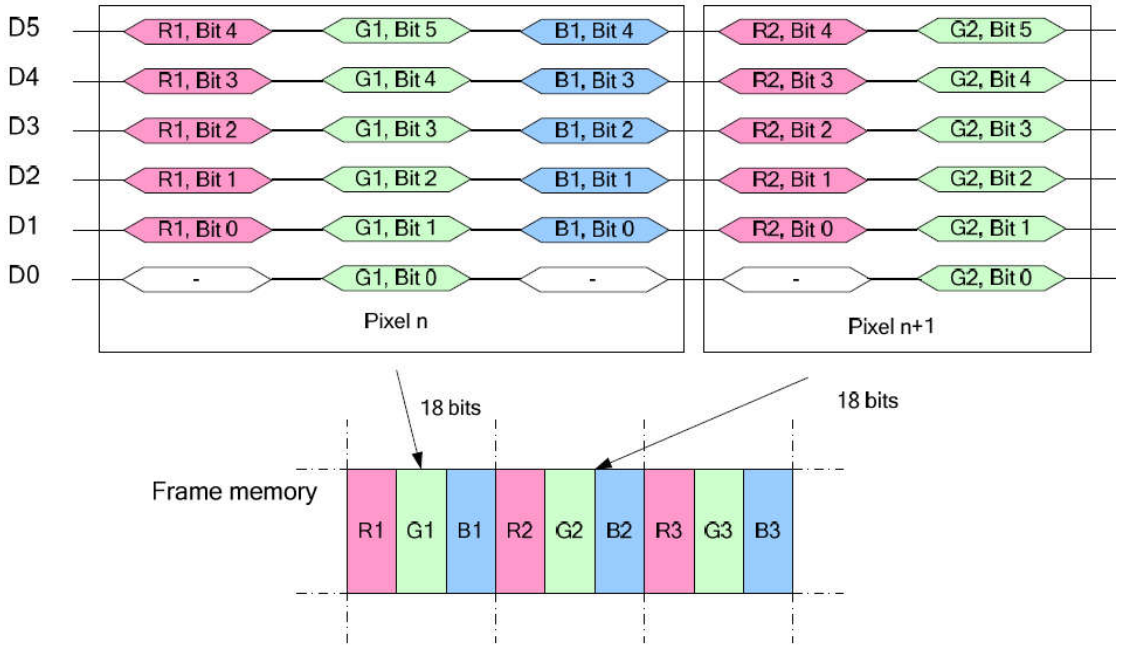
Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors



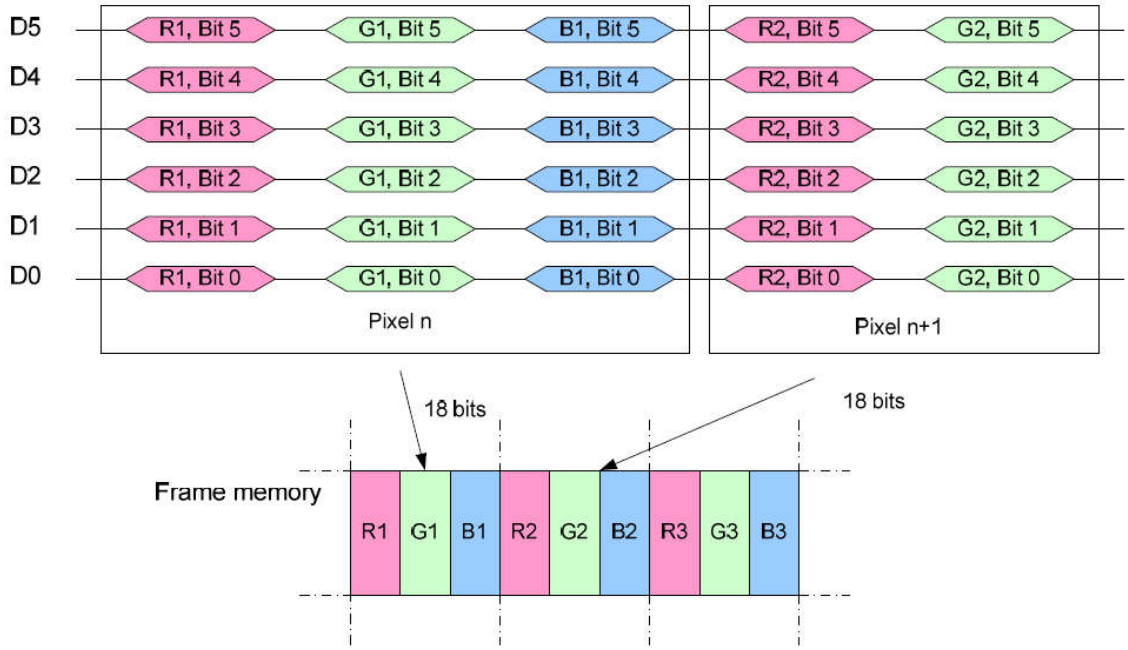
8.3.5.3 6-bit RGB interface



8.3.5.3.1 16-bit/pixel



8.3.5.3.2 18-bit/pixel

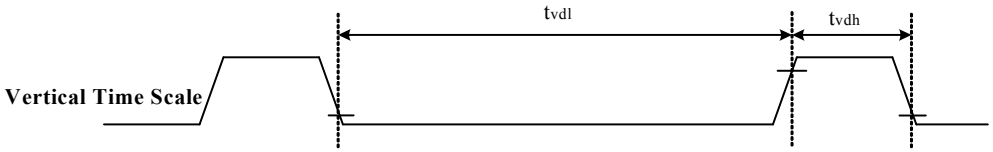


8.4 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

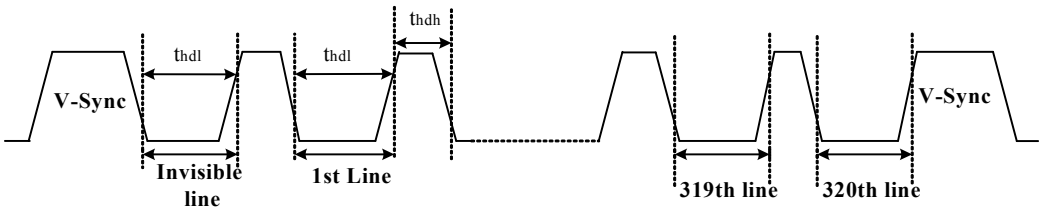
8.4.1 Tearing Effect line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync Information only:

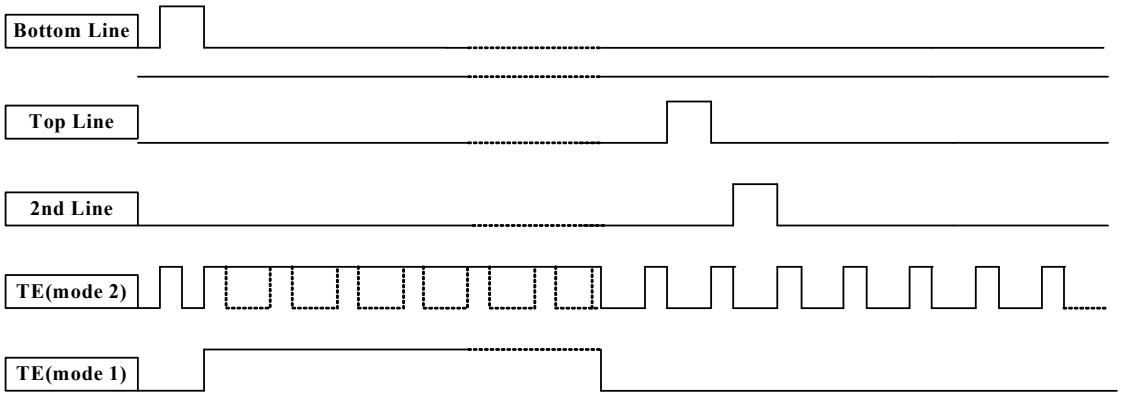


tvdh = The LCD display is not updated from the Frame Memory;
tvdl = The LCD display is updated from the Frame Memory(except Invisible Line – see below).

Mode 2, the Tearing Effect Output signal consists of V-Sync and H-Sync Information, there is one V-sync and 320 H- sync pulses per field:



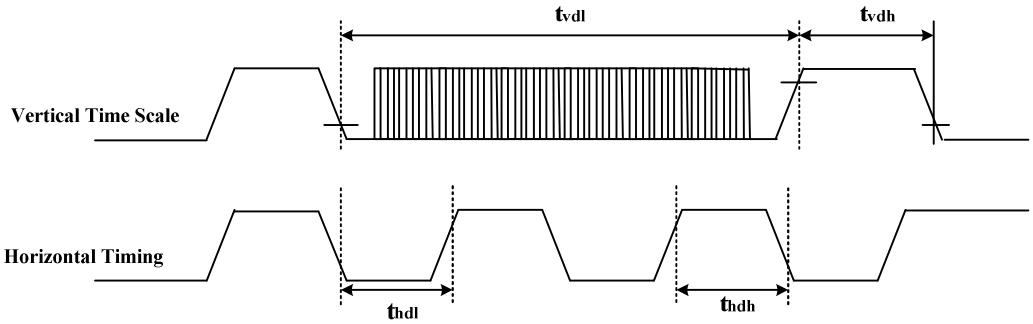
thdh = The LCD display is not updated from the Frame Memory;
thdl = The LCD display is updated from the Frame Memory(except Invisible Line – see below).



Note: During sleep in Mode,the tearing effect Output pin is active low.

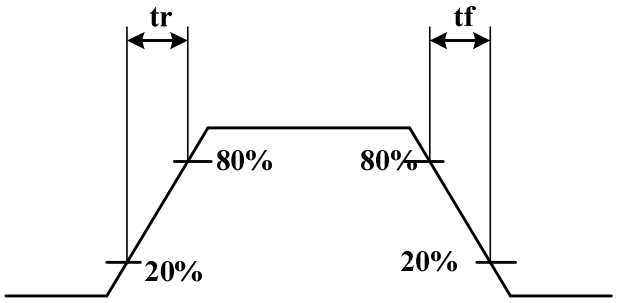
8.4.2 Tearing Effect line Timings

The Tearing Effect signal is described below:



Symbol	Parameter	Min.	Max	Unit
tvdl	Vertical Timing Low Duration	13	17	ms
tvdh	Vertical Timing High Duration	1000	1300	us
thdl	Horizontal Timing Low Duration	20	-	us
thdh	Horizontal Timing High Duration	10	500	us

Notes:
The timings in this table apply when MADCTL B4=0 and B4=1.
The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns.



The tearing effect output line is fed back to the MPU and should be used to avoid tearing effect.

8.5 Power On/Off Sequence

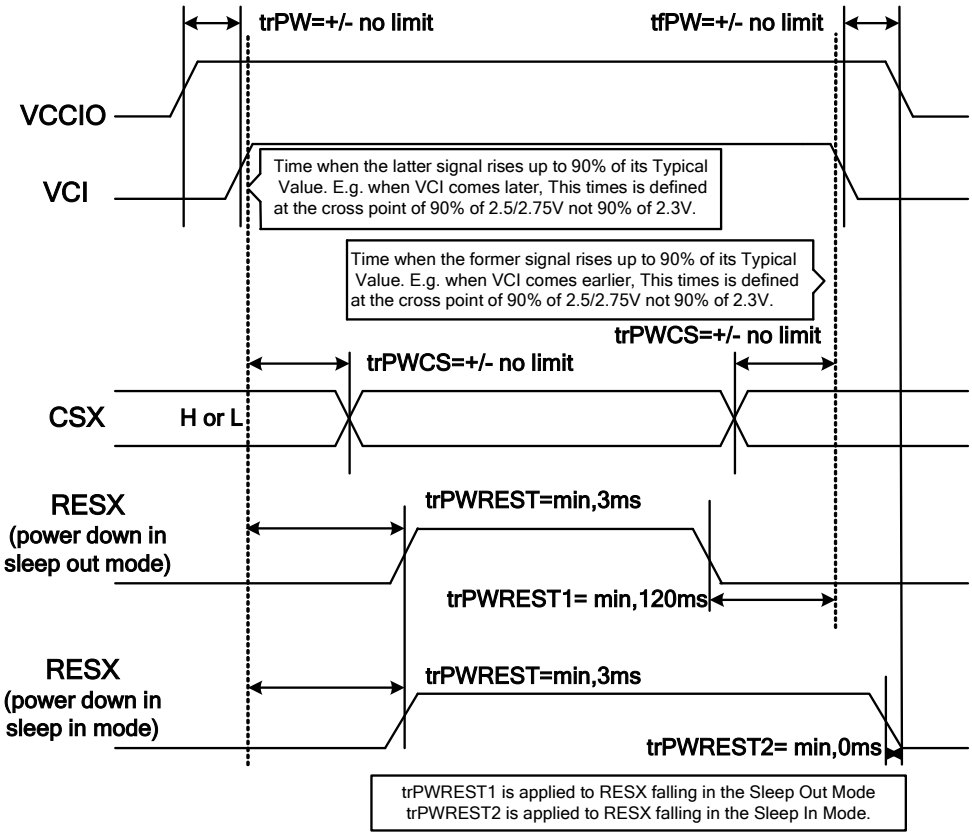
8.5.1 Power On/Off Sequence

VDDI and VCI can be applied in any order.
VCI and VDDI can be powered down in any order.
During power off, if LCD is in the Sleep Out Mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Notes:
1. There will be no damage to the display module if the above power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power off sequence.
4. If RESX line is not held stable by MPU during Power On Sequence ,it will be necessary to apply a Hardware Reset (RESX) after MPU Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

8.5.1.1 Case 1 – RESX line is held high or Unstable by MPU at Power On

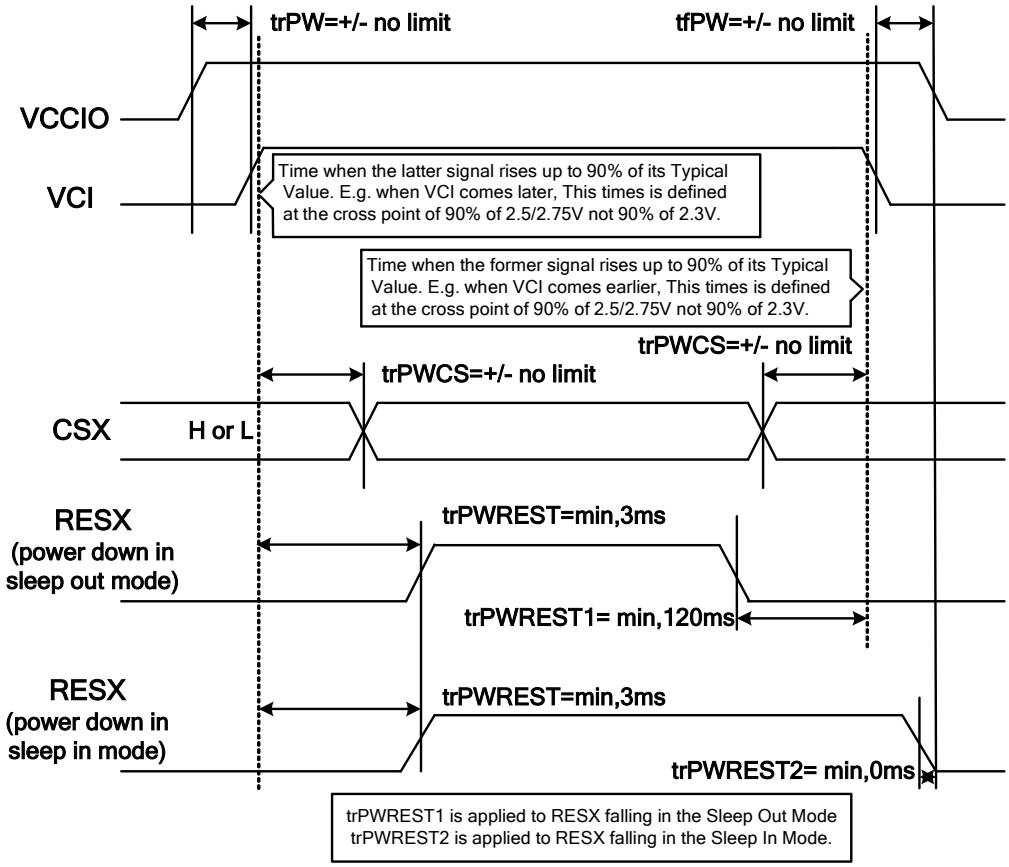
If RESX line is held High or unstable by the MPU during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timing here in show cross point at 50% of signal/power level.

8.5.1.2 Case 2 – RESX line is held low by MPU at Power On

If RESX line is held Low (and stable) by the MPU during Power On, then the RESX must be held low for minimum 3msec after both VCI and VDDI have been applied.



Note: Unless otherwise specilied, timing here in show cross point at 50% of signal/power level.

8.6 Power Level Definition

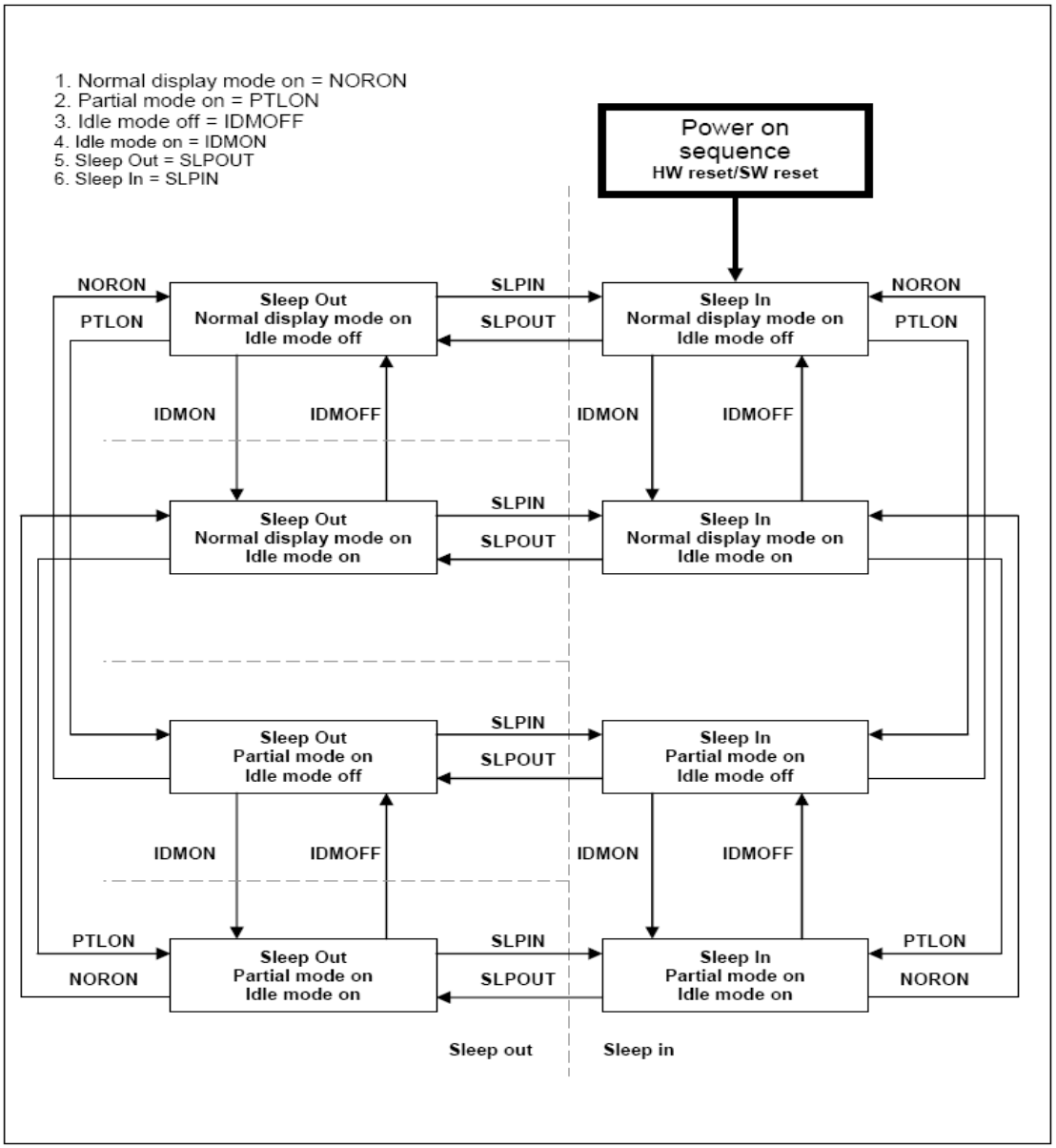
8.6.1 Power levels

6 level modes are defined they are in order of Maximum power consumption to Minimum power consumption.

1. Normal Mode On (full display), Idle Mode Off, Sleep Out
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
   In this mode, part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out
   In this mode, part of the display is used but with 8 colors
5. Sleep In Mode
   In this mode, the DC/DC converter, Internal oscillator and panel driver circuit are stopped. Only the interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and VDDI are removed

Note:
Transition between modes 1-5 is controllable by commands. Mode 6 is entered only when both Power supplies are removed.

8.6.2 Power flow chart

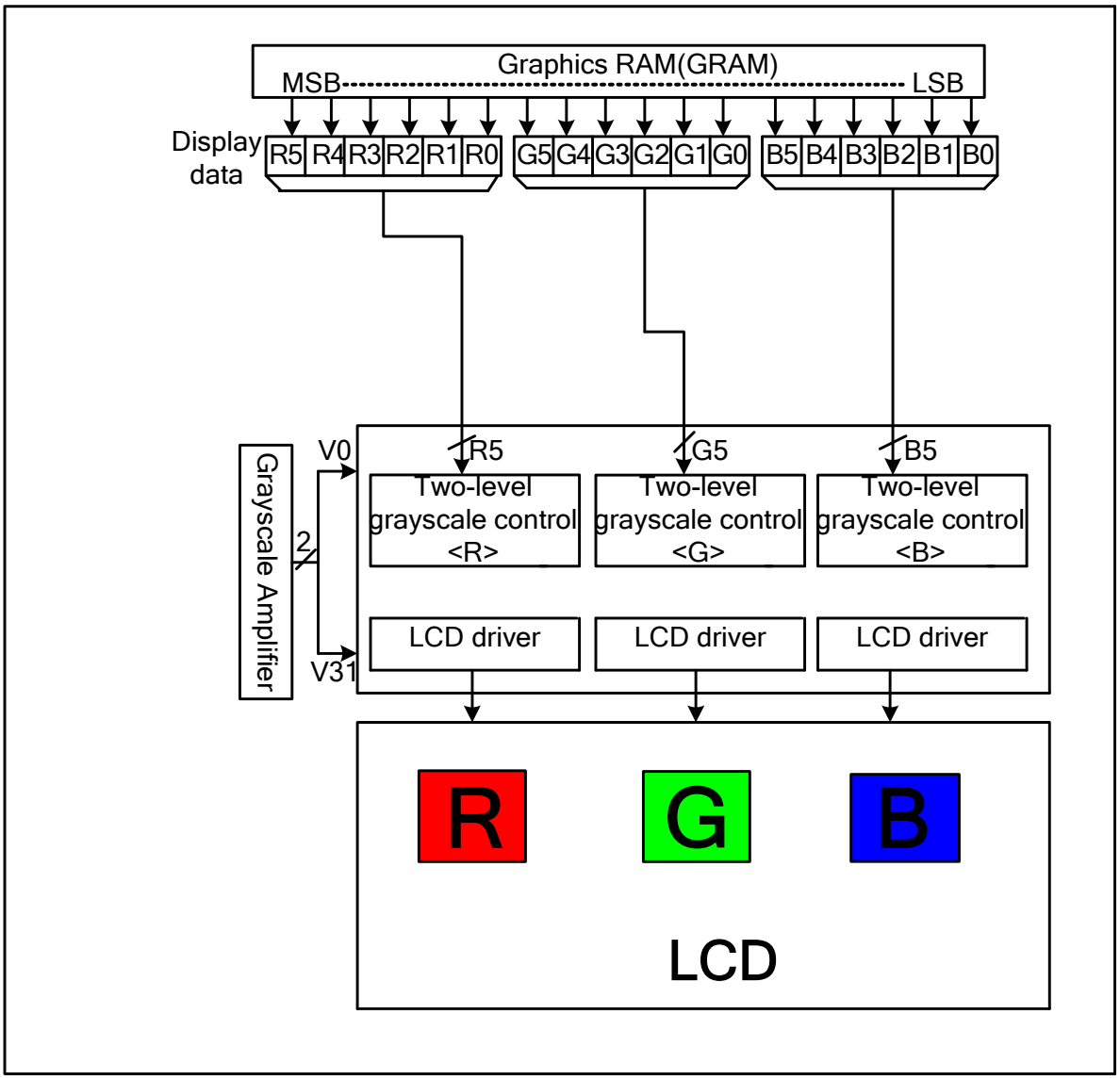


Notes:
1. There is not any abnormal visual effect when there is changing from one power mode to anther power mode.
2. There is not any limitation, which is not specified by Nokia, when there is changing from one power mode to another power mode.

8.7 8-color Display Mode

The NV3030A has a function to display in eight colors. In 8-color mode, the available grayscales are only V0 and V31, and the power supplies for other grayscales (V1 to V30) are cut off to reduce power consumption.

The γ-correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.
In 8-color display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.



8.8 Gamma Correction

The NV3030A incorporates gamma adjustment function for the 32,768-color display (32 grayscale for each R, G and B color). Gamma adjustment operation is implemented by deciding the 15 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available both for positive polarities and negative polarities.

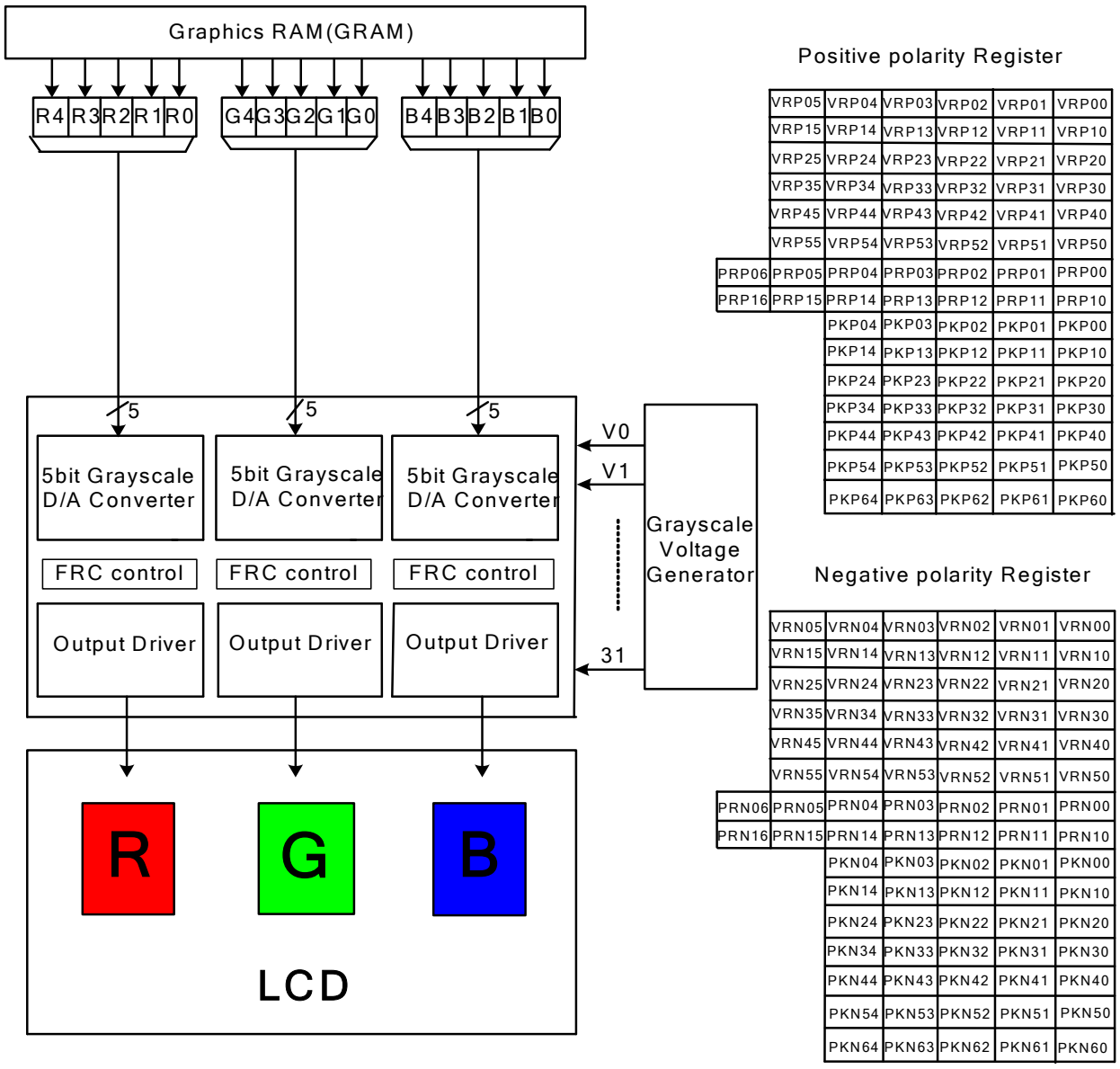


Figure 1: Grayscale control

8.8.1 Gamma-characteristics adjustment registers

This NV3030A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into three groups, which correspond to the gradient, amplitude, and Micro Adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

0- **Offset adjustment registers**

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

0- **Gamma center adjustment registers**

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 128-to-1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

0- **Gamma Micro Adjustment registers**

The gamma Micro Adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~6), each of which has 5 inputs and generates one reference voltage output (VgP/N (3,4,10,15,21,27,28)).

Gamma-adjustment registers			
Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor （PRP/N0）for center adjustment
	PRP1 6-0	PRN1 6-0	Variable resistor （PRP/N1）for center adjustment
Micro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 4)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 10)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 21)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 27)
	PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 28)
	PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 15)
Offset Adjustment	VRP0 5-0	VRN0 5-0	Variable resistor （VRP/N0）for offset adjustment
	VRP1 5-0	VRN1 5-0	Variable resistor （VRP/N1）for offset adjustment
	VRP2 5-0	VRN2 5-0	Variable resistor （VRP/N2）for offset adjustment
	VRP3 5-0	VRN3 5-0	Variable resistor （VRP/N3）for offset adjustment
	VRP4 5-0	VRN4 5-0	Variable resistor （VRP/N4）for offset adjustment
	VRP5 5-0	VRN5 5-0	Variable resistor （VRP/N5）for offset adjustment

8.8.2 Gamma resister stream

The block consists of one gamma resister stream. Use different register setting for positive or negative polarity. Each polarity includes fifteen gamma reference voltages. VgP/N (0, 1, 2, 3, 4, 5, 10, 15, 21, 26, 27, 28, 29, 30, 31).

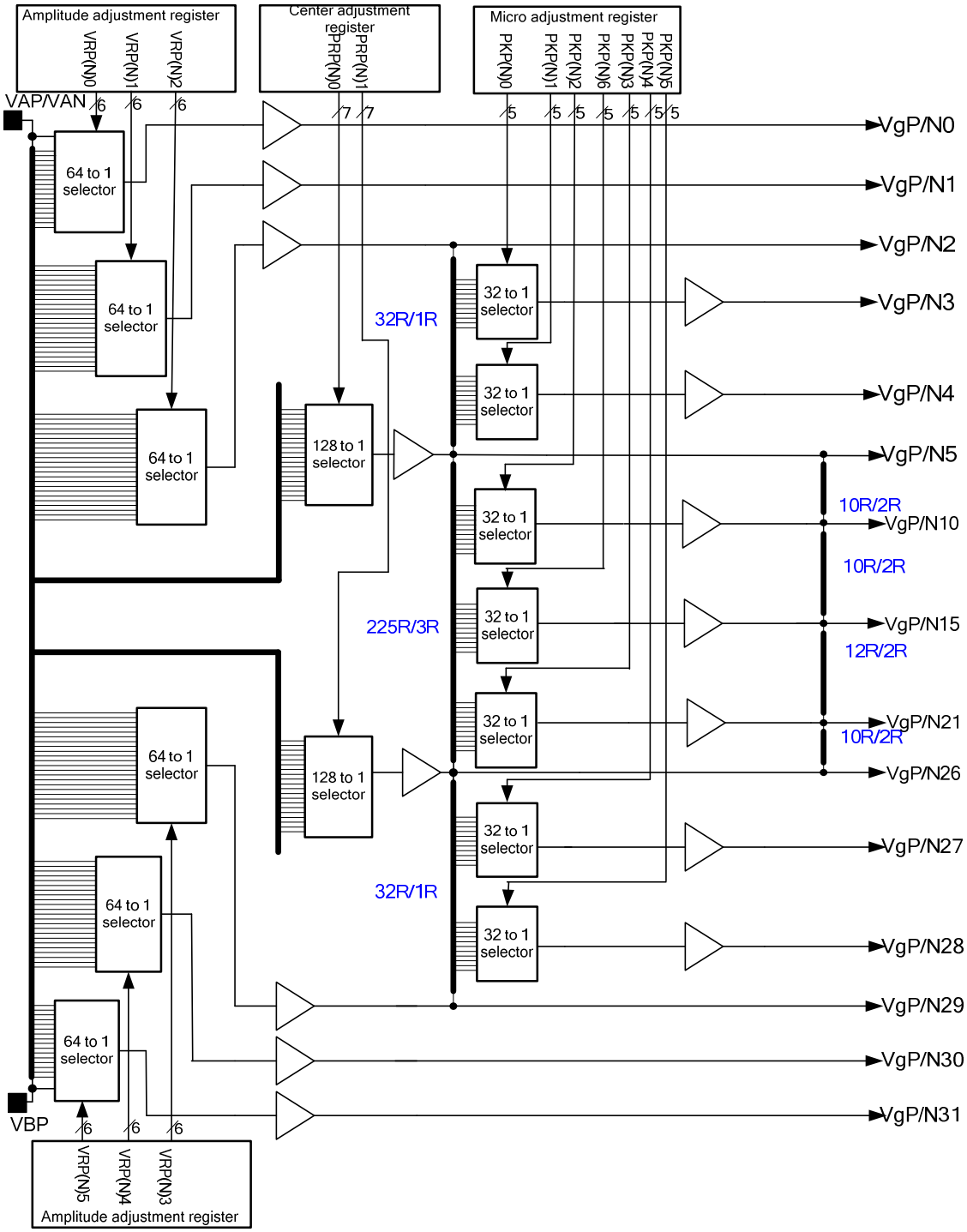


Figure 2 : Gamma resister stream and gamma reference voltage

8.8.3 Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below:

- Table 1: Offset adjustment 0 ~ 5

Register VR(P/N)0[5:0]	Resistance VR(P/N)0
000000	0R
000001	2R
000010	4R
000011	6R
…	…
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
100011	78R
…	…
111101	182R
111110	186R
111111	190R

Register VR(P/N)1[5:0]	Resistance VR(P/N)1
000000	0R
000001	2R
000010	4R
000011	6R
…	…
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
100011	78R
…	…
111101	182R
111110	186R
111111	190R

Register VR(P/N)2[5:0]	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
000011	6R
…	…
011101	58R
011110	60R
011111	62R
100000	66R
100001	70R
100010	74R
100011	78R
…	…
111101	182R
111110	186R
111111	190R

Register VR(P/N)3[5:0]	Resistance VR(P/N)3
000000	0R
000001	4R
000010	8R
…	…
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
…	…
111100	184R
111101	186R
111110	188R
111111	190R

Register VR(P/N)4[5:0]	Resistance VR(P/N)4
000000	0R
000001	4R
000010	8R
…	…
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
…	…
111100	184R
111101	186R
111110	188R
111111	190R

Register VR(P/N)5[5:0]	Resistance VR(P/N)5
000000	0R
000001	4R
000010	8R
…	…
011101	116R
011110	120R
011111	124R
100000	128R
100001	130R
100010	132R
…	…
111100	184R
111101	186R
111110	188R
111111	190R

- Table 2 : Center adjustment

Register PPR(P/N)0[6:0]	Resistance PR(P/N)0
000000	0R
000001	2R
000010	4R
…	…
111101	250R
111110	252R
111111	254R

Register PPR(P/N)1[6:0]	Resistance PR(P/N)1
000000	0R
000001	2R
000010	4R
…	…
111101	250R
111110	252R
111111	254R

8.8.4 The grayscale levels are determined by the following formulas.

Table 3 : VinP/N0

Reference Voltage	Micro Adjustment value	VinP/N0 formula
VinP/N0	VRP/N0 5-0 = 000000	VAP/VAN
	VRP/N0 5-0 = 000001	((450R -2R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000010	((450R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000011	((450R -6R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000100	((450R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000101	((450R -10R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000110	((450R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 000111	((450R -14R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001000	((450R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001001	((450R -18R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001010	((450R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001011	((450R -22R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001100	((450R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001101	((450R -26R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001110	((450R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 001111	((450R -30R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010000	((450R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010001	((450R -34R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010010	((450R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010011	((450R -38R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010100	((450R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010101	((450R -42R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010110	((450R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 010111	((450R -46R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011000	((450R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011001	((450R -50R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011010	((450R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011011	((450R -54R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011100	((450R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011101	((450R -58R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011110	((450R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 011111	((450R -62R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100000	((450R -66R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100001	((450R -70R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100010	((450R -74R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100011	((450R -78R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100100	((450R -82R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100101	((450R -86R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100110	((450R -90R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 100111	((450R -94R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101000	((450R -98R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101001	((450R -102R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101010	((450R -106R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101011	((450R -110R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101100	((450R -114R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101101	((450R -118R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101110	((450R -122R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 101111	((450R -126R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110000	((450R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110001	((450R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110010	((450R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110011	((450R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110100	((450R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110101	((450R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110110	((450R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 110111	((450R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111000	((450R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111001	((450R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111010	((450R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111011	((450R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111100	((450R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111101	((450R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111110	((450R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N0 5-0 = 111111	((450R -190R) / 450R) * (VAP/VAN–VBP) + VBP

Table 4 : VinP/N1

Reference Voltage	Micro Adjustment value	VinP/N1 formula
VinP/N1	VRP/N1 5-0 = 000000	VAP/VAN
	VRP/N1 5-0 = 000001	((450R -2R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000010	((450R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000011	((450R -6R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000100	((450R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000101	((450R -10R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000110	((450R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 000111	((450R -14R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001000	((450R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001001	((450R -18R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001010	((450R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001011	((450R -22R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001100	((450R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001101	((450R -26R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001110	((450R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 001111	((450R -30R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010000	((450R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010001	((450R -34R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010010	((450R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010011	((450R -38R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010100	((450R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010101	((450R -42R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010110	((450R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 010111	((450R -46R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011000	((450R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011001	((450R -50R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011010	((450R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011011	((450R -54R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011100	((450R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011101	((450R -58R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011110	((450R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 011111	((450R -62R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100000	((450R -66R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100001	((450R -70R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100010	((450R -74R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100011	((450R -78R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100100	((450R -82R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100101	((450R -86R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100110	((450R -90R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 100111	((450R -94R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101000	((450R -98R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101001	((450R -102R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101010	((450R -106R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101011	((450R -110R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101100	((450R -114R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101101	((450R -118R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101110	((450R -122R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 101111	((450R -126R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110000	((450R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110001	((450R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110010	((450R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110011	((450R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110100	((450R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110101	((450R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110110	((450R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 110111	((450R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111000	((450R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111001	((450R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111010	((450R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111011	((450R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111100	((450R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111101	((450R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111110	((450R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N1 5-0 = 111111	((450R -190R) / 450R) * (VAP/VAN–VBP) + VBP

Table 5: VinP/N2

Reference Voltage	Micro Adjustment value	VinP/N2 formula
VinP/N2	VRP/N2 5-0 = 000000	(410R / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000001	((410R -2R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000010	((410R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000011	((410R -6R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000100	((410R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000101	((410R -10R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000110	((410R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 000111	((410R -14R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001000	((410R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001001	((410R -18R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001010	((410R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001011	((410R -22R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001100	((410R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001101	((410R -26R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001110	((410R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 001111	((410R -30R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010000	((410R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010001	((410R -34R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010010	((410R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010011	((410R -38R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010100	((410R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010101	((410R -42R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010110	((410R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 010111	((410R -46R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011000	((410R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011001	((410R -50R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011010	((410R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011011	((410R -54R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011100	((410R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011101	((410R -58R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011110	((410R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 011111	((410R -62R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100000	((410R -66R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100001	((410R -70R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100010	((410R -74R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100011	((410R -78R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100100	((410R -82R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100101	((410R -86R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100110	((410R -90R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 100111	((410R -94R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101000	((410R -98R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101001	((410R -102R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101010	((410R -106R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101011	((410R -110R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101100	((410R -114R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101101	((410R -118R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101110	((410R -122R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 101111	((410R -126R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110000	((410R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110001	((410R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110010	((410R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110011	((410R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110100	((410R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110101	((410R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110110	((410R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 110111	((410R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111000	((410R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111001	((410R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111010	((410R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111011	((410R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111100	((410R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111101	((410R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111110	((410R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N2 5-0 = 111111	((410R -190R) / 450R) * (VAP/VAN–VBP) + VBP

Table 6 : VinP/N10

Reference Voltage	Micro Adjustment value	VinP/N10 formula
VinP/N10	VRP/N3 5-0 = 000000	(230R / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000001	((230R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000010	((230R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000011	((230R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000100	((230R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000101	((230R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000110	((230R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 000111	((230R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001000	((230R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001001	((230R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001010	((230R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001011	((230R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001100	((230R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001101	((230R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001110	((230R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 001111	((230R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010000	((230R -64R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010001	((230R -68R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010010	((230R -72R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010011	((230R -76R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010100	((230R -80R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010101	((230R -84R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010110	((230R -88R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 010111	((230R -92R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011000	((230R -96R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011001	((230R -100R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011010	((230R -104R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011011	((230R -108R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011100	((230R -112R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011101	((230R -116R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011110	((230R -120R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 011111	((230R -124R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100000	((230R -128R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100001	((230R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100010	((230R -132R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100011	((230R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100100	((230R -136R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100101	((230R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100110	((230R -140R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 100111	((230R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101000	((230R -144R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101001	((230R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101010	((230R -148R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101011	((230R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101100	((230R -152R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101101	((230R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101110	((230R -156R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 101111	((230R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110000	((230R -160R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110001	((230R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110010	((230R -164R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110011	((230R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110100	((230R -168R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110101	((230R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110110	((230R -172R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 110111	((230R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111000	((230R -176R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111001	((230R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111010	((230R -180R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111011	((230R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111100	((230R -184R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111101	((230R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111110	((230R -188R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N3 5-0 = 111111	((230R -190R) / 450R) * (VAP/VAN–VBP) + VBP

Table 7 : VinP/N11

Reference Voltage	Micro Adjustment value	VinP/N11 formula
VinP/N11	VRP/N4 5-0 = 000000	(190R / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000001	((190R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000010	((190R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000011	((190R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000100	((190R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000101	((190R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000110	((190R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 000111	((190R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001000	((190R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001001	((190R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001010	((190R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001011	((190R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001100	((190R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001101	((190R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001110	((190R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 001111	((190R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010000	((190R -64R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010001	((190R -68R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010010	((190R -72R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010011	((190R -76R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010100	((190R -80R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010101	((190R -84R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010110	((190R -88R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 010111	((190R -92R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011000	((190R -96R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011001	((190R -100R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011010	((190R -104R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011011	((190R -108R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011100	((190R -112R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011101	((190R -116R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011110	((190R -120R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 011111	((190R -124R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100000	((190R -128R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100001	((190R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100010	((190R -132R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100011	((190R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100100	((190R -136R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100101	((190R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100110	((190R -140R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 100111	((190R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101000	((190R -144R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101001	((190R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101010	((190R -148R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101011	((190R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101100	((190R -152R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101101	((190R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101110	((190R -156R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 101111	((190R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110000	((190R -160R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110001	((190R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110010	((190R -164R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110011	((190R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110100	((190R -168R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110101	((190R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110110	((190R -172R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 110111	((190R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111000	((190R -176R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111001	((190R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111010	((190R -180R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111011	((190R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111100	((190R -184R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111101	((190R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111110	((190R -188R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N4 5-0 = 111111	VBP

Table 8 : VinP/N12

Reference Voltage	Micro Adjustment value	VinP/N12 formula
VinP/N12	VRP/N5 5-0 = 000000	(190R / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000001	((190R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000010	((190R -8R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000011	((190R -12R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000100	((190R -16R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000101	((190R -20R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000110	((190R -24R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 000111	((190R -28R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001000	((190R -32R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001001	((190R -36R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001010	((190R -40R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001011	((190R -44R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001100	((190R -48R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001101	((190R -52R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001110	((190R -56R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 001111	((190R -60R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010000	((190R -64R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010001	((190R -68R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010010	((190R -72R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010011	((190R -76R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010100	((190R -80R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010101	((190R -84R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010110	((190R -88R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 010111	((190R -92R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011000	((190R -96R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011001	((190R -100R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011010	((190R -104R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011011	((190R -108R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011100	((190R -112R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011101	((190R -116R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011110	((190R -120R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 011111	((190R -124R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100000	((190R -128R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100001	((190R -130R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100010	((190R -132R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100011	((190R -134R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100100	((190R -136R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100101	((190R -138R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100110	((190R -140R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 100111	((190R -142R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101000	((190R -144R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101001	((190R -146R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101010	((190R -148R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101011	((190R -150R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101100	((190R -152R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101101	((190R -154R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101110	((190R -156R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 101111	((190R -158R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110000	((190R -160R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110001	((190R -162R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110010	((190R -164R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110011	((190R -166R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110100	((190R -168R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110101	((190R -170R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110110	((190R -172R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 110111	((190R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111000	((190R -176R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111001	((190R -178R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111010	((190R -180R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111011	((190R -182R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111100	((190R -184R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111101	((190R -186R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111110	((190R -188R) / 450R) * (VAP/VAN–VBP) + VBP
	VRP/N5 5-0 = 111111	VBP

Table 9 : VinP/N4

Reference Voltage	Micro Adjustment value	VinP/N4 formula
VinP/N4	PRP/N0 6-0 = 0000000	(350R / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000001	((350R – 2R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000010	((350R – 4R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000011	((350R – 6R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000100	((350R – 8R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000101	((350R – 10R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000110	((350R – 12R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0000111	((350R – 14R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001000	((350R – 16R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001001	((350R – 18R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001010	((350R – 20R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001011	((350R – 22R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001100	((350R – 24R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001101	((350R – 26R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001110	((350R – 28R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0001111	((350R – 30R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010000	((350R – 32R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010001	((350R – 34R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010010	((350R – 36R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010011	((350R – 38R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010100	((350R – 40R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010101	((350R – 42R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010110	((350R – 44R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0010111	((350R – 46R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011000	((350R – 48R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011001	((350R – 50R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011010	((350R – 52R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011011	((350R – 54R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011100	((350R – 56R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011101	((350R – 58R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011110	((350R – 60R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0011111	((350R – 62R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100000	((350R – 64R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100001	((350R – 66R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100010	((350R – 68R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100011	((350R – 70R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100100	((350R – 72R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100101	((350R – 74R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100110	((350R – 76R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0100111	((350R – 78R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101000	((350R – 80R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101001	((350R – 82R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101010	((350R – 84R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101011	((350R – 86R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101100	((350R – 88R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101101	((350R – 90R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101110	((350R – 92R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0101111	((350R – 94R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110000	((350R – 96R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110001	((350R – 98R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110010	((350R – 100R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110011	((350R – 102R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110100	((350R – 104R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110101	((350R – 106R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110110	((350R – 108R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0110111	((350R – 110R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111000	((350R – 112R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111001	((350R – 114R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111010	((350R – 116R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111011	((350R – 118R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111100	((350R – 120R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111101	((350R – 122R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111110	((350R – 124R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 0111111	((350R – 126R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000000	((350R – 128R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000001	((350R – 130R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000010	((350R – 132R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000011	((350R – 134R) / 450R) * (VAP/VAN–VBP) + VBP

Reference Voltage	Micro Adjustment value	VinP/N4 formula
	PRP/N0 6-0 = 1000100	((350R – 136R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000101	((350R – 138R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000110	((350R – 140R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1000111	((350R – 142R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001000	((350R – 144R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001001	((350R – 146R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001010	((350R – 148R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001011	((350R – 150R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001100	((350R – 152R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001101	((350R – 154R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001110	((350R – 156R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1001111	((350R – 158R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010000	((350R – 160R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010001	((350R – 162R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010010	((350R – 164R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010011	((350R – 166R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010100	((350R – 168R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010101	((350R – 170R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010110	((350R – 172R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1010111	((350R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011000	((350R – 176R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011001	((350R – 178R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011010	((350R – 180R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011011	((350R – 182R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011100	((350R – 184R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011101	((350R – 186R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011110	((350R – 188R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1011111	((350R – 190R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100000	((350R – 192R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100001	((350R – 194R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100010	((350R – 196R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100011	((350R – 198R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100100	((350R – 200R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100101	((350R – 202R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100110	((350R – 204R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1100111	((350R – 206R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101000	((350R – 208R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101001	((350R – 210R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101010	((350R – 212R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101011	((350R – 214R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101100	((350R – 216R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101101	((350R – 218R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101110	((350R – 220R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1101111	((350R – 222R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110000	((350R – 224R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110001	((350R – 226R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110010	((350R – 228R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110011	((350R – 230R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110100	((350R – 232R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110101	((350R – 234R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110110	((350R – 236R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1110111	((350R – 238R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111000	((350R – 240R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111001	((350R – 242R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111010	((350R – 244R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111011	((350R – 246R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111100	((350R – 248R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111101	((350R – 250R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111110	((350R – 252R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N0 6-0 = 1111111	((350R – 254R) / 450R) * (VAP/VAN–VBP) + VBP

Table 10 : VinP/N8

Reference Voltage	Micro Adjustment value	VinP/N8 formula
VinP/N8	PRP/N1 6-0 = 0000000	(354R / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000001	((354R -2R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000010	((354R -4R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000011	((354R – 6R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000100	((354R – 8R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000101	((354R – 10R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000110	((354R – 12R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0000111	((354R -14R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001000	((354R – 16R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001001	((354R – 18R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001010	((354R – 20R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001011	((354R – 22R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001100	((354R – 24R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001101	((354R – 26R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001110	((354R – 28R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0001111	((354R – 30R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010000	((354R – 32R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010001	((354R -34R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010010	((354R – 36R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010011	((354R – 38R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010100	((354R – 40R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010101	((354R – 42R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010110	((354R – 44R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0010111	((354R – 46R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011000	((354R – 48R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011001	((354R – 50R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011010	((354R – 52R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011011	((354R -54R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011100	((354R – 56R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011101	((354R – 58R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011110	((354R – 60R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0011111	((354R – 62R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100000	((354R -64R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100001	((354R – 66R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100010	((354R – 68R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100011	((354R – 70R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100100	((354R – 72R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100101	((354R – 74R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100110	((354R – 76R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0100111	((354R – 78R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101000	((354R – 80R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101001	((354R – 82R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101010	((354R -84R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101011	((354R – 86R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101100	((354R – 88R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101101	((354R – 90R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101110	((354R – 92R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0101111	((354R – 94R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110000	((354R – 96R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110001	((354R – 98R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110010	((354R – 100R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110011	((354R – 102R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110100	((354R – 104R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110101	((354R – 106R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110110	((354R – 108R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0110111	((354R – 110R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111000	((354R – 112R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111001	((354R – 114R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111010	((354R – 116R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111011	((354R – 118R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111100	((354R – 120R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111101	((354R – 122R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111110	((354R -124R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 0111111	((354R – 126R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000000	((354R – 128R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000001	((354R – 130R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000010	((354R -132R) / 450R) * (VAP/VAN–VBP) + VBP

Reference Voltage	Micro Adjustment value	VinP/N8 formula
VinP/N8	PRP/N1 6-0 = 1000011	((354R – 134R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000100	((354R – 136R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000101	((354R – 138R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000110	((354R – 140R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1000111	((354R – 142R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001000	((354R – 144R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001001	((354R – 146R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001010	((354R – 148R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001011	((354R – 150R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001100	((354R -152R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001101	((354R – 154R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001110	((354R – 156R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1001111	((354R – 158R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010000	((354R – 160R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010001	((354R – 162R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010010	((354R – 164R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010011	((354R – 166R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010100	((354R – 168R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010101	((354R – 170R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010110	((354R – 172R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1010111	((354R -174R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011000	((354R – 176R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011001	((354R – 178R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011010	((354R – 180R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011011	((354R – 182R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011100	((354R – 184R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011101	((354R – 186R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011110	((354R – 188R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1011111	((354R – 190R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100000	((354R – 192R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100001	((354R – 194R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100010	((354R – 196R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100011	((354R – 198R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100100	((354R – 200R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100101	((354R – 202R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100110	((354R – 204R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1100111	((354R – 206R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101000	((354R – 208R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101001	((354R – 210R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101010	((354R – 212R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101011	((354R – 214R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101100	((354R – 216R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101101	((354R – 218R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101110	((354R – 220R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1101111	((354R – 222R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110000	((354R – 224R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110001	((354R – 226R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110010	((354R – 228R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110011	((354R – 230R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110100	((354R – 232R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110101	((354R – 234R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110110	((354R – 236R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1110111	((354R – 238R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111000	((354R – 240R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111001	((354R – 242R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111010	((354R – 244R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111011	((354R – 246R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111100	((354R – 248R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111101	((354R – 250R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111110	((354R – 252R) / 450R) * (VAP/VAN–VBP) + VBP
	PRP/N1 6-0 = 1111111	((354R – 254R) / 450R) * (VAP/VAN–VBP) + VBP

Table 11: VinP/N3

Reference Voltage	Micro Adjustment value	VinP/N3 formula
VinP/N3	PKP/N0 4-0 = 00000	(31R / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00001	((31R – 1R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00010	((31R – 2R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00011	((31R – 3R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00100	((31R – 4R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00101	((31R – 5R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00110	((31R – 6R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 00111	((31R – 7R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01000	((31R – 8R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01001	((31R – 9R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01010	((31R -10R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01011	((31R -11R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01100	((31R -12R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01101	((31R -13R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01110	((31R -14R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 01111	((31R -15R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10000	((31R -16R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10001	((31R -17R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10010	((31R -18R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10011	((31R -19R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10100	((31R -20R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10101	((31R -21R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10110	((31R -22R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 10111	((31R -23R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11000	((31R -24R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11001	((31R -25R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11010	((31R -26R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11011	((31R -27R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11100	((31R -28R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11101	((31R -29R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11110	((31R -30R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N0 4-0 = 11111	((31R -31R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4

Table 12: VinP/N3_2

Reference Voltage	Micro Adjustment value	VinP/N3_2 formula
VinP/N3_2	PKP/N1 4-0 = 00000	(31R / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00001	((31R – 1R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00010	((31R – 2R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00011	((31R – 3R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00100	((31R – 4R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00101	((31R – 5R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00110	((31R – 6R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 00111	((31R – 7R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01000	((31R – 8R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01001	((31R – 9R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01010	((31R -10R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01011	((31R -11R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01100	((31R -12R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01101	((31R -13R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01110	((31R -14R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 01111	((31R -15R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10000	((31R -16R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10001	((31R -17R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10010	((31R -18R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10011	((31R -19R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10100	((31R -20R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10101	((31R -21R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10110	((31R -22R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 10111	((31R -23R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11000	((31R -24R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11001	((31R -25R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11010	((31R -26R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11011	((31R -27R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11100	((31R -28R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11101	((31R -29R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11110	((31R -30R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4
	PKP/N1 4-0 = 11111	((31R -31R) / 32R) * (VinP/N2 –VinP/N4) + VinP/N4

Table 13: VinP/N5

Reference Voltage	Micro Adjustment value	VinP/N5 formula
VinP/N5	PKP/N2 4-0 = 00000	(195R / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00001	((195R -3R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00010	((195R -6R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00011	((195R -9R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00100	((195R -12R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00101	((195R -15R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00110	((195R -18R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 00111	((195R -21R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01000	((195R -24R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01001	((195R -27R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01010	((195R -30R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01011	((195R -33R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01100	((195R -36R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01101	((195R -39R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01110	((195R -42R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 01111	((195R -45R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10000	((195R -48R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10001	((195R -51R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10010	((195R -54R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10011	((195R -57R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10100	((195R -60R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10101	((195R -63R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10110	((195R -66R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 10111	((195R -69R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11000	((195R -72R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11001	((195R -75R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11010	((195R -78R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11011	((195R -81R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11100	((195R -84R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11101	((195R -87R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11110	((195R -90R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N2 4-0 = 11111	((195R -93R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8

Table 13a: VinP/N6

Reference Voltage	Micro Adjustment value	VinP/N6 formula
VinP/N6	PKP/N6 4-0 = 00000	(159R / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00001	((159R -3R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00010	((159R -6R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00011	((159R -9R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00100	((159R -12R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00101	((159R -15R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00110	((159R -18R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 00111	((159R -21R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01000	((159R -24R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01001	((159R -27R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01010	((159R -30R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01011	((159R -33R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01100	((159R -36R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01101	((159R -39R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01110	((159R -42R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 01111	((159R -45R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10000	((159R -48R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10001	((159R -51R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10010	((159R -54R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10011	((159R -57R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10100	((159R -60R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10101	((159R -63R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10110	((159R -66R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 10111	((159R -69R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11000	((159R -72R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11001	((159R -75R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11010	((159R -78R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11011	((159R -81R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11100	((159R -84R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11101	((159R -87R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11110	((159R -90R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N6 4-0 = 11111	((159R -93R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8

Table 14: VinP/N7

Reference Voltage	Micro Adjustment value	VinP/N7 formula
VinP/N7	PKP/N3 4-0 = 00000	(123R / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00001	((123R -3R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00010	((123R -6R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00011	((123R -9R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00100	((123R -12R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00101	((123R -15R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00110	((123R -18R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 00111	((123R -21R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01000	((123R -24R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01001	((123R -27R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01010	((123R -30R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01011	((123R -33R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01100	((123R -36R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01101	((123R -39R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01110	((123R -42R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 01111	((123R -45R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10000	((123R -48R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10001	((123R -51R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10010	((123R -54R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10011	((123R -57R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10100	((123R -60R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10101	((123R -63R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10110	((123R -66R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 10111	((123R -69R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11000	((123R -72R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11001	((123R -75R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11010	((123R -78R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11011	((123R -81R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11100	((123R -84R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11101	((123R -87R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11110	((123R -90R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8
	PKP/N3 4-0 = 11111	((123R -93R) / 225R) * (VinP/N4 –VinP/N8) + VinP/N8

Table 15: VinP/N9_2

Reference Voltage	Micro Adjustment value	VinP/N9_2 formula
VinP/N9_2	PKP/N4 4-0 = 00000	(31R / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00001	((31R -1R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00010	((31R -2R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00011	((31R -3R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00100	((31R -4R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00101	((31R -5R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00110	((31R -6R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 00111	((31R -7R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01000	((31R -8R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01001	((31R -9R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01010	((31R -10R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01011	((31R -11R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01100	((31R -12R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01101	((31R -13R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01110	((31R -14R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 01111	((31R -15R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10000	((31R -16R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10001	((31R -17R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10010	((31R -18R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10011	((31R -19R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10100	((31R -20R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10101	((31R -21R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10110	((31R -22R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 10111	((31R -23R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11000	((31R -24R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11001	((31R -25R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11010	((31R -26R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11011	((31R -27R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11100	((31R -28R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11101	((31R -29R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11110	((31R -30R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N4 4-0 = 11111	((31R -31R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10

Table 16: VinP/N9

Reference Voltage	Micro Adjustment value	VinP/N9 formula
VinP/N9	PKP/N5 4-0 = 00000	(31R / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00001	((31R -1R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00010	((31R -2R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00011	((31R -3R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00100	((31R -4R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00101	((31R -5R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00110	((31R -6R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 00111	((31R -7R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01000	((31R -8R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01001	((31R -9R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01010	((31R -10R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01011	((31R -11R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01100	((31R -12R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01101	((31R -13R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01110	((31R -14R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 01111	((31R -15R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10000	((31R -16R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10001	((31R -17R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10010	((31R -18R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10011	((31R -19R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10100	((31R -20R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10101	((31R -21R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10110	((31R -22R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 10111	((31R -23R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11000	((31R -24R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11001	((31R -25R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11010	((31R -26R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11011	((31R -27R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11100	((31R -28R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11101	((31R -29R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11110	((31R -30R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10
	PKP/N5 4-0 = 11111	((31R -31R) / 32R) * (VinP/N8 –VinP/N10) + VinP/N10

Table 17:Positive polarity

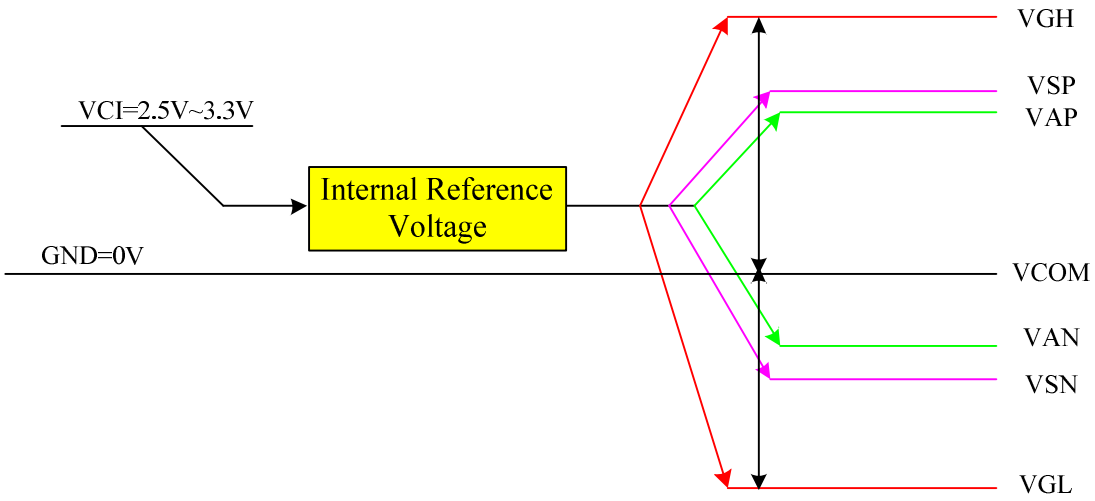
Grayscale voltage	Formula
v0	VinP0
v1	VinP1
v2	VinP2
v3	VinP3
v4	VinP3_2
v5	VinP4
v6	VinP5+(VinP4-VinP5)*(8R/10R)
v7	VinP5+(VinP4-VinP5)*(6R/10R)
v8	VinP5+(VinP4-VinP5)*(4R/10R)
v9	VinP5+(VinP4-VinP5)*(2R/10R)
v10	VinP5
v11	VinP6+(VinP5-VinP6)*(8R/10R)
v12	VinP6+(VinP5-VinP6)*(6R/10R)
v13	VinP6+(VinP5-VinP6)*(4R/10R)
v14	VinP6+(VinP5-VinP6)*(2R/10R)
v15	VinP6
v16	VinP7+(VinP6-VinP7)*(10R/12R)
v17	VinP7+(VinP6-VinP7)*(8R/12R)
v18	VinP7+(VinP6-VinP7)*(6R/12R)
v19	VinP7+(VinP6-VinP7)*(4R/12R)
v20	VinP7+(VinP6-VinP7)*(2R/12R)
v21	VinP7
v22	VinP8+(VinP7-VinP8)*(8R/10R)
v23	VinP8+(VinP7-VinP8)*(6R/10R)
v24	VinP8+(VinP7-VinP8)*(4R/10R)
v25	VinP8+(VinP7-VinP8)*(2R/10R)
v26	VinP8
v27	VinP9_2
v28	VinP9
v29	VinP10
v30	VinP11
v31	VinP12

Table 18: Negative polarity

Grayscale voltage	Formula
v31	VinN0
v30	VinN1
v29	VinN2
v28	VinN3
v27	VinN3_2
v26	VinN4
v25	VinN5+(VinN4-VinN5)*(8R/10R)
v24	VinN5+(VinN4-VinN5)*(6R/10R)
v23	VinN5+(VinN4-VinN5)*(4R/10R)
v22	VinN5+(VinN4-VinN5)*(2R/10R)
v21	VinN5
v20	VinN6+(VinN5-VinN6)*(8R/10R)
v19	VinN6+(VinN5-VinN6)*(6R/10R)
v18	VinN6+(VinN5-VinN6)*(4R/10R)
v17	VinN6+(VinN5-VinN6)*(2R/10R)
v16	VinN6
v15	VinN7+(VinN6-VinN7)*(10R/12R)
v14	VinN7+(VinN6-VinN7)*(8R/12R)
v13	VinN7+(VinN6-VinN7)*(6R/12R)
v12	VinN7+(VinN6-VinN7)*(4R/12R)
v11	VinN7+(VinN6-VinN7)*(2R/12R)
v10	VinN7
v9	VinN8+(VinN7-VinN8)*(8R/10R)
v8	VinN8+(VinN7-VinN8)*(6R/10R)
v7	VinN8+(VinN7-VinN8)*(4R/10R)
v6	VinN8+(VinN7-VinN8)*(2R/10R)
v5	VinN8
v4	VinN9_2
v3	VinN9
v2	VinN10
v1	VinN11
v0	VinN12

8.9 Voltage Generation

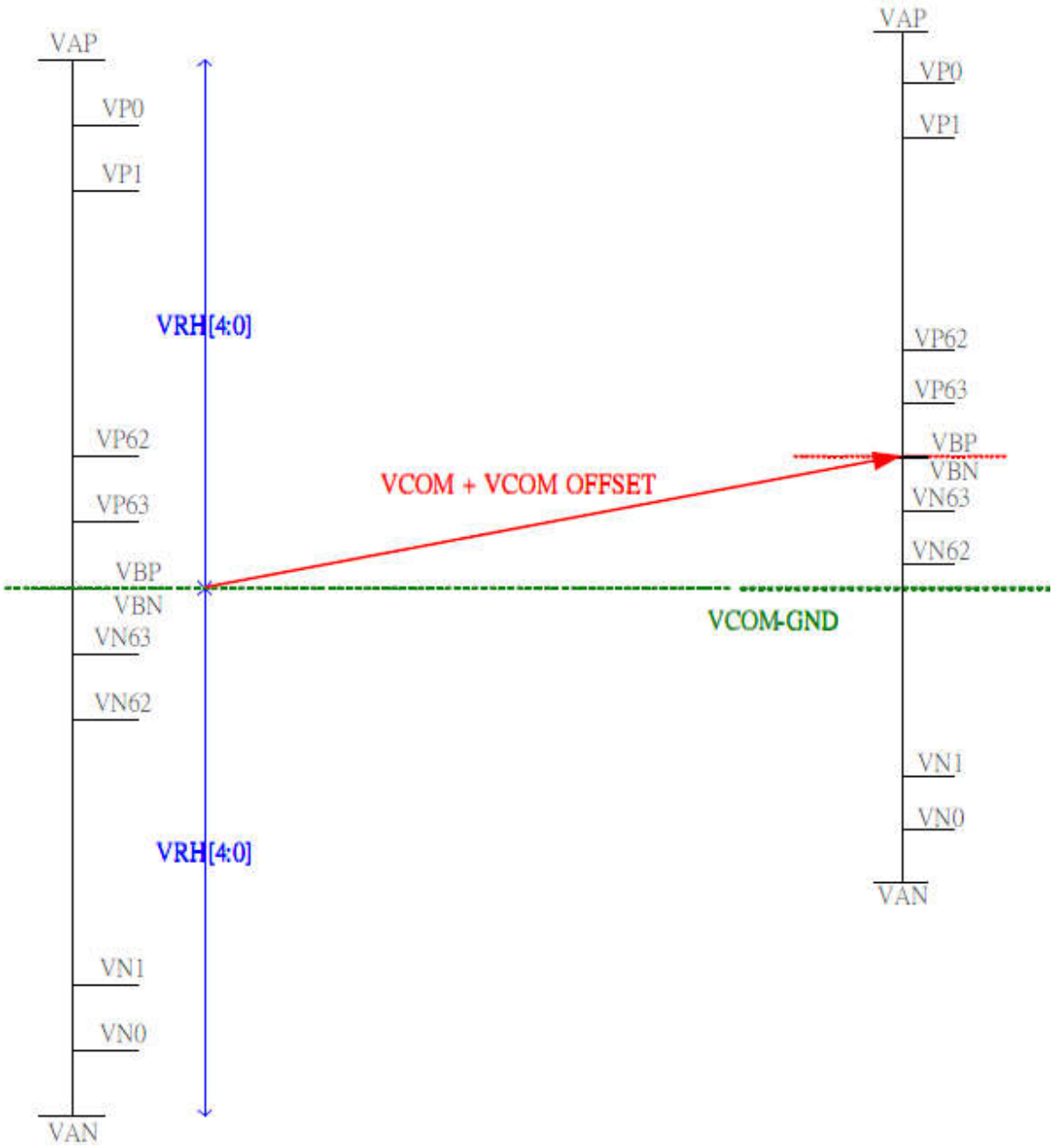
The following is the NV3030A analog voltage pattern diagram:



Power Booster Level

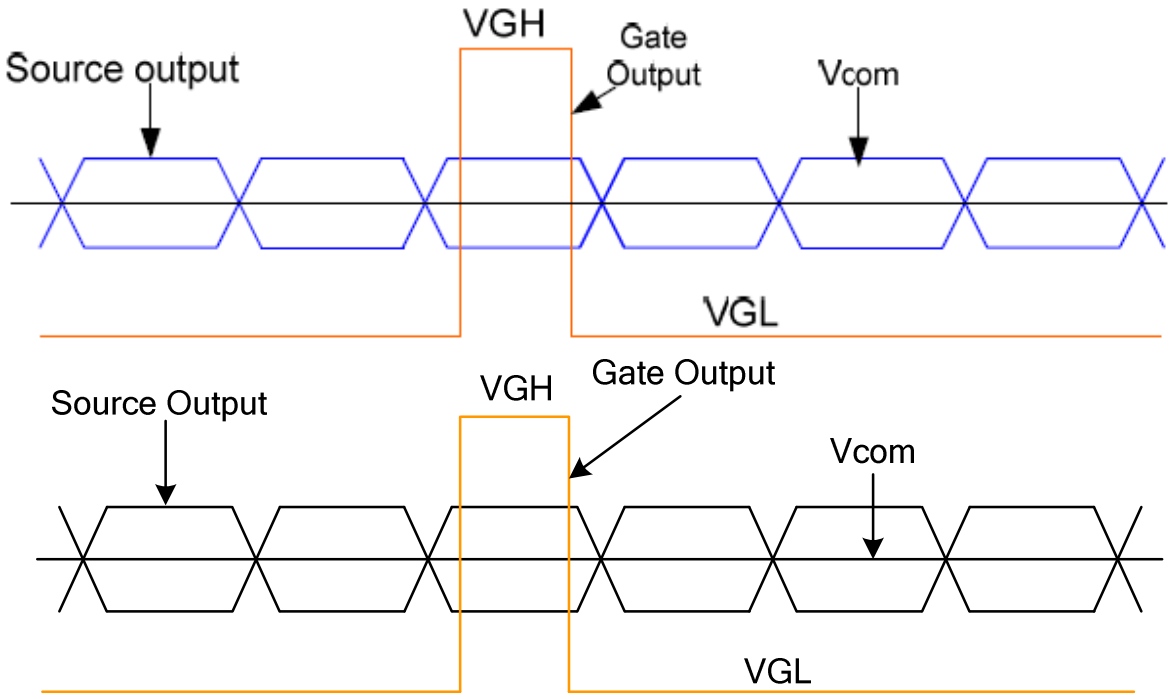
8.10 Relationship about source voltage

The relationship about source voltage is shown as below:



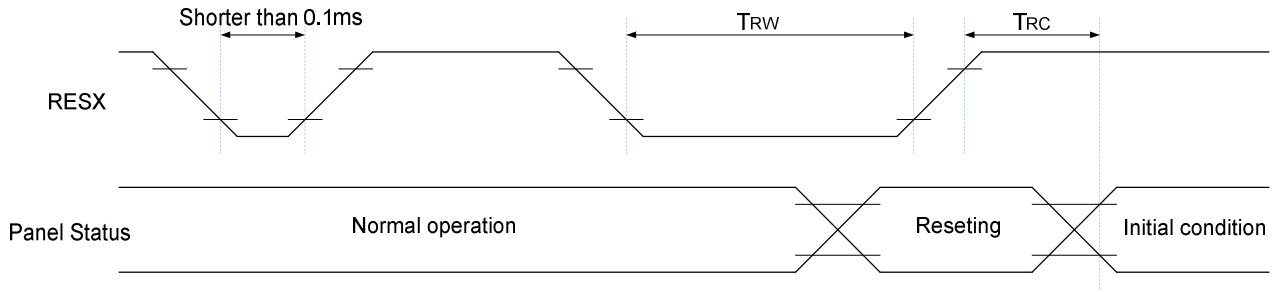
Relationship about source voltage

8.11 Applied Voltage to the TFT panel



Voltage Output to TFT LCD Panel

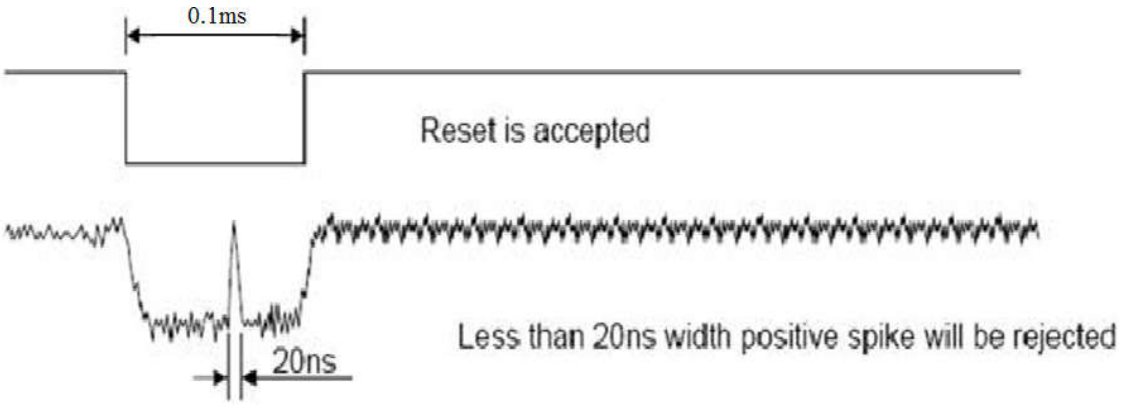
8.12 Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	T_{RW}	RESX low pulse duration	0.1		ms
	T_{RC}	Reset cancel			ms

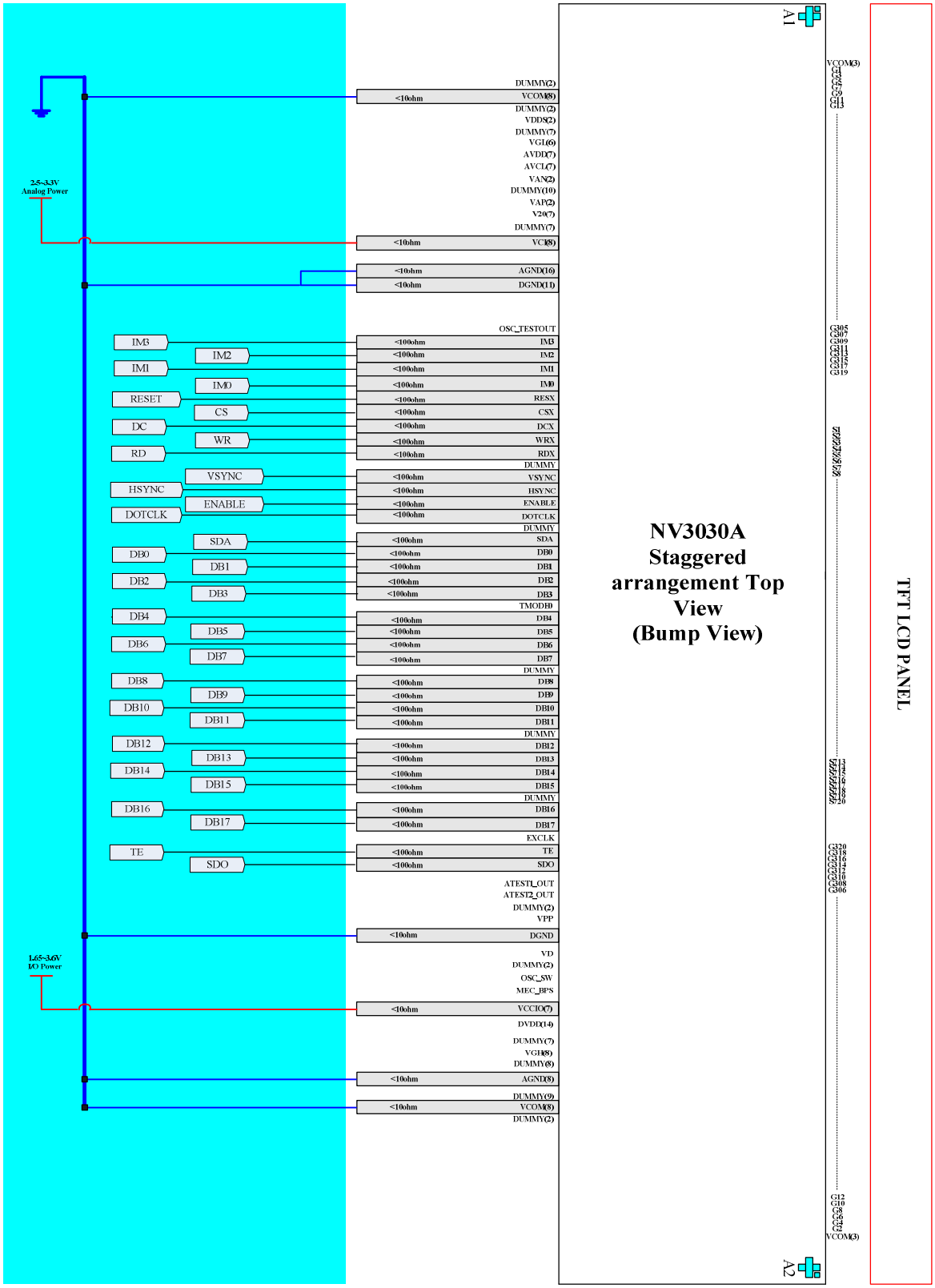
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time(RT) within 5ms after a rising edge of RESX.
2. Spice due to and electrostatic discharge on RESX line does not cause irregular system reset.
   When short than 0.1ms, reset rejected.
3. During the Resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in sleep in-mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

9. Application



10.

Electrical Characteristics

10.1 Absolute Maximum Ratings

Item	Symbol	Unit	Ratings	Notes
Power-supply voltage(1)	VCI,VDDI	V	-0.3 to +3.6	1,2
Power-supply voltage(2)	VCI-VSSA	V	-0.3 to +3.6	1,3
Power-supply voltage(3)	VSP-VSSA	V	-0.3 to +6.0	1,4
Power-supply voltage(4)	VGH-VGL	V	-0.3 to +30.0	1,4
Power-supply voltage(5)	VSSA-VGL	V	+3.0 to +13.0	1,7
Power-supply voltage(6)	VSP-VGL	V	+4.0 to +19.0	1,5
Power-supply voltage(7)	VCI-VGL	V	+3.0 to + 16.8	1,7
Input voltage	Vt	V	-0.3 to 3.9	1
Operating temperature	Topr	℃	-40 to +85	1
Storage temperature	Tstg	℃	-55 to +110	1

10.2 DC Characteristic

VCI = 2.5 ~ 3.3V, VDDI = 1.65~3.6V, Ta = -40 ~ 85 °C

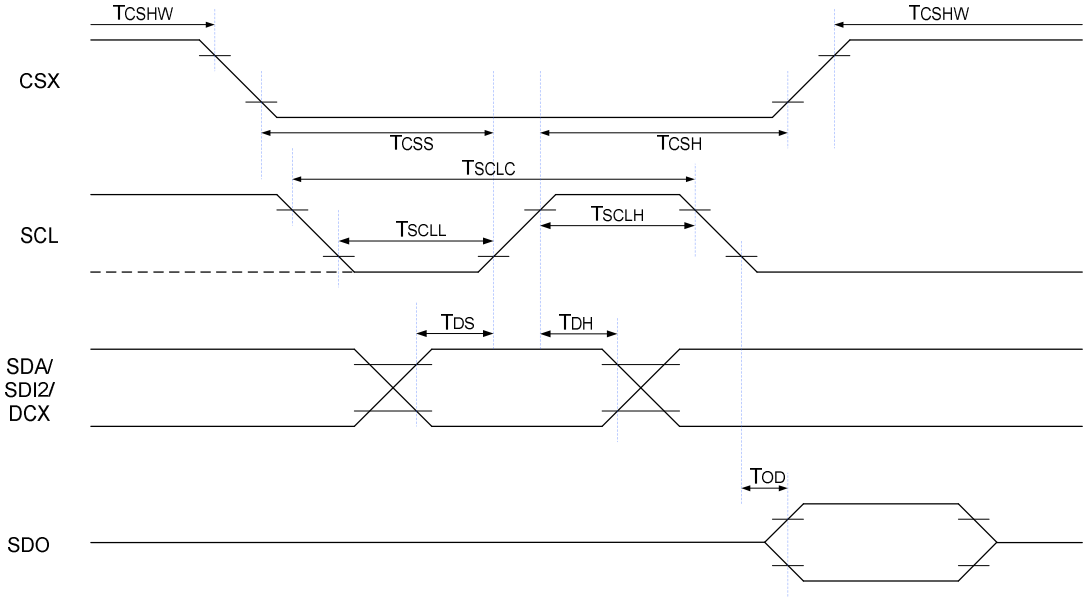
Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	VDDI = 1.65V ~ 3.6 V	0.8* VDDI	-	VDDI	2,3
Input low voltage	V_{IL}	V	VDDI = 1.65V ~ 3.6 V	– 0.3V	-	0.2* VDDI	2,3
Output high voltage (D0-17 pins, FMARK)	V_{OH}	V	IOH = -0.1mA	0.8 * VDDI	-	-	2
Output low voltage (D0-17 pins, FMARK)	V_{OL}	V	VDDI = 1.65 ~ 3.6 V I_{OL} = 0.1mA	-	-	0.2* VDDI	2
I/O leak current	Ili	µA	Vin = 0 ~ VDDI	-1	-	1	4
Current consumption during normal operation (VCI-VSSA)+(VDDI-GND)	IOP(VCI)	mA	VDDI=VCI=2.8V, Ta=25C, Fosc=45MHZ(320 Line)GRAM data =0000h, Frame rate=70HZ, REV=0, SAP=100,AP=100,DC0 =000,DC1=010,B/C=0, VC=001,VRH=0011, VCM=10011,VDV=100 00,VCOMG=1,CL=0, NO panel load	-	TBD	-	
Current consumption during standby operation (VCI-VSSA)+(VDDI-GND)	IOP(VCI)	µA		-	45		5,6

Notes:

1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI within the electrical characteristics conditions in normal operation. Exposure to a condition not within the electrical characteristics may affect reliability of the device.
2. Make sure VCI (high) ≥ GND (low) and VDDI (high) ≥ GND (low).
3. Make sure VCI (high) ≥ VSSA (low).
4. Make sure VSP (high) ≥ VSSA (low).
5. Make sure VSP (high) ≥ VGL (low).
6. Make sure VGH (high) ≥ VSSA (low).
7. Make sure VSSA (high) ≥ VGL (low).
8. The DC/AC characteristics of die and wafer products are guaranteed at 85 ºC.

10.3 AC Characteristics

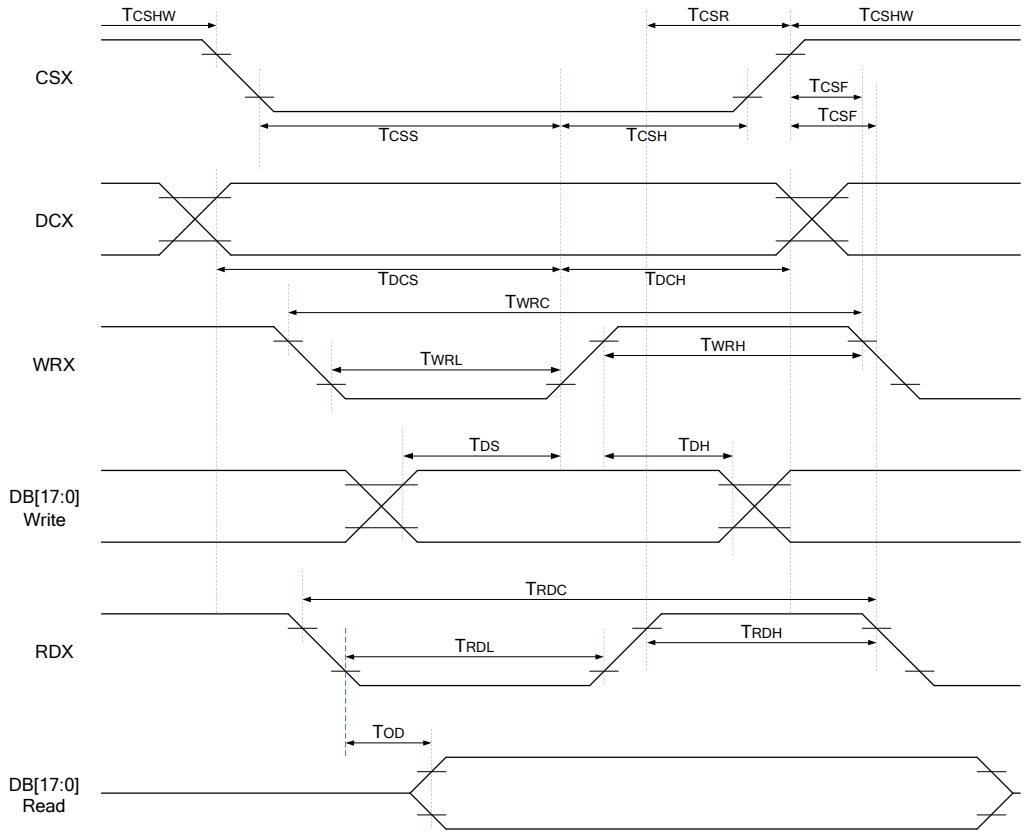
10.3.1 Serial Interface Timing Characteristics (3/4-wire SPI system)



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	CSX setup time	7.7	-	ns	Write
	T_{CSH}	CSX hold time	7.7	-	ns	
	T_{CSHW}	CSX high level width	15.4	-	ns	
	T_{CSS}	CSX setup time	40	-	ns	Read
	T_{CSH}	CSX hold time	40	-	ns	
	T_{CSHW}	CSX high level width	80	-	ns	
SCL	T_{SCLC}	SCL cycle	15.4	-	ns	Write
	T_{SCLS}	SCL low pulse duration	6.16	-	ns	
	T_{SCLH}	SCL high pulse duration	6.16	-	ns	
	T_{SCLC}	SCL cycle	80	-	ns	Read
	T_{SCLS}	SCL low pulse duration	32	-	ns	
	T_{SCLH}	SCL high pulse duration	32	-	ns	
SDA/ SDI2/ DCX	T_{DS}	SDA/SDI2/DCX setup time	6.16	-	ns	Write
	T_{DH}	SDA/SDI2/DCX hold time	6.16	-	ns	
SDO	T_{OD}	Read data output dealy	-	24	ns	Read

Note: Ta=-30℃~70℃, VDDI=1.65V to 3.6V, VCI=2.5V to 3.3V, VSSA=VSSD=0V.

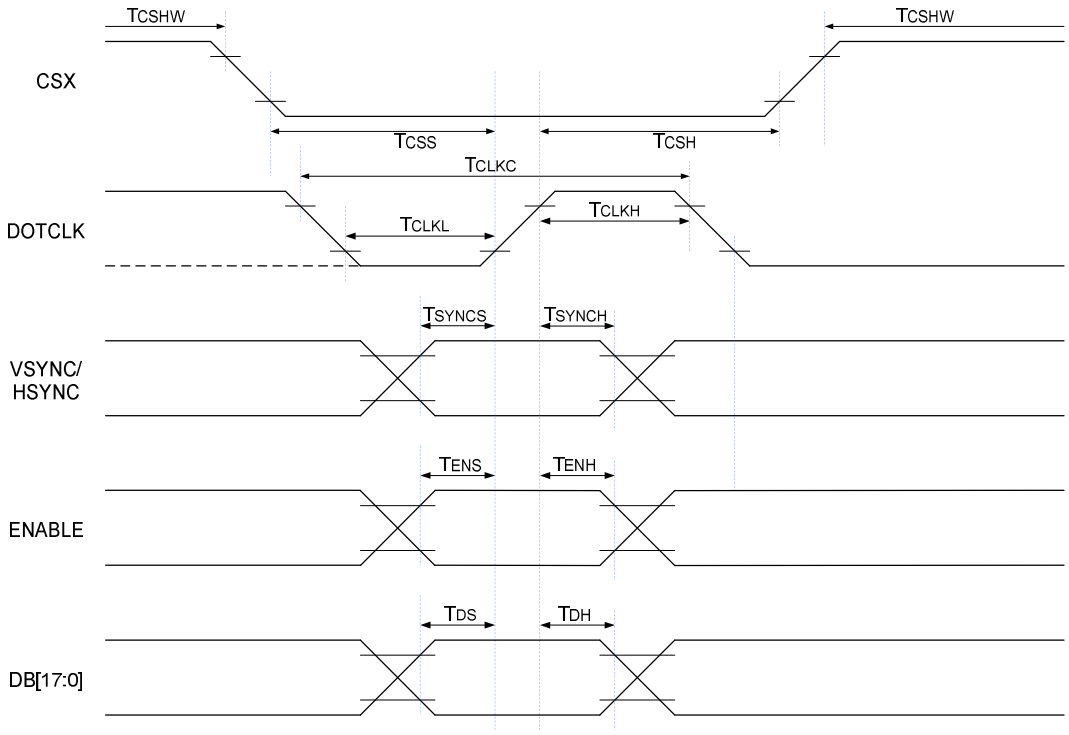
10.3.2 Parallel Interface Timing Characteristics(8080 series 8/9/16/18-Bit Parallel Interface)



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	CSX setup time	15	-	ns	
	T_{CSH}	CSX hold time	15	-	ns	
	T_{CSF}	CSX falling edge before WRX/RDX falling edge	10	-	ns	
	T_{CSHW}	CSX high level width	0	-	ns	
	T_{CSR}	CSX rising edge after RDX rising edge	0	-	ns	
DCX	T_{DCS}	DCX setup time	10	-	ns	
	T_{DCH}	DCX hold time	10	-	ns	
WRX	T_{WRC}	WRX cycle	30	-	ns	
	T_{WRL}	WRX low pulse duration	10	-	ns	
	T_{WRH}	WRX high pulse duration	10	-	ns	
DB[17:0]	T_{DS}	Write data setup time	10	-	ns	Write
	T_{DH}	Write data hold time	10	-	ns	
RDX	T_{RDC}	RDX cycle	160	-	ns	
	T_{RDL}	RDX low pulse duration	48	-	ns	
	T_{RDH}	RDX high pulse duration	48	-	ns	
DB[17:0]	T_{OD}	Read data output delay	-	30	ns	Read

Note: Ta=-30℃~70℃, VDDI=1.65V to 3.6V, VCI=2.5V to 3.3V, VSSA=VSSD=0V.

10.3.3 RGB Interface Timing Characteristics



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	CSX setup time	16	-	ns	
	T_{CSH}	CSX hold time	16	-	ns	
	T_{CSHW}	CSX high level width	0	-	ns	
DOTCLK	T_{CLKC}	DOTCLK cycle	40	-	ns	
	T_{CLKL}	DOTCLK low pulse duration	16	-	ns	
	T_{CLKH}	DOTCLK high pulse duration	16	-	ns	
HSYNC/ VSYNC	T_{SYNCS}	HSYNC/VSYNC setup time	16	-	ns	
	T_{SYNCH}	HSYNC/VSYNC hold time	16	-	ns	
ENABLE	T_{ENS}	ENABLE setup time	16	-	ns	
	T_{ENH}	ENABLE hold time	16	-	ns	
DB[17:0]	T_{DS}	RGB data setup time	16	-	ns	
	T_{DH}	RGB data hold time	16	-	ns	

Note: Ta=-30℃~70℃, VDDI=1.65V to 3.6V, VCI=2.5V to 3.3V, VSSA=VSSD=0V.

Revision history

Version No.	Date	Page	Introduction
0.1	2018-3-19	All	New build.
0.2	2020-8-11	6,7,10	QSPI
0.3	2021-1-8	All	Update register address