Lecture 5

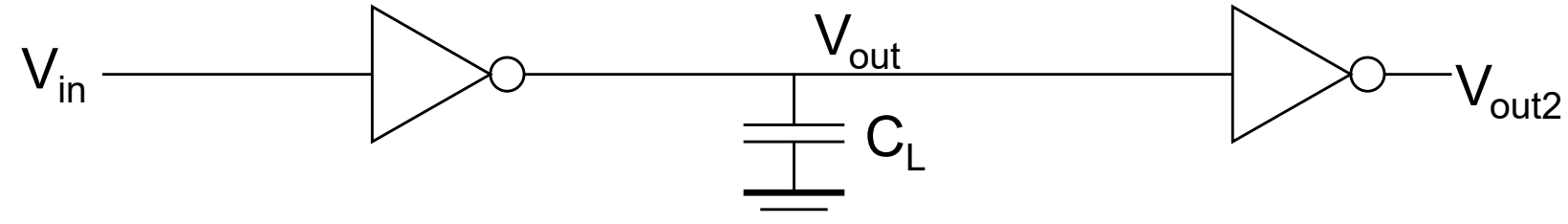
Hazards

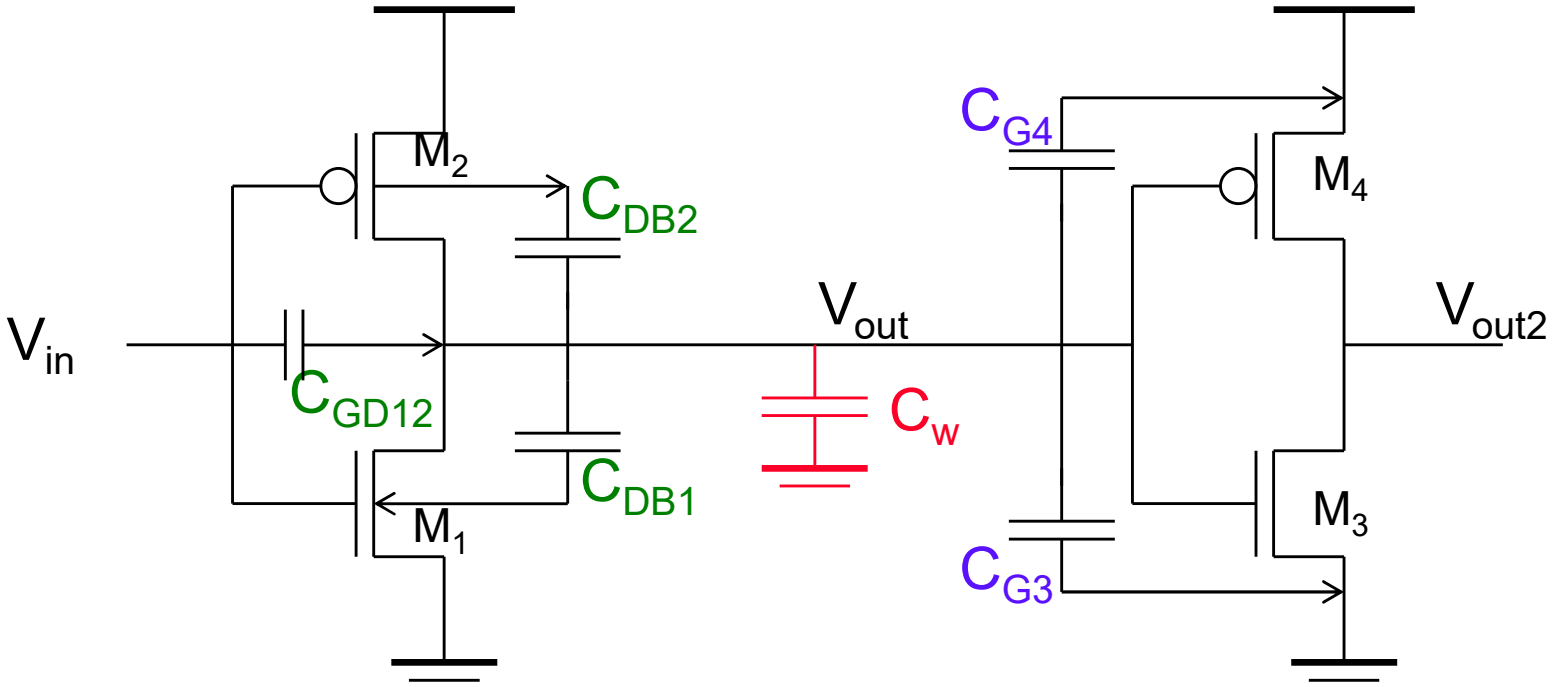
Learning outcomes

- Describe how the timing of a circuit can produce erroneous glitches.
- Define static and dynamic hazards.
- Identify and eliminate static hazards using a k-map.

Introduction

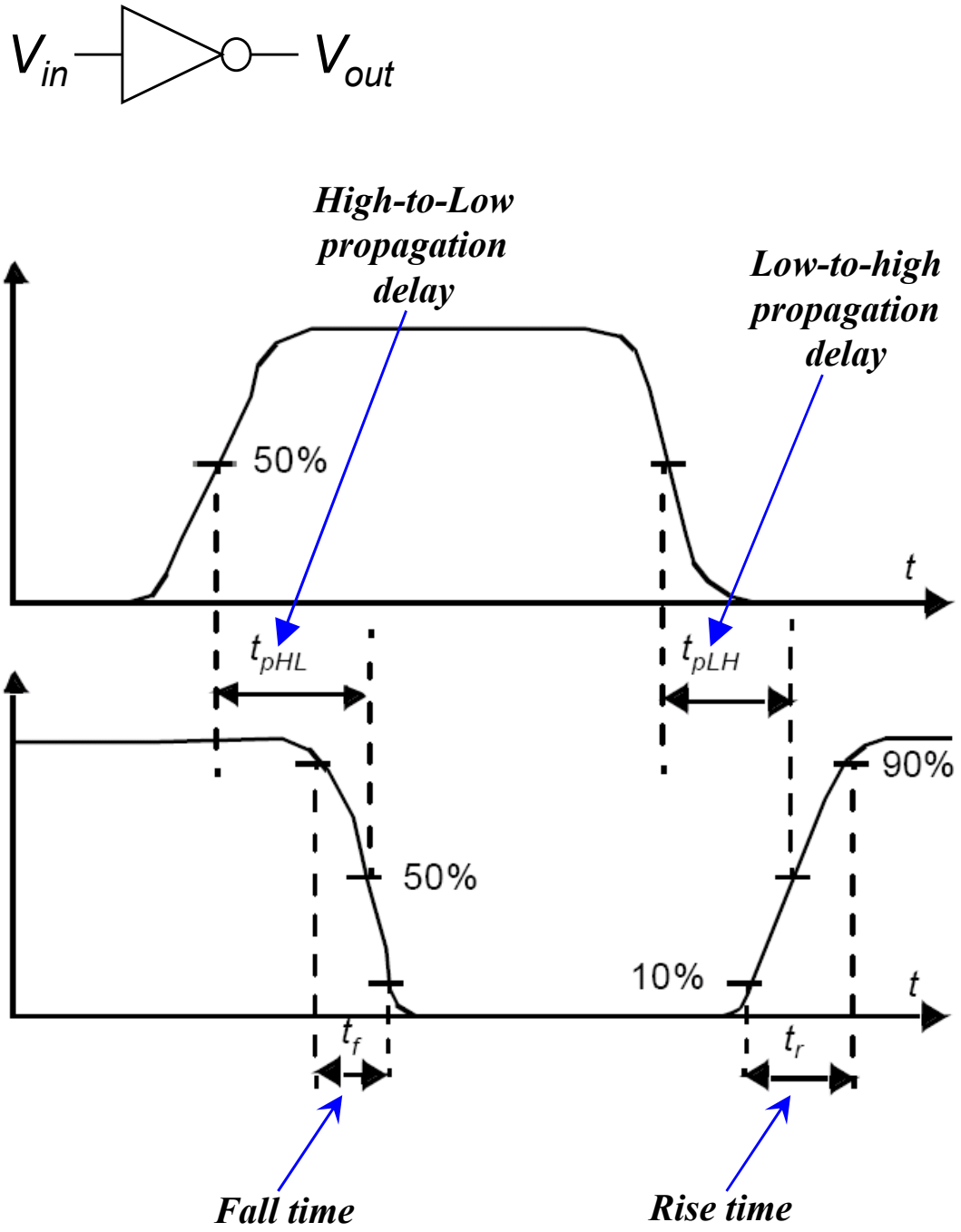
- Speed of operation of digital systems is limited by the *propagation delay* of logic gates from which circuit is constructed. In MOS circuits, capacitive loading is the main cause of delay due to:
  - Device capacitance, Interconnect capacitance and Fan-out gates





Propagation Delay t_p Definitions

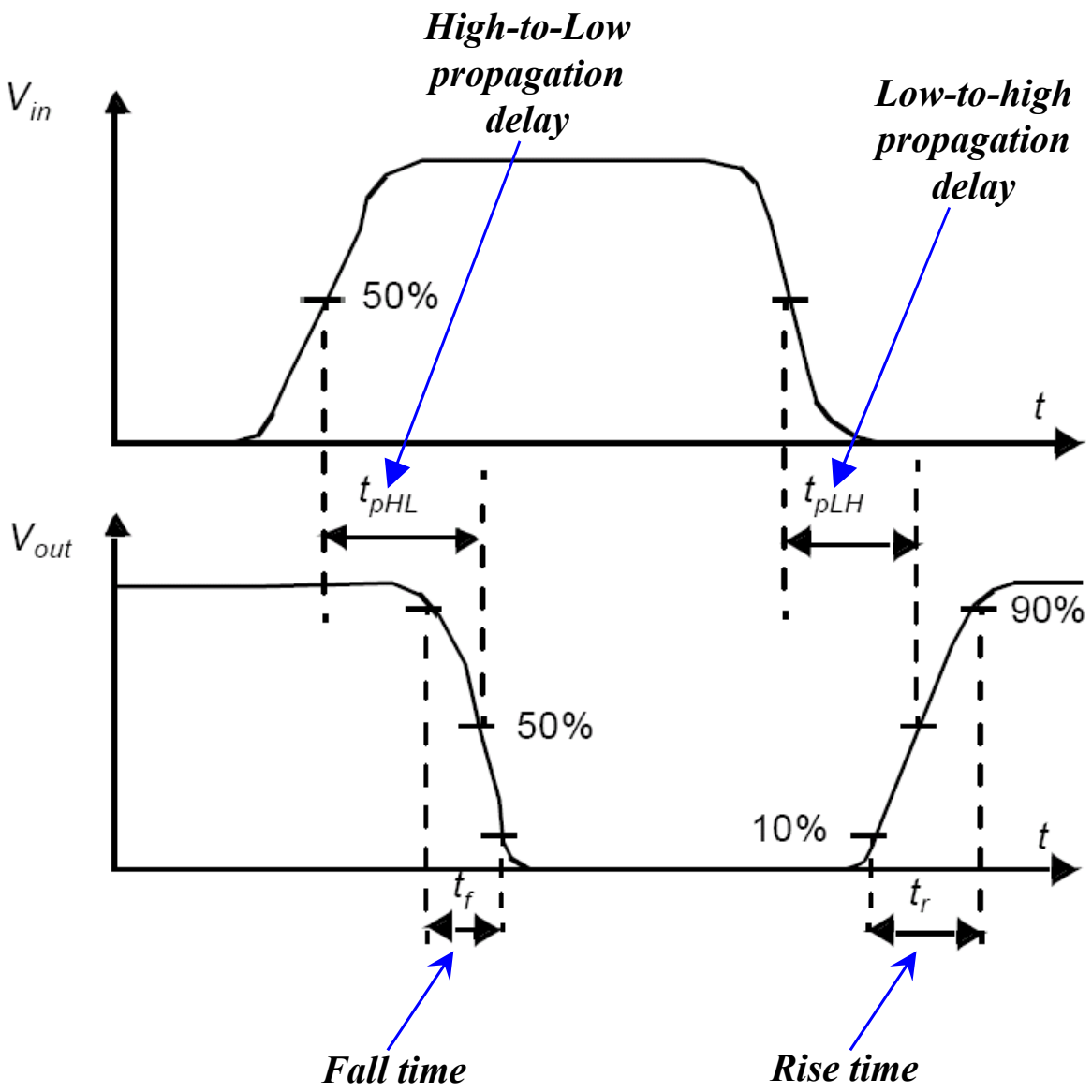
- Defines how quickly it responds to a change at its input(s).
- Expresses *the delay experienced by a signal when passing through a gate*.
- Measured between the 50% transition points of the input and output waveforms, as shown for an inverting gate.
- Because a gate displays different response times for rising or falling input waveforms, two definitions of the propagation delay are necessary.



Propagation Delay Definitions

- t_{pLH} defines the response time of the gate for a *low to high* (or positive) output transition.
- t_{pHL} refers to a *high to low* (or negative) transition.
- The propagation delay t_p is defined as the average of the two:

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$



Propagation Delay: A Quality metric

- In contrast to t_{pLH} and t_{pHL}, the propagation delay t_p is an artificial gate quality metric, and has no physical meaning per se. It is mostly used to compare different semiconductor technologies, or logic design styles.

- The propagation delay is not only a function of the circuit technology and topology, but depends upon other factors as well. Most importantly, the delay is a function of the *slopes* of the input and output signals of the gate.

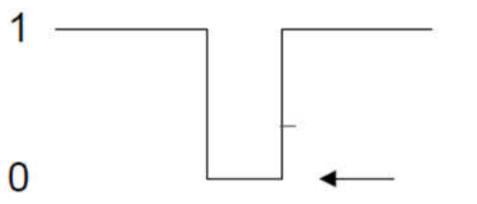
- To quantify these properties, we introduce the *rise and fall times* t_r and t_f, which are metrics that apply to individual signal waveforms rather than gates and express how fast a signal transits between the different levels. The uncertainty over when a transition actually starts or ends is avoided by defining the rise and fall times between the 10% and 90% points of the waveform.

Circuit's Behavior

- The **steady-state behavior** of a circuit is the value of the output after the inputs have been stable for a long time.
- The **transient behavior** of a circuit is the value of the output while (or soon after) the inputs change
- The **glitch** is a (often undesirable) short pulse produced in the output during a transient phase.
- If a circuit has **the possibility** of producing a glitch, the circuit has a **hazard**.

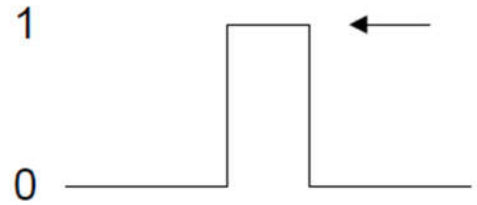
Types of Hazards

- Static 1-hazard
  - Occurs when output should remain static at 1 but temporarily switches to a 0 due to a change in an input.



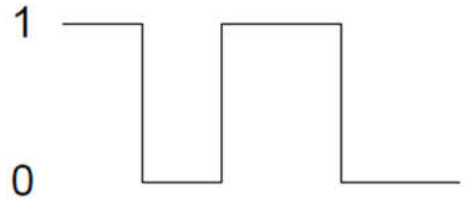
static-1 hazard (1->1)

- Static 0-hazard
  - Occurs when output should remain static at 0 but temporarily switches to a 1 due to a change in an input.

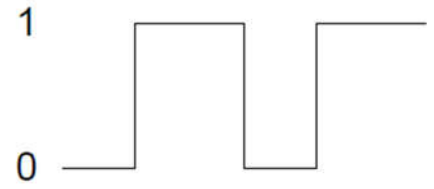


static-0 hazard (0->0)

- Dynamic hazards
  - Occurs when an input changes, and a circuit output should change 0 -> 1 or 1 ->0, but temporarily flips multiple times between values.



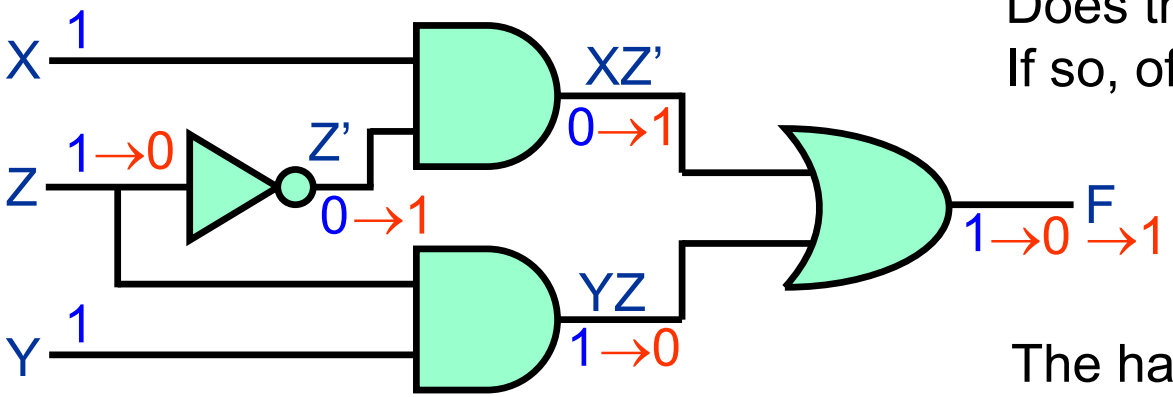
dynamic hazard (1->0)



dynamic hazard (0->1)

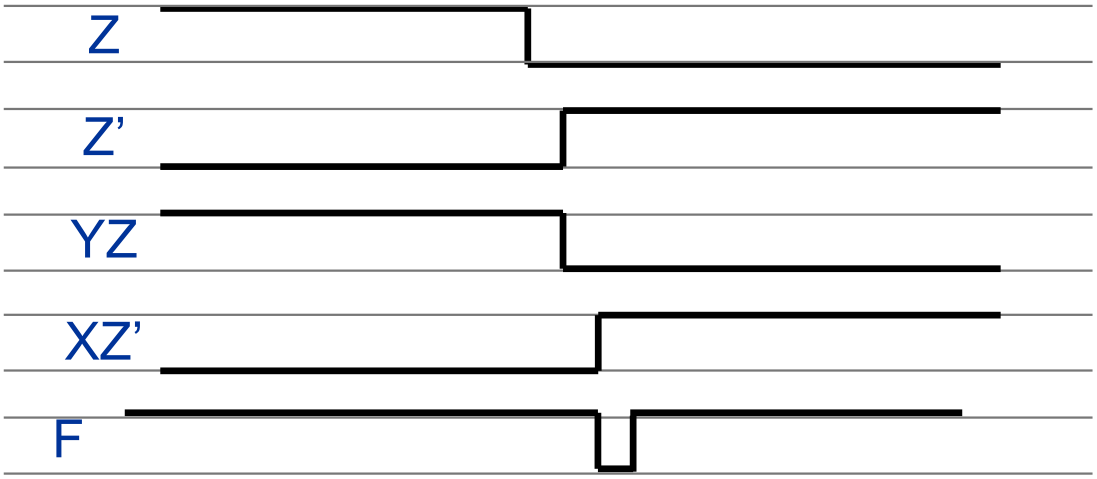
Example

Assume all gates have the same propagation delay



Does this circuit have a hazard?
If so, of what kind?

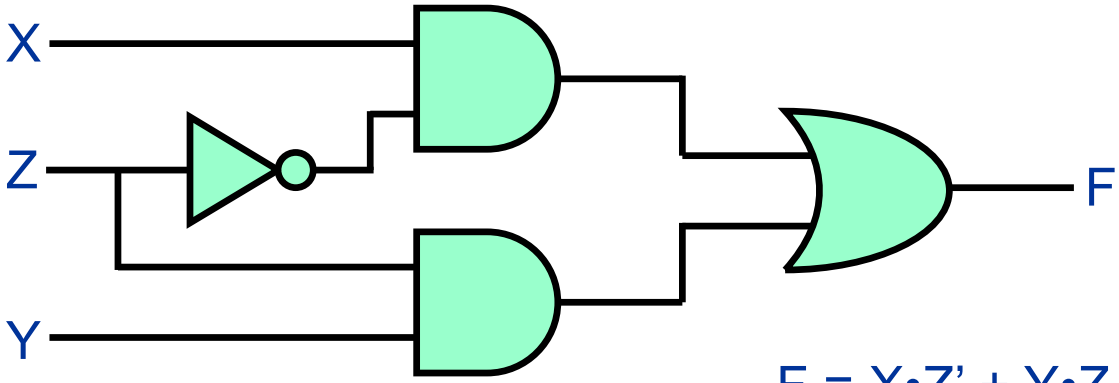
The hazard occurs in the transition from X,Y,Z = 111 to X,Y,Z = 110



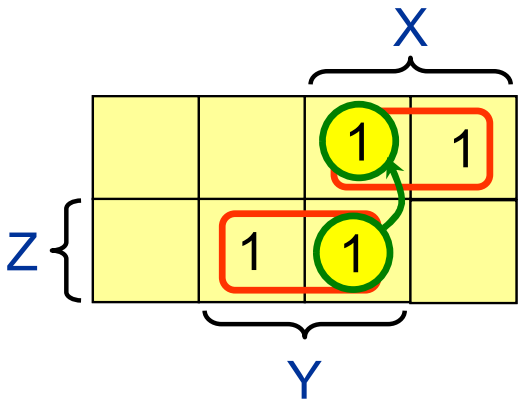
Static 1 Hazard

Static 1 Hazards in Karnaugh Maps

- When circuits are implemented as 2-level SOP, we can detect and remove static-1 hazards by inspecting the k-map and adding redundant product terms.



$F = X \cdot Z' + Y \cdot Z$

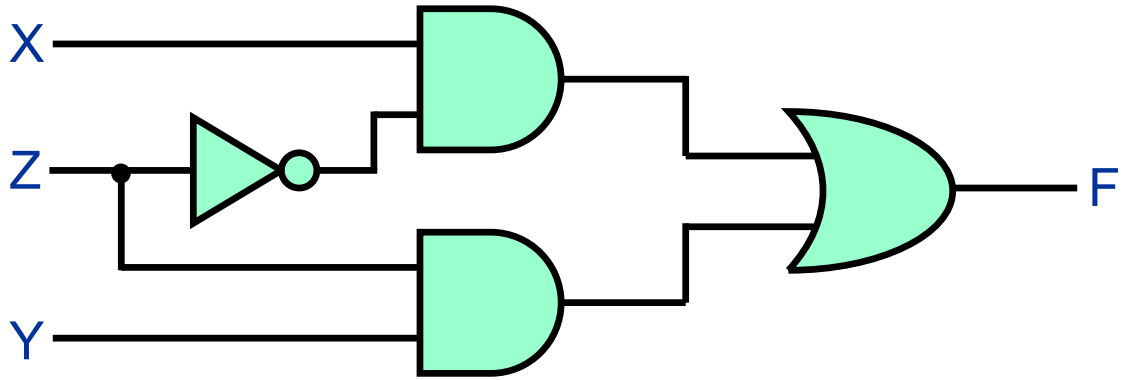


How can we identify a static-1 hazard in this Karnaugh map?

Two adjacent 1's that are not covered in the same term cause a static-1 hazard.

Note that the occurrence of a static hazard can depend on the direction of a signal change. Here no hazard for Z:0 ➡ 1 but hazard for Z:1 ➡ 0, with XY=11.

Static 1 Hazards in Karnaugh Maps



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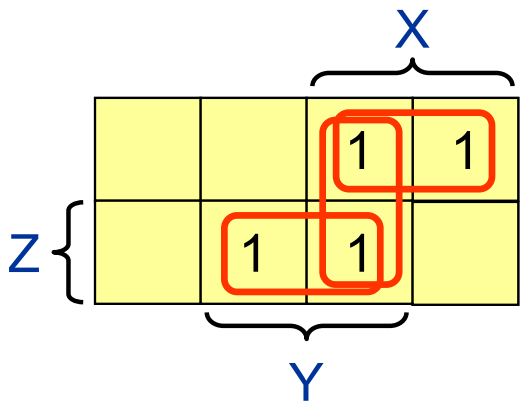


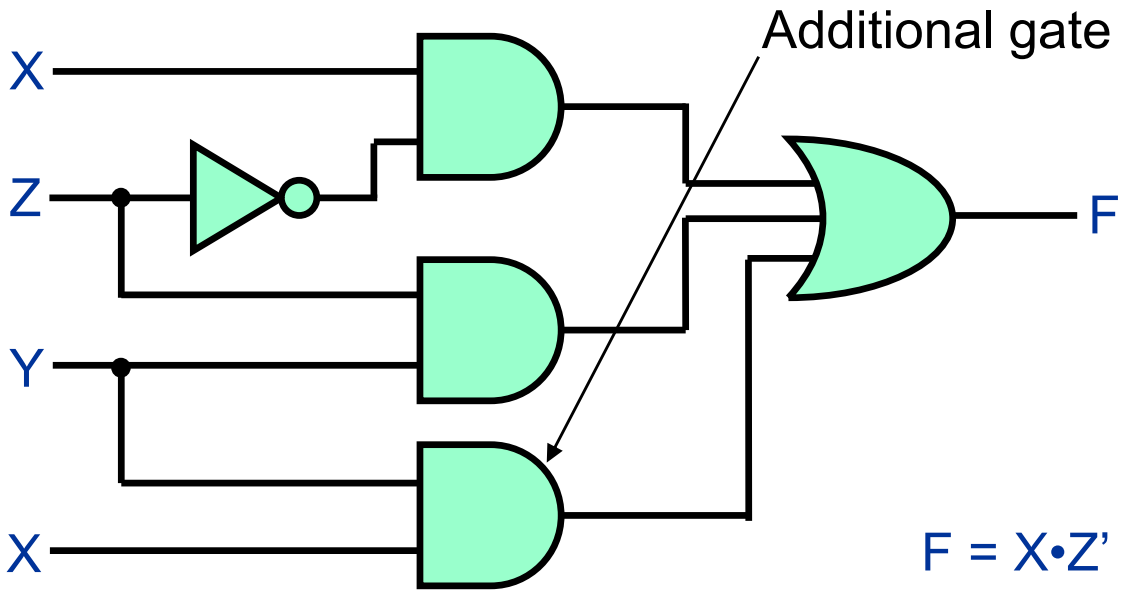
How can we eliminate the hazard?

We can add one extra term to F.

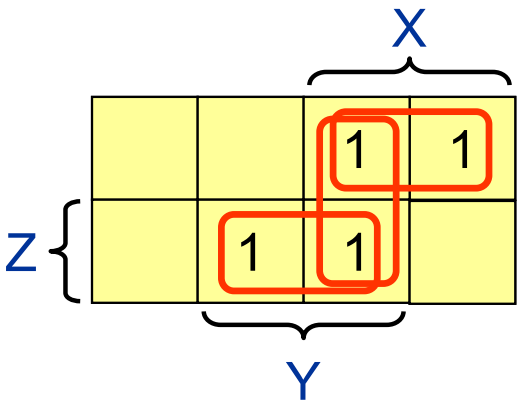
$F = X \cdot Z' + Y \cdot Z + X \cdot Y$

Additional
Prime implicant

Static 1 Hazards in Karnaugh Maps



$F = X \cdot Z' + Y \cdot Z$



How can we eliminate the hazard?

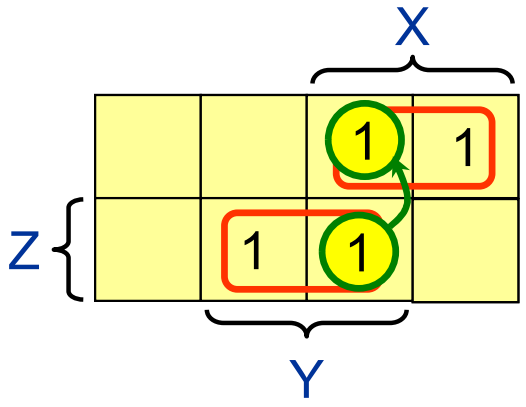
We can add one extra term to F.

$F = X \cdot Z' + Y \cdot Z + X \cdot Y$

Additional prime implicant

Hazards

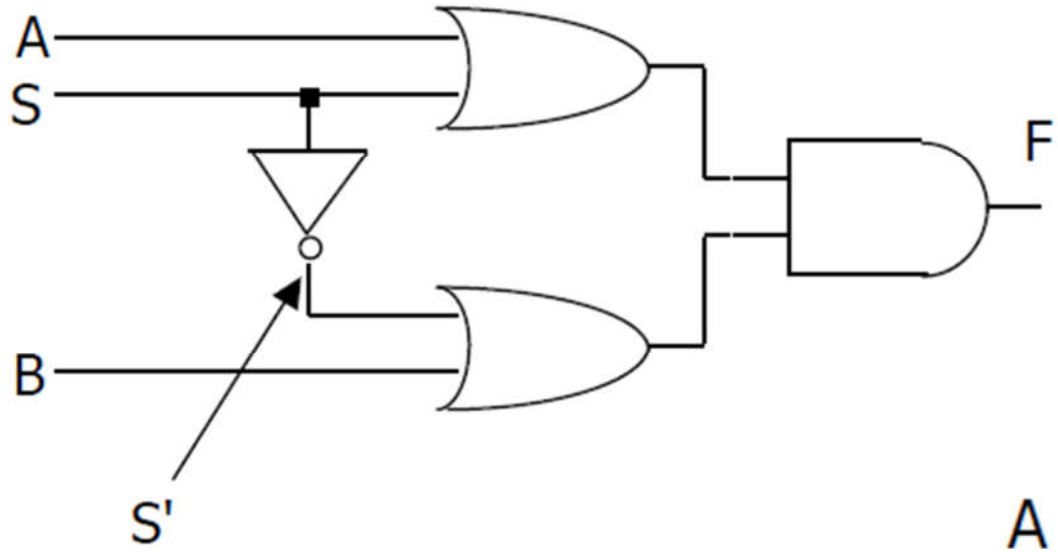
- In our study of hazards, we'll assume that input variable changes are spaced such that the effects of a change in one variable is permitted to propagate throughout the circuit before another variable is allowed to change.
- This is the single-input change case, since input signal patterns can change in only one variable at a time. For example, 00 can be followed by 01 or 10, but not 11.
- A *static hazard* is here a momentary change in an output that occurs as the result of the change of a single input variable when the value of the output variable is to remain fixed.

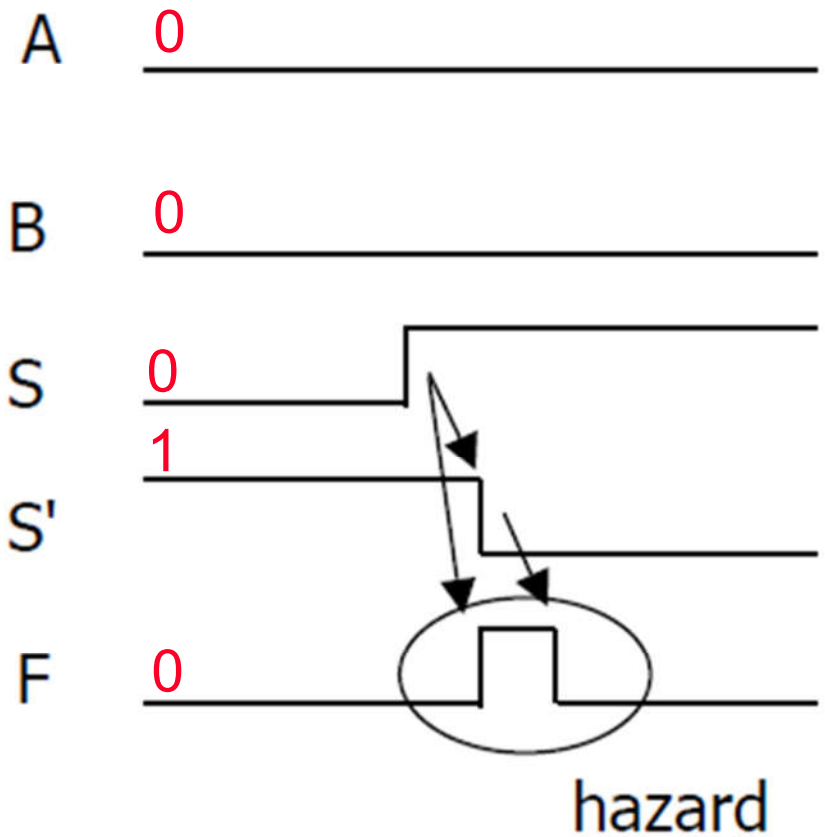


Hazards

- The cause of hazards is the timing delay of different components in the circuit.
- When certain paths through the circuit allow a variable change to propagate faster than other paths, this may cause glitches.
- The resulting glitches in the circuit may or may not induce additional problems - other than increased issues due to switching noise. It is good design practice to design circuits to minimize these hazards.
- **Static-1 hazards** occur **in sum-of-products** implementations, but do not occur in product-of-sums implementations.
- **Static-0 hazards** occur in **product-of-sums** implementations, but do not occur in sum-of-products implementations.

Static-0 Hazards





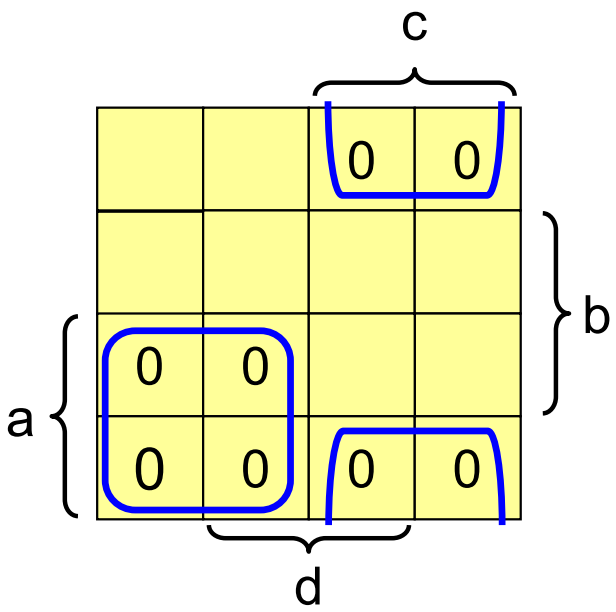
Static-0 Hazards in Karnaugh Maps

- We have seen that a logic circuit has **a static-1 hazard if there are two adjacent 1's not covered by a common product term in a sum of products implementation.**

- Similarly, a logic circuit has **a static-0 hazard if there are two adjacent 0's not covered by a common sum term in a product of sums implementation**.

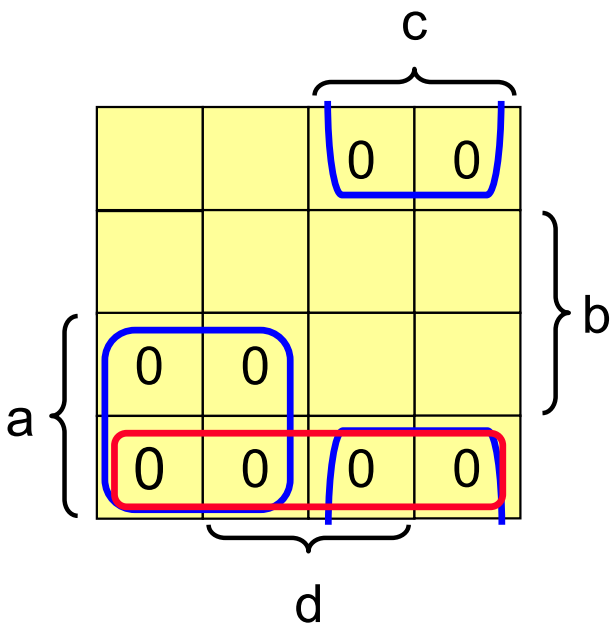
Static 0 Hazards in Karnaugh Maps

Minimal implementation



F = (a'+c)(b+c')

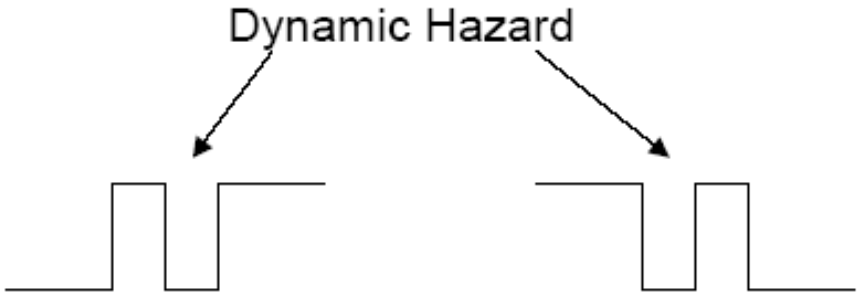
Static-0 Hazard-free
Minimal implementation



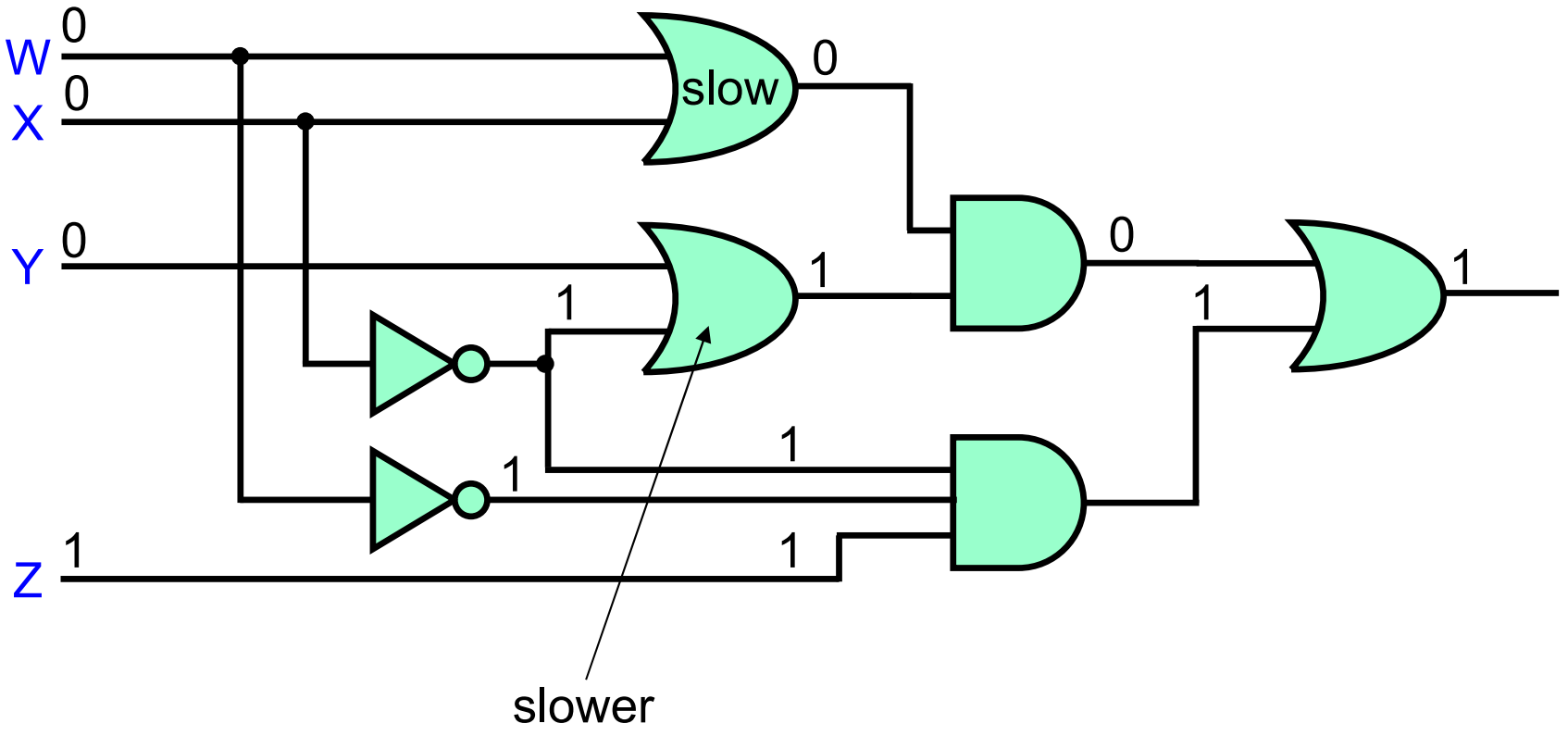
F = (a'+c)(b+c')(a'+b)

Dynamic Hazards: Multiple Glitches

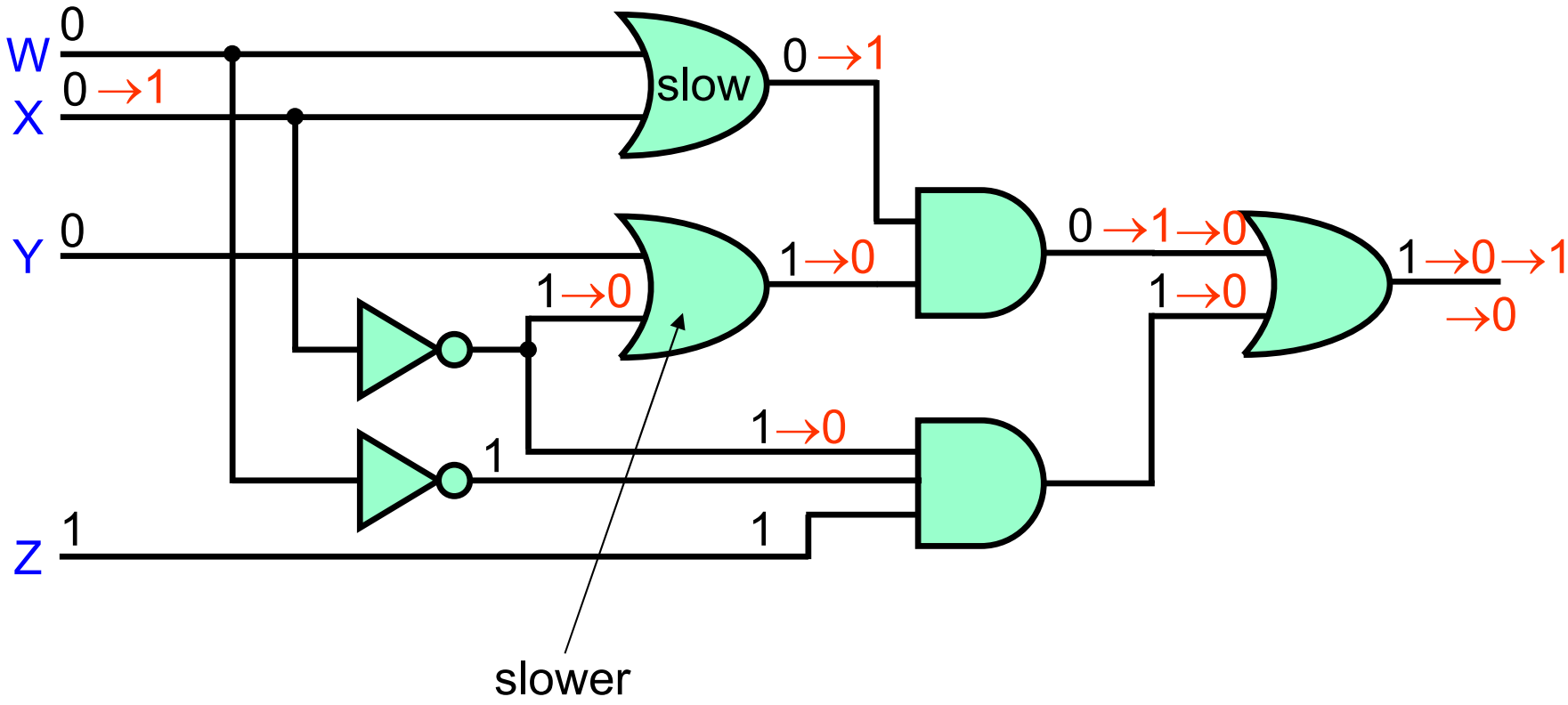
- A circuit has a dynamic hazard if an input transition is supposed to cause a single transition in an output, but causes two or more transitions before reached its expected value.
- Dynamic hazards are a consequence of multiple static hazards in a multi-level circuit.
- In general, very difficult to eliminate all dynamic hazards.
- Design critical circuits to be two-level circuits and eliminate all of the static hazards.
- Wait until signals are stable.



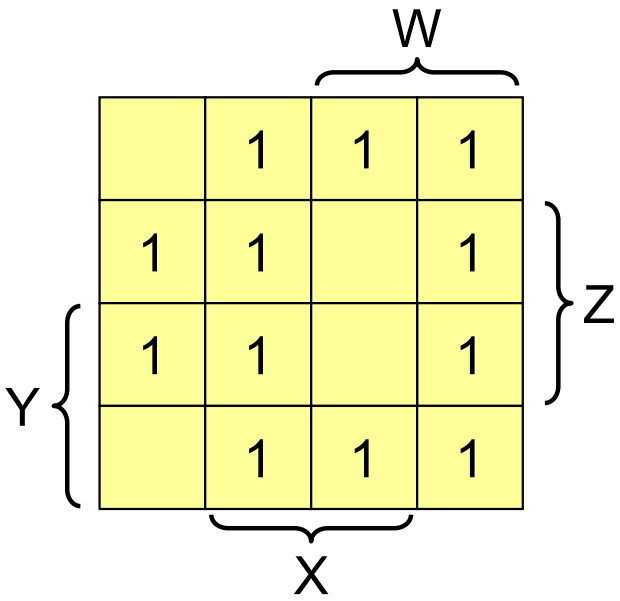
Dynamic Hazard Example



Dynamic Hazard Example

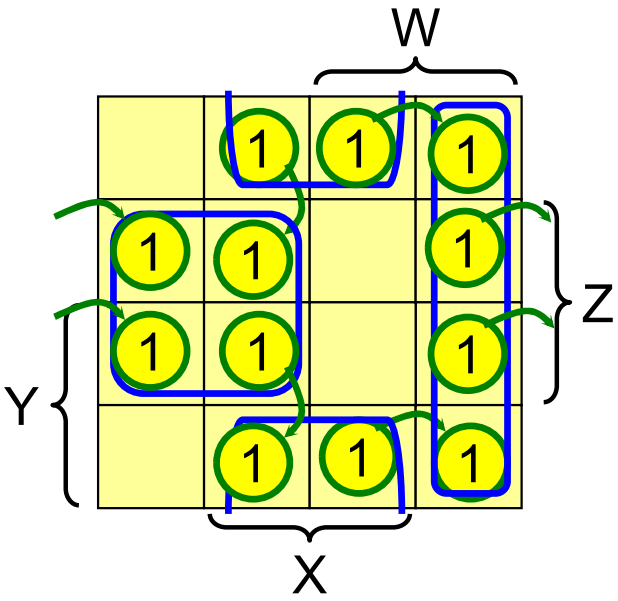


Exercise

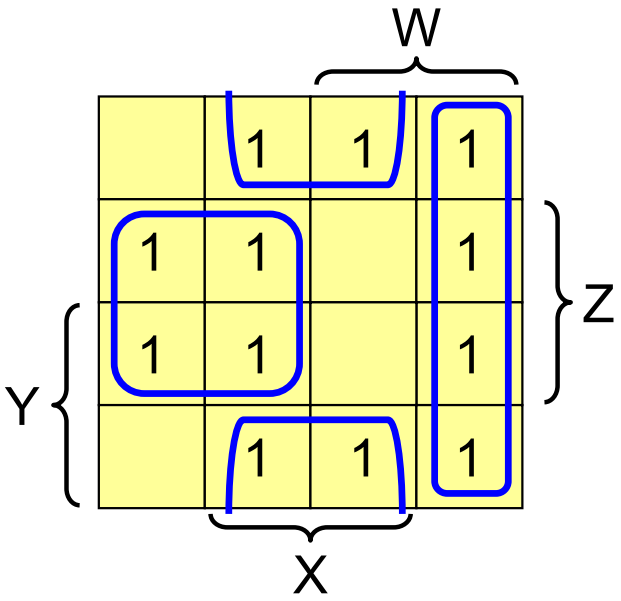


1. Write minimal form for F
2. Identify static-1 hazards
3. Eliminate static-1 hazards

Exercise



F = W'•Z + X•Z' + X'•W



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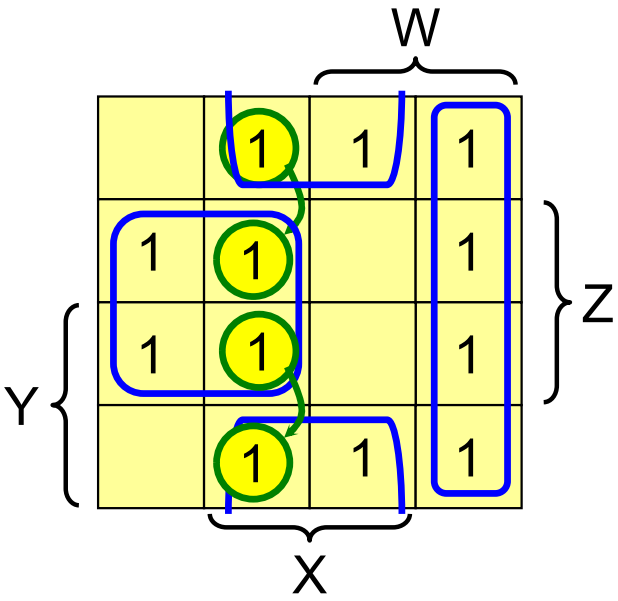
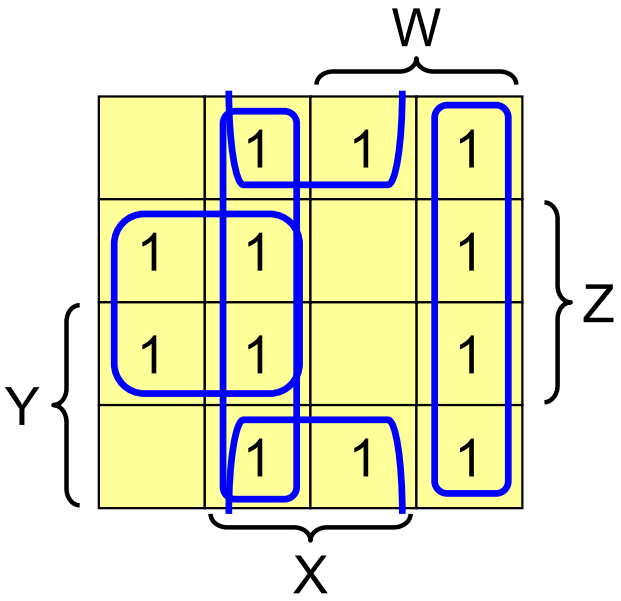
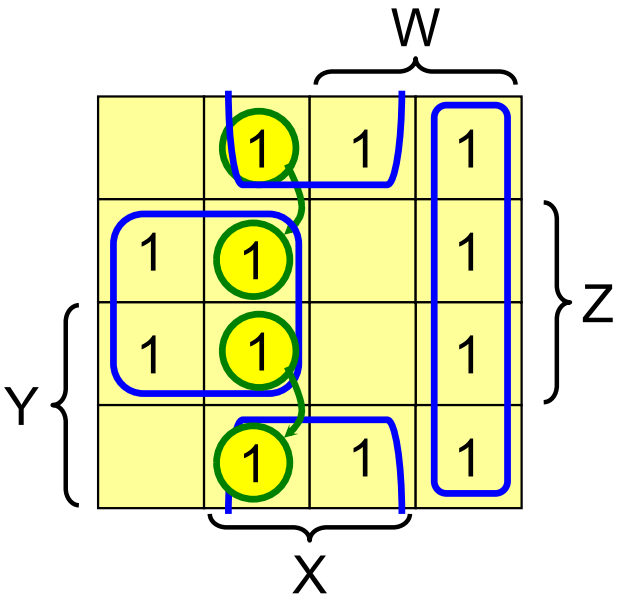


F = W'•Z + X•Z' + X'•W

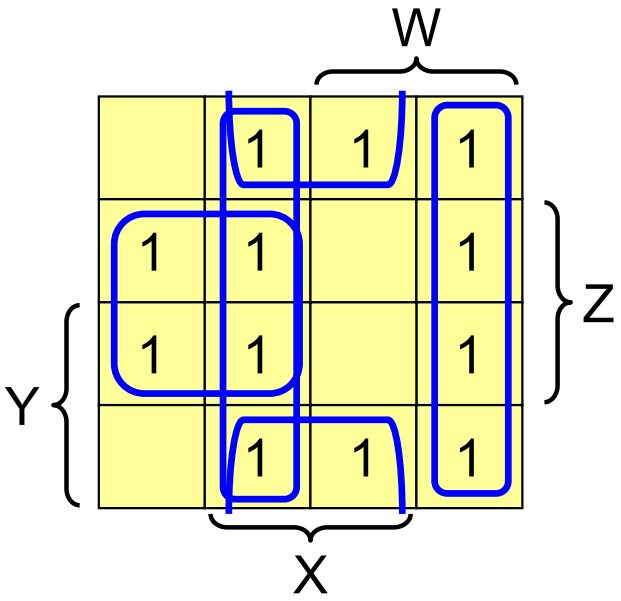


F = W'•Z + X•Z' + X'•W + X•W'

Exercise



F = W'•Z + X•Z' + X'•W



F = W'•Z + X•Z' + X'•W + X•W'

1. Write minimal form for F
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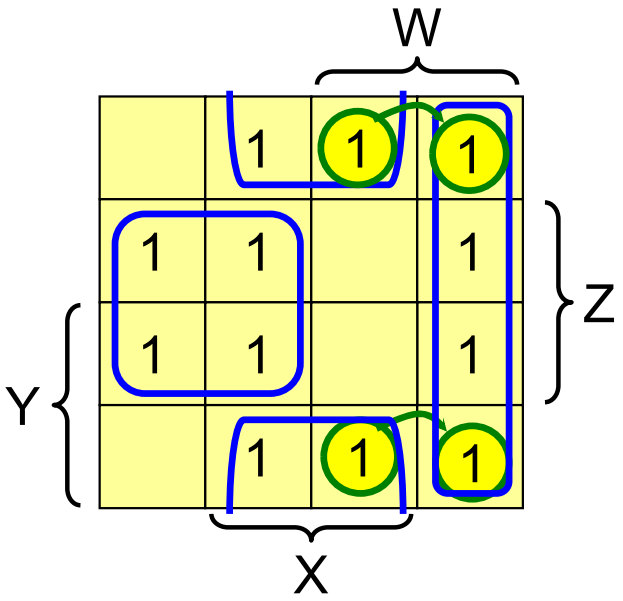
Exercise



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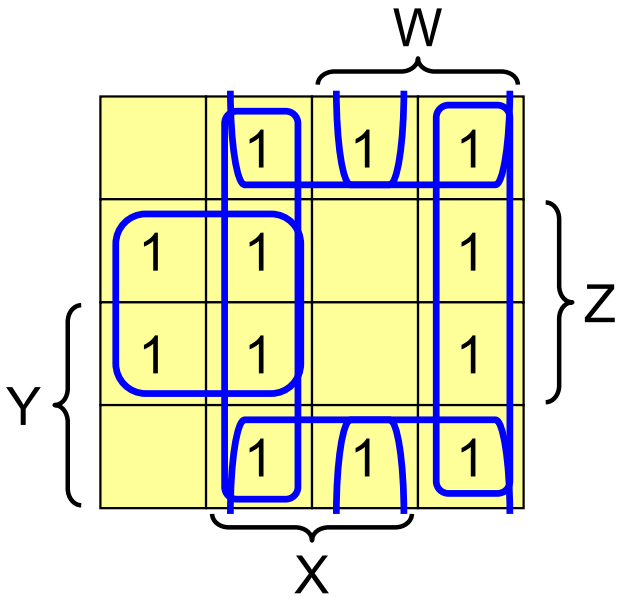

F = W'•Z + X•Z' + X'•W + X•W' + W•Z'

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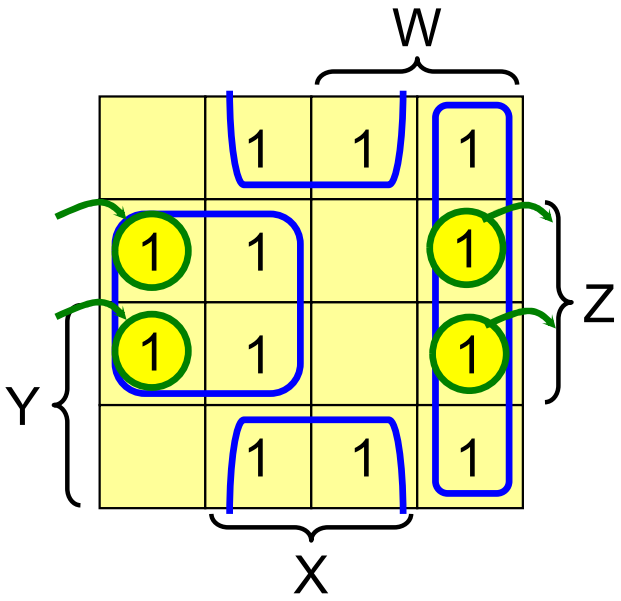
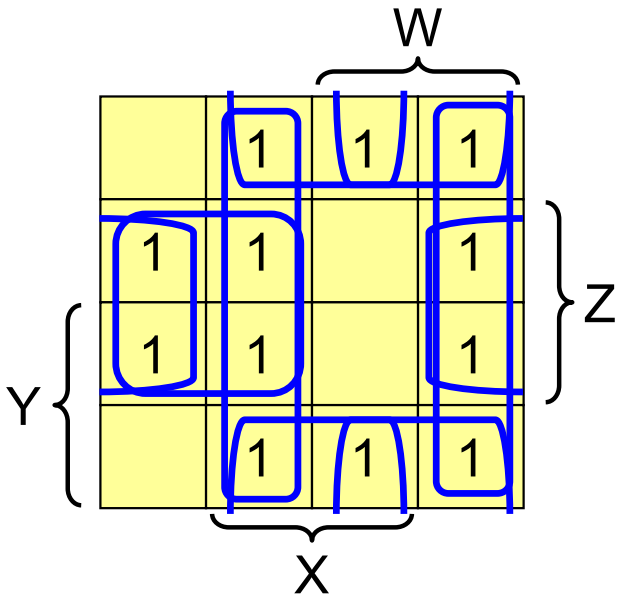
Exercise



F = W'•Z + X•Z' + X'•W



F = W'•Z + X•Z' + X'•W + X•W' + W•Z' + X'•Z

1. Write minimal form for F
2. Identify static-1 hazards
3. Eliminate static-1 hazards

Summary

- Glitching is due to a mismatch in the path lengths in the logic network; if all input signals of a gate change simultaneously, no glitching occurs.
- Equalizing the lengths of timing paths through logic is not easy.
- Glitches increase power dissipation and noise.
- Glitches can cause circuit failure if value is read while output is still unstable.
- A Karnaugh map can be used to eliminate static hazards but it usually results in more devices (a non-minimal circuit).
- Another method to eliminate timing hazards uses a clock to wait long enough for the output to become stable before reading it.
- Clocking the signal does not eliminate the glitch but stops it from causing circuit failure.

Acknowledgments

- Credit is acknowledged where credit is due. Please refer to the full list of references.