Homework Questions

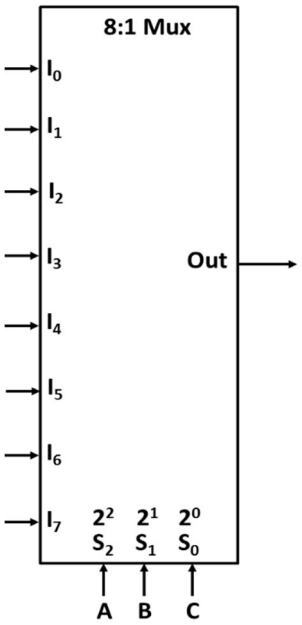
Circuits and Electronics

Week 2

Q.1 a) Consider the following function F(A,B,C,D) = Σm(2,3,8,10,13,14) that is F(A,B,C,D)=1 for ABCD=0010, 0011, etc…

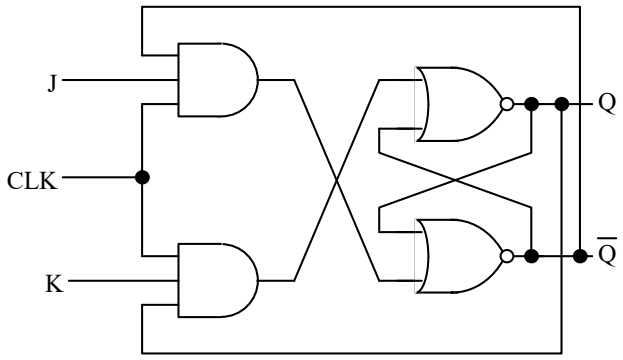
Implement the above function using **ONLY the 8-to-1 multiplexer shown below and any logic gates**. Note that in the 8:1 multiplexer shown below, **input variables A, B, C have been connected to select lines S_2, S_1, S_0**, respectively. Assume variables A, B, C and D **are NOT available in their complemented form**. Show your working using the truth table drawn below.

A	B	C	D	F	
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		



Q.2

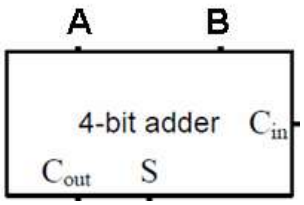
Describe the operation of the JK latch below.



J	K	CLK	Q^{n+1}
X	X	0	
0	0	1	
0	1	1	
1	0	1	
1	1	1	

Q.3

a) Draw a diagram showing how an 8-bit adder can be constructed from 4-bit adders using the CARRY-SELECT principle. Label all multiplexers and signal lines. Indicate the number of bits for every signal line. Use the following representation for each 4-bit adder.



Q.4

For the following circuit, complete the timing diagram shown below. **Ensure that you clearly indicate any delays between signals.** Assume all components (gates and flip-flops) have the same propagation delay δ. Assume that δ is significantly shorter than the clock period. Note that Q1 is initially low, and input to D1 is high, and output Z is low.