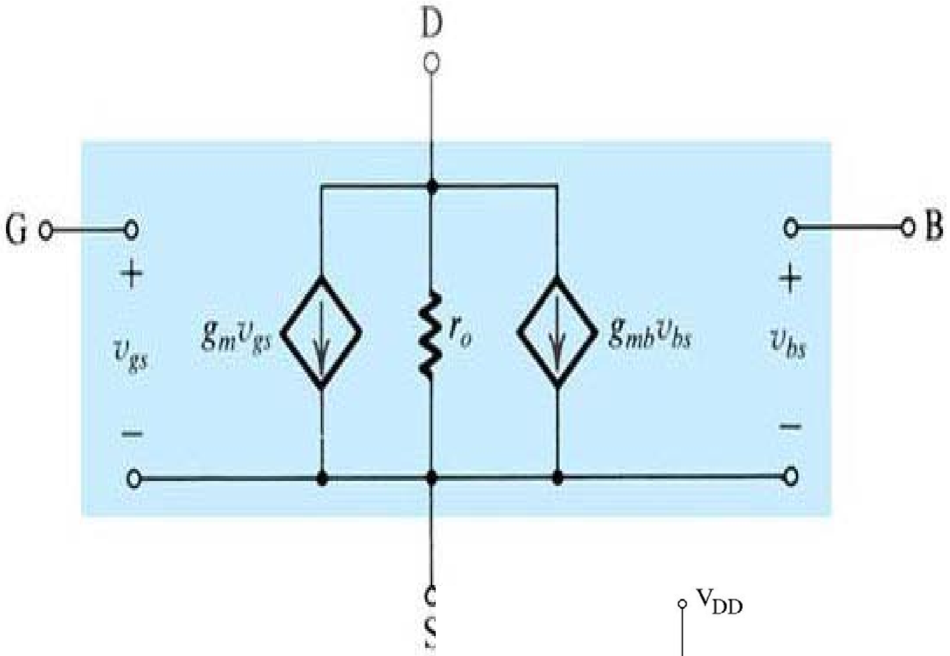
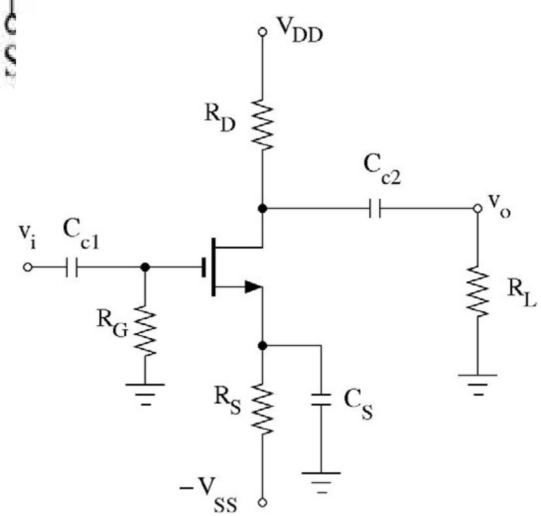
Lecture 11

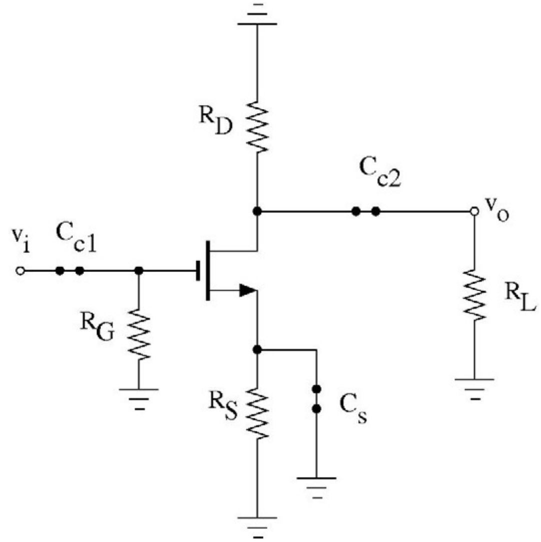
The MOS Transistor as an Amplifier – part II

Low-frequency MOS small signal "circuit" model



How about high fre signal?





Capacitors are short for low fre signal when draw the equivalent circuit.

The internal capacitance and high fre model

- Internal capacitances
  - The gate capacitive effect
    - Triode region
    - Saturation region
    - Cut-off region
    - Overlap capacitance
  - The junction capacitances
    - Source-body depletion-layer capacitance
    - Drain-body depletion-layer capacitance
- High frequency model

The gate capacitive effect

- MOSFET operates at triode region

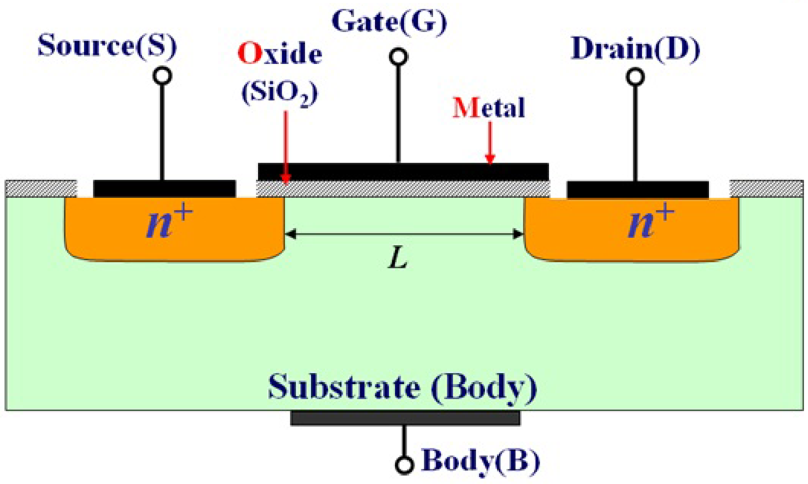
$$C_{gs} = C_{gd} = \tfrac{1}{2} WLC_{ox}$$

- MOSFET operates at saturation region

$$\begin{cases} C_{gs} = \tfrac{2}{3} WLC_{ox} \\ C_{gd} = 0 \end{cases}$$

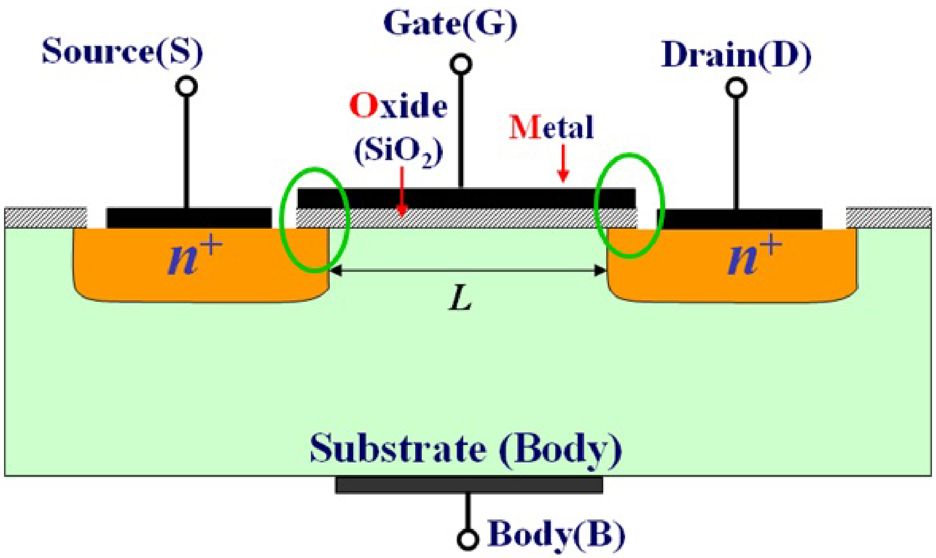
- MOSFET operates at cutoff region

$$\begin{cases} C_{gs} = C_{gd} = 0 \\ C_{gb} = WLC_{ox} \end{cases}$$



Overlap capacitance

- Overlap capacitance results from the fact the source and drain diffusions extend slightly under the gate oxide.
- The expression for overlap capacitance $C_{ov} = WL_{ov}C_{ox}$
- Typical value $L_{ov} = 0.05 - 0.1L$
- This additional component should be added to C_{gs} and C_{gd} in all preceding formulas



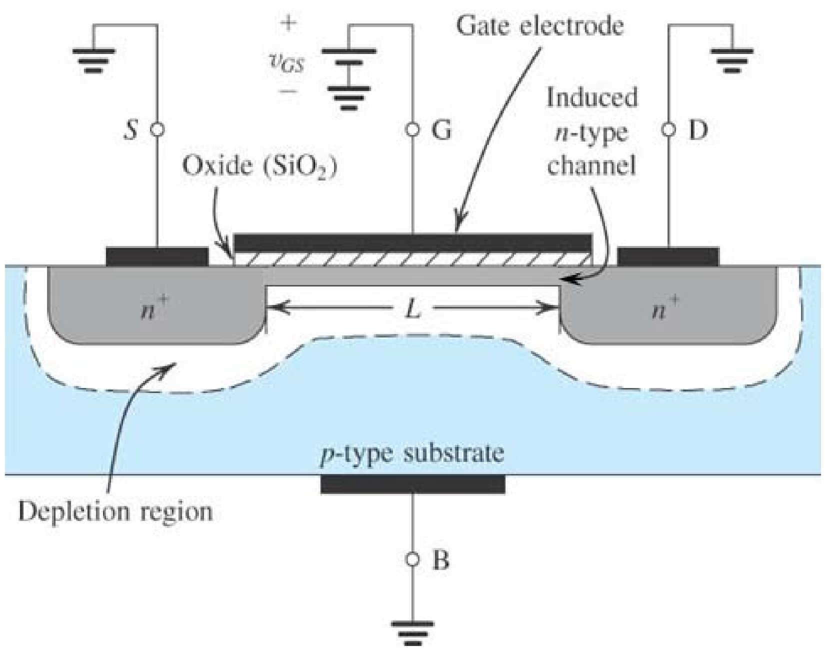
The junction capacitances

- Source-body depletion-layer capacitance

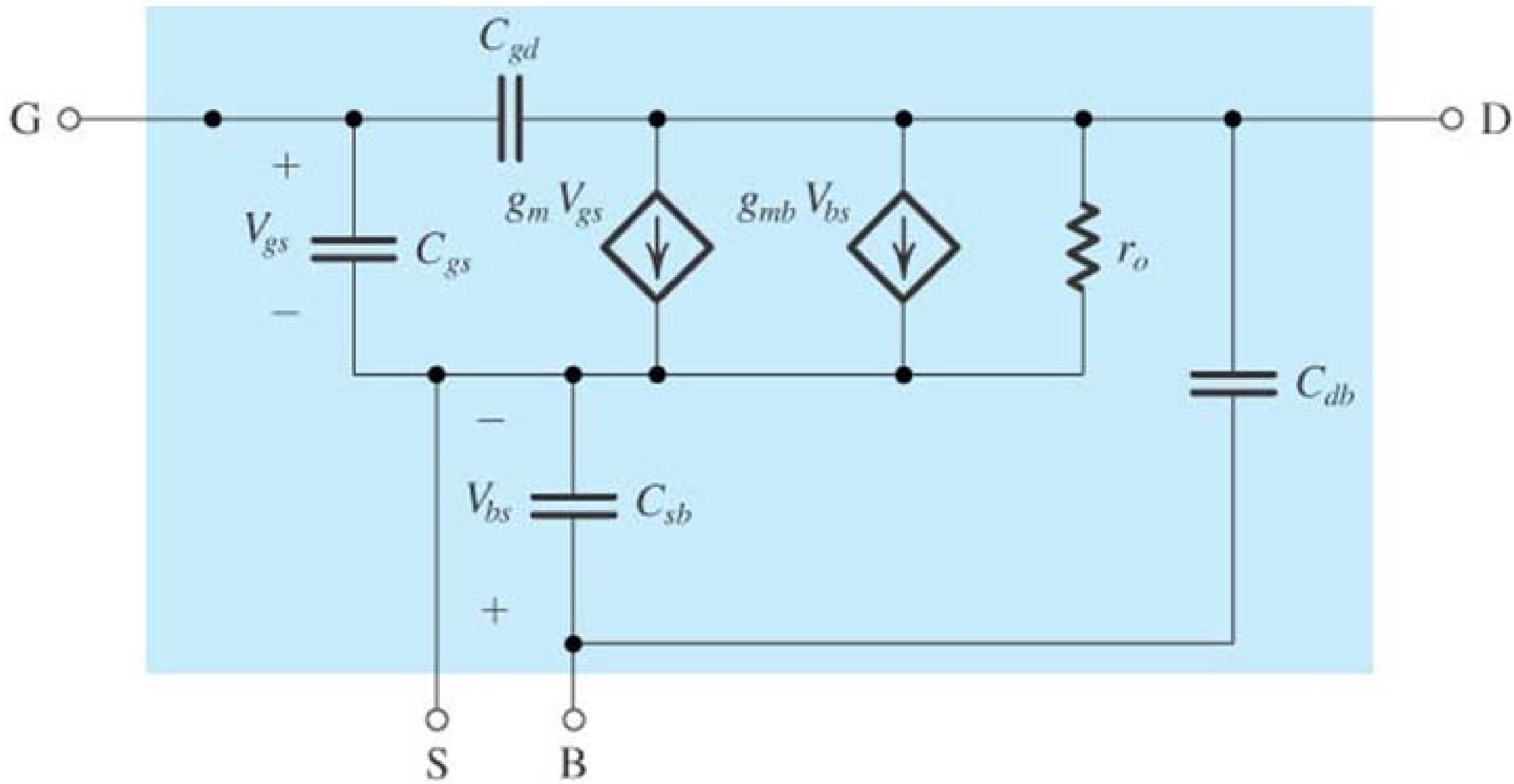
$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{V_{SB}}{V_o}}}$$

- Drain-body depletion-layer capacitance

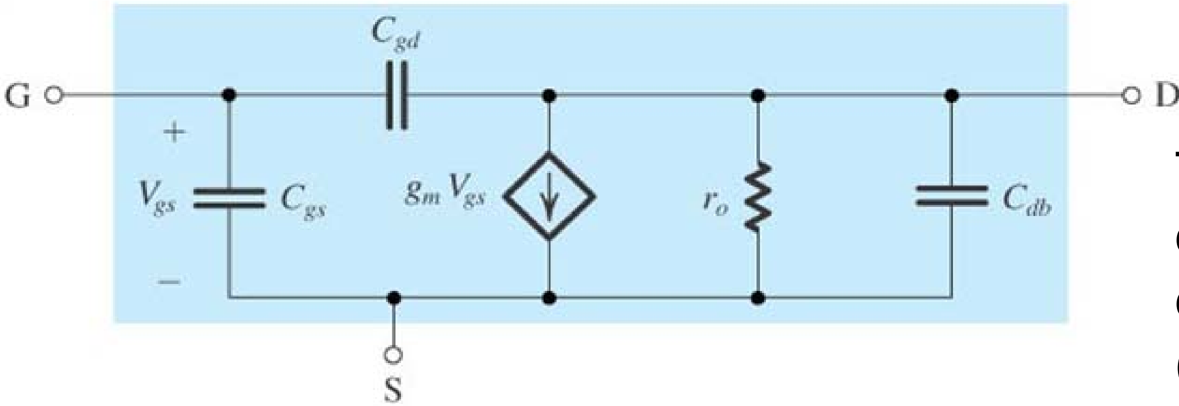
$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{V_o}}}$$



High-frequency model

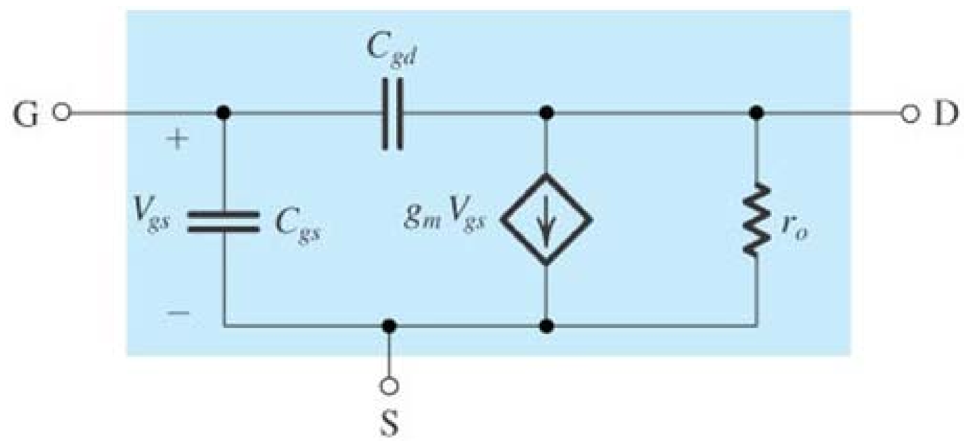


High-frequency model



The equivalent circuit for the case in which the source is connected to the substrate (body)

The equivalent circuit model with C_{db} neglected (to simplify analysis)



The MOSFET unity-gain frequency

- Current gain

$$\frac{I_o}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})}$$

- Unity-gain frequency

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

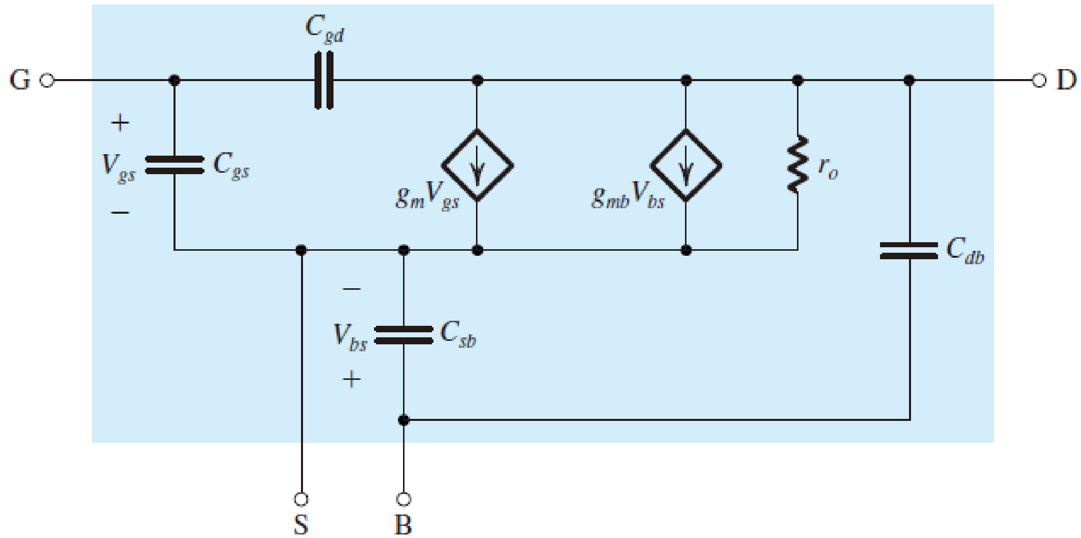
Frequency at which magnitude of the short-circuit current gain of CS configuration becomes 1

$$f_T \sim 5 - 50\ GHz$$

Summary of MOSFET high-frequency model

Table 9.1 The MOSFET High-Frequency Model

Model



Model Parameters

$$g_m = \mu_n C_{ox} \frac{W}{L} |V_{OV}| = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{|V_{OV}|}$$

$$g_{mb} = \chi g_m, \quad \chi = 0.1 \text{ to } 0.2$$

$$r_o = |V_A| / I_D$$

$$C_{gs} = \tfrac{2}{3} W L C_{ox} + W L_{ov} C_{ox}$$

$$C_{gd} = W L_{ov} C_{ox}$$

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{|V_{SB}|}{V_0}}}$$

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{|V_{DB}|}{V_0}}}$$

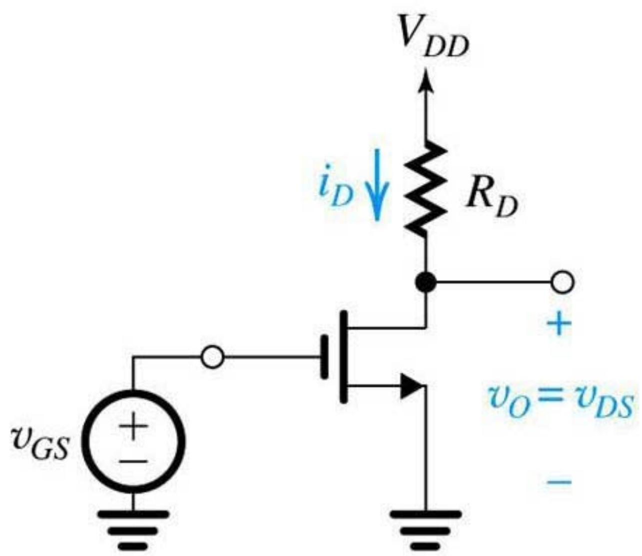
$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

Example

For an n-channel MOSFET with $t_{ox} = 10$ nm, $L = 1.0$ µm, $W = 10$ µm, $L_{ov} = 0.05$ µm, $C_{sb0} = C_{db0} =$ 10 fF, $V_0 = 0.6$ V, $V_{SB} = 1$ V, and $V_{DS} = 2$ V, calculate the following capacitances when the transistor is operating in saturation: C_{ox}, C_{ov}, C_{gs}, C_{gd}, C_{sb}, and C_{db}.
Ans. 3.45 fF/µm^2; 1.72 fF; 24.7 fF; 1.72 fF; 6.1 fF; 4.1 fF

Calculate f_T for the n-channel MOSFET whose capacitances were found as above. Assume operation at 100 µA, and that $k_n' = 160$ µA/V^2.
Ans. 3.7 GHz.

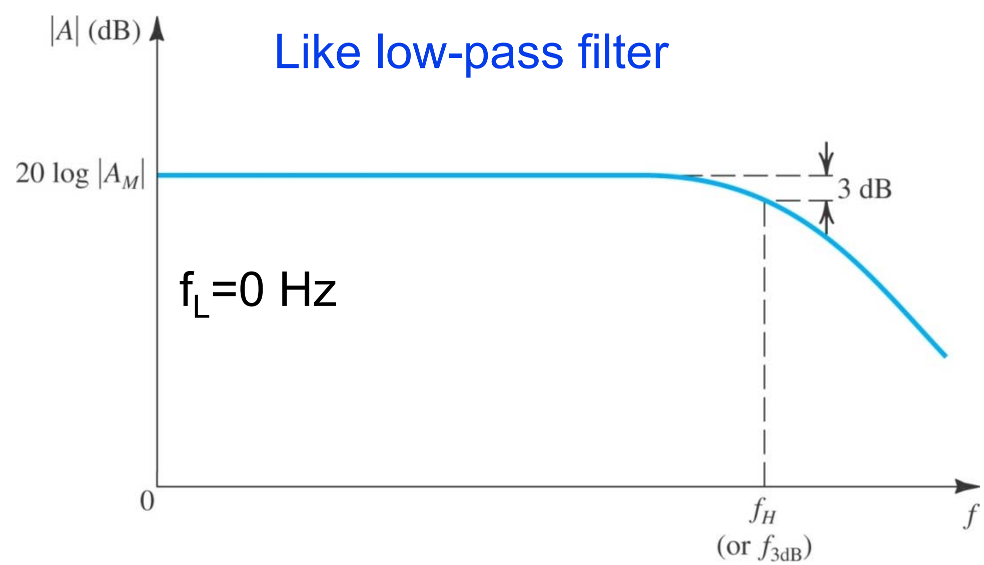
Frequency Response of a CS amplifier



DC-coupled CS amplifier

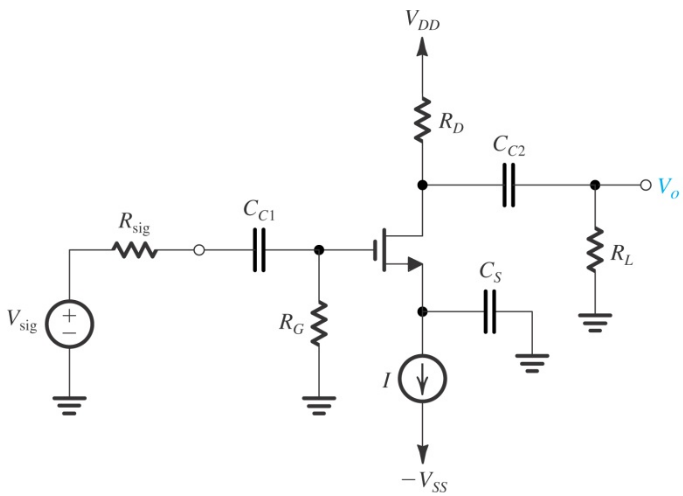
Bandwidth is the frequency range over which gain is flat. Here, bandwidth is f_H for DC-coupled CS amplifier.

Like low-pass filter



At high frequencies, gain drops due to effects of internal capacitances of the device

Frequency Response of a CS amplifier (cont'd)

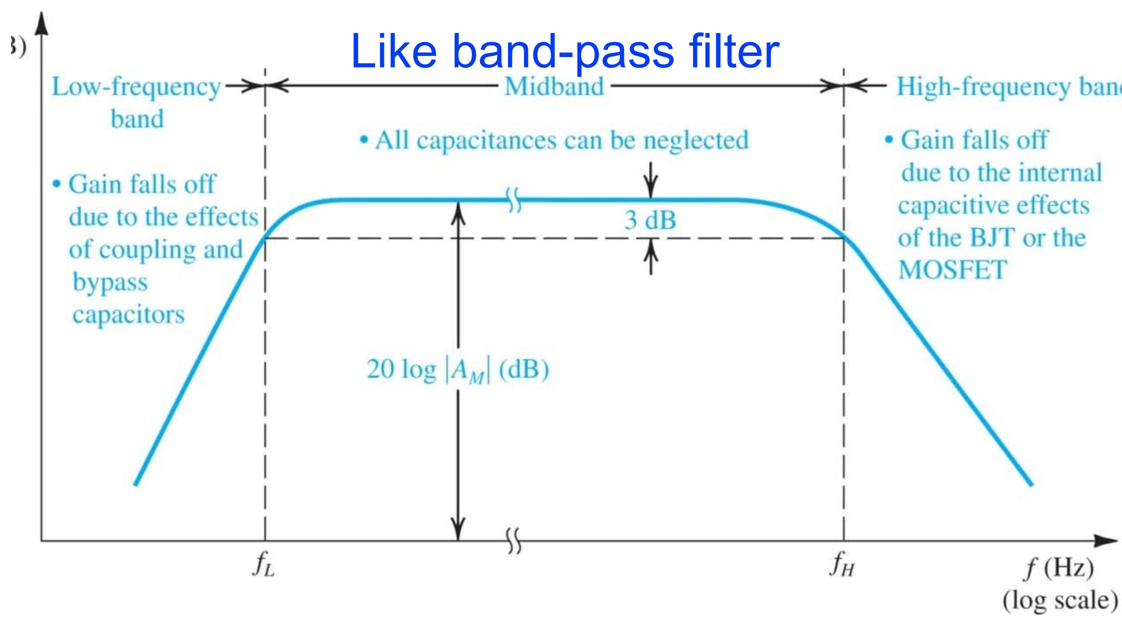


Bandwidth is the frequency range over which gain is flat. Here, bandwidth is f_H - f_L for AC-coupled CS amplifier.

three frequency bands of interest

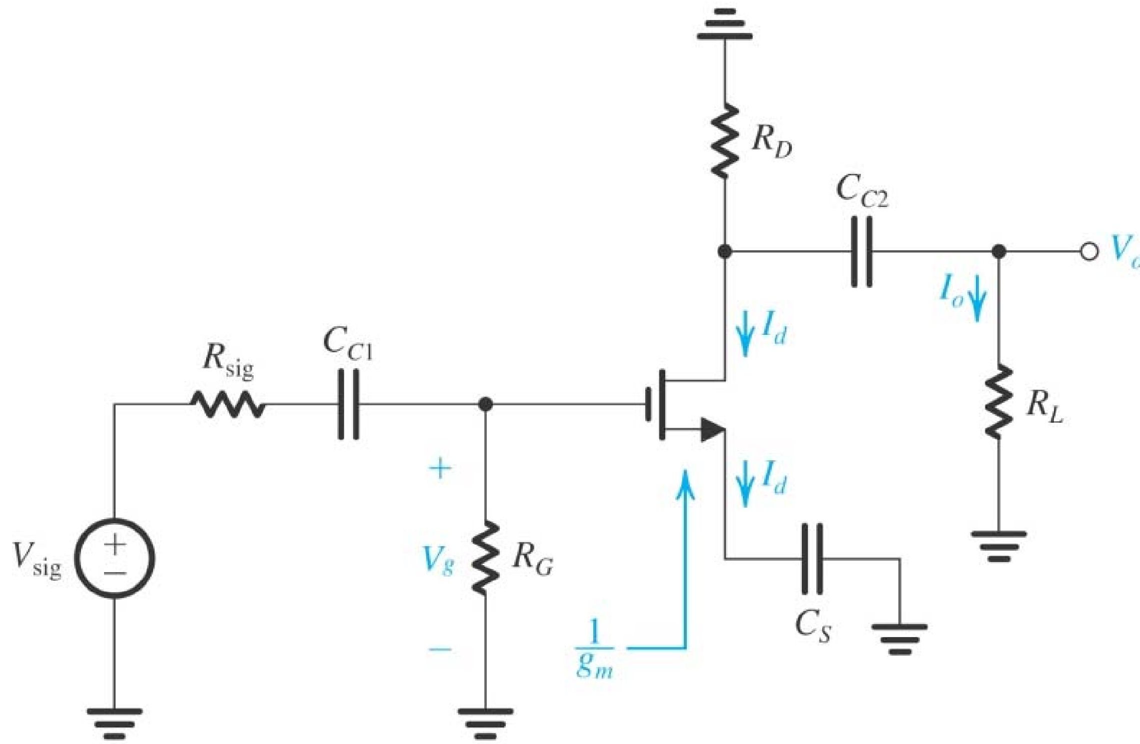
AC-coupled amplifier

Like band-pass filter



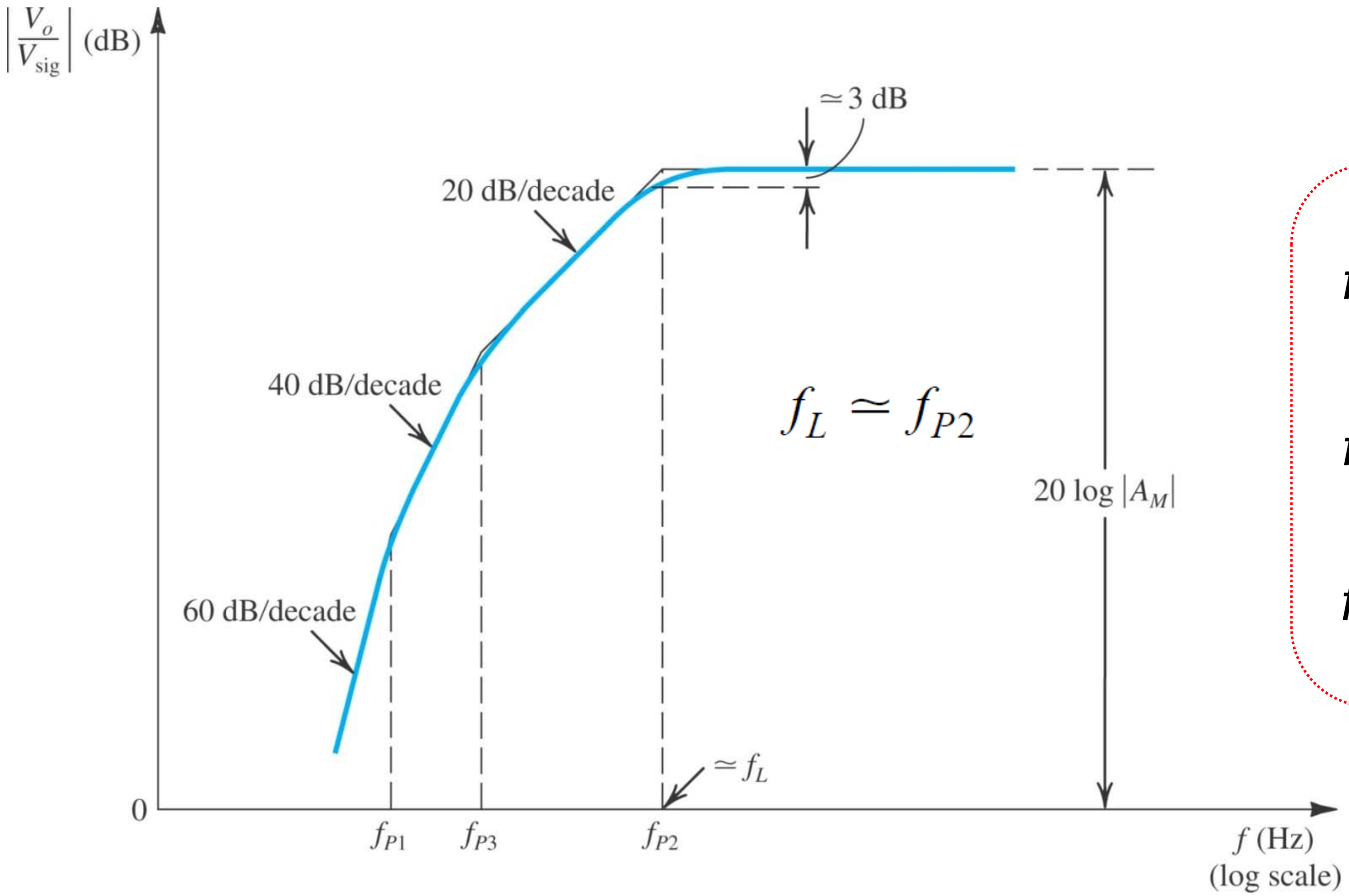
At low frequency, gain drops due to impedance from coupling capacitances increasing for low frequencies

Low Frequency Response



Analysis of the CS amplifier to determine its low-frequency transfer function. For simplicity, r_o is neglected

Low Frequency Response



$$f_{P1} = \frac{1}{C_{C1}(R_G + R_{sig})}$$

$$f_{P2} = \frac{g_m}{C_S}$$

$$f_{P3} = \frac{1}{C_{C2}(R_D + R_L)}$$

low-frequency magnitude response of a CS amplifier for which the three break frequencies are sufficiently separated for their effects to appear distinct.

Example

We wish to select appropriate values for the coupling capacitors C_{C1} and C_{C2} and the bypass capacitor C_S for a CS amplifier for which $R_G = 4.7\ \text{M}\Omega$, $R_D = R_L = 15\ \text{k}\Omega$, $R_{sig} = 100\ \text{k}\Omega$, and $g_m = 1\ \text{mA/V}$. It is required to have f_L at 100 Hz and that the nearest break frequency be at least a decade lower.

Solution:

We select CS so that

$$f_{P2} = \frac{1}{2\pi(C_S/g_m)} = f_L$$

Thus,

$$C_S = \frac{g_m}{2\pi f_L} = \frac{1 \times 10^{-3}}{2\pi \times 100} = 1.6\ \mu\text{F}$$

For $f_{P1} = f_{P3} = 10$ Hz, we obtain

$$10 = \frac{1}{2\pi C_{C1}(0.1 + 4.7) \times 10^6}$$

which yields

$$C_{C1} = 3.3\ \text{nF}$$

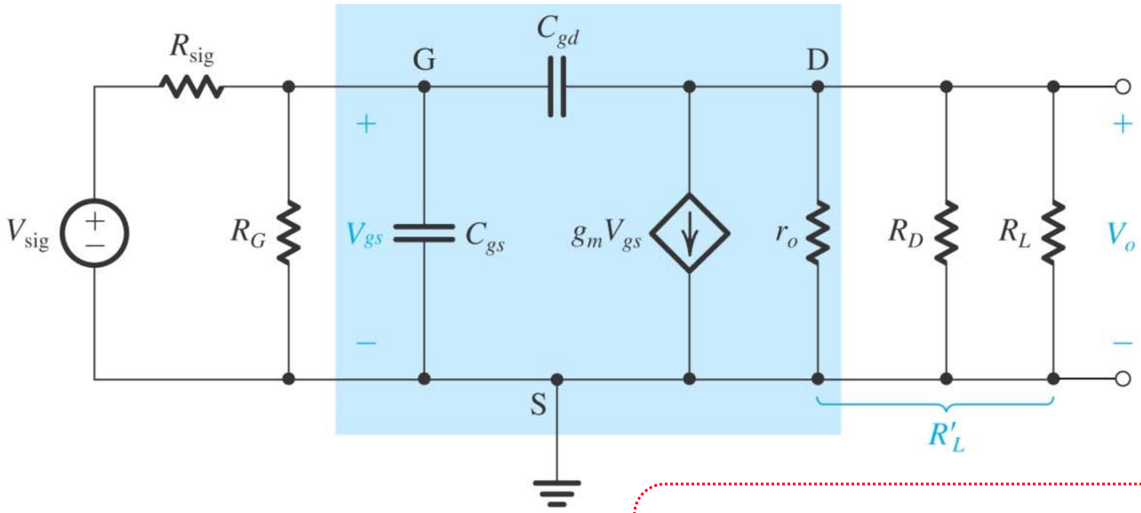
and

$$10 = \frac{1}{2\pi C_{C2}(15 + 15) \times 10^3}$$

which results in

$$C_{C2} = 0.53\ \mu\text{F}$$

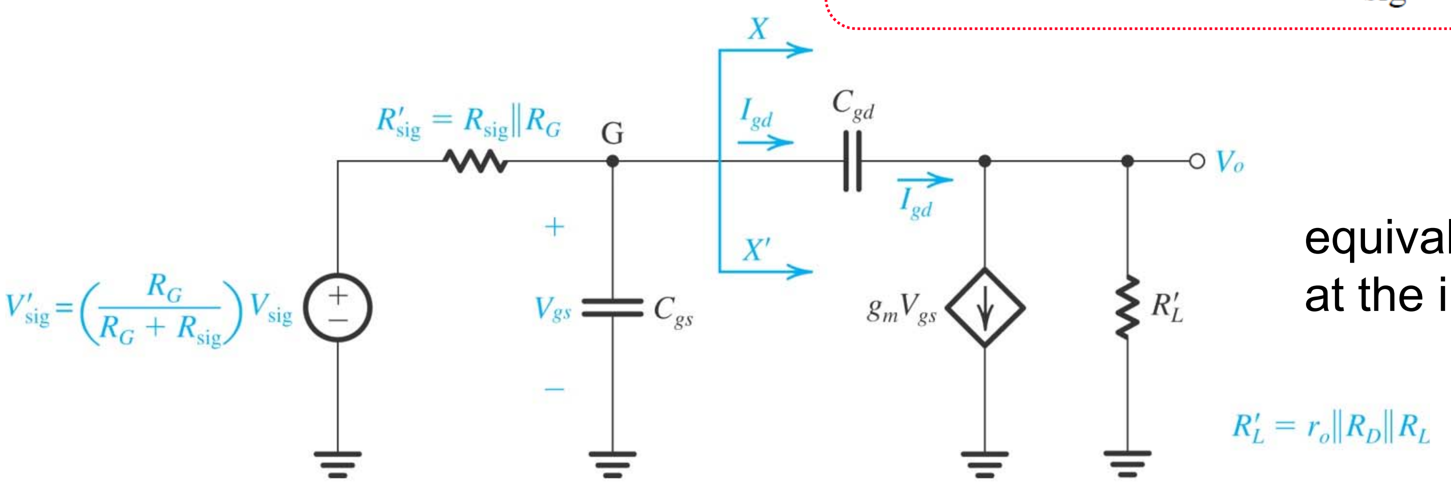
High Frequency Response



(a)

equivalent circuit

Mid-band gain: $A_M = \dfrac{V_o}{V_{sig}} = -\dfrac{R_G}{R_G + R_{sig}}(g_m R_L')$

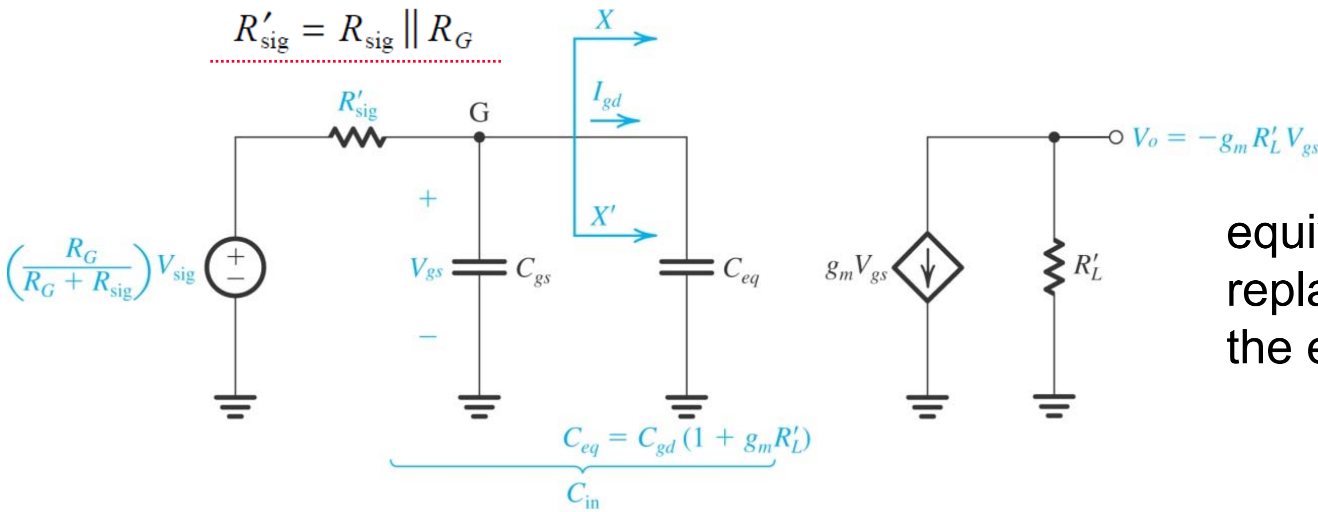


(b)

equivalent circuit simplified at the input and the output

High Frequency Response

$$R'_{sig} = R_{sig} \parallel R_G$$

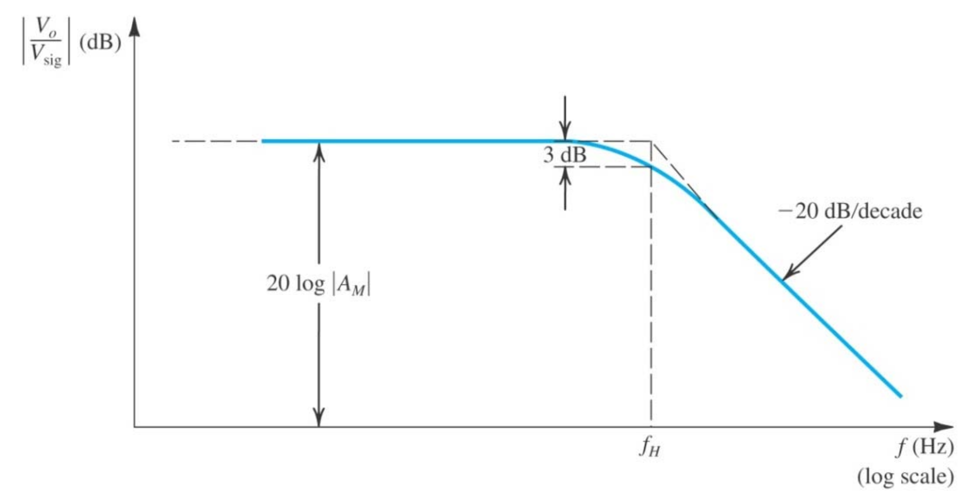


equivalent circuit with C_{gd} replaced at the input side with the equivalent capacitance C_{eq}

$$C_{in} = C_{gs} + C_{eq} = C_{gs} + C_{gd}(1 + g_m R'_L)$$

$$f_H = \frac{1}{2\pi C_{in} R'_{sig}}$$

frequency response of a low-pass single-time-constant circuit.



Example

Find the midband gain A_M and the upper 3-dB frequency f_H of a CS amplifier fed with a signal source having an internal resistance $R_{sig} = 100\ k\Omega$. The amplifier has $R_G = 4.7\ M\Omega$, $R_D = R_L = 15\ k\Omega$, $g_m = 1\ mA/V$, $r_o = 150\ k\Omega$, $C_{gs} = 1\ pF$, and $C_{gd} = 0.4\ pF$.

Solution:

$$A_M = -\frac{R_G}{R_G + R_{sig}} g_m R_L'$$

where

$$R_L' = r_o \| R_D \| R_L = 150 \| 15 \| 15 = 7.14\ k\Omega.$$

$$g_m R_L' = 1 \times 7.14 = 7.14\ V/V$$

Thus,

$$A_M = -\frac{4.7}{4.7 + 0.1} \times 7.14 = -7\ V/V$$

The equivalent capacitance, C_{eq}, is found as

$$C_{eq} = (1 + g_m R_L') C_{gd}$$

$$= (1 + 7.14) \times 0.4 = 3.26\ pF$$

The total input capacitance C_{in} can be now obtained as

$$C_{in} = C_{gs} + C_{eq} = 1 + 3.26 = 4.26\ pF$$

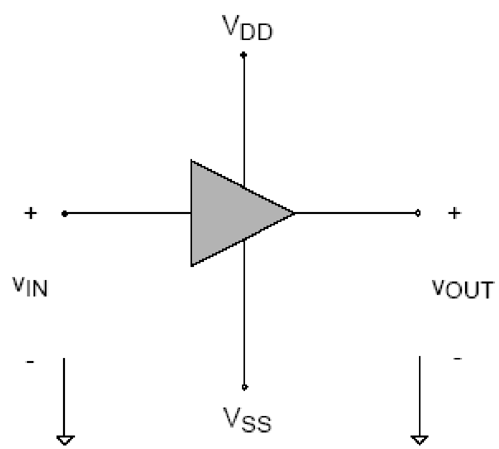
The upper 3-dB frequency f_H is found from

$$f_H = \frac{1}{2\pi C_{in}(R_{sig} \| R_G)} = \frac{1}{2\pi \times 4.26 \times 10^{-12} (0.1 \| 4.7) \times 10^6} = 382\ kHz$$

Differential amplifier

Disadvantages of single ended/stage transistor amplifier:

- Bias and gain sensitive to device parameters ($\mu C_{ox}, V_T$); sensitivity can be mitigated but often paying price in performance or cost (gain, power, device area, etc.)
- Vulnerable to ground and power-supply noise (in dense IC's there is cross-talk, 60 Hz coupling, substrate noise, etc.)
- Many signal sources exhibit "common-mode" drift that gets amplified.

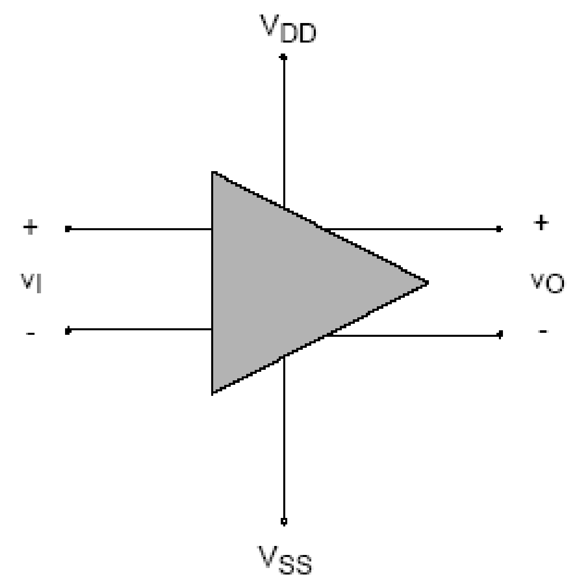


Differential amplifier

How to address the disadvantages of single-ended amplifier ?

- Represent signal by difference between two voltages:

- Differential amplifier:



amplifies difference between two voltages

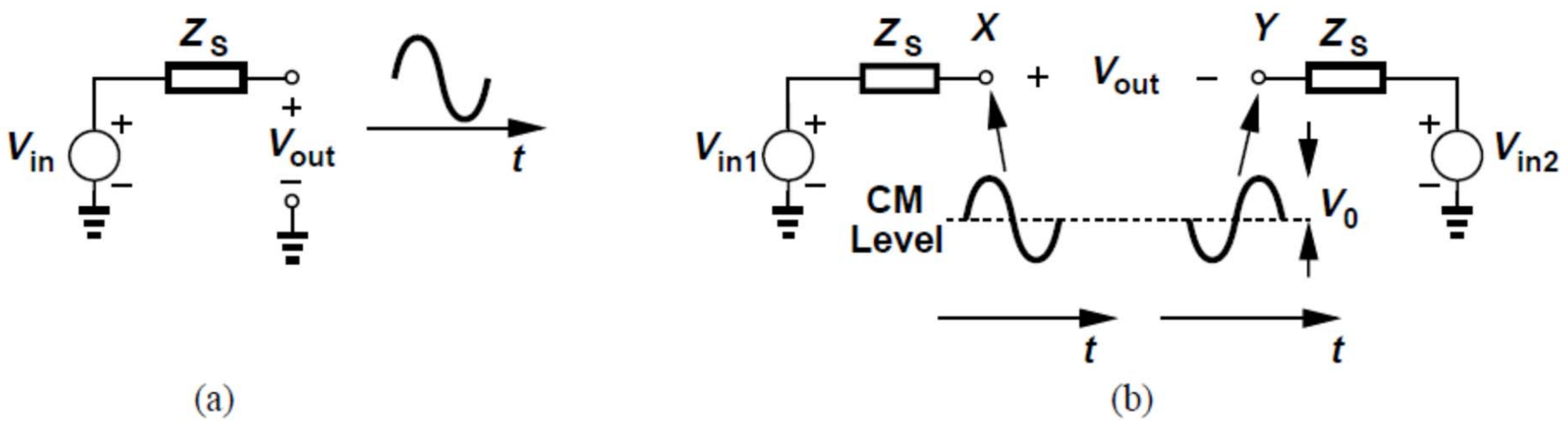
rejects components common to both voltages

Differential amplifier !

Single-Ended and Differential Operation

- Single-ended signal

  Signal measured with respect to a fixed potential (e.g. gnd)



- Differential signal

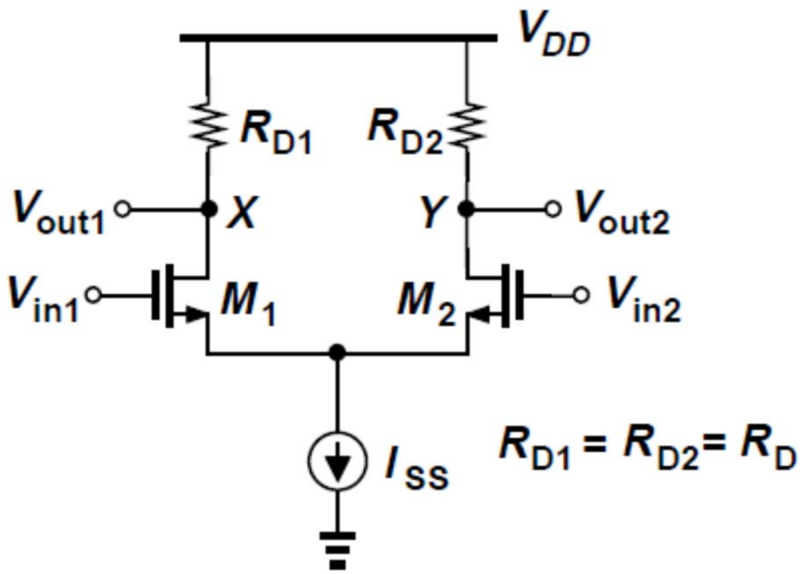
  Signal measured between two nodes that have equal and opposite signal excursions around a fixed potential

  Dotted line -> common-mode level

Common Mode $\boxed{v_c = \frac{v_1 + v_2}{2}}$

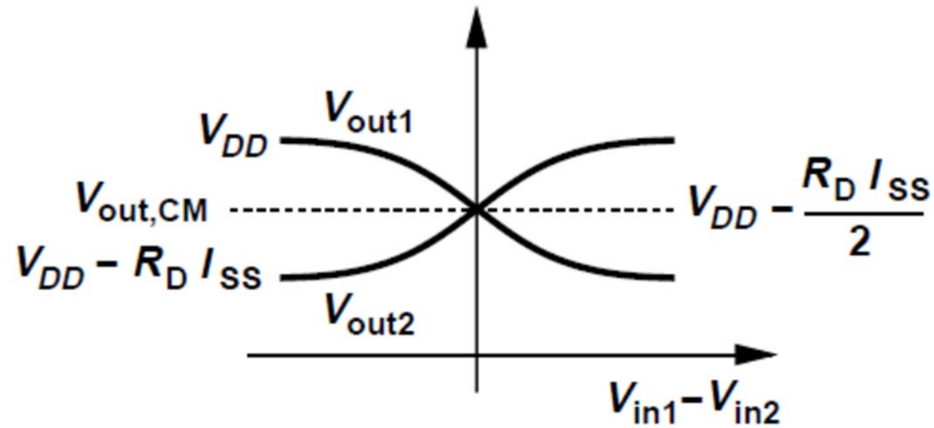
Differential Mode $\boxed{v_d = v_2 - v_1}$

Basic Differential Pair



- Two identical transistor M_1 and M_2, whose sources are connected together, are biased by a constant current source I_{SS}, which makes $I_{D1} + I_{D2}$ independent of $V_{in,CM}$
- If $V_{in1} = V_{in2}$, the bias current of both M_1 and M_2 is $I_{SS}/2$ and the output CM level is $V_{DD} – R_D I_{SS}/2$
- Assume that M_1 and M_2 are always biased in the saturation region.

Differential Pair – Qualitative Analysis

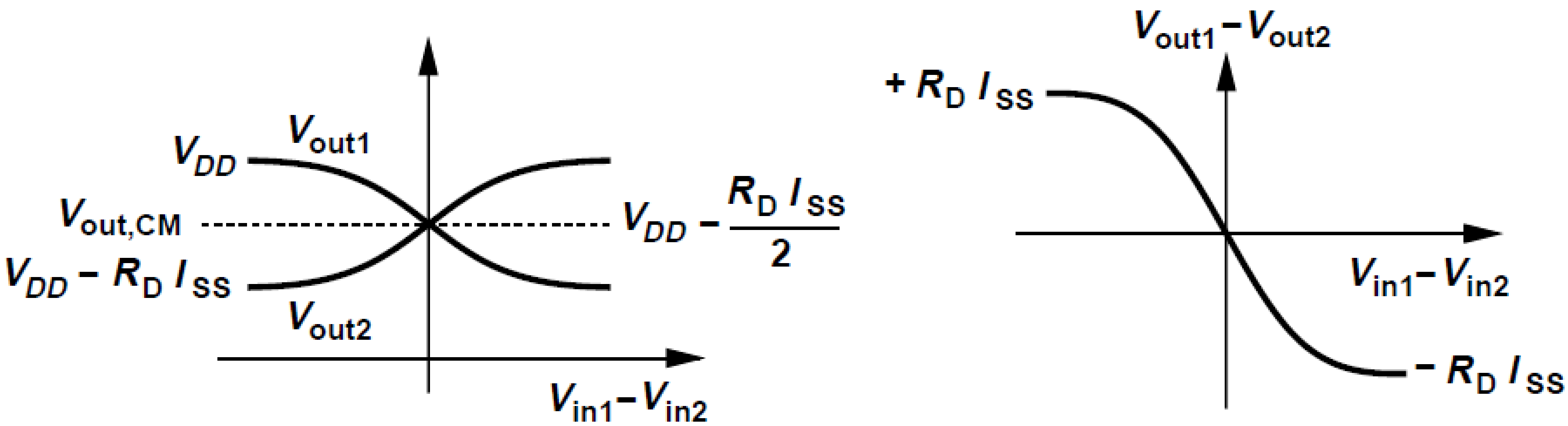


(a)

- Assume $-\infty < V_{in1} - V_{in2} < \infty$
- Case 1: V_{in1} more –ve than V_{in2}
  - M_1 off, M_2 on -> $I_{D2} = I_{SS}$
    - $V_{out1} = V_{DD}$
    - $V_{out2} = V_{DD} - I_{SS}R_{D2}$
- Case 2: As V_{in1} brought closer to V_{in2}
  - M_1 gradually turns on
    - Draws a fraction of I_{SS} from R_{D1} ($I_{SS} = I_{D1} + I_{D2}$), lowering V_{out1}
- Eventually, V_{in1} more +ve than V_{in2}
  - I_{SS} flows through M_1 (on), none through M_2 (off)
  - $V_{out2} = V_{DD}$
  - $V_{out1} = V_{DD} - I_{SS}R_{D1}$

For $V_{in1} = V_{in2}$, $V_{out1} = V_{out2} = V_{DD} - R_D I_{SS}/2$, which is the output CM level.

Cont'd …

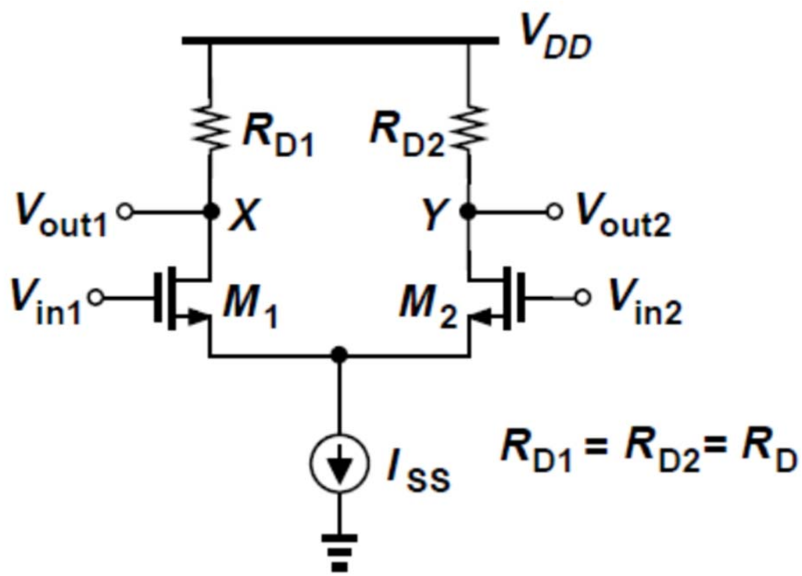


(a) (b)

Two important characteristics :

- Char 1: output's maximum and minimum levels well-defined (V_{DD} and V_{DD}-$R_D I_{SS}$), independent of input CM level
- Char 2: small-signal gain (slope of V_{out1}-V_{out2} vs. V_{in1}-V_{in2}) is maximum for V_{in1}=V_{in2}
    - Gradually falling to zero as |V_{in1}-V_{in2}| increases
        - i.e. circuit becomes more nonlinear as input voltage swing increases
        - Circuit is in equilibrium when V_{in1}=V_{in2}

Small-signal (input) differential voltage gain

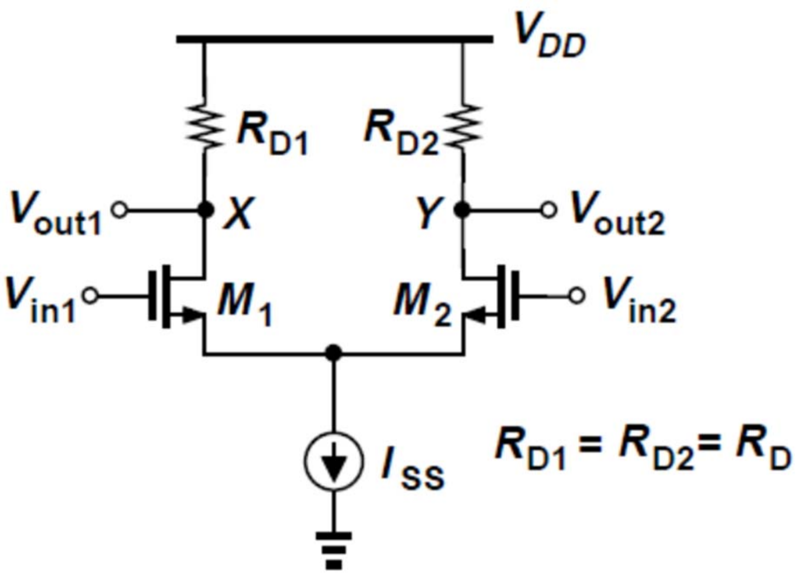


- For $|\Delta V_{in}| \approx 0$ (sufficiently small) we have:

$$|A_V| = \frac{\Delta V_{out}}{\Delta V_{in}} = G_{m,\max} R_D = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}\, R_D = g_m R_D$$

where $G_m = \frac{\partial \Delta I_D}{\partial \Delta V_{in}}$ *and* g_m *is that of a NMOS with a current of* $I_{SS}/2$.

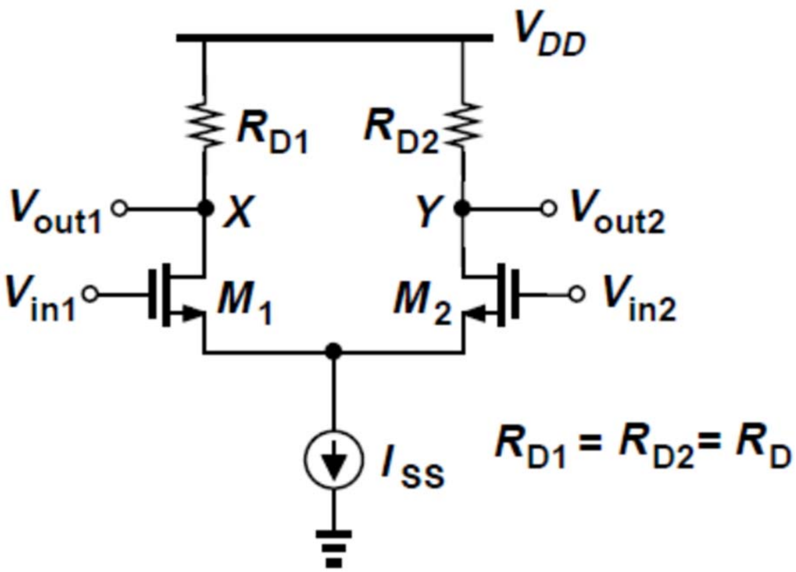
Single-ended differential voltage gain



$$A_{V,SE} = \frac{V_X}{V_{in1} - V_{in2}} = -\frac{g_m}{2} R_D$$

$$A_{V,SE} = \frac{V_Y}{V_{in1} - V_{in2}} = \frac{g_m}{2} R_D$$

Common-mode (input) gains



$A_{V,CM}$: Single-ended output due to CM signal.

$$A_{V,CM} = \frac{V_X}{V_{in,CM}} = \frac{V_Y}{V_{in,CM}}$$

$A_{V,CM\text{-}DM}$: Differential output due to CM signal.

$$A_{V,CM-DM} = \frac{V_X - V_Y}{V_{in,CM}}$$

$V_{in1} - V_{in2} = 0$ or $V_{in1} = V_{in2} = V_{CM}$

Common mode (CM)

Common-mode rejection ratio (CMRR)

- Common mode rejection ratio (*CMRR*) $$CMRR = \left|\frac{A_{vD}}{A_{vC}}\right|$$

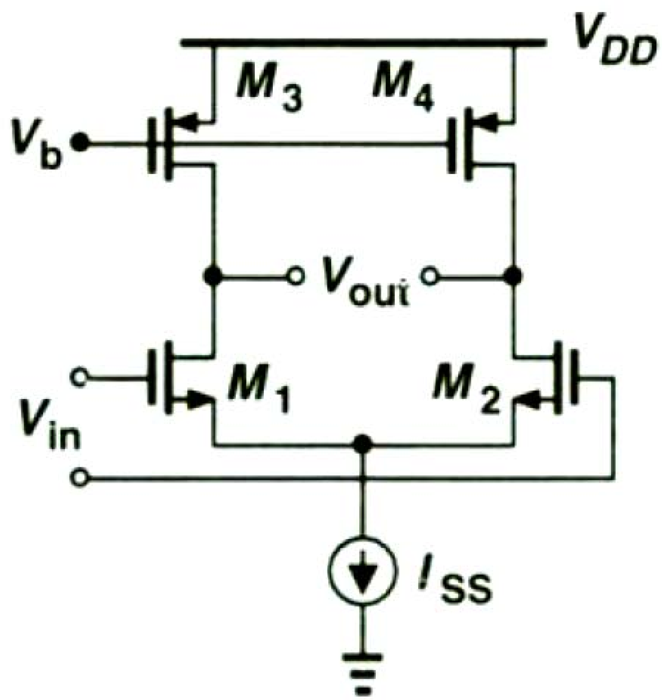
  CMRR is a measure of how well the differential amplifier rejects the common-mode input voltage in favor of the differential-input voltage.

Single ended: $$CMRR = CMRR_{SE} = \left|\frac{A_{DM}}{A_{CM}}\right|$$

Differential: $$CMRR = CMRR_{diff} = \left|\frac{A_{DM}}{A_{CM-DM}}\right|$$

In both cases we want CMRR to be as large as possible, and it translates into small matching errors and R_{SS} as large as possible

Differential pair with active loads



M_3 and m_4 are PMOS current sources

(active loads)

$$A_v = -g_{mN}\left(r_{oN} \| r_{oP}\right) = -g_{m1}\left(r_{o1} \| r_{o3}\right)$$

Acknowledgments

- Lecture slides are based on lecture materials from various sources, including book "Microelectronic Circuits" by Sedra and Smith (Oxford Publishing), and, Nikolay Tchamov and Ivan Uzunov (Tampere University of Technology).

- Credit is acknowledged where credit is due. Please refer to the full list of references.