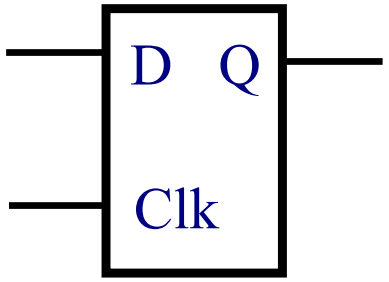
Lecture 10
Clock & Timing

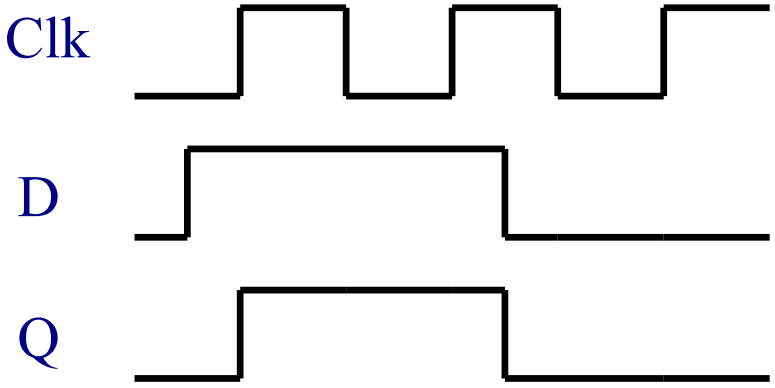
Learning outcomes

- Define timing parameters for latches and flip-flops.
- Determine the maximum clock operating frequency period for which a synchronous circuit is not subject to setup time violations.
- Identify hold-time violations in a sequential circuit.
- Define metastability and discuss mitigation strategies.
- Define clock skew and jitter.

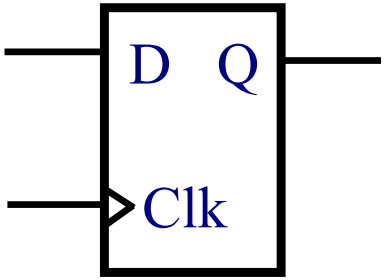
Latches vs Flip-Flops

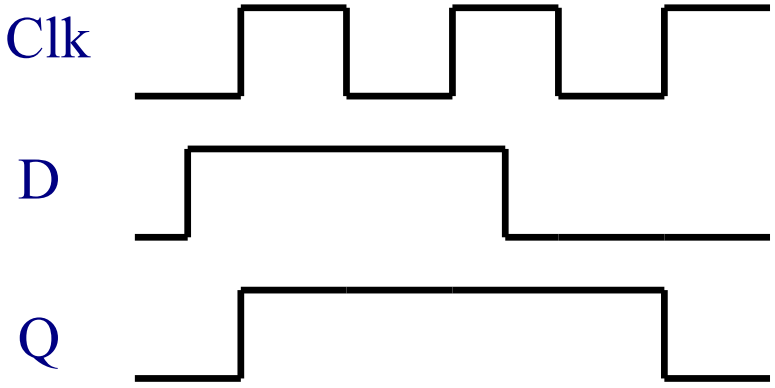
- Latch stores data when clock is high (or low)





- Flip-flop stores data when clock rises (or falls)



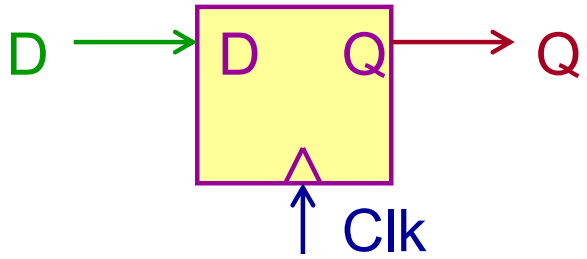


Latches vs Flip-flops

- Latches
  - level sensitive circuit that passes inputs to Q when the clock is high (or low) - transparent mode
  - input sampled on the falling edge of the clock is held stable when clock is low (or high) - hold mode

- Flip-flops (edge-triggered)
  - edge sensitive circuits that sample the inputs on a clock transition
    - positive edge-triggered: $0 \rightarrow 1$
    - negative edge-triggered: $1 \rightarrow 0$
  - built using latches (e.g., master-slave flipflops)

Racing the clock



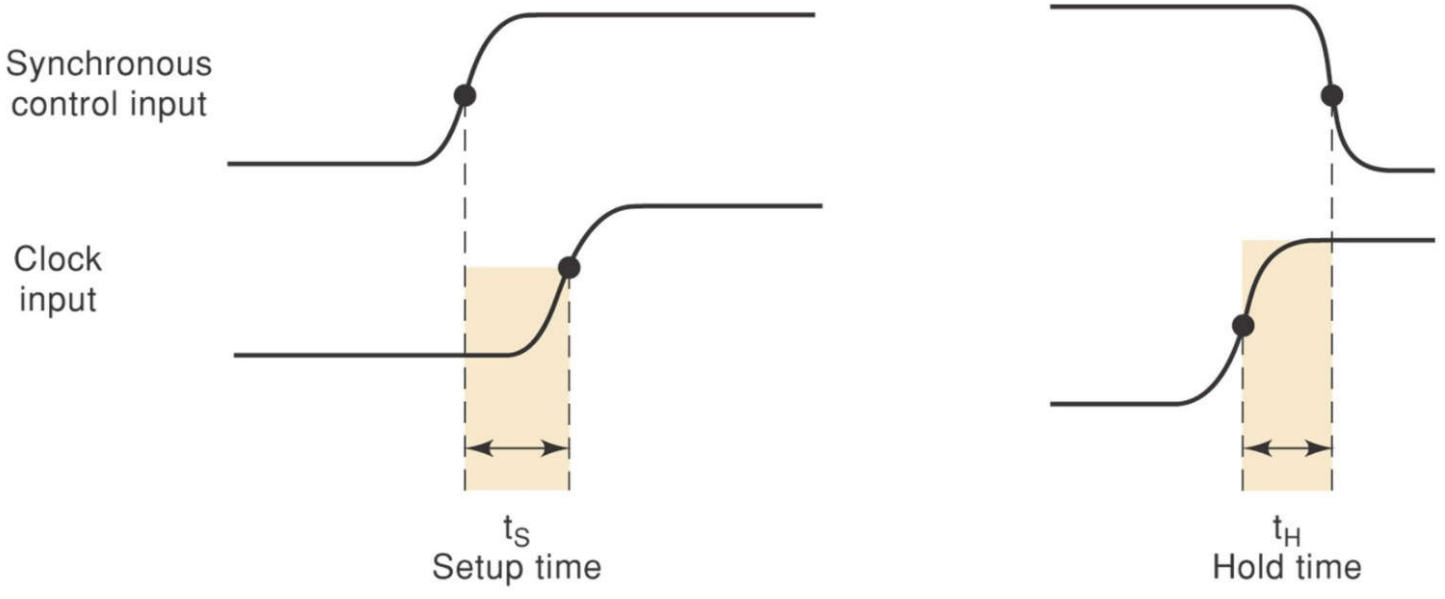
Real signals don't change instantly

D is changing during the rising edge of Clk. Is a '1' or '0' clocked in?

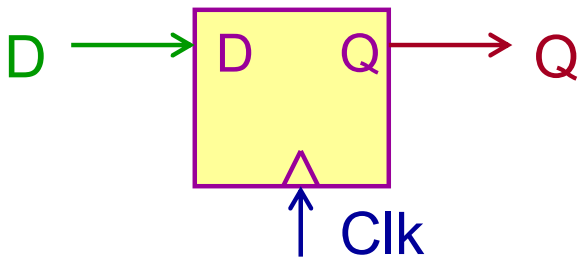
D is changing right after the rising edge of Clk. Is a '1' or '0' clocked in?

Setup and Hold Times

- Two timing requirements must be met if a clocked FF is to respond reliably to its control inputs when the active CLK transition occurs.
- The setup time is the time interval immediately preceding the active transition of the CLK signal during which the control input must be maintained at a proper level. IC manufacturers usually specify the minimum allowable t_s(min). Typical range is 5 to 50ns.
- The hold time the time interval immediately following the active transition of the CLK signal during which the control input must be maintained at a proper level. IC manufacturers usually specify the minimum acceptable value of hold time t_H(min). Typical range is 0 to 10ns.

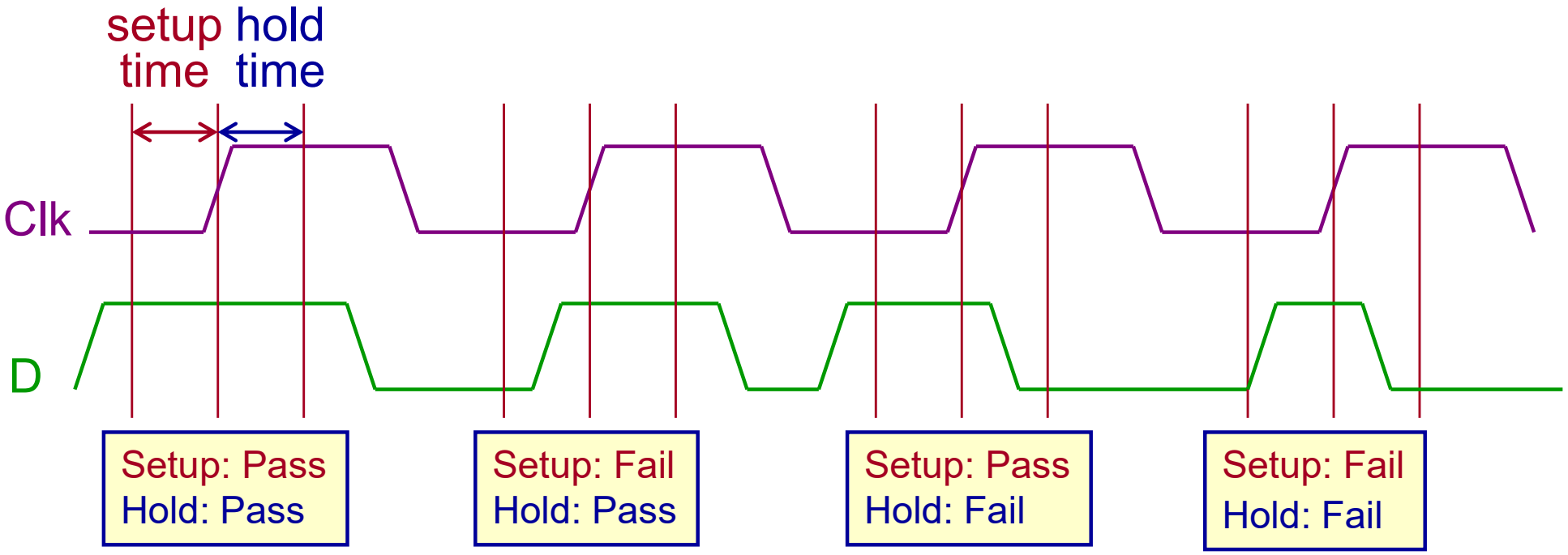


Setup and Hold Times



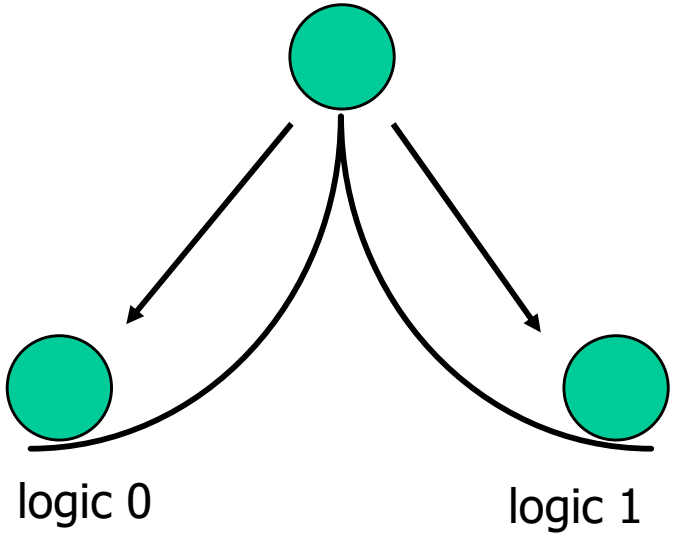
Setup Time: How long a signal must be stable preceding the clock edge

Hold Time: How long a signal must be stable after the clock edge

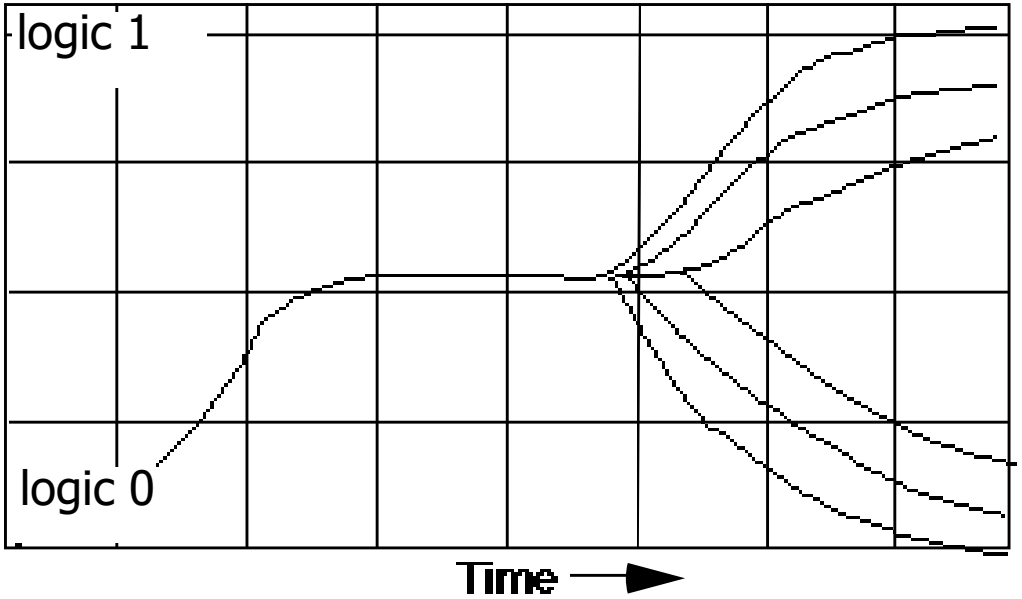


Metastability: synchronization Failure

- Occurs when FF input changes close to clock edge
  - FF may enter a metastable state – neither a logic 0 nor 1 –
  - May stay in this state an indefinite amount of time
  - Is not likely in practice but has some probability



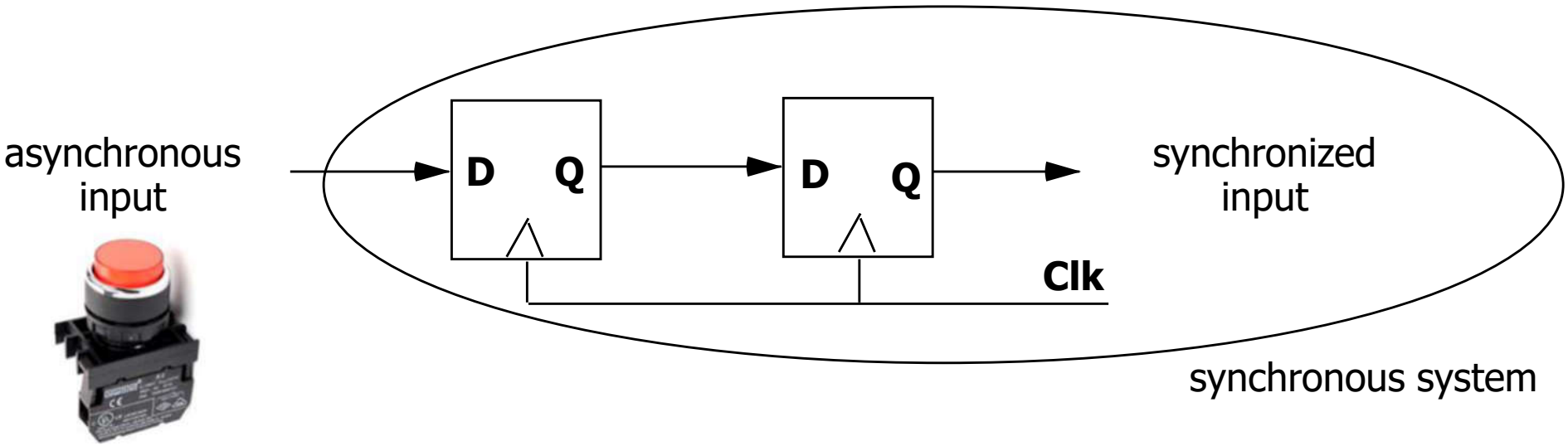
small, but non-zero probability that the FF output will get stuck in an in-between state



oscilloscope traces demonstrating synchronizer failure and eventual decay to steady state

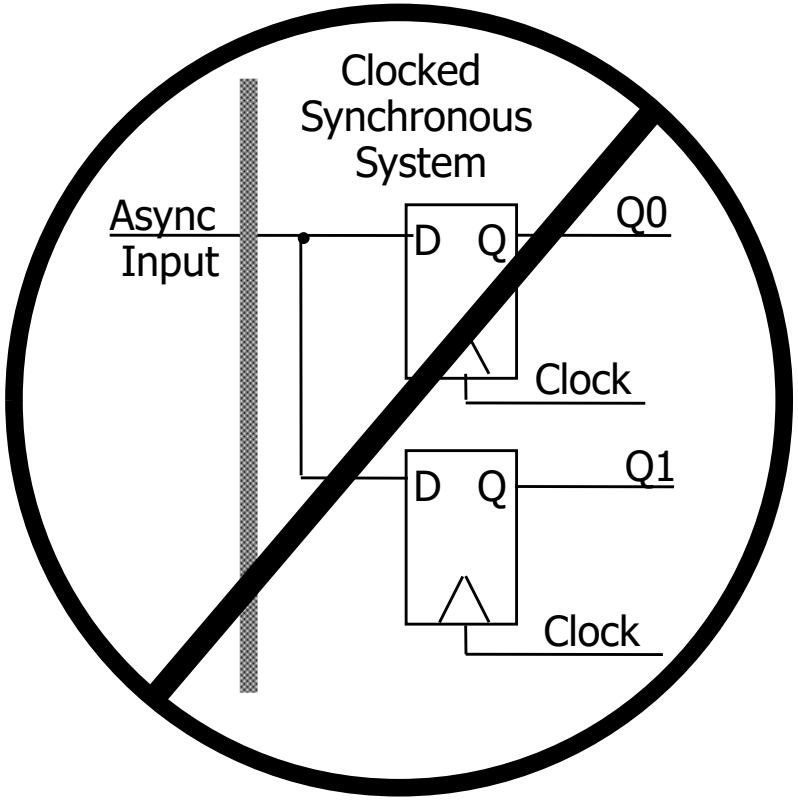
Dealing with Synchronization Failure

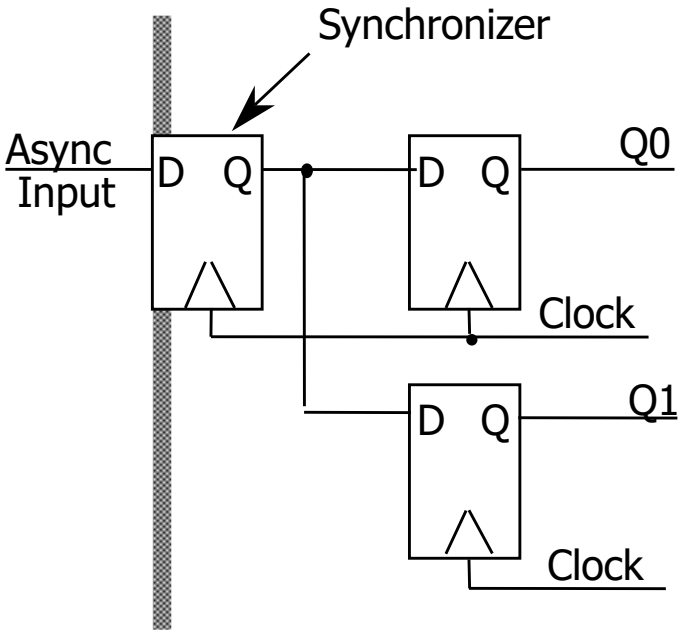
- Asynchronized external input signal is not synchronized to the CLK signal and may violate setup/hold time constraints.
- Probability of failure can never be reduced to 0, but it can be reduced
  - slow down the system clock: this gives the synchronizer more time to decay into a steady state; synchronizer failure becomes a big problem for very high speed systems.
  - use fastest possible logic technology in the synchronizer: this makes for a very sharp "peak" upon which to balance
  - cascade two synchronizers: this effectively synchronizes twice (both would have to fail)



Handling Asynchronous Inputs

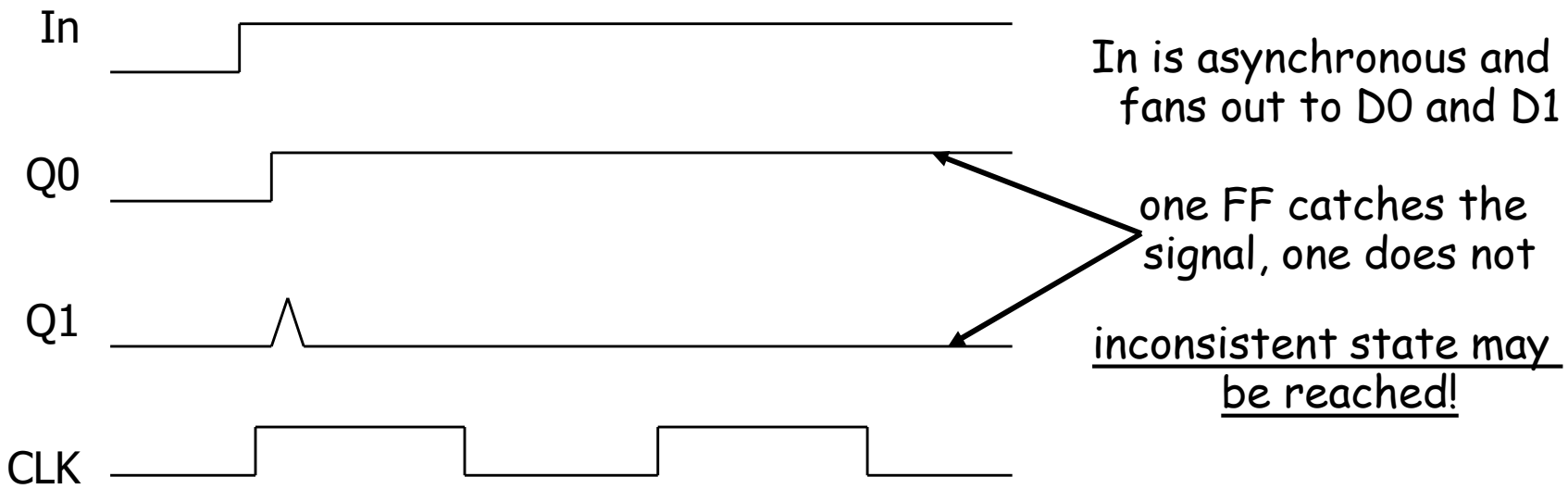
- Never allow asynchronous inputs to fan-out to more than one flip-flop
  - Synchronize as soon as possible and then treat as synchronous signal





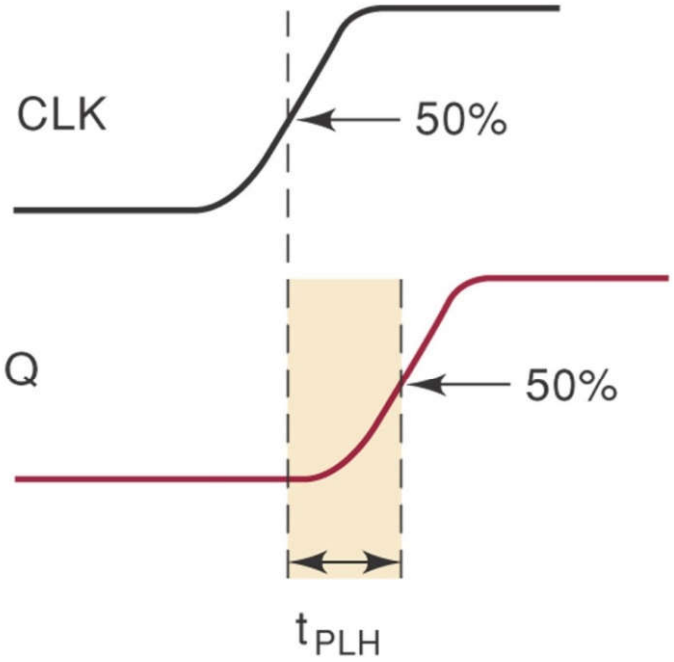
Handling Asynchronous Inputs (cont'd)

- What can go wrong?
  - Input changes too close to clock edge (violating setup time constraint)

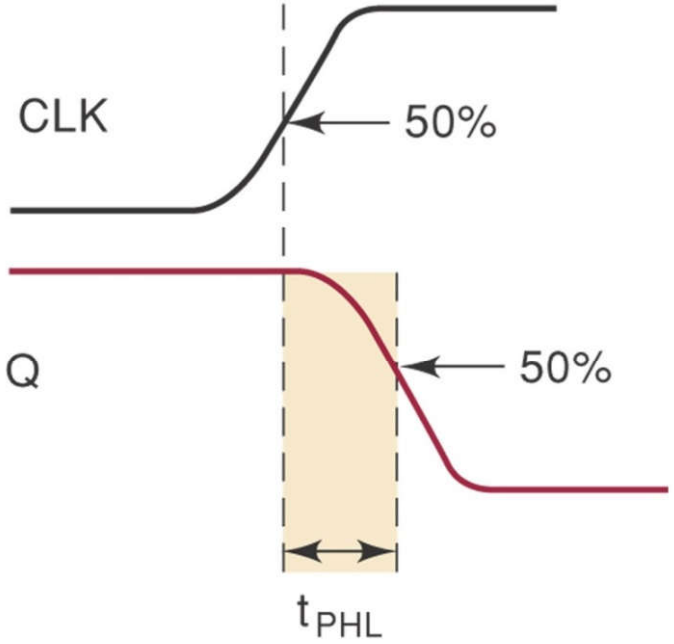


Propagation Delays t_{C-Q}

- Whenever a signal is to change the state of a FF's output, there is a delay from the time the signal is applied to the time when the output makes its change.
- These delays are measured between the 50% points on the input and output waveforms. The manufacturers's data sheets usually specify the maximum values for t_{pHL} and t_{pLH}. Typical range from a few ns to around 100ns.

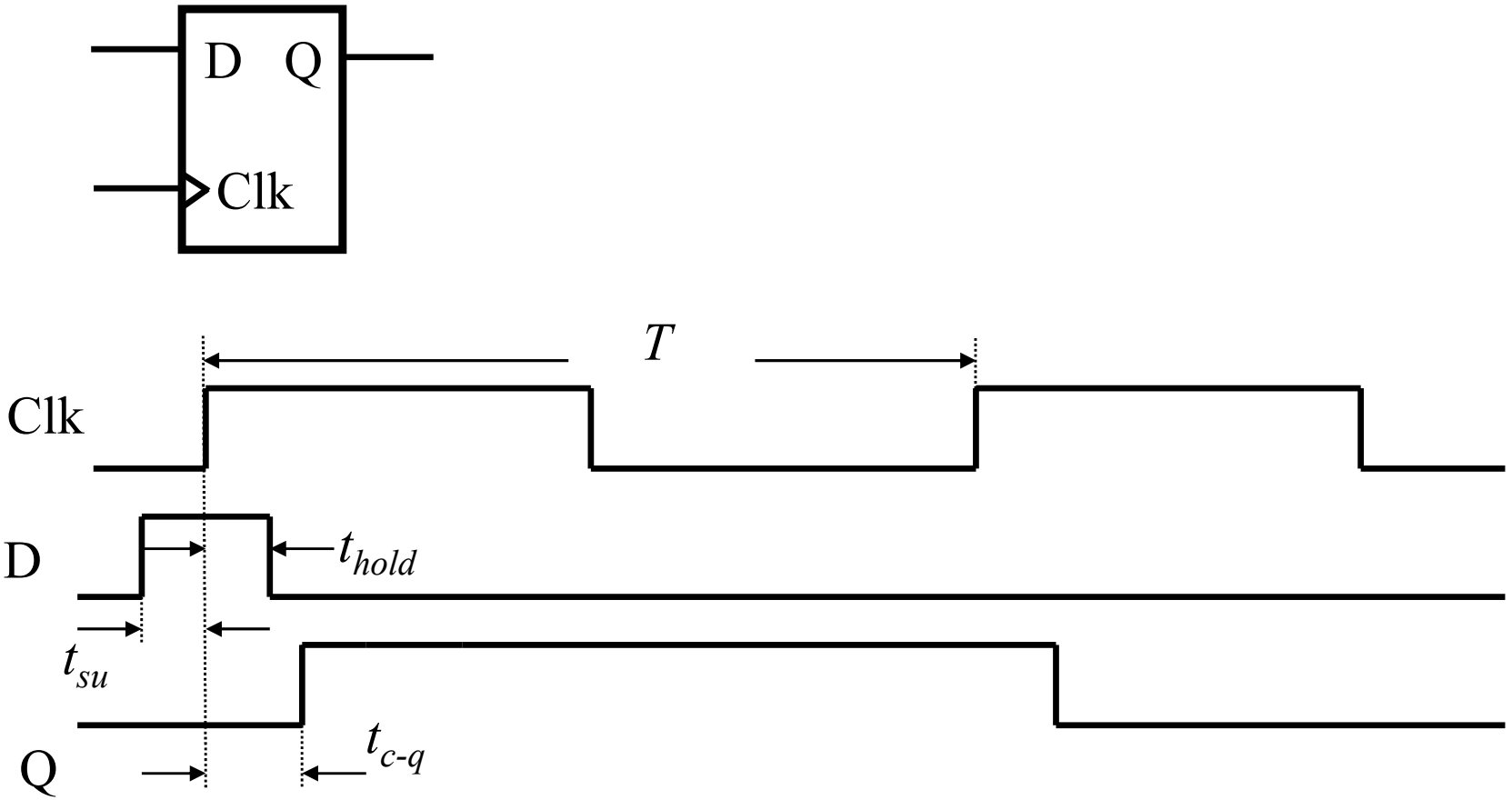


Delay going from LOW to HIGH



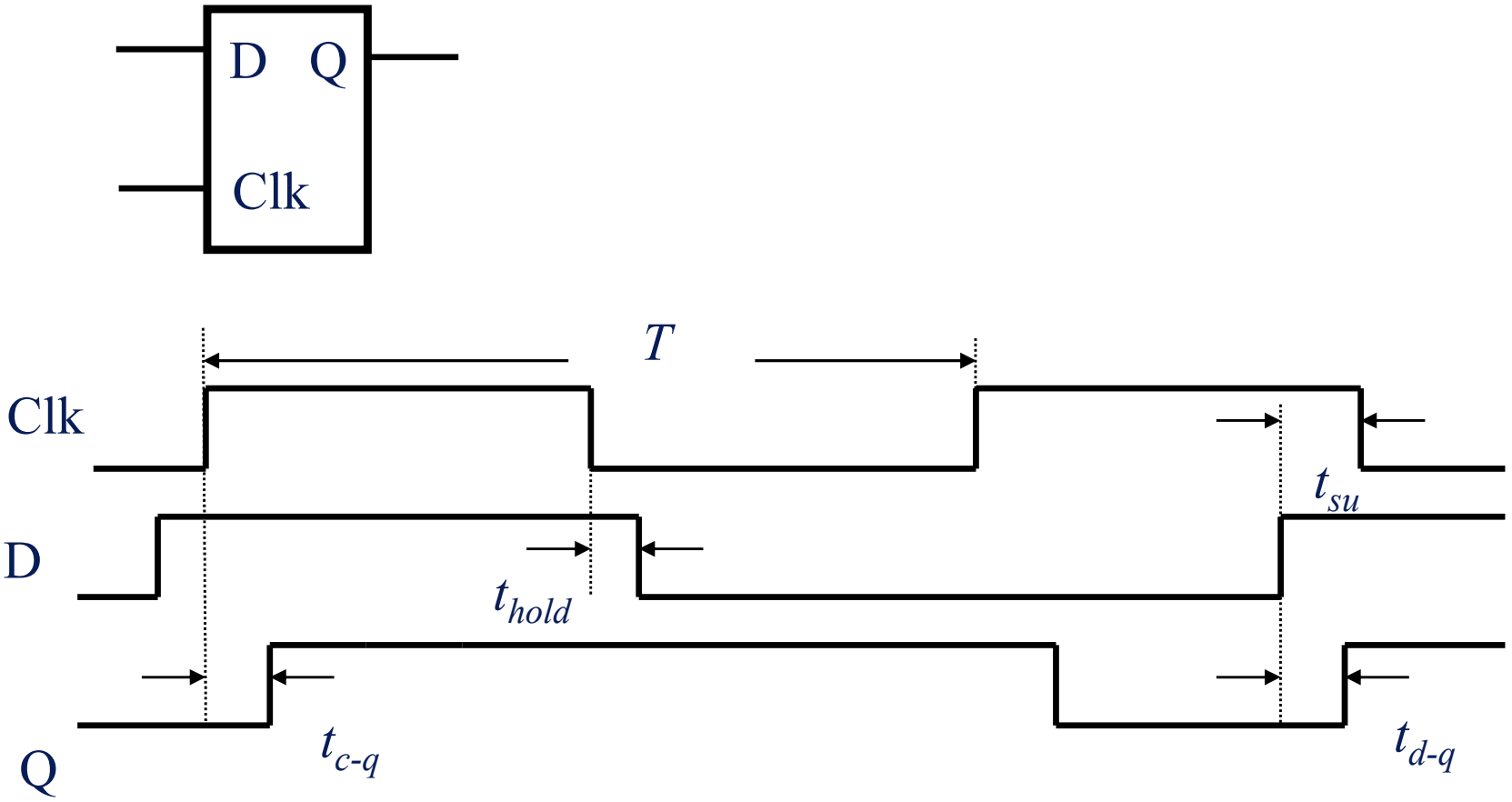
Delay going from HIGH to LOW

Flip-Flop Parameters



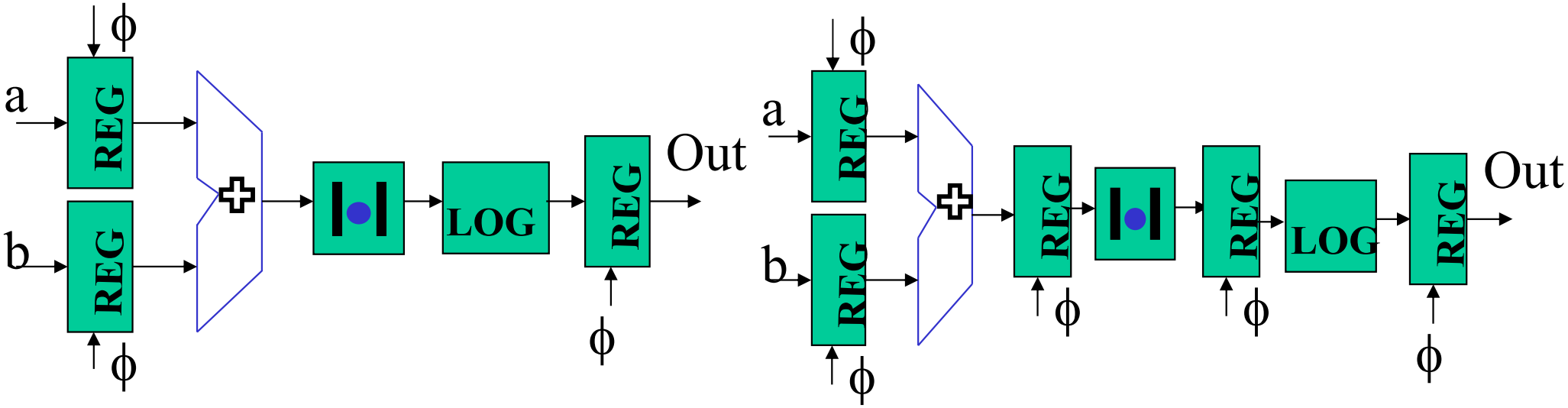
Delays can be different for rising and falling data transitions

Latch Parameters



Delays can be different for rising and falling data transitions

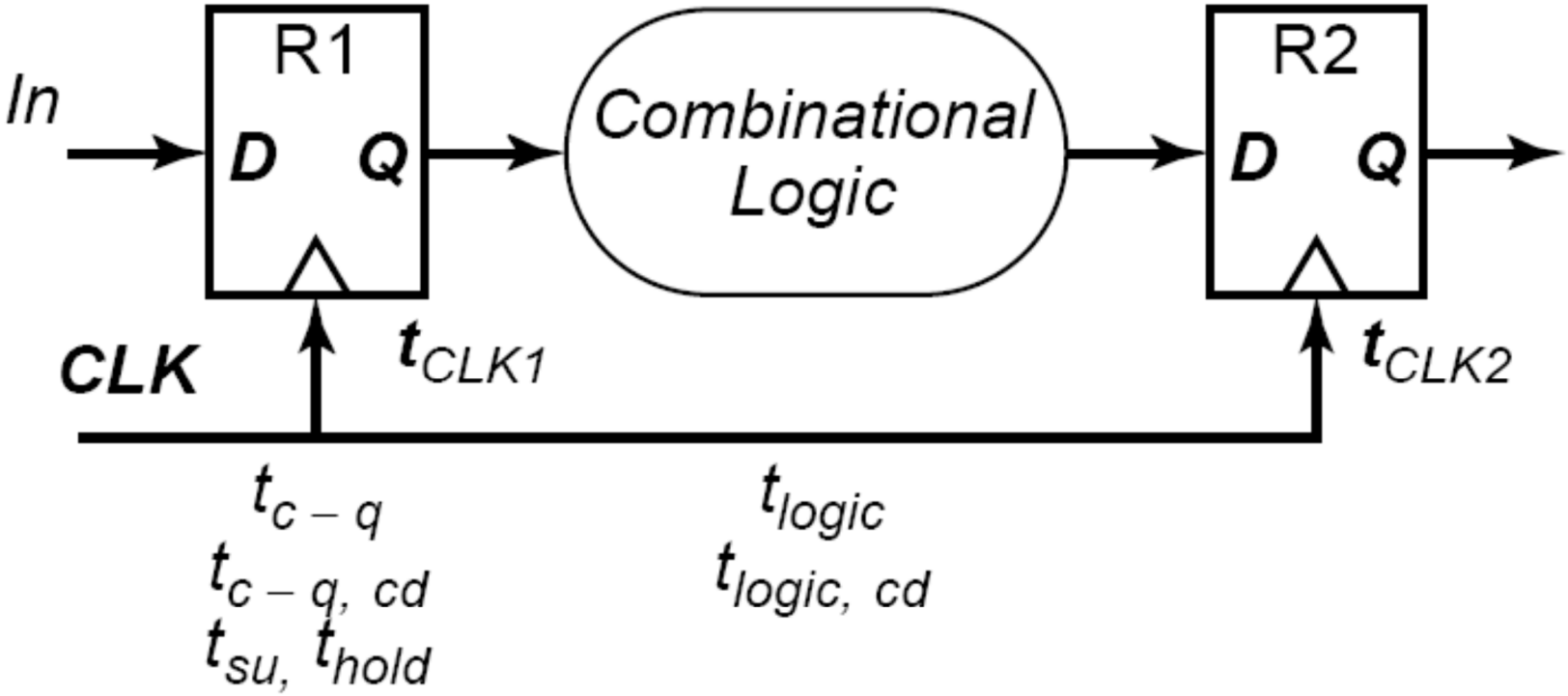
Pipelining



Using memory to pipeline the system enables new operations to start before the old ones are completed.

Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\lvert a_1 + b_1 \rvert$	
3	$a_3 + b_3$	$\lvert a_2 + b_2 \rvert$	$\log(\lvert a_1 + b_1 \rvert)$
4	$a_4 + b_4$	$\lvert a_3 + b_3 \rvert$	$\log(\lvert a_2 + b_2 \rvert)$
5	$a_5 + b_5$	$\lvert a_4 + b_4 \rvert$	$\log(\lvert a_3 + b_3 \rvert)$

Timing Constraints

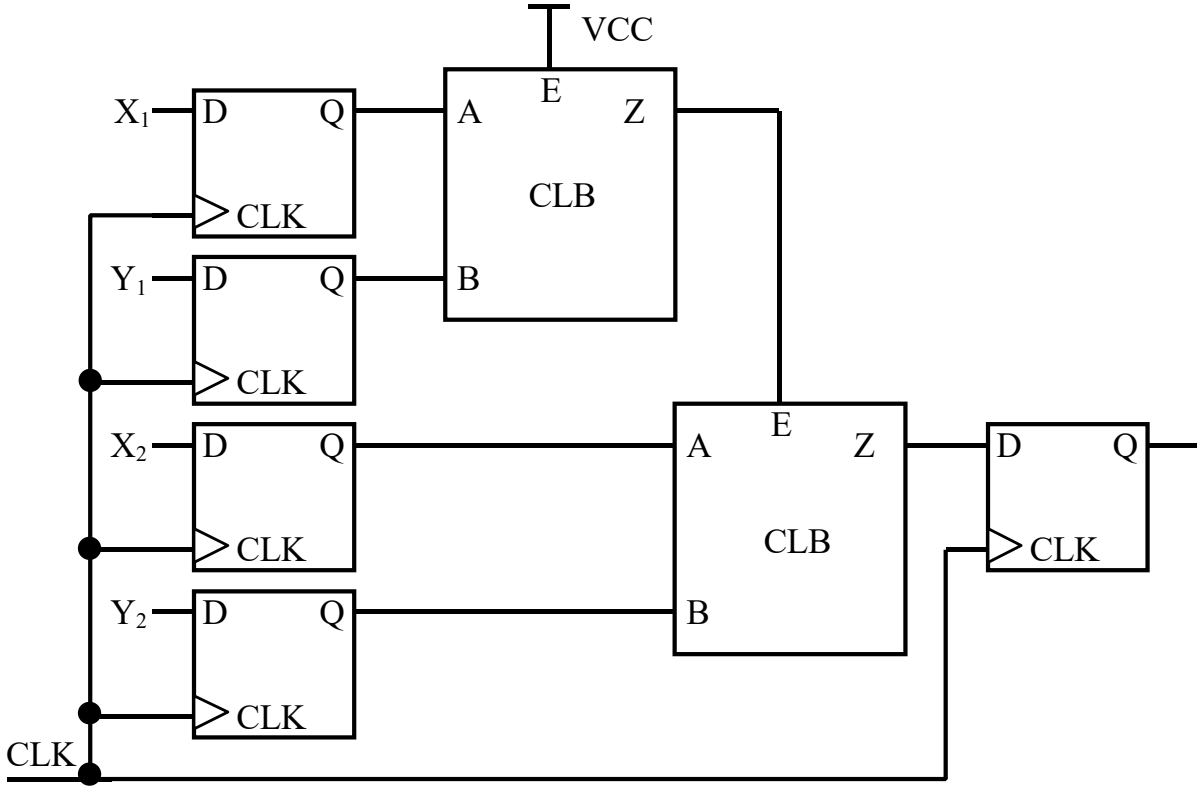


$$\text{Cycle time: } T_{Clk} > t_{c\text{-}q} + t_{logic} + t_{su}$$

$$\text{Race margin: } t_{hold} < t_{c\text{-}q,cd} + t_{logic,cd}$$

Maximum clock frequency

The circuit below takes two inputs, X and Y, each two bits wide, registers them in D-type flip-flops, performs some combinatorial logic on the values, and registers the result in a D-type flip-flop.

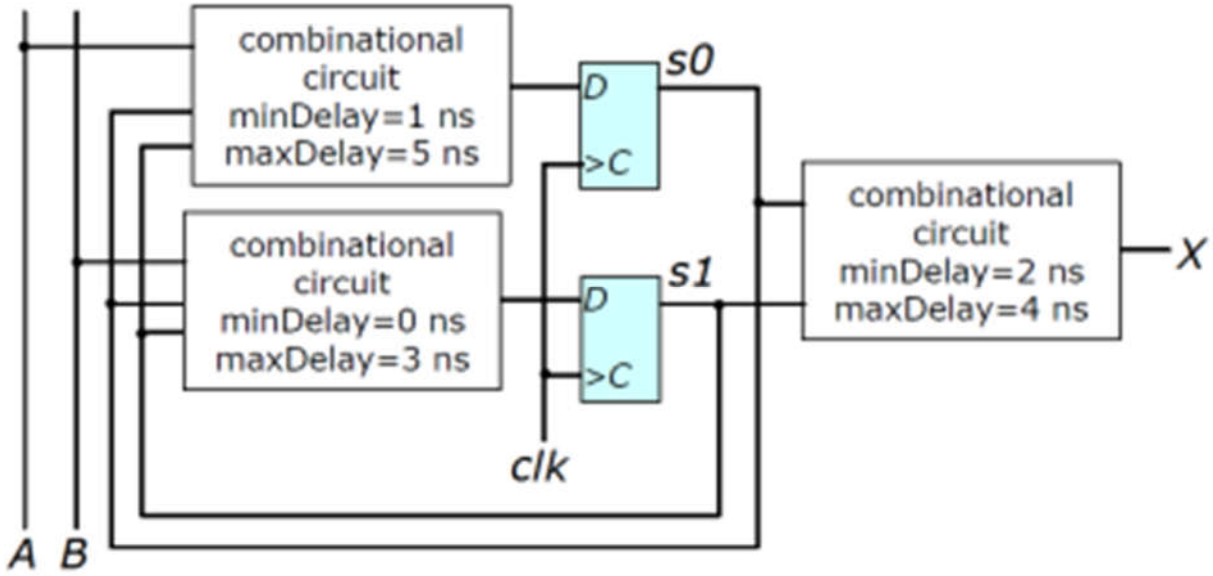


The combinatorial logic is performed in two stages on the low order bits and high order bits of X and Y using two identical combinatorial logic blocks (CLB).

Component	Parameter	Symbol	Min	Typical	Max
D-type flip-flop	Propagation delay (Clock to output)	t_{CO}	25ns	28ns	35ns
	Set-up time	t_S	10ns	12ns	15ns
	Hold time	t_H	3ns	3ns	3ns
CLB	Propagation delay Inputs A or B to output Z	t_{PABZ}	34ns	43ns	51ns
	Propagation delay Input E to output Z	t_{PEZ}	25ns	31ns	38ns

Practice problem 2

- For the state machine shown below, assume that the flip flop setup time is 2 ns, the hold time is 0.5 ns and the flip flop propagation delay is between 1 and 3 ns.



1. Is this circuit subject to internal hold time violations? Assume inputs A & B are constant.

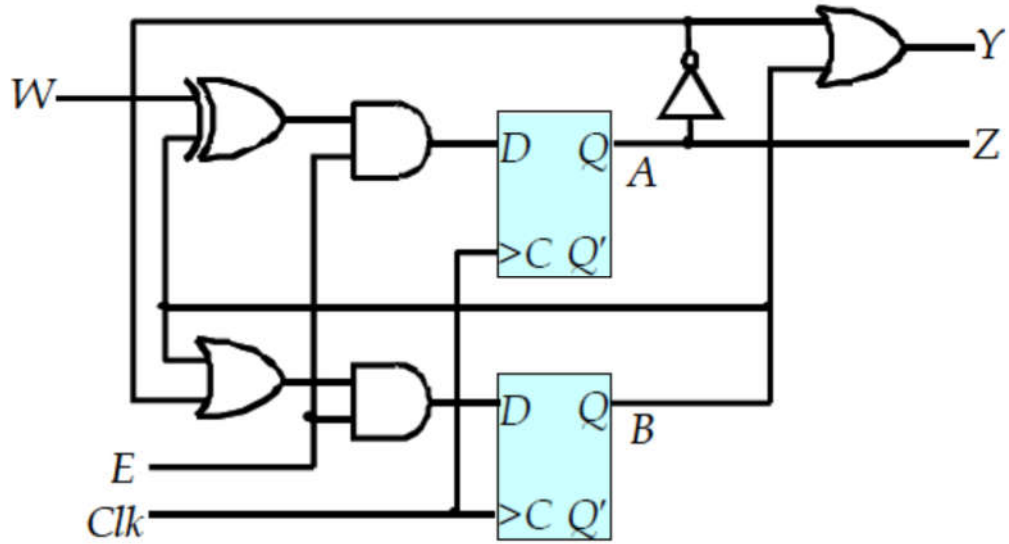
2. What is the smallest clock period for which the circuit is not subject to setup time violations? Assume inputs A & B are constant.

3. What is the latest time before the occurrence of the clock edge, when it is safe for input *B* to change? Assume input A is constant.

4. What is the latest time after the clock edge when output *X* can be changing?

Practice problem 3

- Consider the following circuit, with the following data given: setup time=2ns, hold time=2 ns, flip-flop propagation delay=1 to 3 ns, gate delay= 0.4 to 1.5 ns.

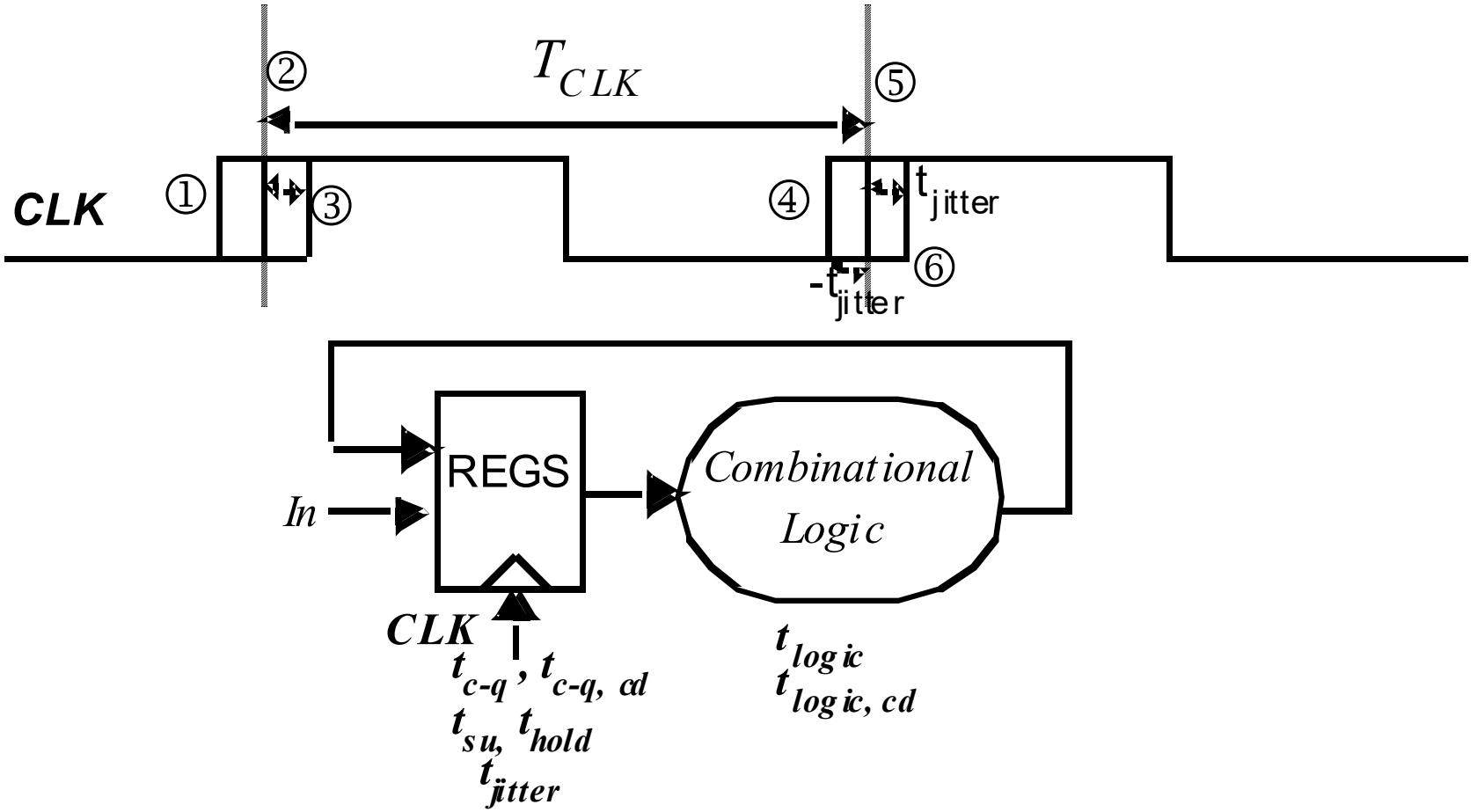


1. Do we have a hold time violations? If so, how can we eliminate them? Assume inputs E and W are constant.
2. What is the smallest clock period for which we do not have setup time violations? Assume inputs E and W are constant.
3. Assume the clock becomes high at t=0, over what time period must W be stable to avoid setup or hold time violations? Assume input E is constant. Same question for input E assuming e input W is constant?
4. Assume the clock becomes high at t=0, over what time period can Y experience a change? Same question for output Z? Assume inputs E and W are constant.

Clock Non-idealities

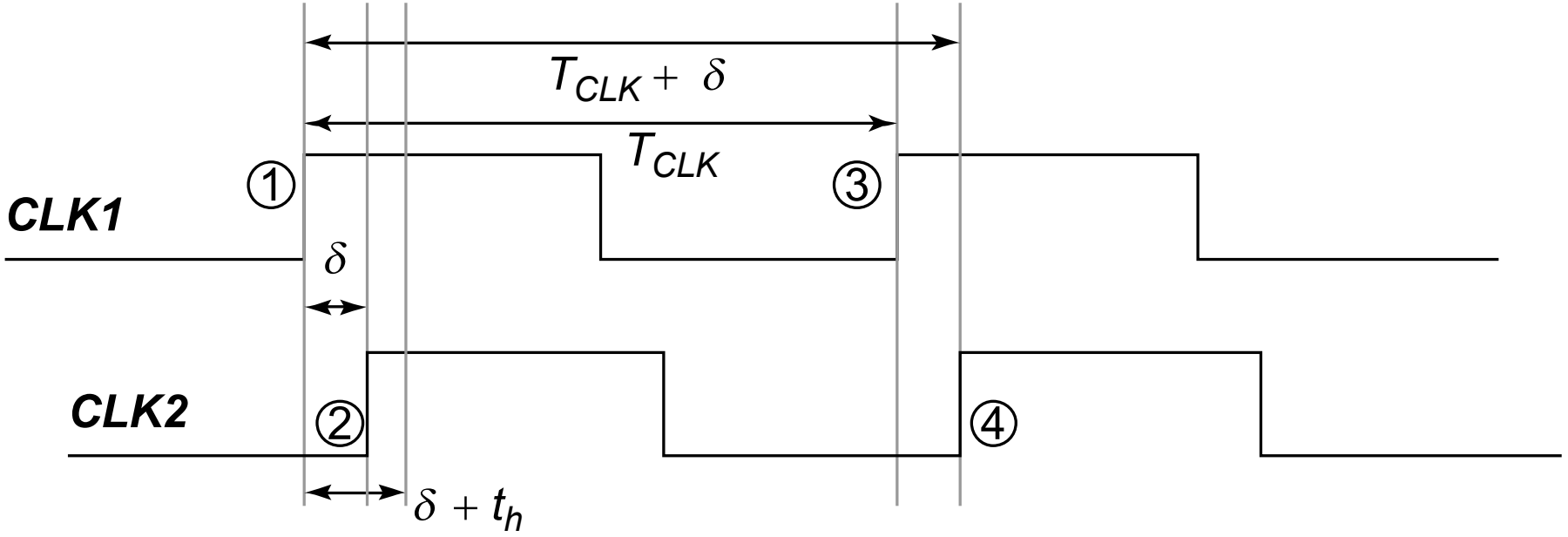
- Under real conditions, the clock signal can have both spatial (clock skew) and temporal (clock jitter) variations
- Clock skew
  - Spatial variation in temporally equivalent clock edges; Skew is constant from cycle to cycle. (by definition); skew can be positive (clock and data flowing in the same direction) or negative (clock and data flowing in opposite directions)
- Clock jitter
  - Temporal variations in consecutive edges of the clock signal; Jitter causes T to change on a cycle-by-cycle basis
- Clock skew and jitter can ultimately limit the performance of a digital system, so designing a clock network that minimizes both is important

Clock Jitter

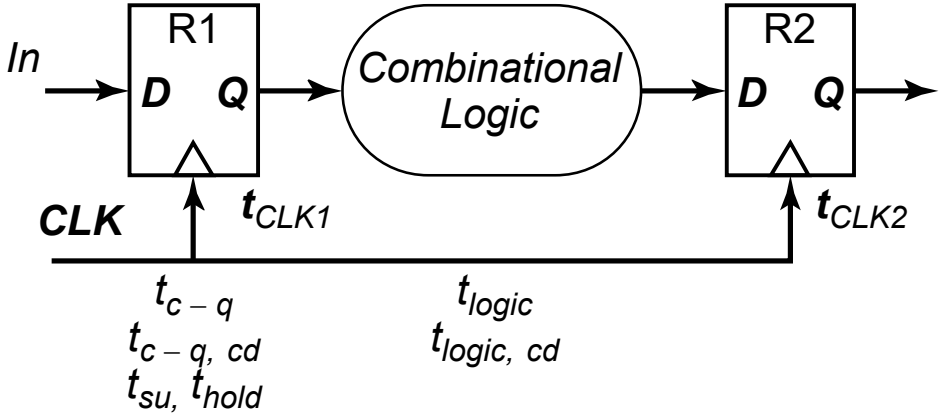


Temporal variation in the clock edge.

Positive Skew

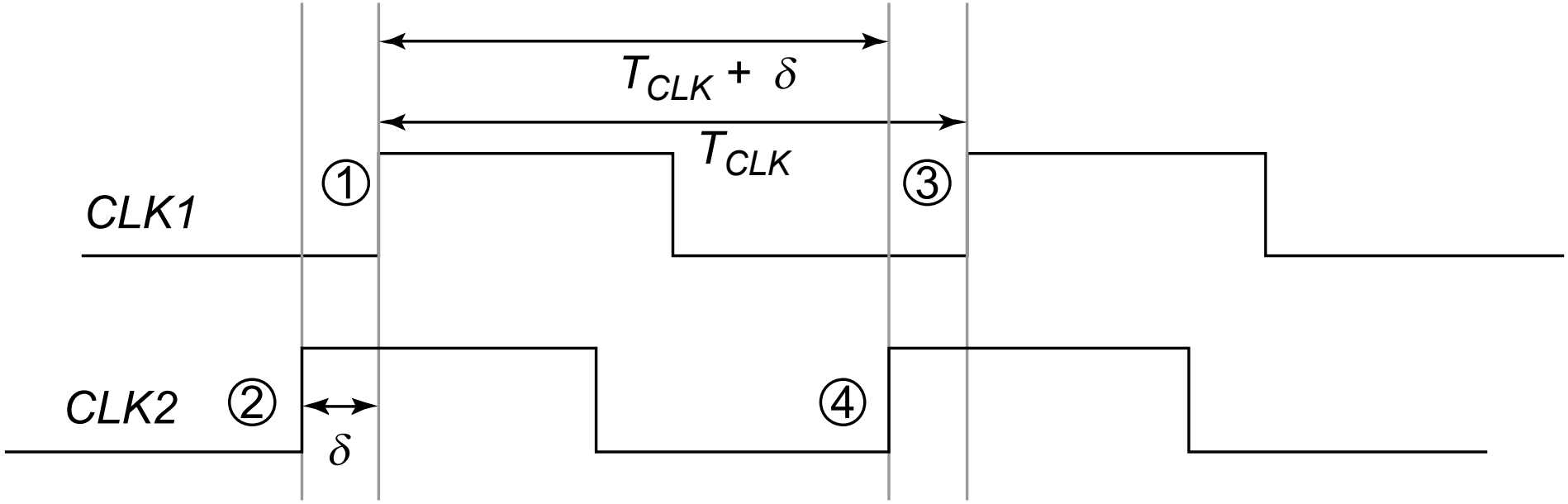


Positive skew: clock is routed in the same direction of the data flow.

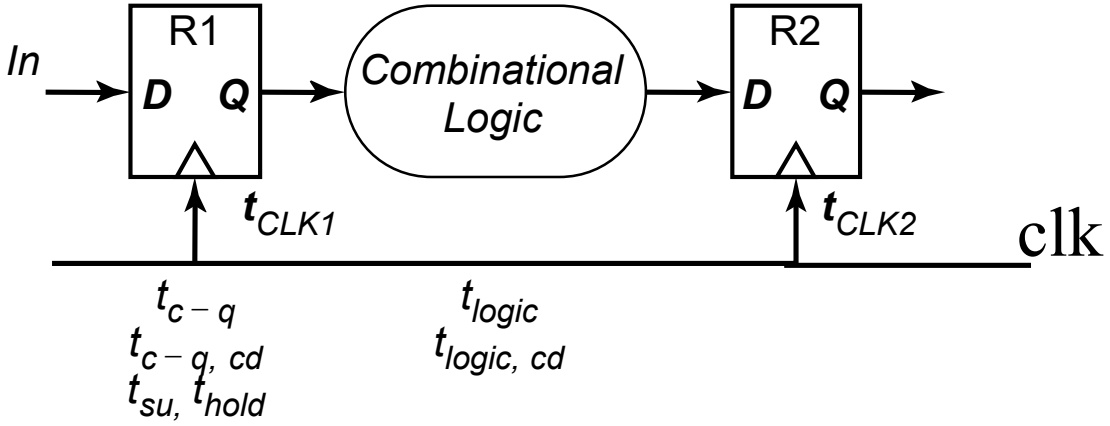


Launching edge arrives before the receiving edge

Negative Skew

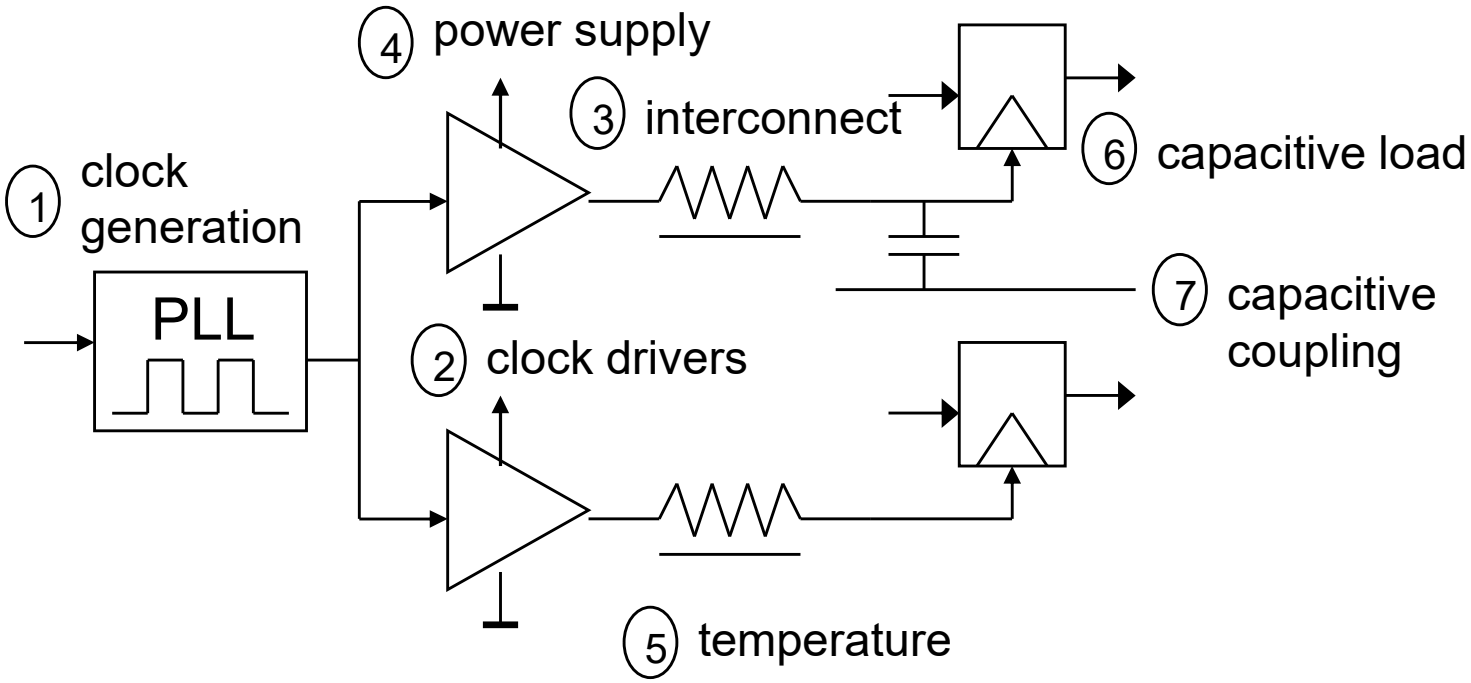


Negative skew: clock is routed in the opposite direction of the data flow



Receiving edge arrives before the launching edge

Sources of Clock Skew and Jitter



- Skew
  - manufacturing device variations in clock drivers
  - interconnect variations
  - environmental variations (power supply and temperature)
- Jitter
  - clock generation
  - capacitive loading and coupling
  - environmental variations (power supply and temperature)

Acknowledgments

- Credit is acknowledged where credit is due. Please refer to the full list of references.