

Homework 1 - Solutions

Q1.

$$F = \overline{X}\overline{Z} + XYZ$$

X	Y	Z	$\overline{X}\overline{Z}$	XYZ	F
0	0	0	1	0	1
0	0	1	0	0	0
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	1	1

Q2.

$$F = \overline{(XYZ)} \overline{(XY)}$$

X	Y	Z	\overline{XYZ}	\overline{XY}	F
0	0	0	1	1	0
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	0	1	1

Q3.

(a)

$$\begin{aligned}
 \overline{F} &= \overline{B}D + \overline{A}B\overline{C} + A\overline{C}D + \overline{A}BC \\
 F &= \overline{(\overline{B}D + \overline{A}B\overline{C} + A\overline{C}D + \overline{A}BC)} \\
 &= \overline{(\overline{B}D + \overline{A}B(\overline{C} + C) + A\overline{C}D)} \\
 &= \overline{(\overline{B}D + \overline{A}B + A\overline{C}D)} \\
 &= (\overline{B} + \overline{D})(\overline{A} + \overline{B})(\overline{A} + \overline{C} + \overline{D}) \\
 &= (\overline{A}B + \overline{A}\overline{D} + \overline{B}\overline{C} + \overline{B}\overline{D})(\overline{A} + \overline{C} + \overline{D}) \\
 &= \overline{A}\overline{B}\overline{D} + \overline{A}B\overline{C} + \overline{A}\overline{C}\overline{D} + \overline{B}\overline{C}\overline{D} \\
 &\quad + \overline{A}B\overline{D} + \overline{A}\overline{D} + \overline{B}\overline{D} \\
 &= \overline{B}\overline{D} \overline{[1 + \overline{A} + \overline{C}]} + \overline{A}\overline{D} \overline{[1 + \overline{C} + B]} \\
 &\quad + \overline{A}B\overline{C} \\
 F &= \overline{B}\overline{D} + \overline{A}\overline{D} + \overline{A}B\overline{C}
 \end{aligned}$$

The diagram shows three 3-input AND gates on the left and one 3-input OR gate on the right. The first AND gate has inputs \bar{B} and \bar{D} (with \bar{C} as a don't-care input) and produces output $\bar{B}\bar{D}$. The second AND gate has inputs A and \bar{D} (with \bar{C} as a don't-care input) and produces output $A\bar{D}$. The third AND gate has inputs A , B , and \bar{C} and produces output $AB\bar{C}$. The outputs of these three AND gates are connected to the inputs of the 3-input OR gate, which produces the final output F .

The diagram shows a computer system with a central PC (Program Counter) block. Above the PC is an ALU (Arithmetic Logic Unit) block labeled '+2'. To the right of the PC is a Register block labeled 'ld'. The PC contains a value '00'. The ALU is connected to the PC and the Register. The Register is connected to the PC and the ALU. The PC is connected to the ALU and the Register. The ALU is connected to the PC and the Register. The Register is connected to the PC and the ALU.

Q6.

Address	Opcode Data	Mnemonic	Comment
00	08 00	LOAD #0	Clear result memory cell (\$FF)
02	01 FF	STORE FF	
04	00 A1	LOAD	Load first operand (\$ A1) ..
06	07 FF	BEQ -1	.. done if 0 (BEQ -1 equiv. to dynamic HALT)
08	0C 01	SUB #1	Subtract 1 from first operand
0A	01 A1	STORE A1	
0C	00 A2	LOAD A2	Load second operand (\$ A2) and add to result
0E	03 FF	ADD FF	
10	01 FF	STORE FF	
12	0F F1	BRA -15	Branch to loop (address 4)