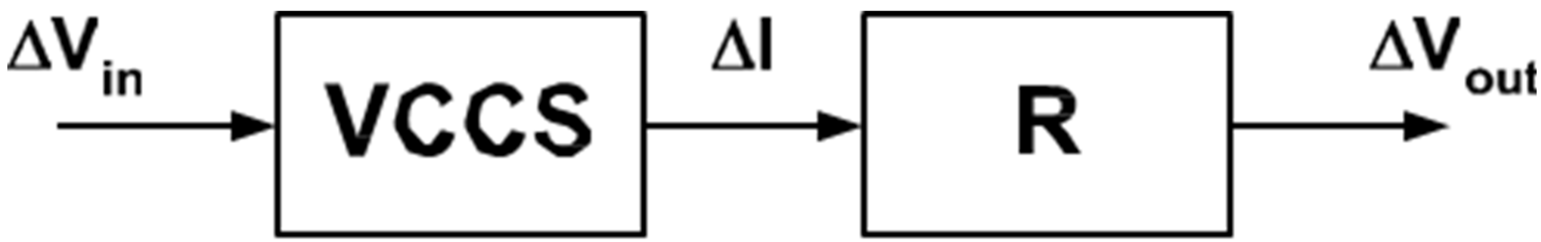
Lecture 10

The MOS Transistor as an Amplifier

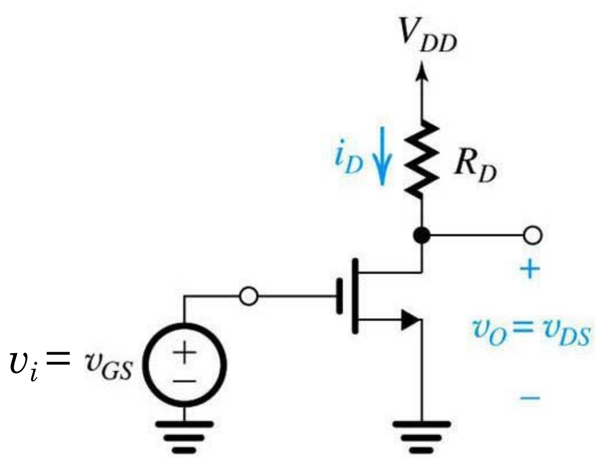
Let's Build Our First Amplifier

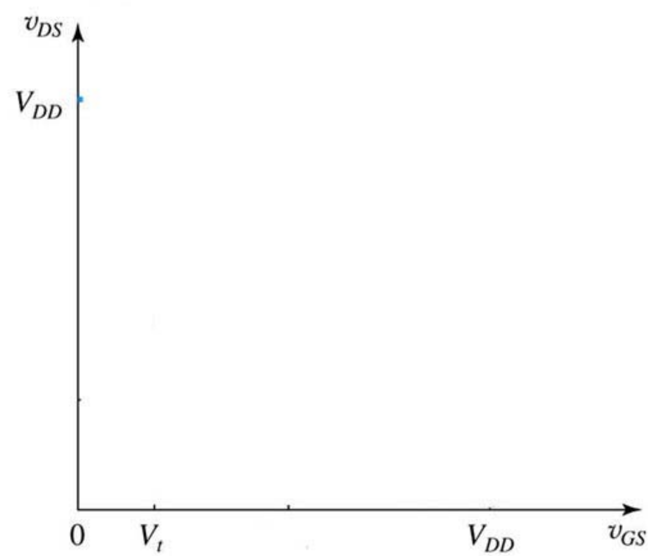
- One way to amplify
  - Convert input voltage to current using voltage controlled current source (VCCS)
  - Convert back to voltage using a resistor (R)
- "Voltage gain" = ΔVout/ΔVin



Common Source Amplifier

- MOS device acts as VCCS
- Transfer Function: Relation between output and input voltages





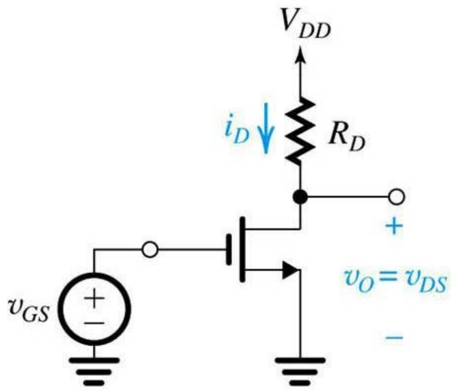
NMOS i-v Characterisitics : $i_D = f(v_{GS}, v_{DS})$ KVL : $V_{DD} = R_D i_D + v_{DS}$

* To find the transfer function, we start with $v_{GS} = 0$ and increase v_{GS}

Let's determine its Transfer Function

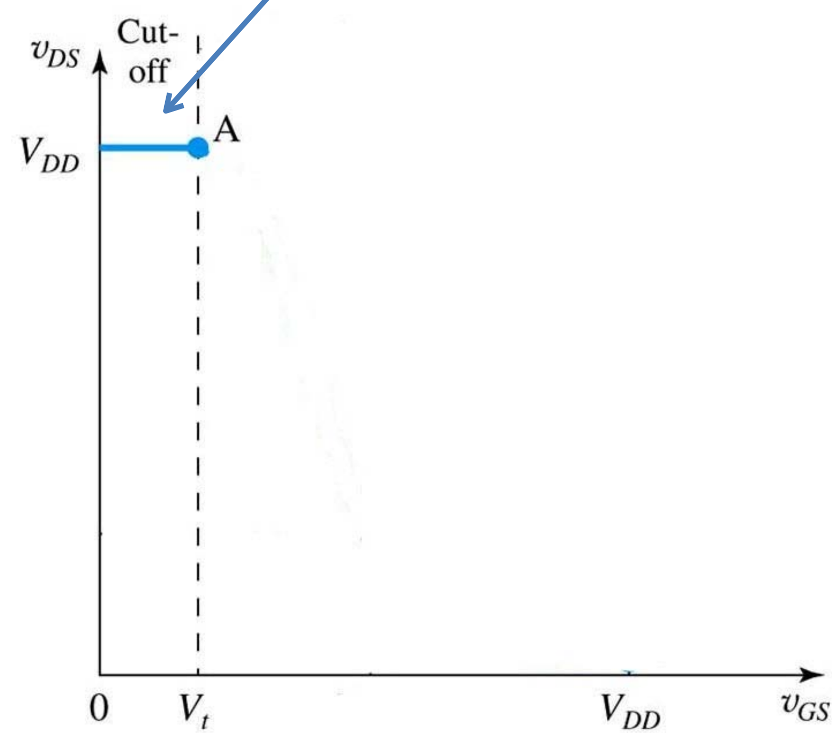
NMOS *i*-*v* Characterisitics : $i_D = f(v_{GS}, v_{DS})$

KVL : $V_{DD} = R_D i_D + v_{DS}$



For $v_{GS} < V_t$, NMOS is in cutoff: $i_D = 0$

$$v_{DS} = V_{DD} - R_D i_D = V_{DD}$$



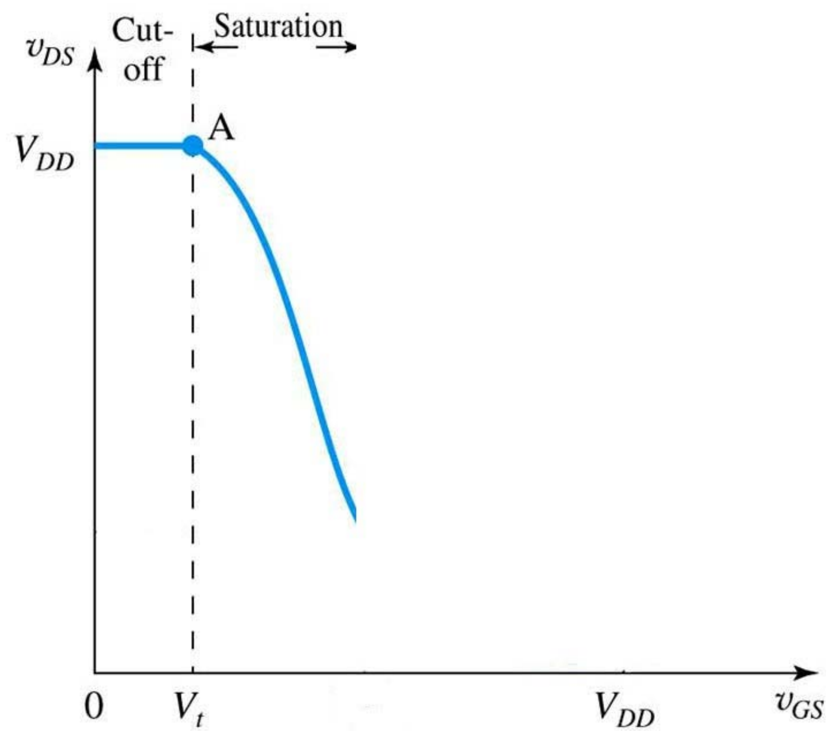
- As we increase v_{GS} passing V_t, NMOS will come out of cut-off: i_D increases leading to a decrease in v_{DS} (due to KVL)
- $v_{GS} \uparrow \rightarrow \quad i_D \uparrow \quad \rightarrow \quad v_{DS} \downarrow$

Transfer Function

- To the right of point A, $v_{GS} > V_t$, and NMOS is ON.
- Just to the right of point A:
  - o $V_{ov} = v_{GS} - V_t$ is small.
  - o v_{DS} is close to V_{DD} because transfer function cannot have a discontinuity.
  - o Thus, $v_{DS} > V_{ov} = v_{GS} - V_t$ and NMOS is in saturation.

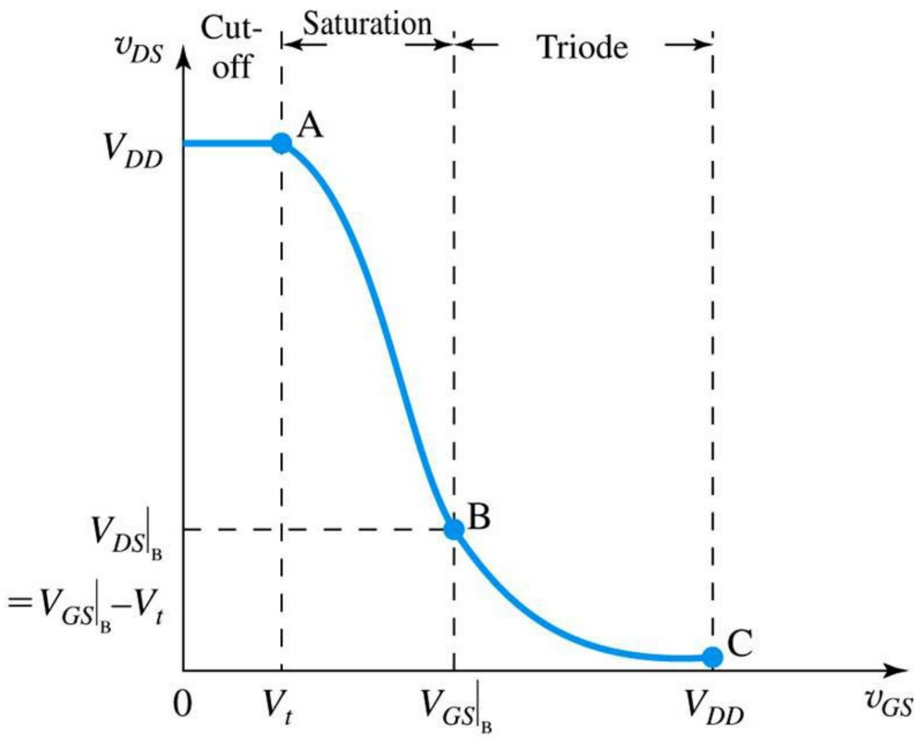
$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

$$v_{DS} = V_{DD} - R_D i_D$$

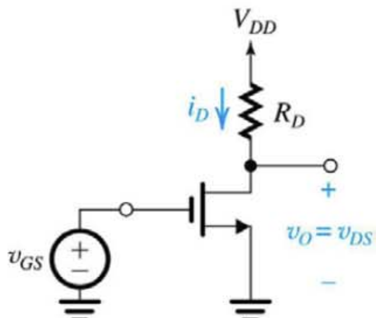


Transfer Function

- As v_{GS} increase:
  - o $V_{ov} = v_{GS} - V_t$ becomes larger;
  - o v_{DS} becomes smaller.
  - o At point B, $v_{DS} = V_{ov} = v_{GS} - V_t$
- To the right of point B, $v_{DS} < V_{ov} = v_{GS} - V_t$ and NMOS enters triode.
- Point B is called the **"Edge of Saturation"**



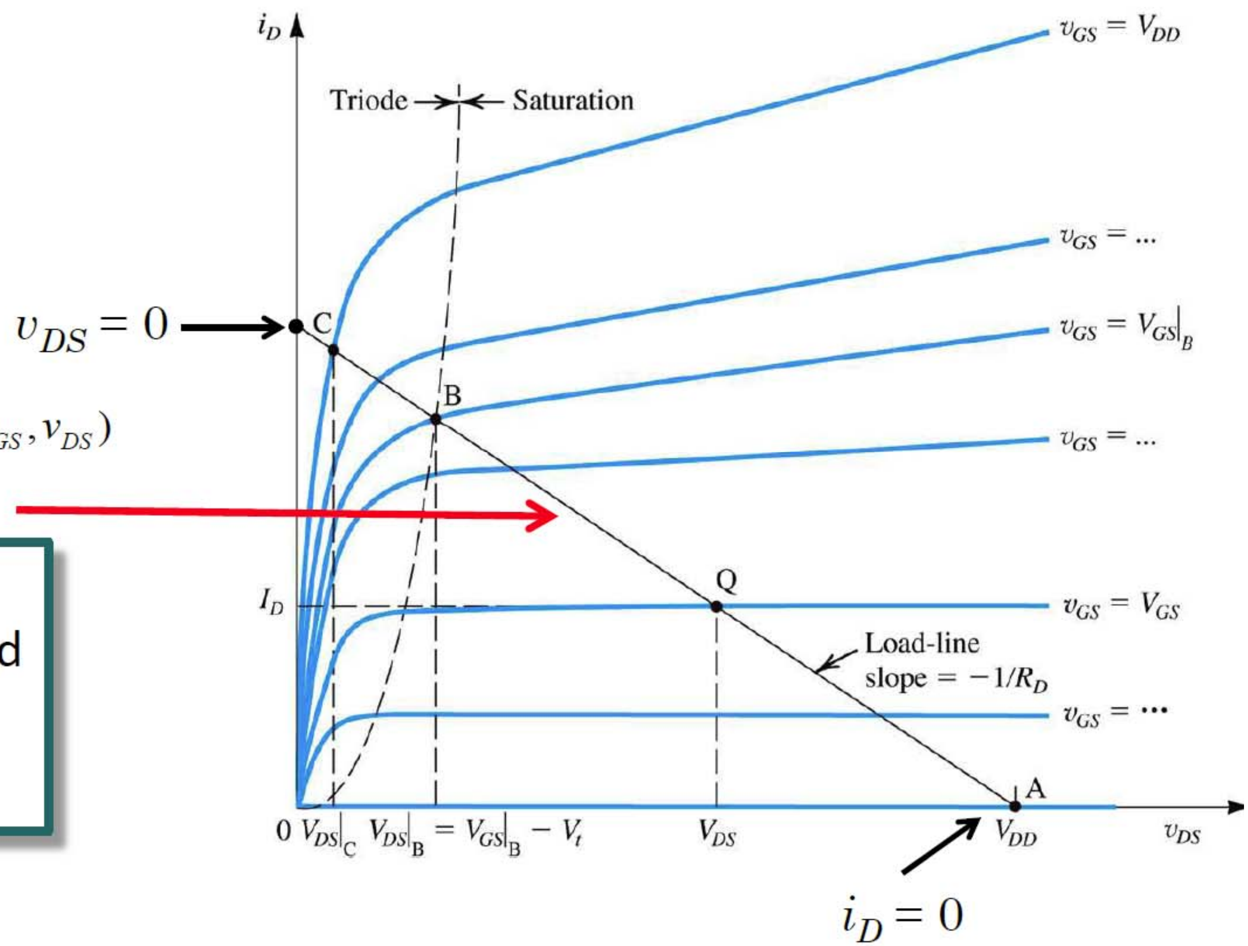
Load Line



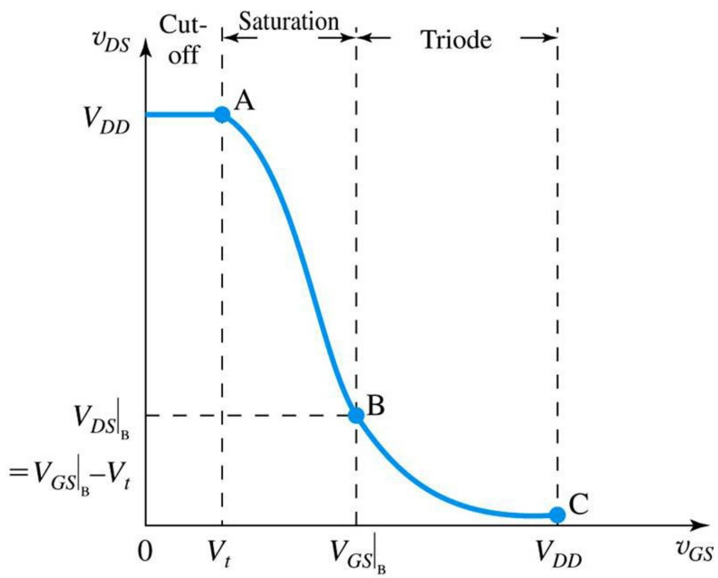
NMOS *i*-*v* Characterisitics : $i_D = f(v_{GS}, v_{DS})$

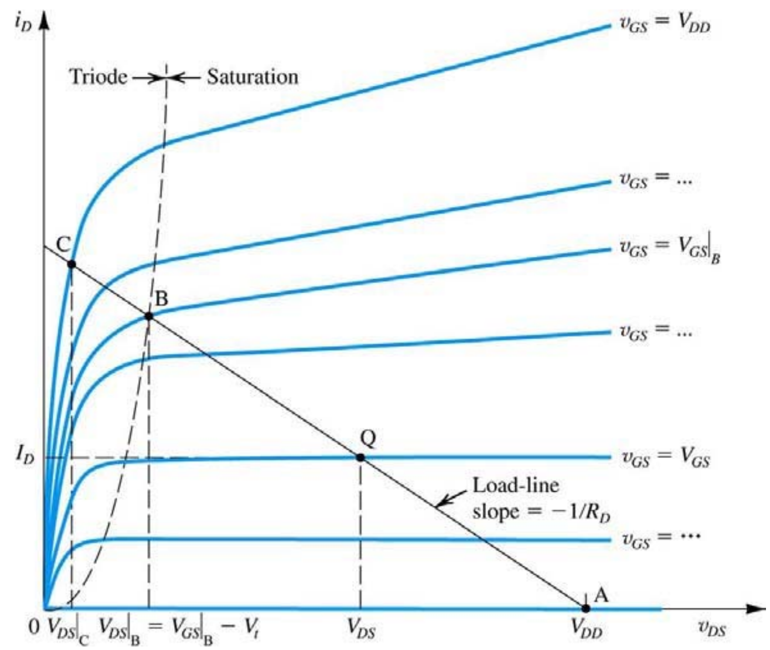
KVL : $V_{DD} = R_D i_D + v_{DS}$

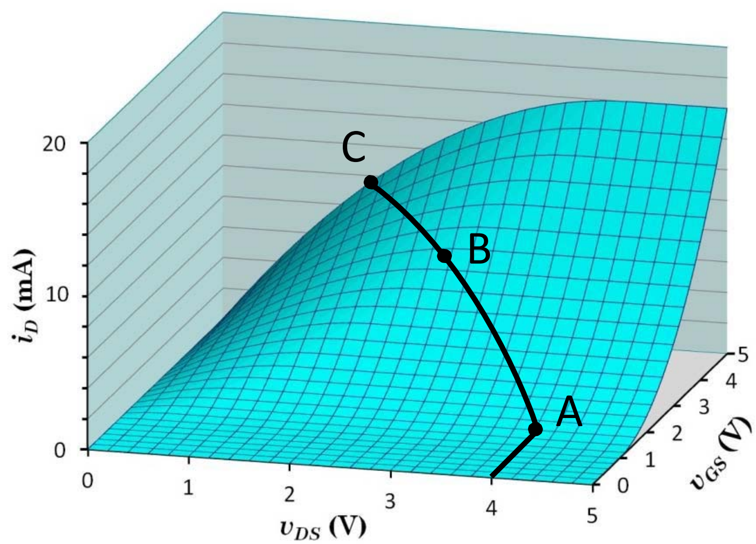
The "Load Line" is the relationship between i_D and v_{DS} imposed by the circuit (outside of NMOS).



Load Line



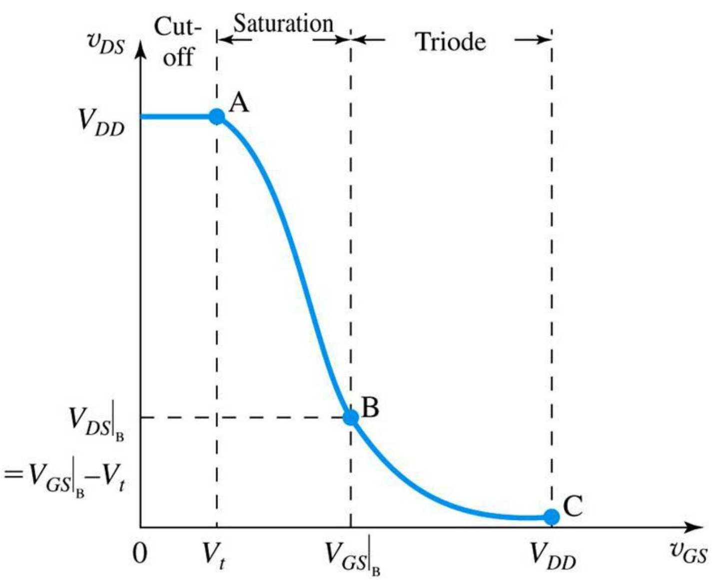




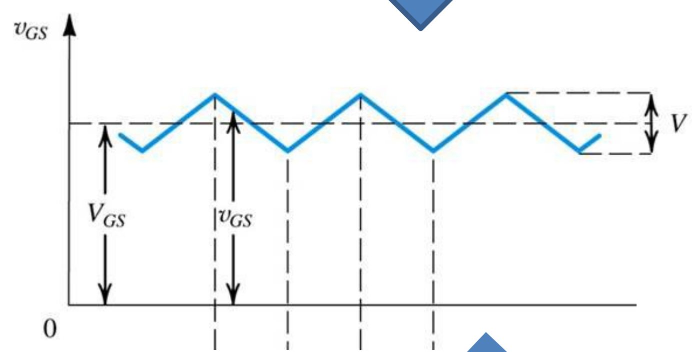
- Every point on the load line corresponds to a specific v_{GS} value.
- As v_{GS} increases, NMOS moves "up" the load line.

Principle of Transistor Amplification

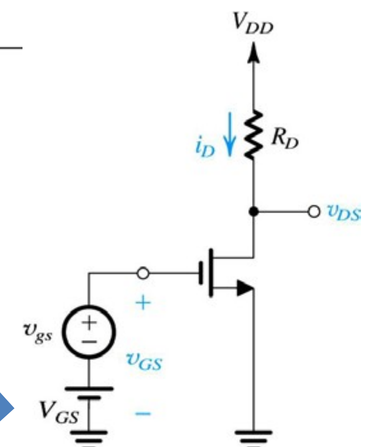
- A voltage amplifier requires $v_o / v_i = \text{const.}$
  - Transfer function has to be linear (but NMOS transfer function is NOT).



- Let us consider the response if NMOS remain in saturation at all times:
  - v_{GS} should be a combination of constant value and a time-varying signal.



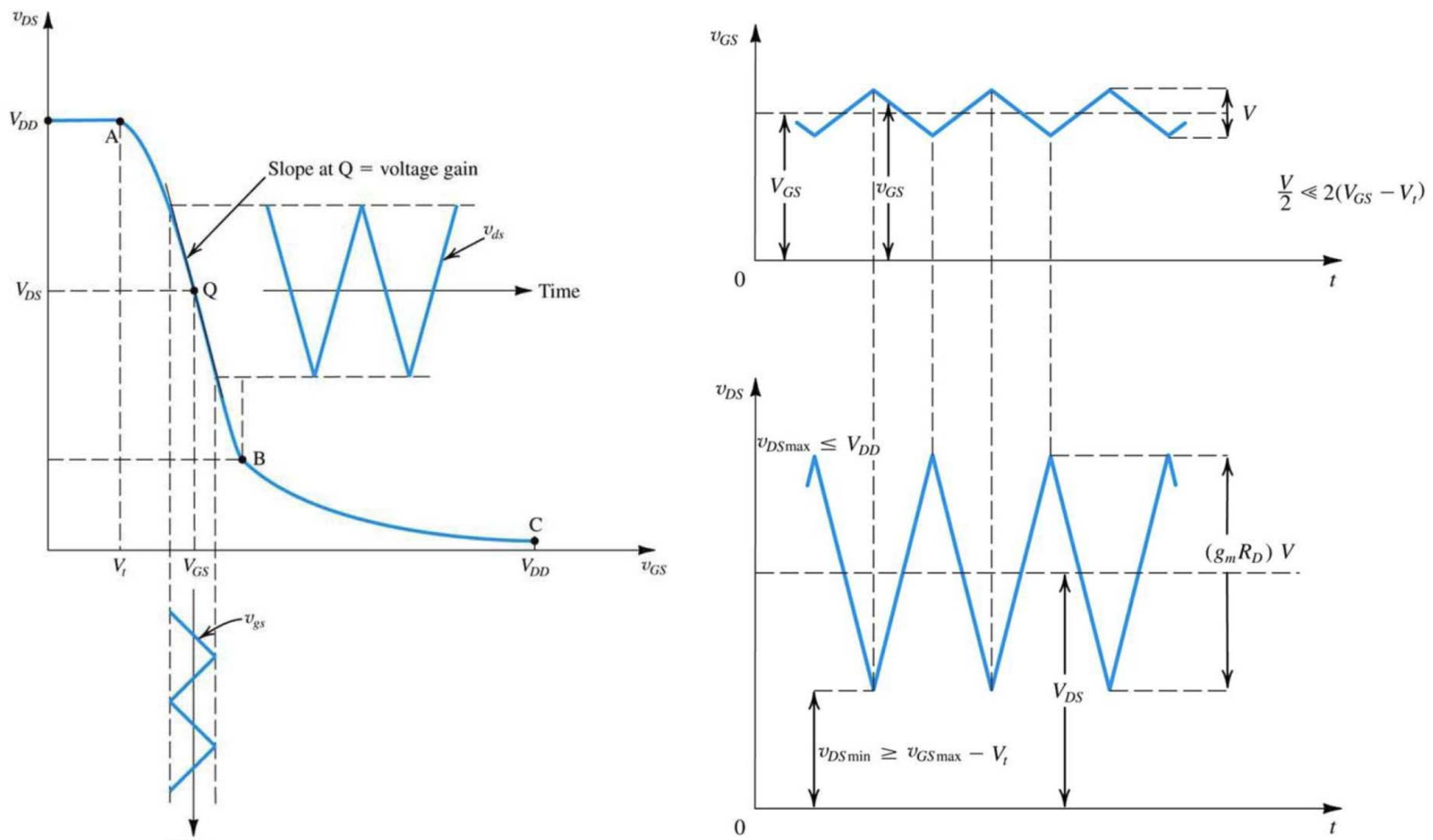
$$\frac{V}{2} \ll 2(V_{GS} - V_t)$$



- Need some sort of "battery" that brings input voltage into useful operating region: this is called Biasing

Principle of Transistor Amplification

- The response to a combination of V_{GS} and v_{gs} (signal) can be found from the transfer function



- **Response to the signal appears to be linear!**

Signal current in the drain terminal

- When you apply a small signal v_{gs} to the gate:

$$
\begin{aligned}
v_{GS} &= V_{GS} + v_{gs} \\
i_D &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - v_{gs} - V_t)^2 \\
i_D &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2 + \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)v_{gs} + \frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{gs}^2
\end{aligned}
$$

- Three components of i_D
  - First term = DC current
  - Second term = current proportional to v_{gs}
  - Third term = undesired nonlinear distortion

- Make v_{gs} small to reduce effect of third term

$$
\begin{aligned}
\frac{1}{2}\mu_n C_{ox}\frac{W}{L}v_{gs}^2 &<< \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})v_{gs} \\
v_{gs} &<< 2(V_{GS} - V_{th})
\end{aligned}
$$

- **This is the small-signal condition, which enables the following approximation:**

$$
i_D \cong I_D + i_d \text{ where } i_d = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})v_{gs}
$$

Transconductance g_m

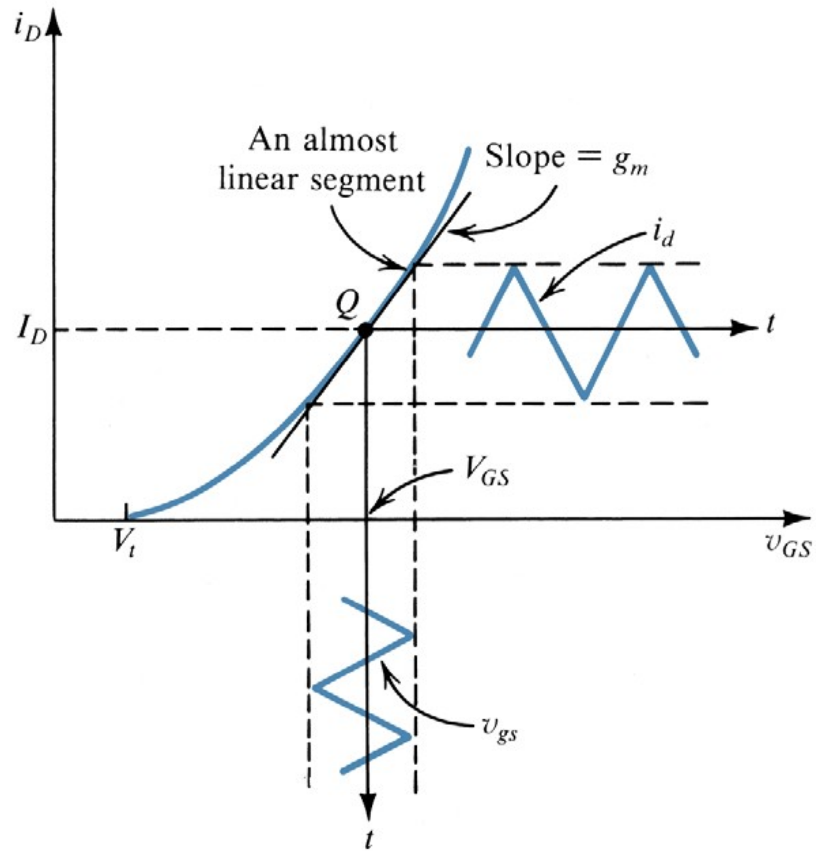
- The parameter relating i_d and v_{gs} is called transconductance g_m

$$g_m = \frac{\partial i_d}{\partial v_{gs}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})$$

or

$$\boxed{g_m = \frac{2 \cdot I_D}{V_{OV}}}$$

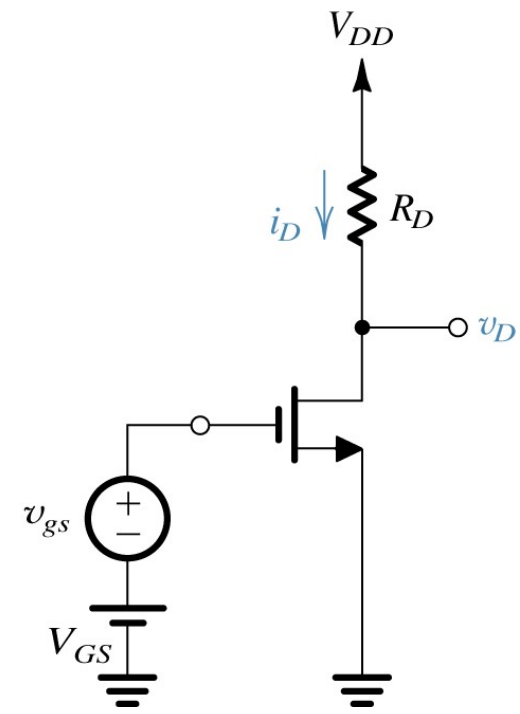
- Depends on
  - process technology – μnCox
  - physical geometry – W/L
  - DC biasing conditions – V_{GS}
  - making V_{GS} large increases g_m, but can limit voltage range on drain



Small signal voltage gain Av

- Small-Signal Voltage Gain (vd/vgs)

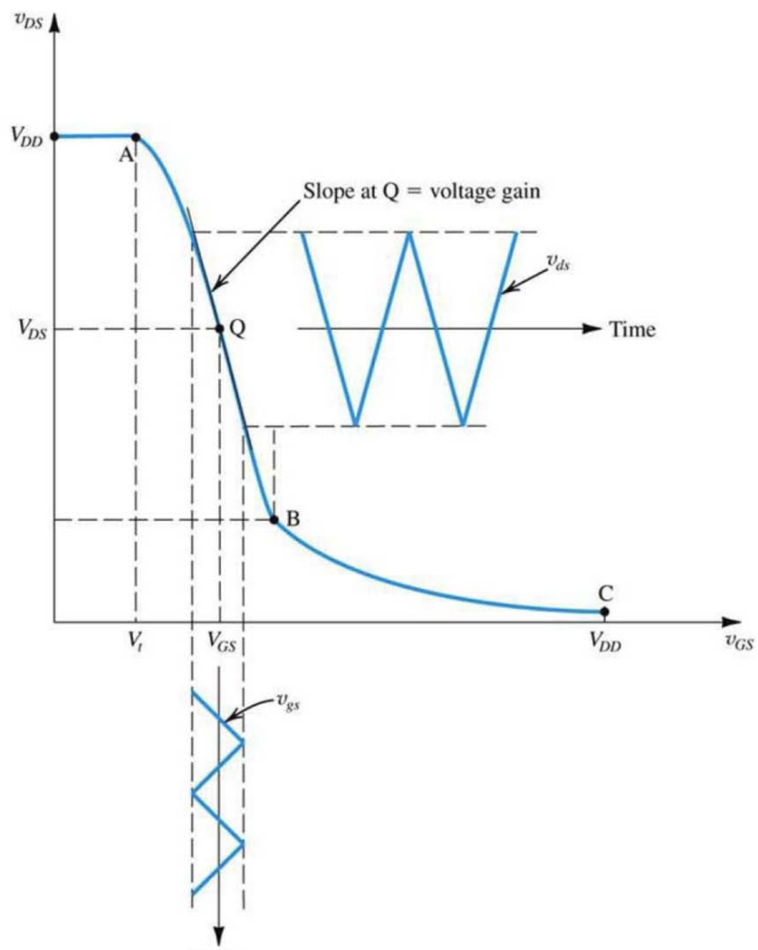
$$
\begin{aligned}
v_D &= V_{DD} - R_D i_D \\
v_D &= V_{DD} - R_D (I_D + i_d) \\
v_D &= V_D - R_D i_d \\
v_d &= -R_D i_d = -g_m R_D v_{gs} \\
\frac{v_d}{v_{gs}} &= -g_m R_D
\end{aligned}
$$

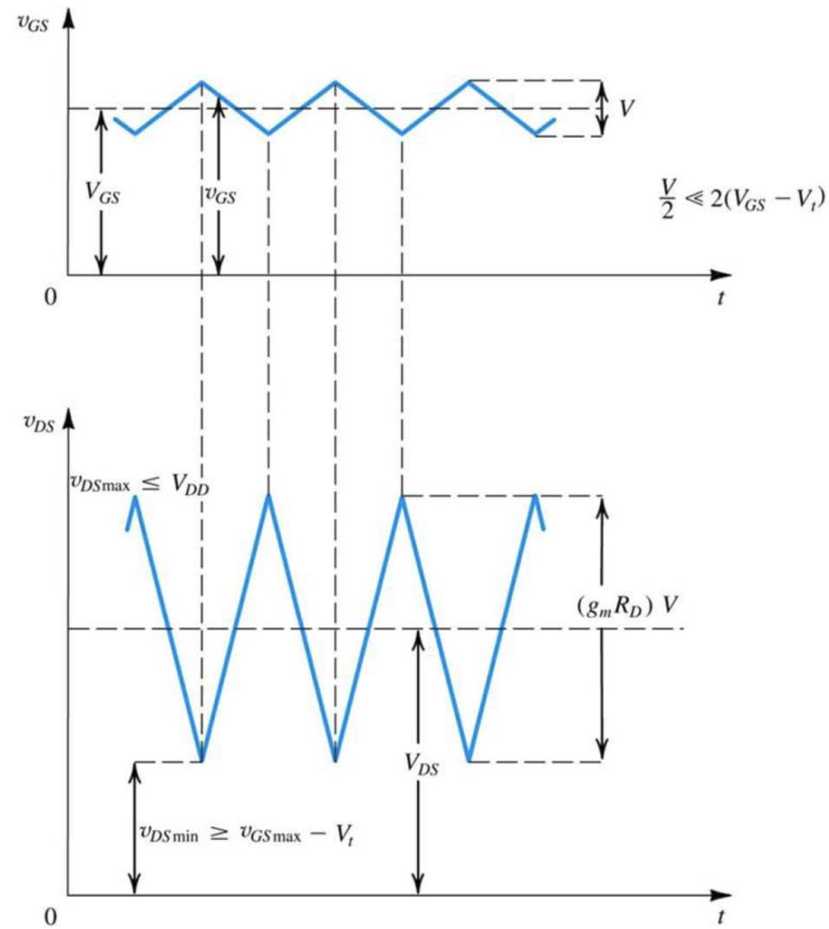


- This gain equation hold for small signals
- Notice that the output is 180° out of phase w.r.t. the input
- Again, we can separate out the DC bias conditions and the small-signal operation of the circuit

Separating DC analysis & Signal Analysis

- The response to a combination of V_{GS} and v_{gs} (signal) can be found from the transfer function





- **Response to the signal appears to be linear!**

Separating DC analysis & Signal Analysis

- We can see that under the small signal approximation, signal quantities are superimposed on DC quantities.

- For instance, the total drain current i_D equals the dc current I_D plus the signal current i_d, and so on.

Constant Bias

$$v_{GS} = \boxed{V_{GS}} + \boxed{v_{gs}}$$

$$v_{DS} = \boxed{V_{DS}} + \boxed{v_{ds}}$$

$$i_D = \boxed{I_{DS}} + \boxed{i_d}$$

Signal and response

Non-linear relationship among these parameters

Linear relationship among these parameters

Separating DC analysis & Signal Analysis

- It follows that the analysis and design can be greatly simplified by separating dc or bias calculations from small-signal calculations.
- That is, once a stable dc operating point has been established and all dc quantities calculated, we may then perform signal analysis ignoring dc quantities.

Constant Bias

$$v_{GS} = V_{GS} + v_{gs}$$

$$v_{DS} = V_{DS} + v_{ds}$$

$$i_D = I_{DS} + i_d$$

Signal and response

Non-linear relationship among these parameters

Linear relationship among these parameters

Small Signal Approximation

- Nobody likes nonlinear equations; we need a simpler model

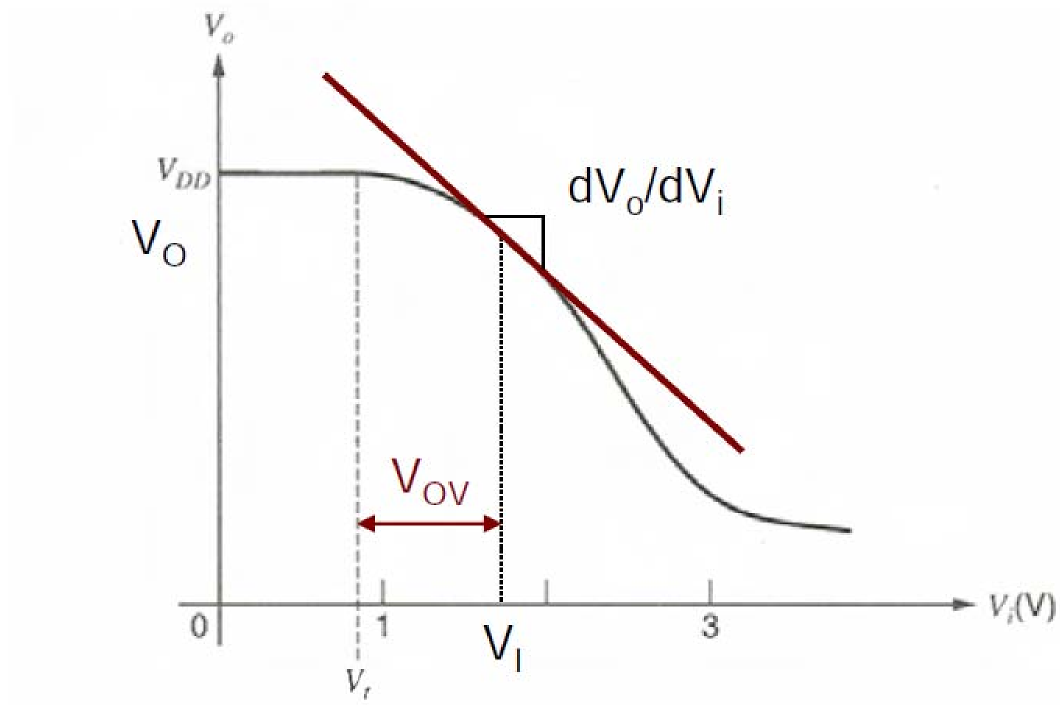
- Fortunately, a linear approximation to the above expression is sufficient for 90% of all analog circuit analysis

- If we further pretend that the input voltage increment is infinitely small, we can find the gain of the circuit directly by taking the derivative of the large signal transfer function at the "operating point Q"

$$\left.\frac{dV_o}{dV_i}\right|_{V_i=V_{GSQ}}$$

Small Signal Approximation

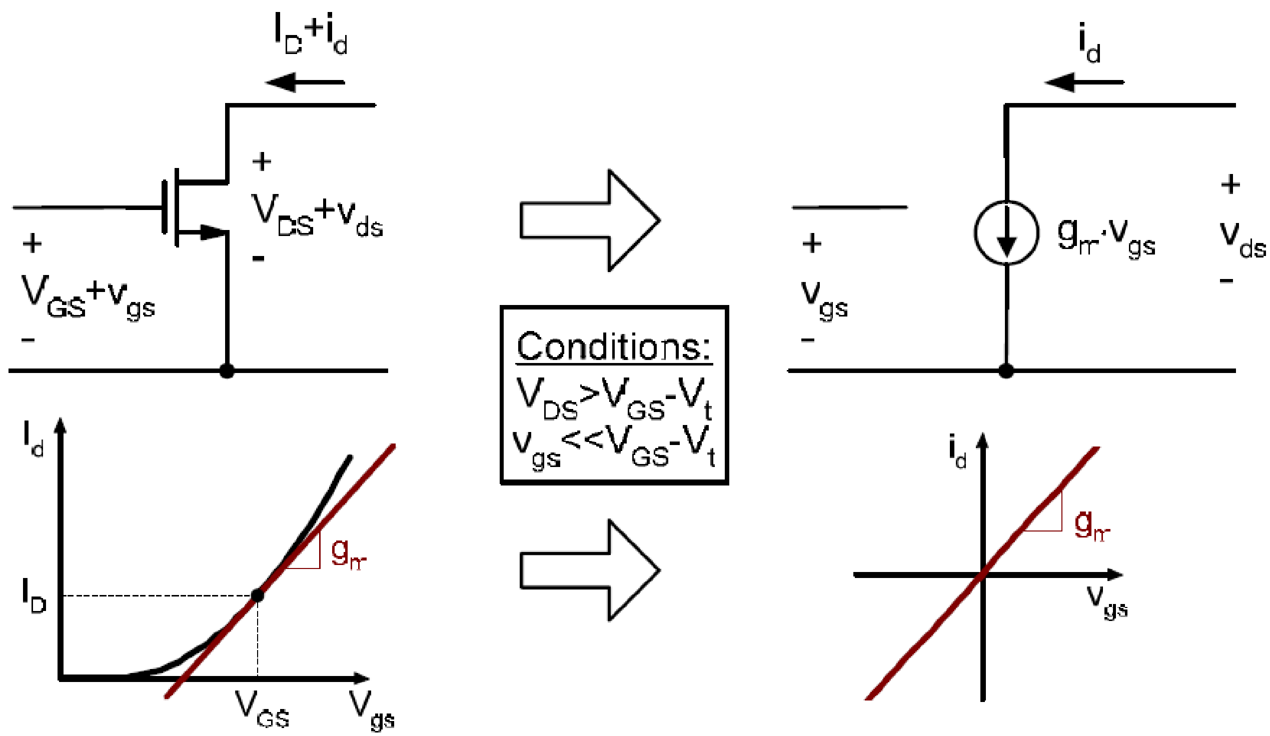
- Graphical illustration:



- The slope of the above tangent is the so called "small signal gain" of our amplifier

Small Signal MOS Model

- Fortunately we don't have to repeat this analysis for every single circuit we build
- Instead, we derive a linearized circuit model for the MOS transistor and plug it into arbitrary circuits



Derivation of MOS small signal model

$$\begin{cases} i_G = 0 \\ i_D = 0.5\mu_n C_{ox}\dfrac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS}) = f(v_{GS}, v_{DS}) \end{cases} \qquad \begin{cases} I_G = 0 \\ I_D = 0.5\mu_n C_{ox}\dfrac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS}) \end{cases}$$

$$i_D = f(x,y) \quad \text{with} \quad v_{GS} \leftrightarrow x, \quad v_{DS} \leftrightarrow y$$

$$i_d = \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} \cdot v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}} \cdot v_{ds} \Rightarrow$$

$$\boxed{\begin{aligned} i_d &= g_m \cdot v_{gs} + \frac{v_{ds}}{r_o} \\ i_g &= 0 \\ g_m &= \frac{2I_D}{V_{OV}} \\ {}^{*}\ r_o &= \frac{1}{\lambda \cdot I_D} \end{aligned}}$$

(* For $\lambda\, v_{DS} << 1$)

$$\left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = 2\times 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)(1+\lambda v_{DS})\ \Big|_{V_{GS},V_{DS}}$$

$$= 2\times\frac{0.5\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})}{(V_{GS}-V_t)} = \frac{2I_D}{V_{OV}} \equiv g_m$$

$$\left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS},V_{DS}} = \lambda\times 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS}-V_t)^2\Big|_{V_{GS},V_{DS}}$$

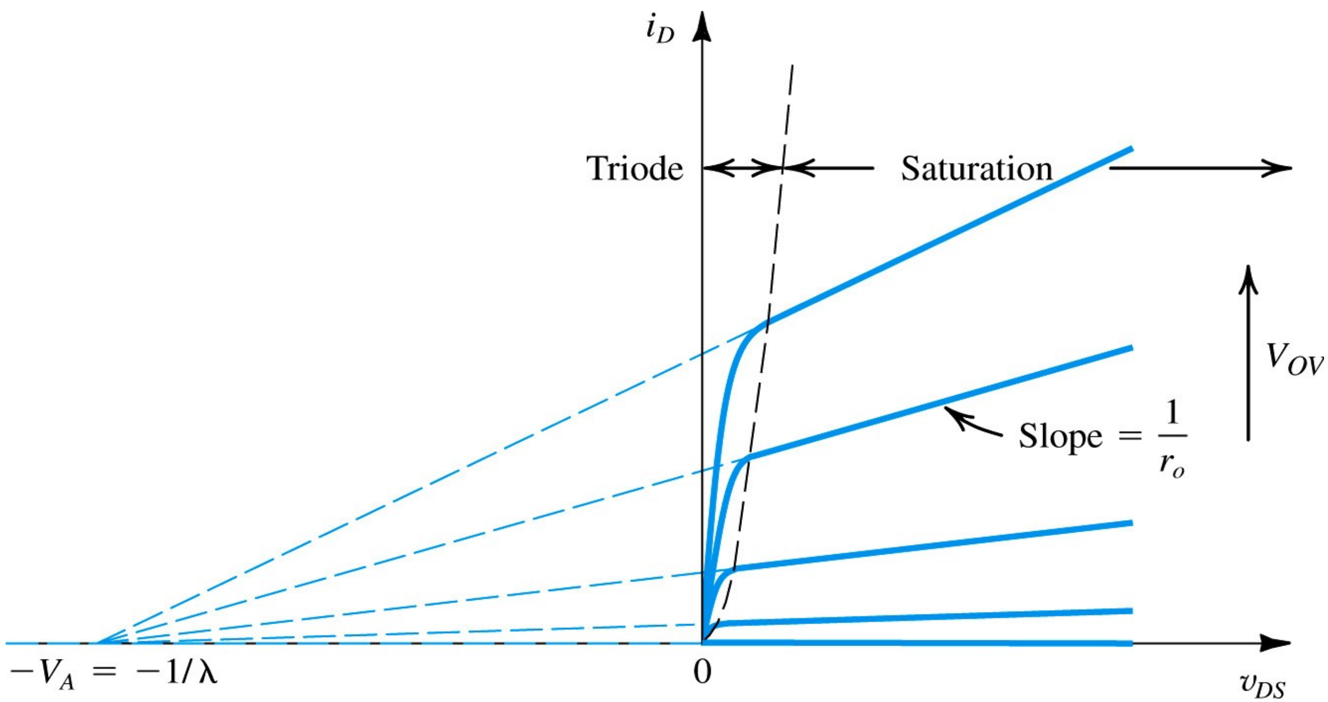
$$= \lambda\times\frac{0.5\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})}{(1+\lambda V_{DS})} = \frac{\lambda I_D}{(1+\lambda V_{DS})} \equiv \frac{1}{r_o}$$

Output or drain conductance

- The output resistance — that is, the resistance looking into the drain — is high but not infinite as the drain current does in fact depend on v_{DS} ina linear manner. Such dependence is modeled by a finite resistance r_o (conductance g_o) between drain and source.

$$\boxed{r_o \approx \frac{1}{\lambda \cdot I_D}}$$

- r_o in the range of 10-1000kΩ
- $\lambda = 1/V_A$ is a MOSFET parameter that can be measured.

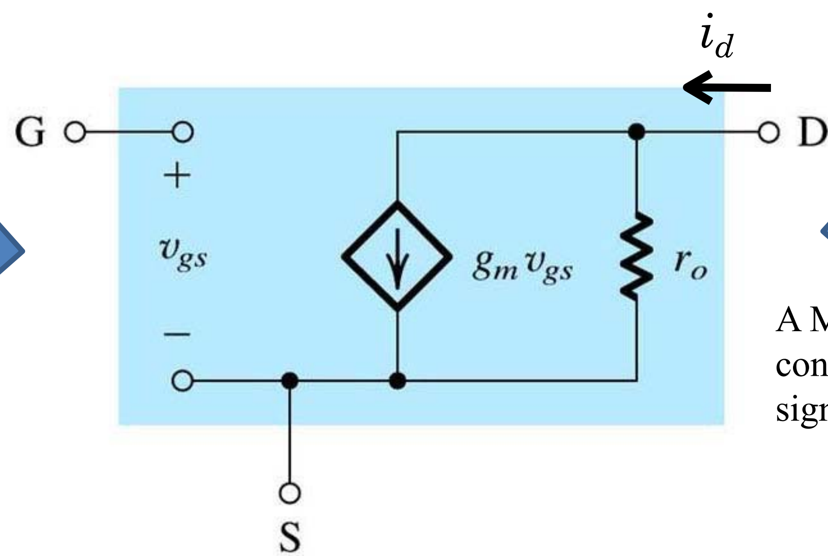


Low-frequency MOS small signal "circuit" model

$$i_g = 0 \quad \text{and} \quad i_d = g_m \cdot v_{gs} + \frac{v_{ds}}{r_o}$$

Input open circuit

Statement of KCL
Two elements in parallel



A MOSFET operates like voltage controlled current source (for small signals)

$$g_m = \frac{2 \cdot I_D}{V_{OV}}$$

$$r_o \approx \frac{1}{\lambda \cdot I_D}$$

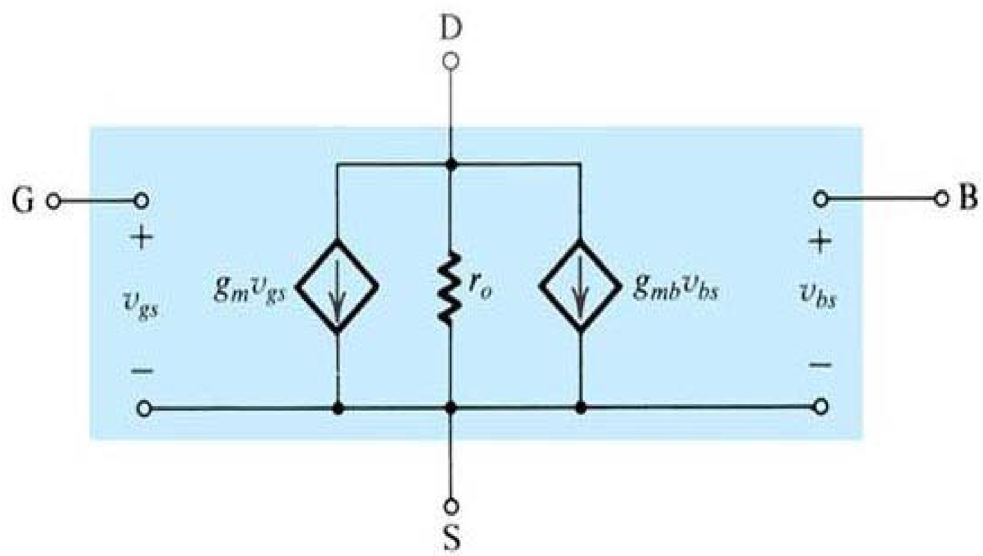
$$g_m r_o = \frac{2}{\lambda V_{OV}} = \frac{2V_A}{V_{OV}} >> 1$$

When using small-signal equivalent circuits, all DC sources are set to 0 since they do not change

Body Effect

- We saw that the substrate bias V_{BS} affects V_t which has the effect of influencing current like another gate

$$V_t = V_{t,0} + \gamma\left(\sqrt{|2\phi_F + v_{SB}|} - \sqrt{|2\phi_F|}\right) , \qquad i_D = 0.5\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2(1+\lambda v_{DS}) = f(v_{GS}, v_{DS}, v_{SB})$$



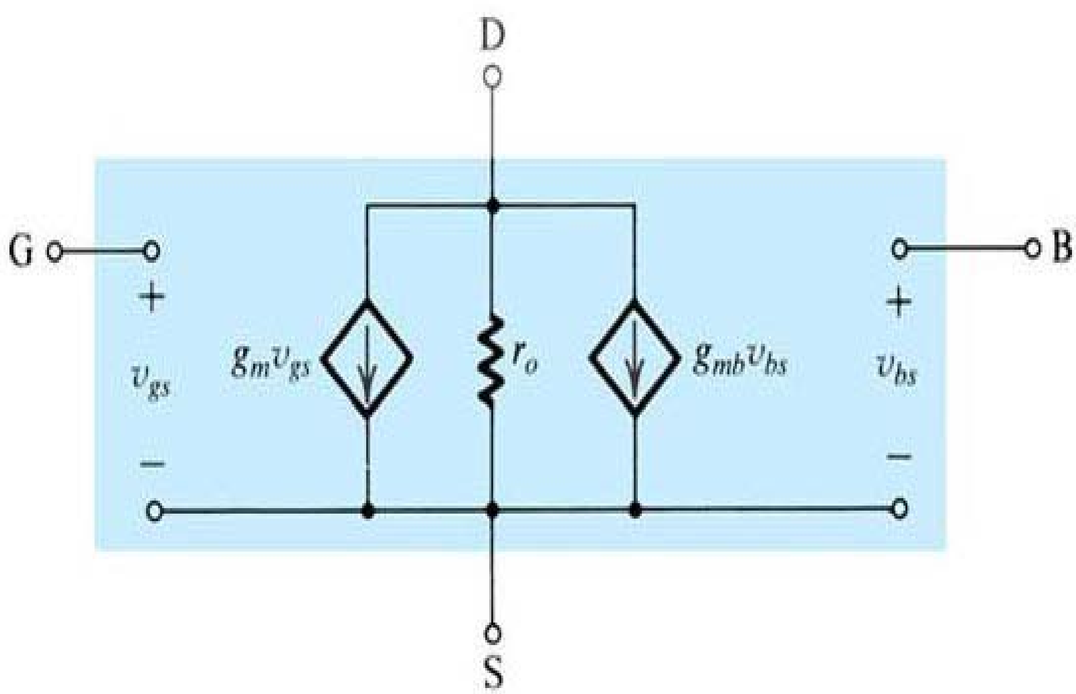
Body Transconductance

$$g_{mb} \equiv \left.\frac{\partial i_d}{\partial v_{BS}}\right|_{v_{GS} \text{ and } v_{DS} \text{ constant}}$$

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} g_m$$

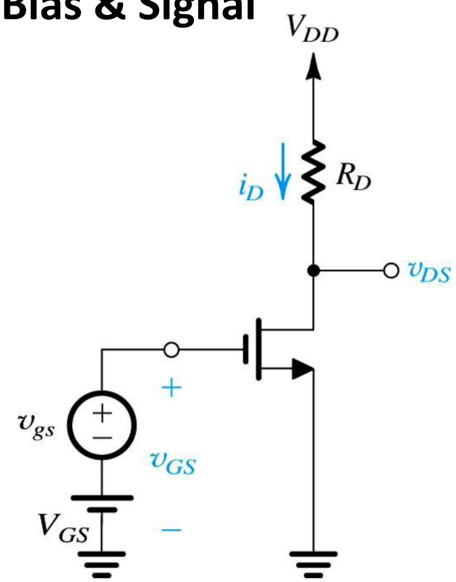
Low-frequency PMOS small signal "circuit" model

- PMOS small-signal circuit model is identical to NMOS
- Same expressions for conductances g_m, g_{mb}, g_0, all of which are positive.



“Signal-only” circuit is different!

Bias & Signal



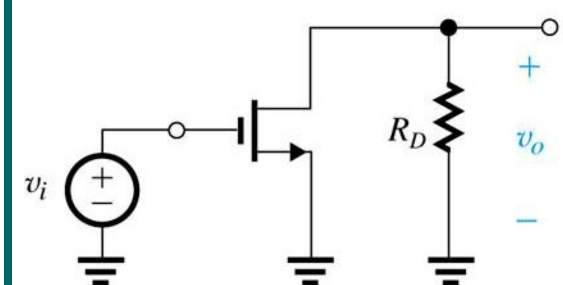
No signal here!

V_{DD}: V_{DD}

R_D: $v_{RD} = V_{RD} + v_{rd}$
$i_{RD} = i_D = I_D + i_d$

MOS: $v_{GS} = V_{GS} + v_{gs}$
$v_{DS} = V_{DS} + v_{ds}$
$i_D = I_D + i_d$

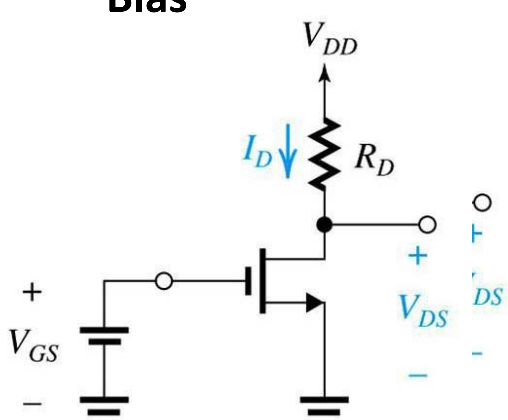
Signal only
= (Bias + Signal) - Bias



R_D: v_{rd}
$i_{rd} = i_d$

MOS: v_{gs}, i_d, v_{ds}

Bias



V_{DD}: V_{DD}

R_D: V_{RD}
$I_{RD} = I_D$

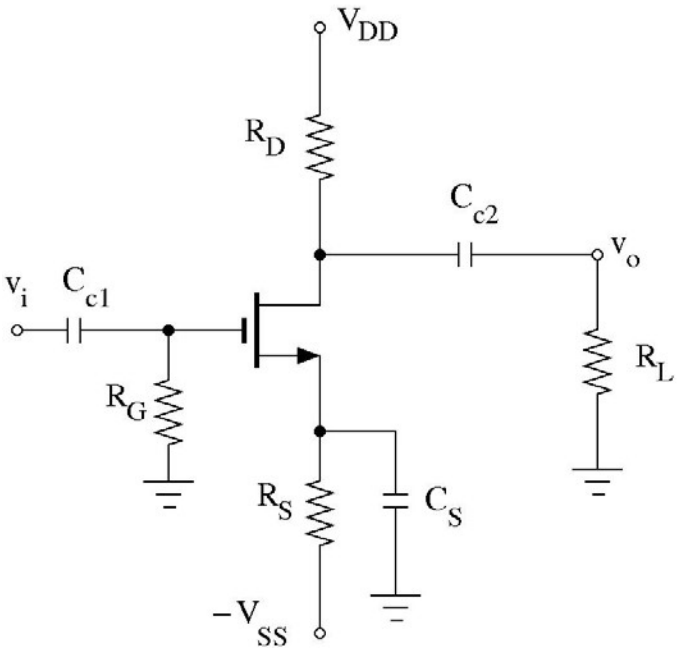
MOS: V_{GS}, I_D, V_{DS}

Small Signal or incremental analysis

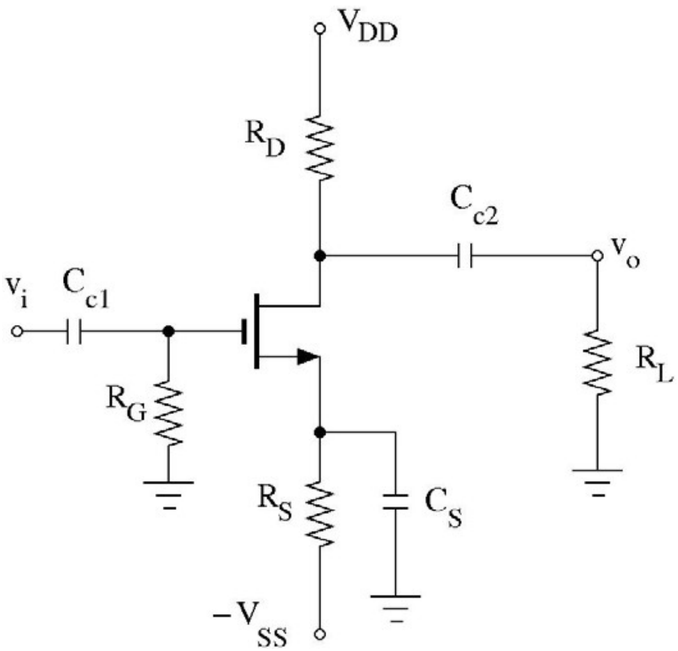
- All DC sources are set to 0 since they do not change
  - Short-circuit independent voltage sources (V_{DD},…)
  - Open-circuit current sources
- Resistors, capacitors, inductors remain
- Dependent sources remain the same with the control parameter related to the signal!
- Transistors are replaced with their small signal circuit models

Example 1

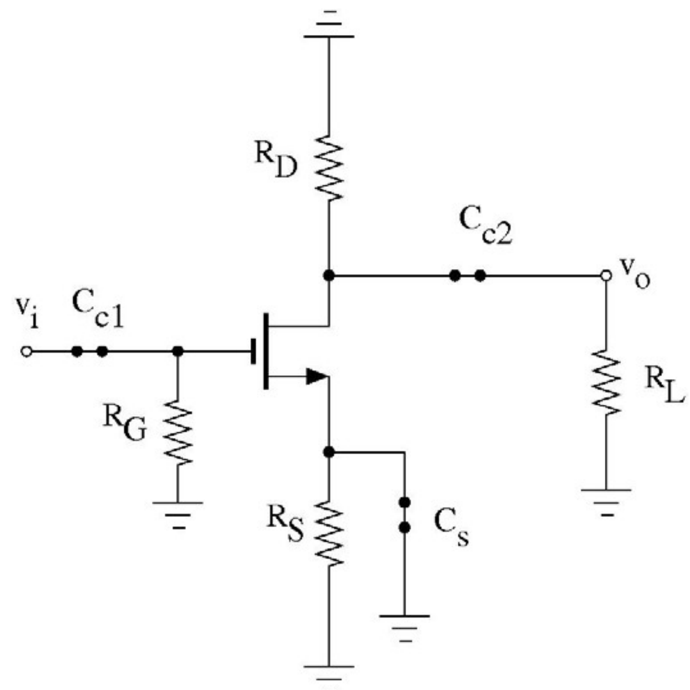
Draw the small-signal equivalent of the circuit below (assume capacitors are short for small signal).



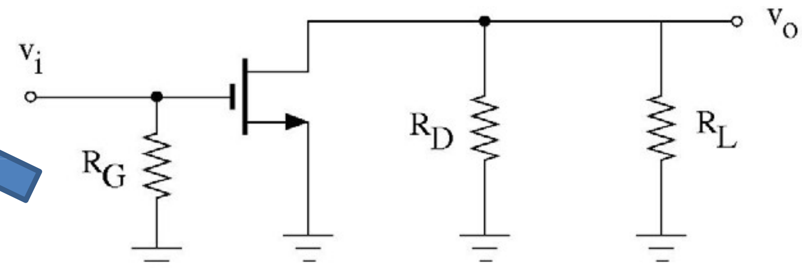
Example 1

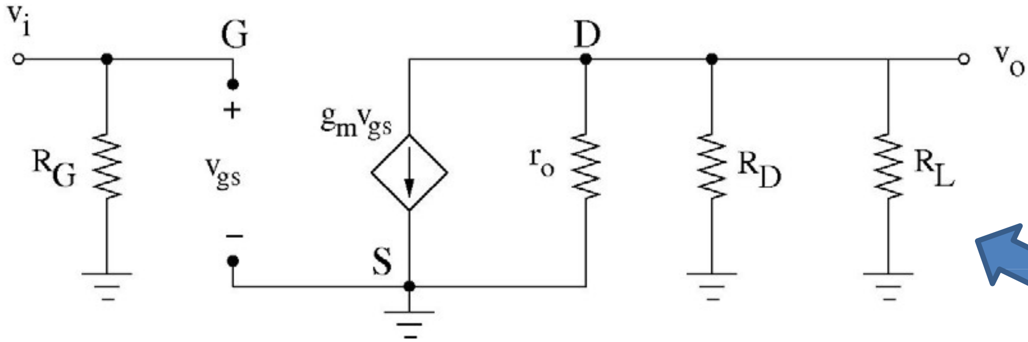


IVS $\rightarrow$ 0
R remains



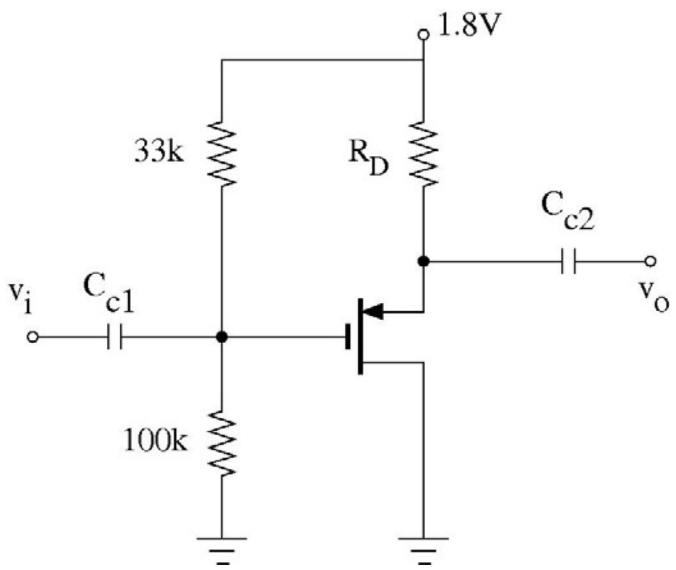
Ground at the bottom



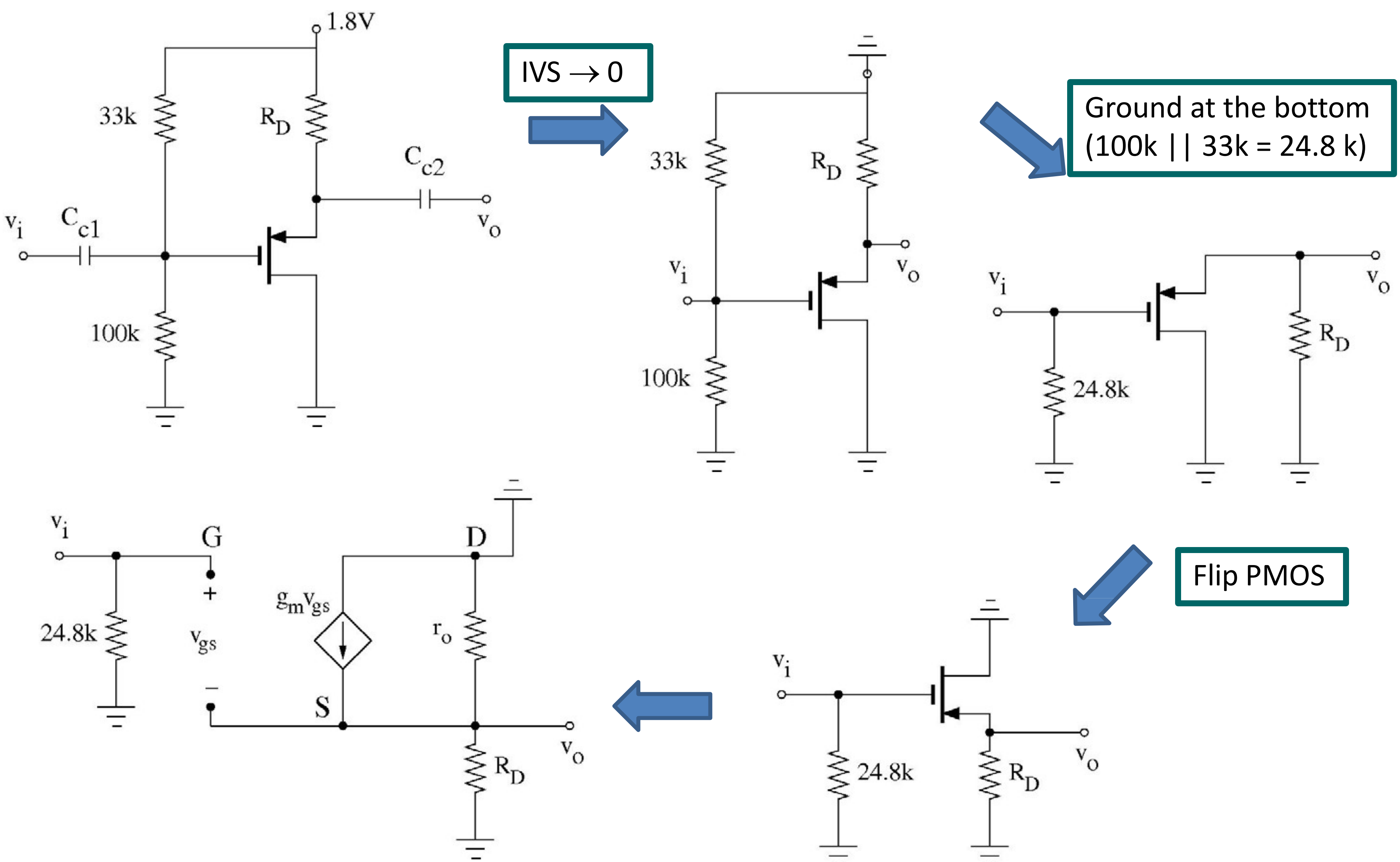


Example 2

Draw the small-signal equivalent of the circuit below (assume capacitors are short for small signal).

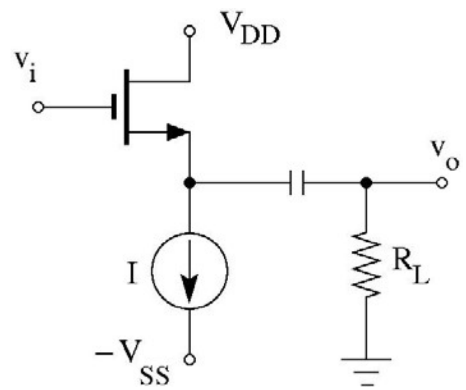


Example 2

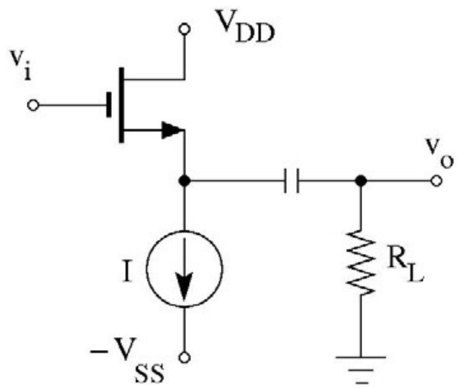

1.8V
33k
R_D
C_{c2}
v_i
C_{c1}
v_o
100k
IVS → 0
Ground at the bottom
(100k || 33k = 24.8 k)
24.8k
Flip PMOS
G
D
+
$g_m v_{gs}$
v_{gs}
r_o
−
S

Example 3

Draw the small-signal equivalent of the circuit below (assume capacitors are short for small signal).

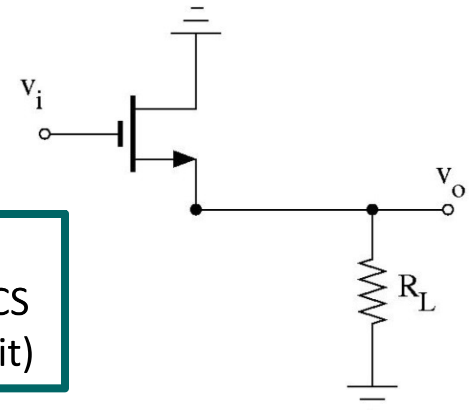


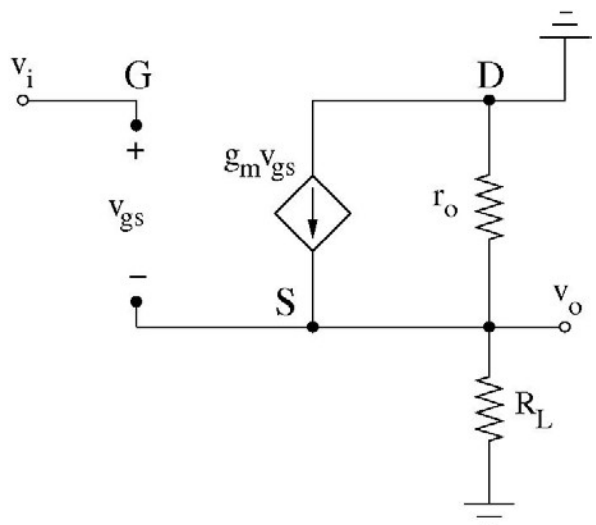
Example 3



IVS → 0

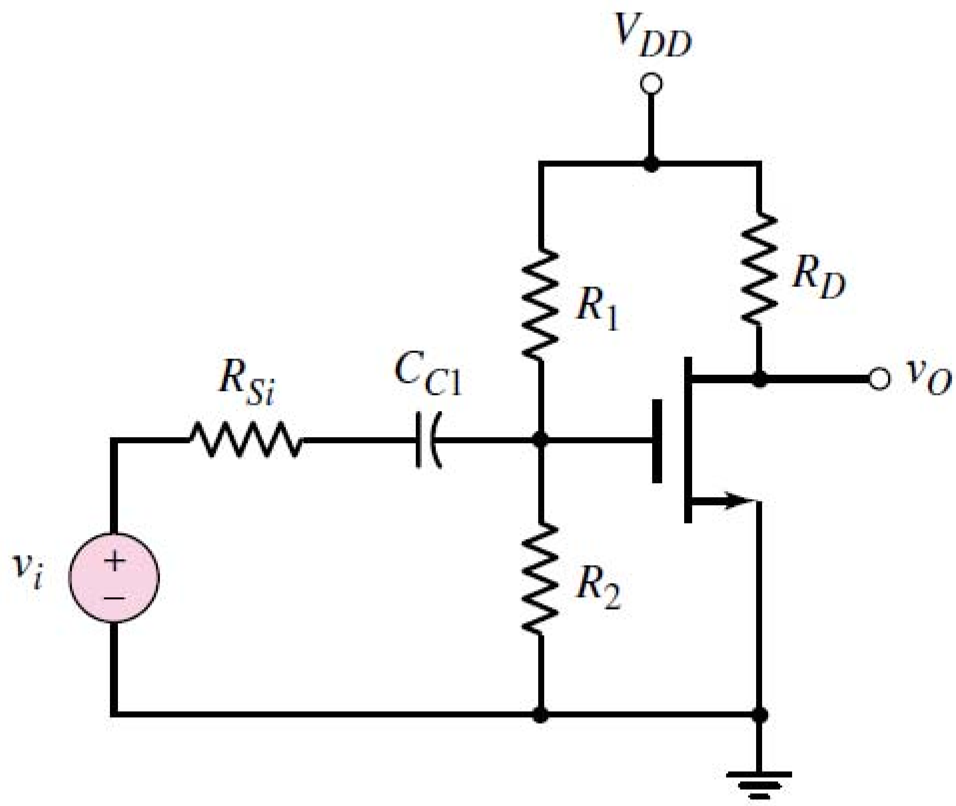
ICS → 0
(This makes ICS an open circuit)



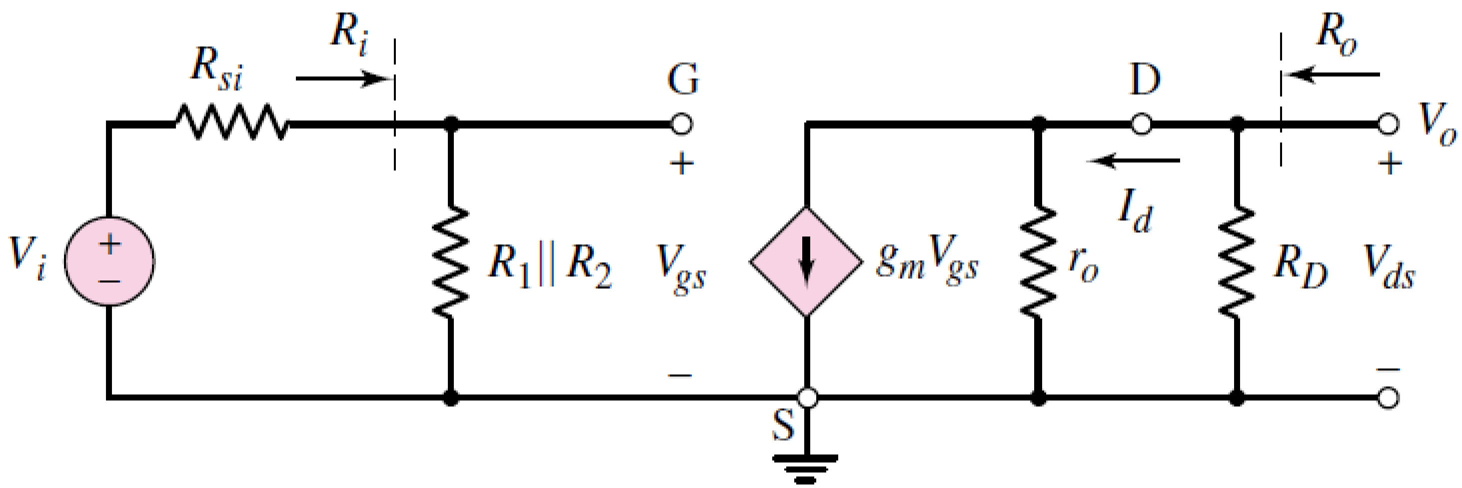


Example 4

- Determine the small-signal voltage gain and input and output resistances of the following common-source amplifier.



Example 4



$$V_o = -g_m V_{gs}(r_o \| R_D)$$

The input gate-to-source voltage is

$$V_{gs} = \left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i$$

so the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_D) \cdot \left(\frac{R_i}{R_i + R_{Si}}\right)$$

$$R_{is} = R_1 \| R_2$$

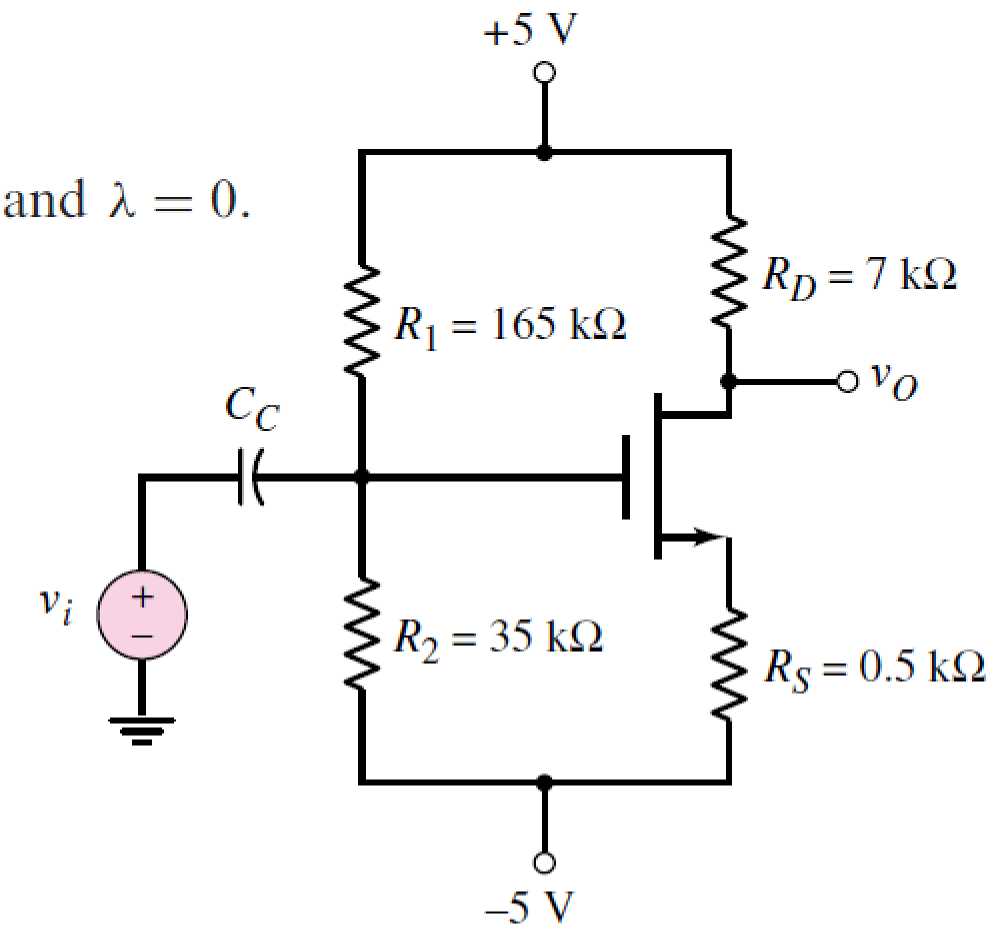
$$R_o = R_D \| r_o.$$

Example 5

- Determine the small-signal voltage gain and input and output resistances of the following common-source amplifier.

$V_{TN} = 0.8\text{ V}$

$K_n = 1\text{ mA/V}^2$, and $\lambda = 0$.



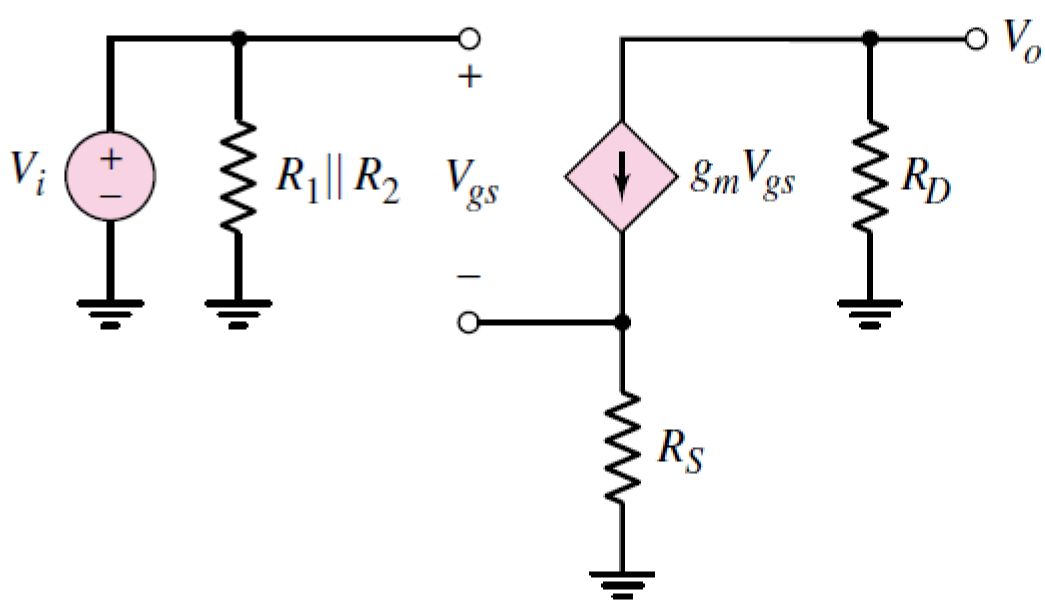
Example 5

Solution: From the dc analysis of the circuit, we find that $V_{GSQ} = 1.50\,\text{V}$, $I_{DQ} = 0.50\,\text{mA}$, and $V_{DSQ} = 6.25\,\text{V}$. The small-signal transconductance is

$$g_m = 2K_n(V_{GS} - V_{TN}) = 2(1)(1.50 - 0.8) = 1.4\,\text{mA/V}$$

and the small-signal resistance is

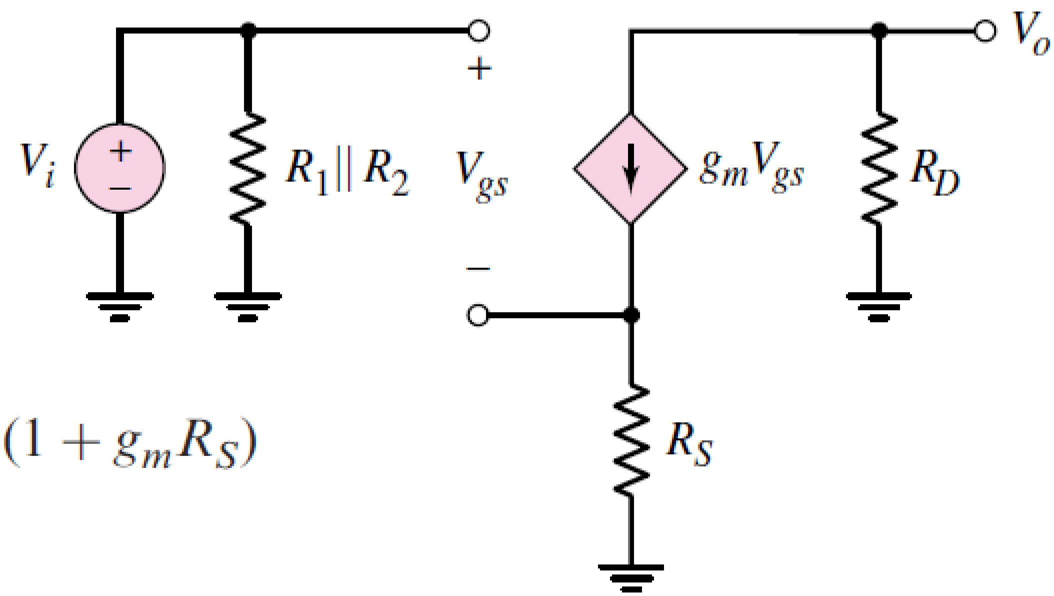
$$r_o \cong [\lambda I_{DQ}]^{-1} = \infty$$



Example 5

The output voltage is

$$V_o = -g_m V_{gs} R_D$$



$$V_i = V_{gs} + (g_m V_{gs}) R_S = V_{gs}(1 + g_m R_S)$$

$$V_{gs} = \frac{V_i}{1 + g_m R_S}$$

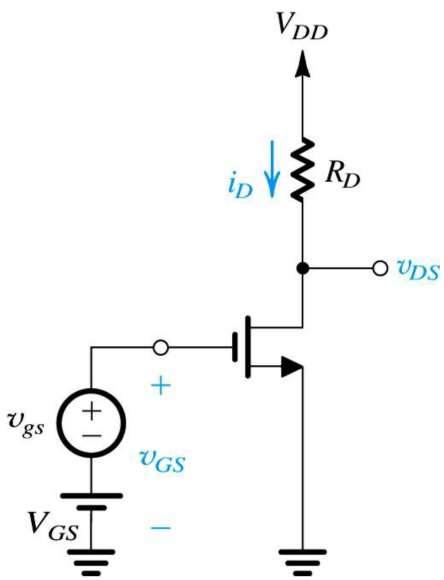
The small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_S}$$

$$A_v = \frac{-(1.4)(7)}{1 + (1.4)(0.5)} = -5.76$$

Comment: A source resistor reduces the small-signal voltage gain.

Limitations & Constraints



- Bias: V_{GS} , V_{DS} , I_D
- Bias + Signal: v_{GS} , v_{DS} , i_D
- Signal & response: v_{gs} , v_{ds} , i_d

Transistor

- MOS should be in saturation at all times!

- o Bias point in Saturation

$$V_{GS} > V_{tn}$$
$$V_{DS} > V_{GS} - V_{tn}$$

- o Signal amplitude cannot become too large (depends on Bias point!)

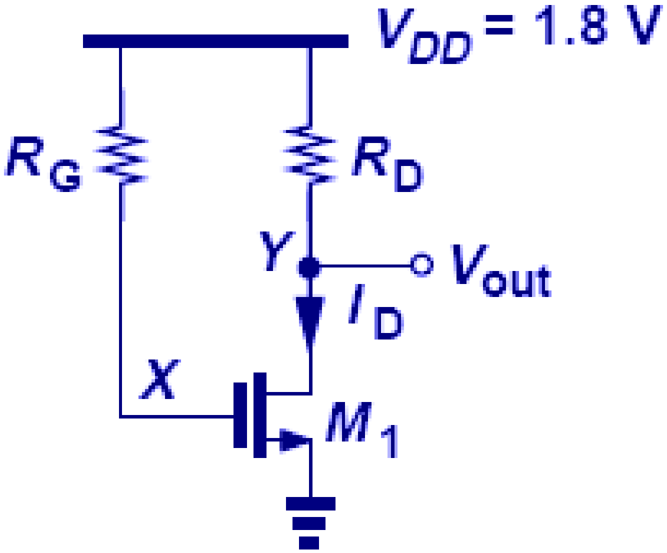
$$v_{GS} = V_{GS} + v_{gs} > V_{tn}$$
$$v_{DS} = V_{DS} + v_{ds} > V_{GS} + v_{gs} - V_{tn}$$

IMPORTANT POINTS

- **Signal:** We want the response of the circuit to this input.
- **Bias:** State of the system when there is no signal (current and voltages in all elements).
  - Bias is constant in time (may vary extremely slowly compared to signal)
  - Should be stable and robust bias point should be resilient to variations in $\mu_n C_{ox}(W/L), V_t$, … due to temperature and/or manufacturing variability.
  - Purpose of the bias is to ensure that MOS is in saturation at all times.
- **Response** of the circuit and elements to the signal is different than the response of the circuit and its elements to Bias (or to Bias + signal):
  - Different transfer functions for the circuit
  - Different iv characteristics for the elements, i.e. relationships among v_{gs} , v_{ds} , i_d is <u>different</u> than relationships among v_{GS} , v_{DS} , i_D .

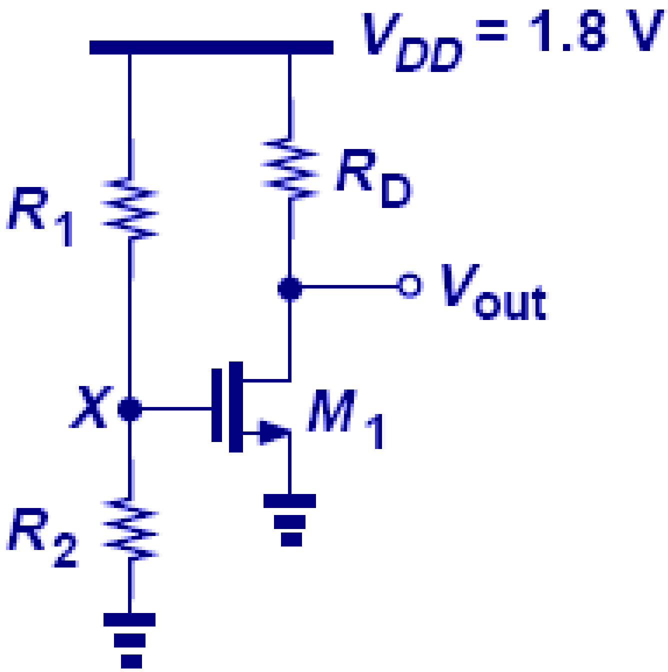
MOSFET biasing configurations

Biasing with fixed voltage



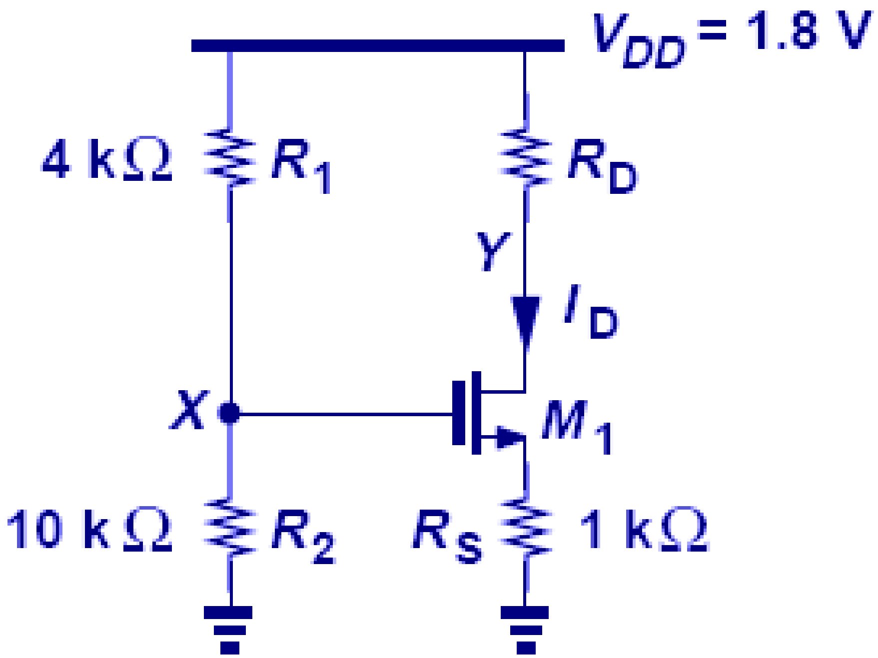
$$V_{GS}=V_{DD}$$

Biasing with voltage divider



$$V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD}$$

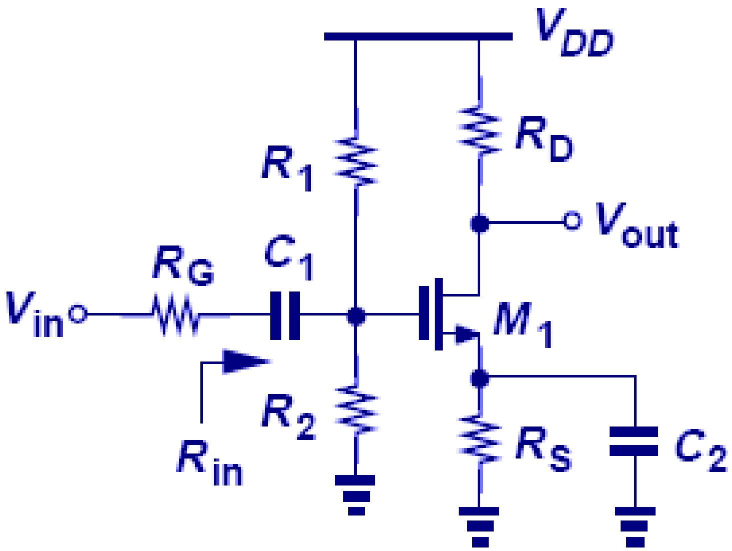
Biasing with Source Degeneration



$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1\left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH}\right)}$$

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_S}$$

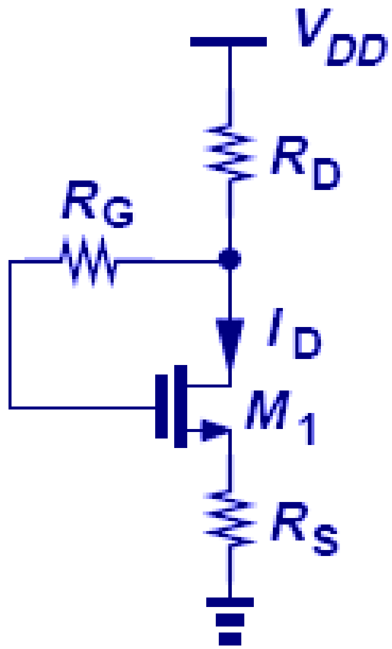
Source Degeneration with Bypass Capacitor



$$A_v = -\frac{R_1 \parallel R_2}{R_G + R_1 \parallel R_2} g_m R_D$$

It is possible to utilize degeneration for biasing but eliminate its effect on the small-signal by adding a bypass capacitor.

Self-biasing

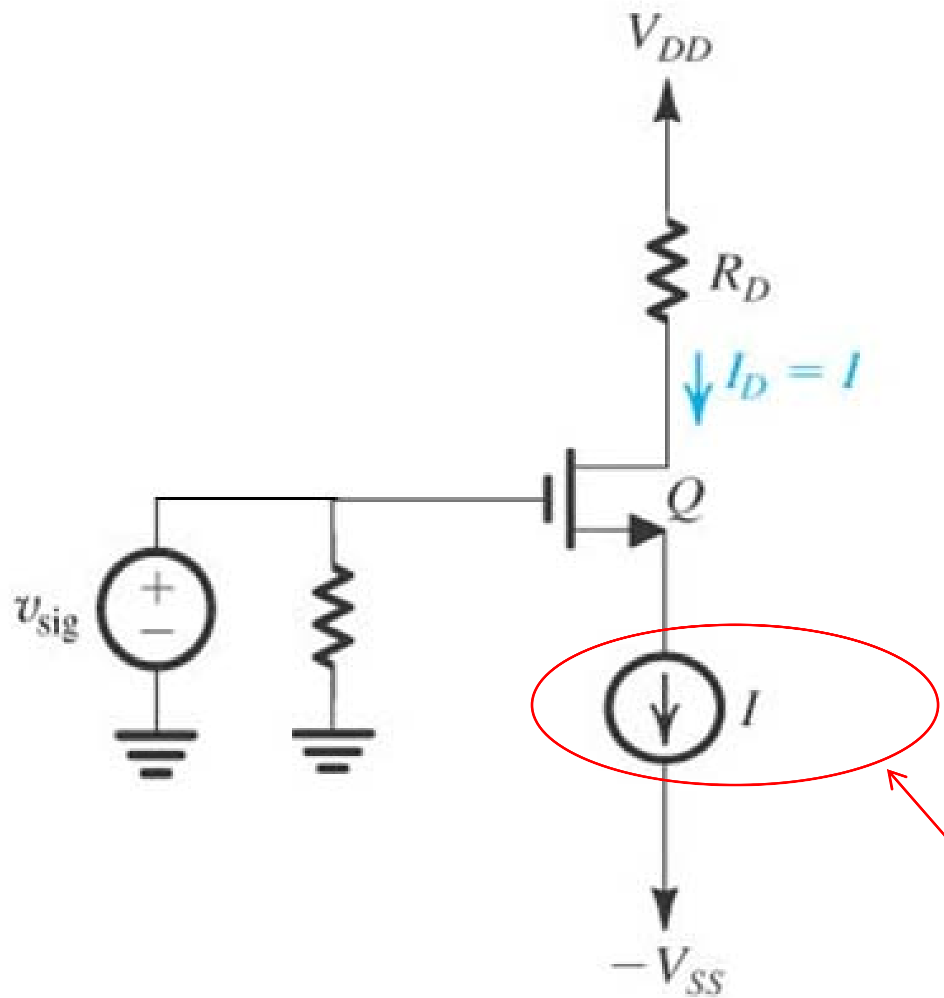


The self-bias configuration eliminates the need for two dc supplies as required for fixed-bias configuration. The gate voltage is provided by the drain with no voltage drop across R_G and M_1 is always in saturation.

$$V_{GS}=V_{DD}-I_D*R_D$$

Note that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

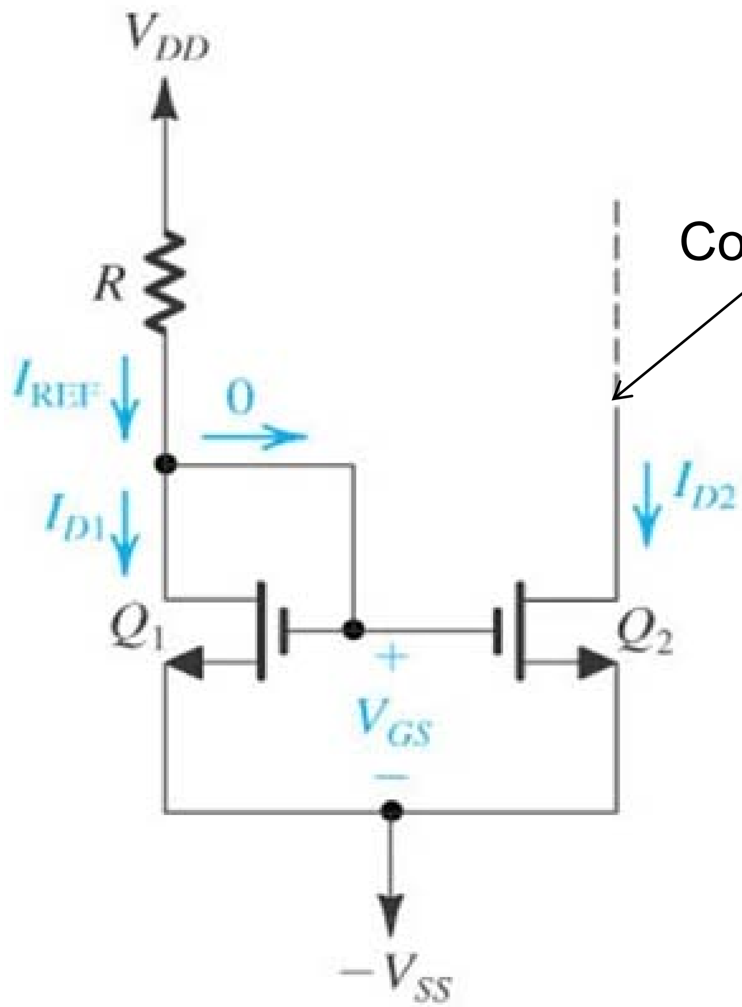
Biasing with current source



$$V_{GS}=V_{DD} - I*R_D$$

Current source I can be replaced with a current mirror design for better drain current stability.

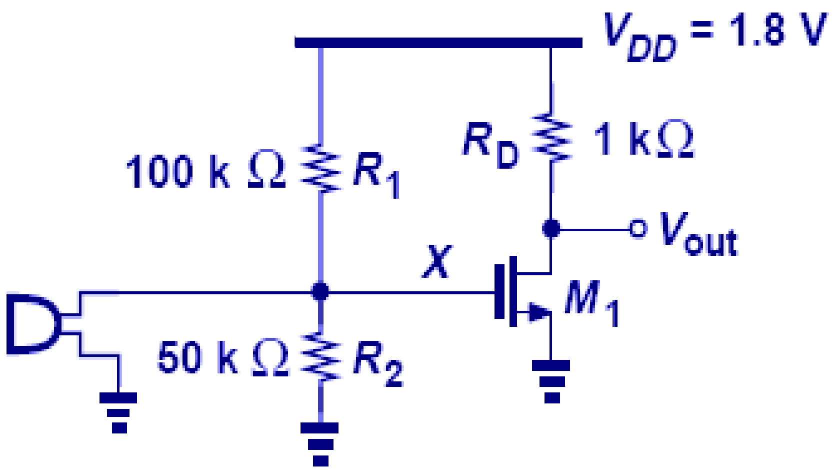
Biasing with a current mirror



Connect to the source leg of transistor Q

Current mirror design can maximize the drain current **stability.**

Example: Microphone Amplifier

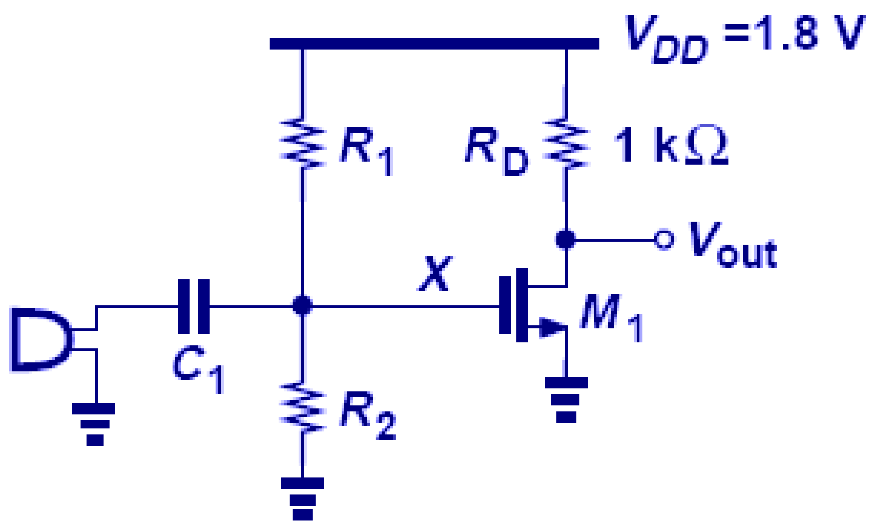


No Amplification!!

$$V_X = \frac{100\Omega \,||\, 50K\Omega}{100K\Omega + 100\Omega \,||\, 50K\Omega} \times 1.8V \approx 1.8mV$$

Because of the microphone’s small low-frequency output resistance (100Ω), the bias voltage at the gate is not sufficient to turn on M_1.

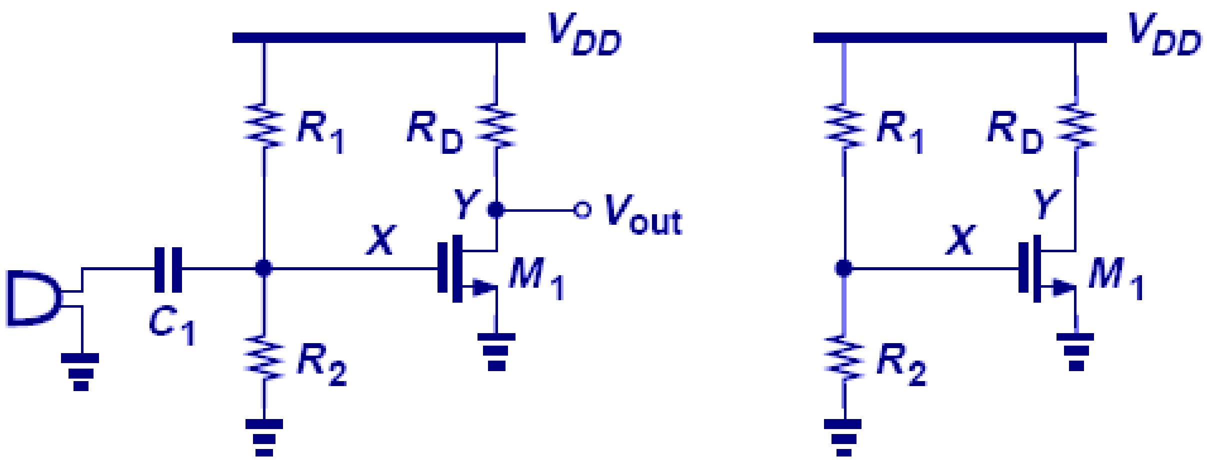
Capacitive Coupling



$$V_X = \frac{50K\Omega}{100K\Omega + 50K\Omega} \times 1.8V \approx 0.6V$$

To fix the problem in the previous example, a method known as *capacitive coupling* is used to block the DC content of the microphone and pass the AC signal to the amplifier.

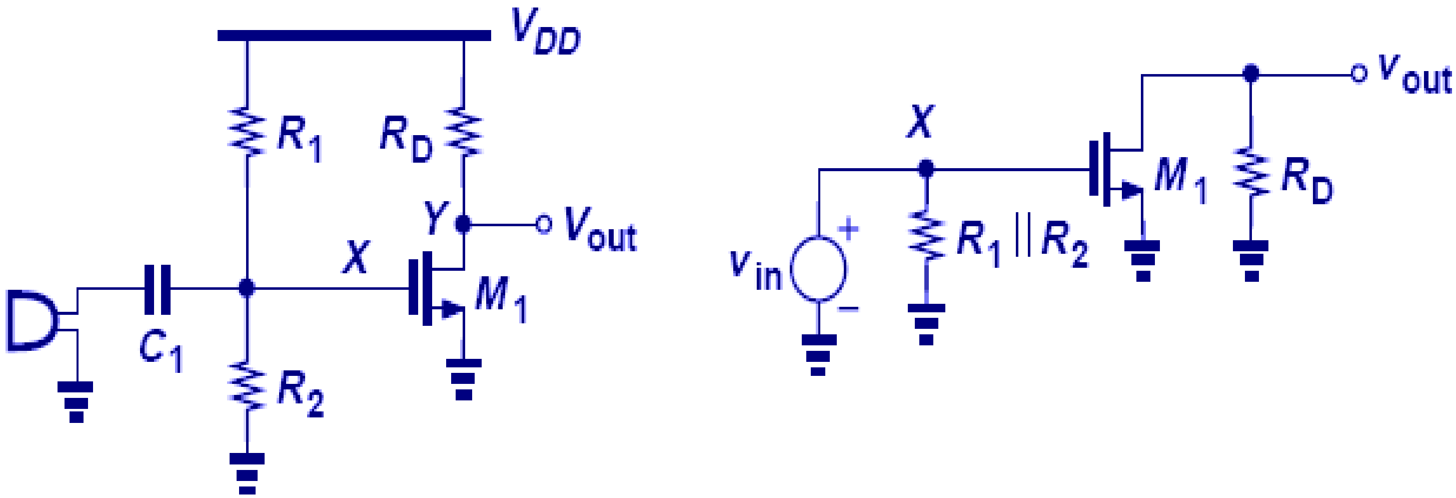
Capacitive Coupling: Bias Analysis



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD} - V_{TH}\right)^2$$

Since a capacitor is an open at DC, it can be replaced by an open during bias point analysis.

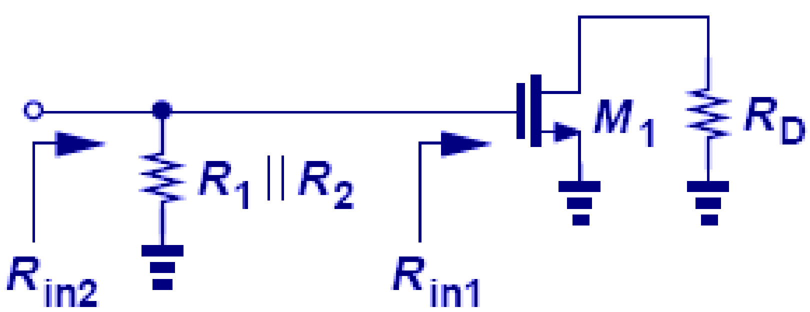
Capacitive Coupling: AC Analysis

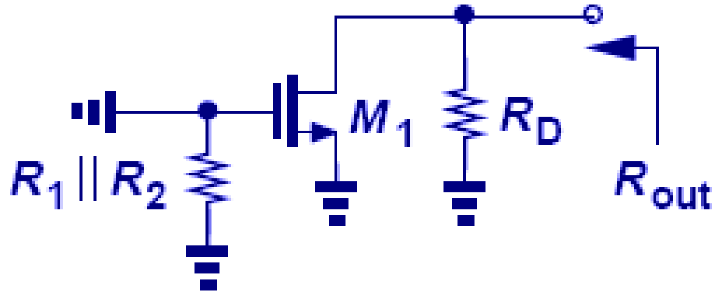


$$\frac{v_{out}}{v_{in}} = -g_m \left(R_D \parallel r_O \right)$$

Since a capacitor is a short at AC, it can be replaced by a short during AC analysis.

Capacitive Coupling: I/O Impedances



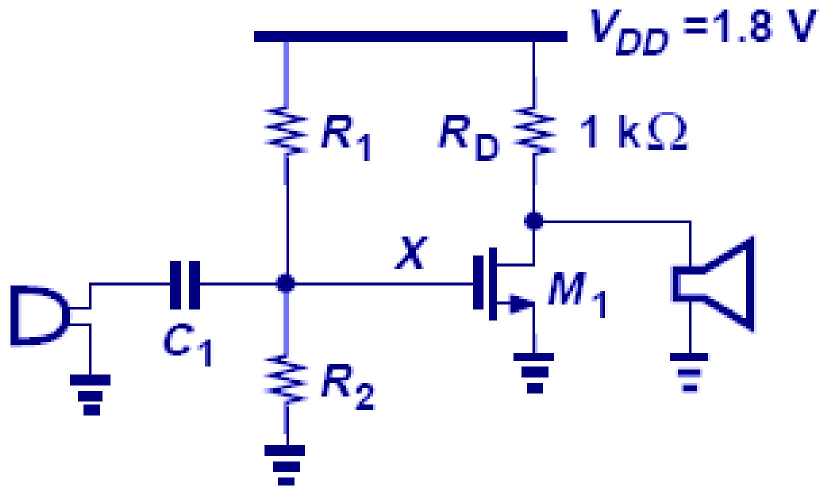


$$R_{in1} = \infty$$

$$R_{in2} = R_1 \parallel R_2$$

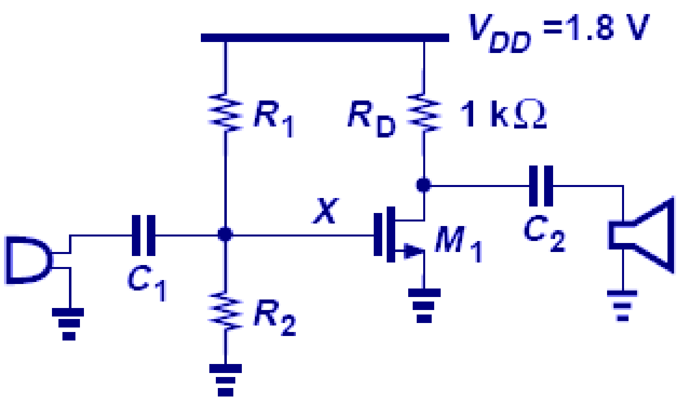
$$R_{out} = R_D \parallel r_O$$

Example: Amplifier with Direction Connection of Speaker

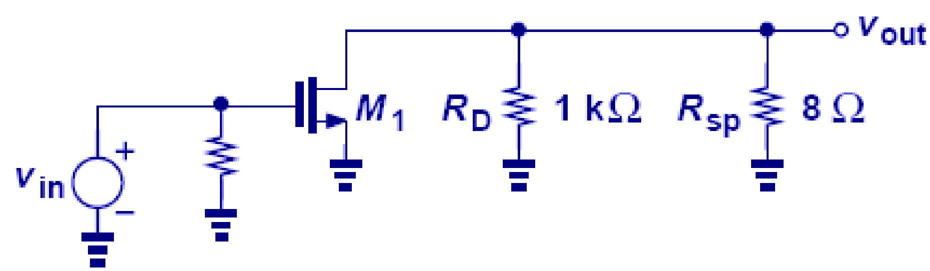


This amplifier design still fails because the solenoid of the speaker shorts the drain to ground.

Example: Amplifier with Capacitive Coupling at I/O



(a)



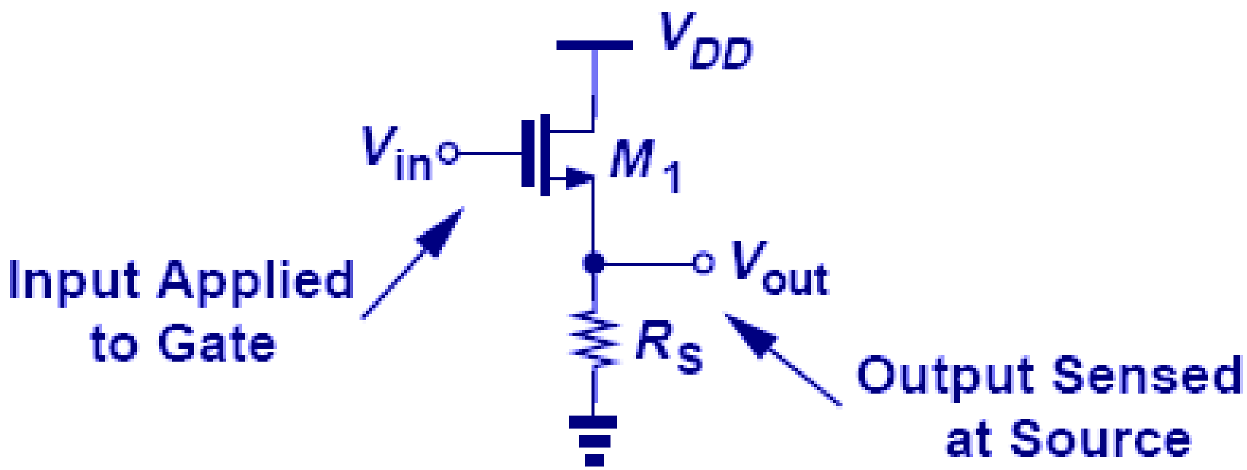
(b)

$$R_{eq} = R_D \,||\, R_{sp} \approx 8\Omega$$

$$|A_v| = g_m\left(R_D \,||\, R_{sp}\right) = 0.08$$

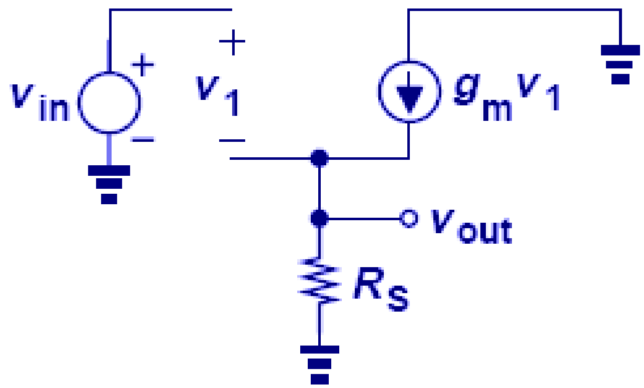
This amplifier design produces very little gain because its equivalent output resistance is too small.

Source Follower (common drain configuration)



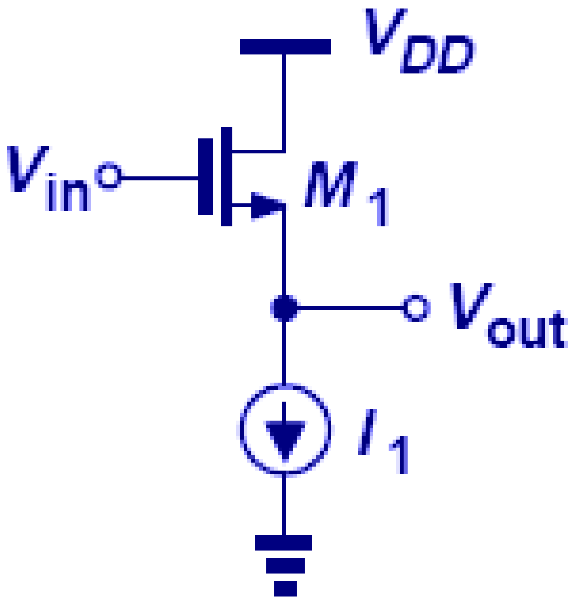
Source follower sense the input at the gate and produces the output at the source.

Small-Signal Model and Voltage Gain for Source Follower



$$\frac{v_{out}}{v_{in}} = \frac{R_S}{R_S + \frac{1}{g_m}}$$

Example: Source Follower with Current Source



$$A_v = 1$$

Acknowledgments

- Lecture slides are based on lecture materials from various sources, including Behzad Razavi (UCLA).

- Credit is acknowledged where credit is due. Please refer to the full list of references.