Example 1

(a)

$$F_1 = \bar{X}\bar{Y} + XY\bar{Z}$$

$$F_2 = \bar{X} + Y$$

$$F_3 = XY + \bar{X}\bar{Y}$$

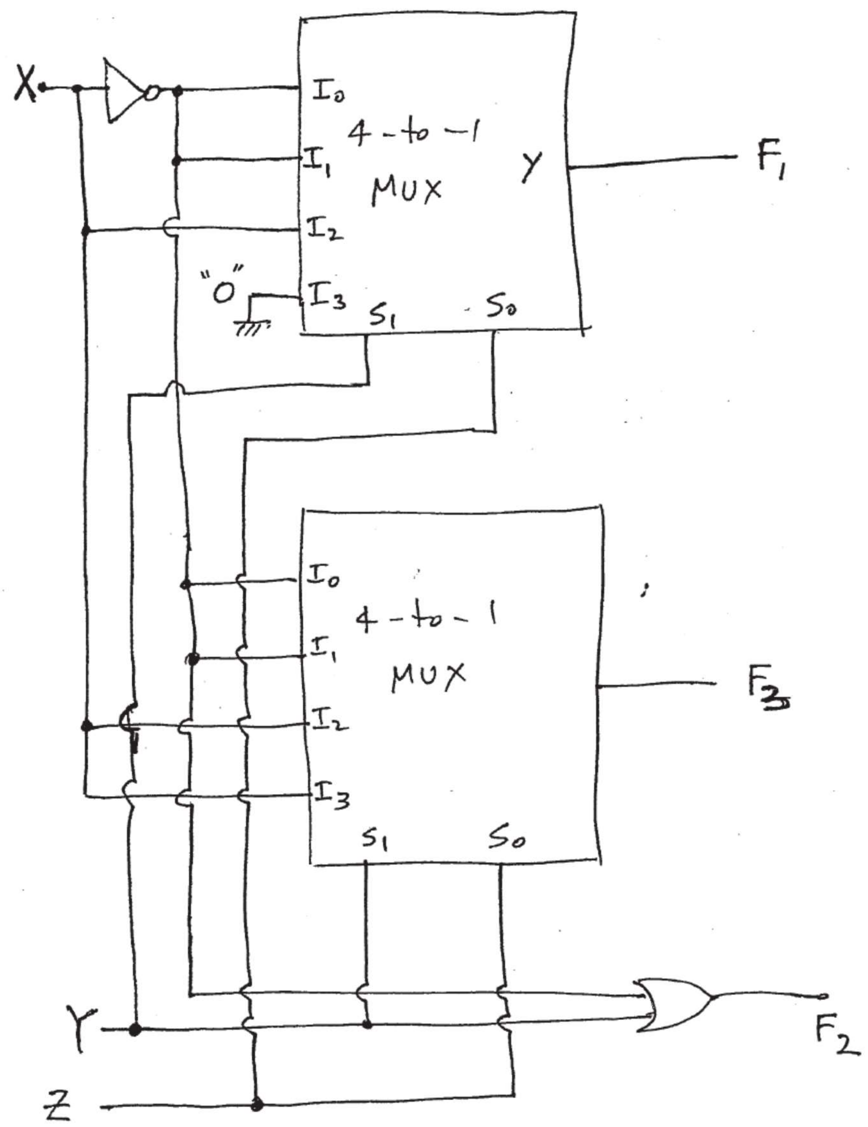
F_2 can be readily implemented using an inverter and an OR gate

Assign Y to S_1

Z to S_0

truth table

Y	Z	X	F_1	F_1	F_3	F_3
0	0	0	1	$I_0 = \bar{X}$	1	$I_0 = \bar{X}$
0	0	1	0		0	
0	1	0	1	$I_1 = \bar{X}$	1	$I_1 = \bar{X}$
0	1	1	0		0	
1	0	0	0	$I_2 = X$	0	$I_2 = X$
1	0	1	1		1	
1	1	0	0	$I_3 = 0$	0	$I_3 = X$
1	1	1	0		1	



(b)

$$F_1 = \overline{X}\,\overline{Y} + XY\overline{Z}$$

$$= \overline{X}\,\overline{Y}\,\overline{Z} + \overline{X}\,\overline{Y}Z + XY\overline{Z}$$

$$= \Sigma m\,(0, 1, 6)$$

X \ YZ	00	01	11	10
0	1	1		
1				1

$$F_2 = \bar{X} + Y$$

$$= \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + \bar{X}\bar{Y}\bar{Z} + \bar{X}YZ$$

$$+ \bar{X}YZ + \bar{X}Y\bar{Z} + XYZ + XY\bar{Z}$$

$$= \sum m(0,1,2,3,6,7)$$

X \ YZ	00	01	11	10
0	1	1	1	1
1			1	1

⇒ Note that $\bar{F_2}$ is a simpler expression $\bar{F_2} = \sum m(4,5)$.

$$F_3 = XY + \bar{X}\bar{Y}$$

$$= XYZ + XY\bar{Z} + \bar{X}\bar{Y}Z + \bar{X}\bar{Y}\bar{Z}$$

X \ YZ	00	01	11	10
0	1	1		
1			1	1

$$F_3 = \sum m(0,1,6,7)$$

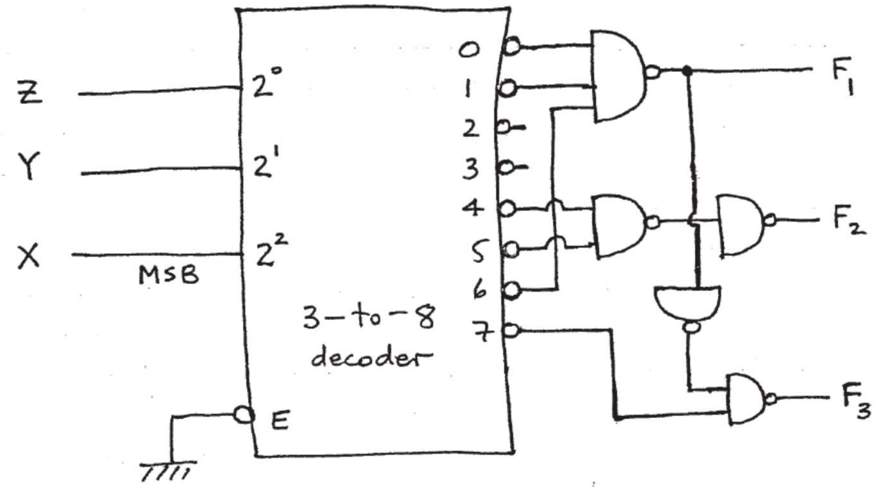
⇒ Note that $F_3 = F_1 + m_7$

$$= \overline{\overline{F_1 + m_7}}$$

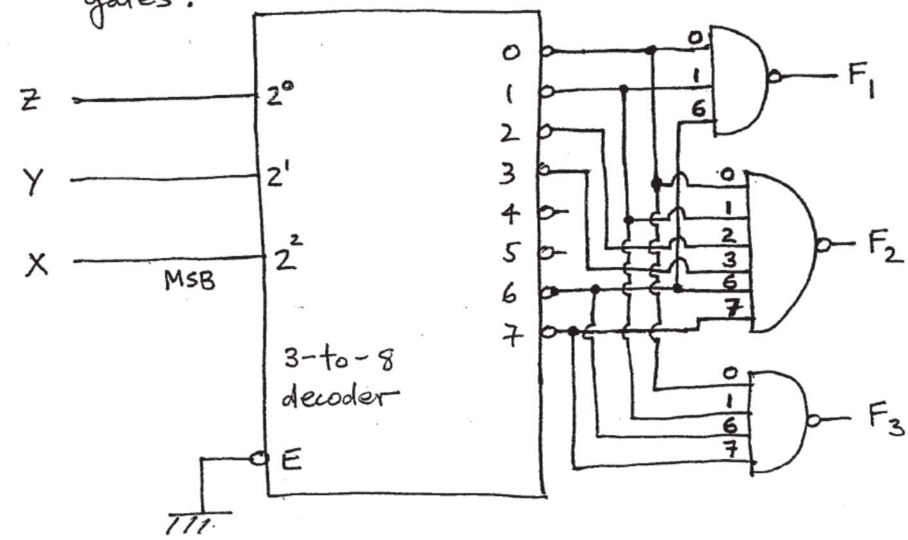
$$= \overline{\bar{F_1} \cdot \bar{m_7}}$$

ie NAND of $\bar{F_1}$ and $\bar{m_7}$

Hence using a 3-to-8 line decoder and NAND gates (minimum number of connections).

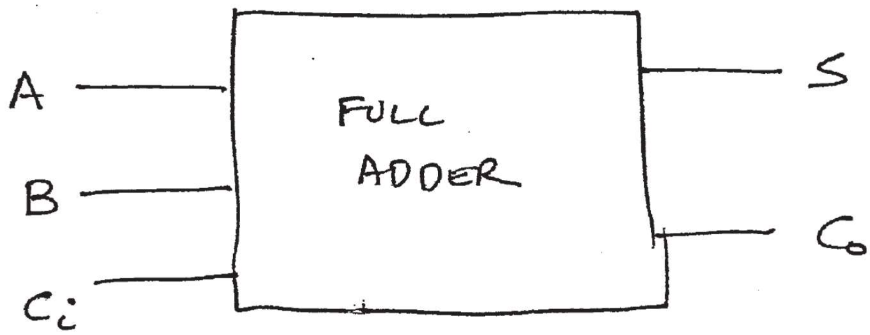


OR Using the minimum number of external gates:



Example 2

bits are A and B
Carry-in is C_i
Carry-out is C_o.
Sum is S.

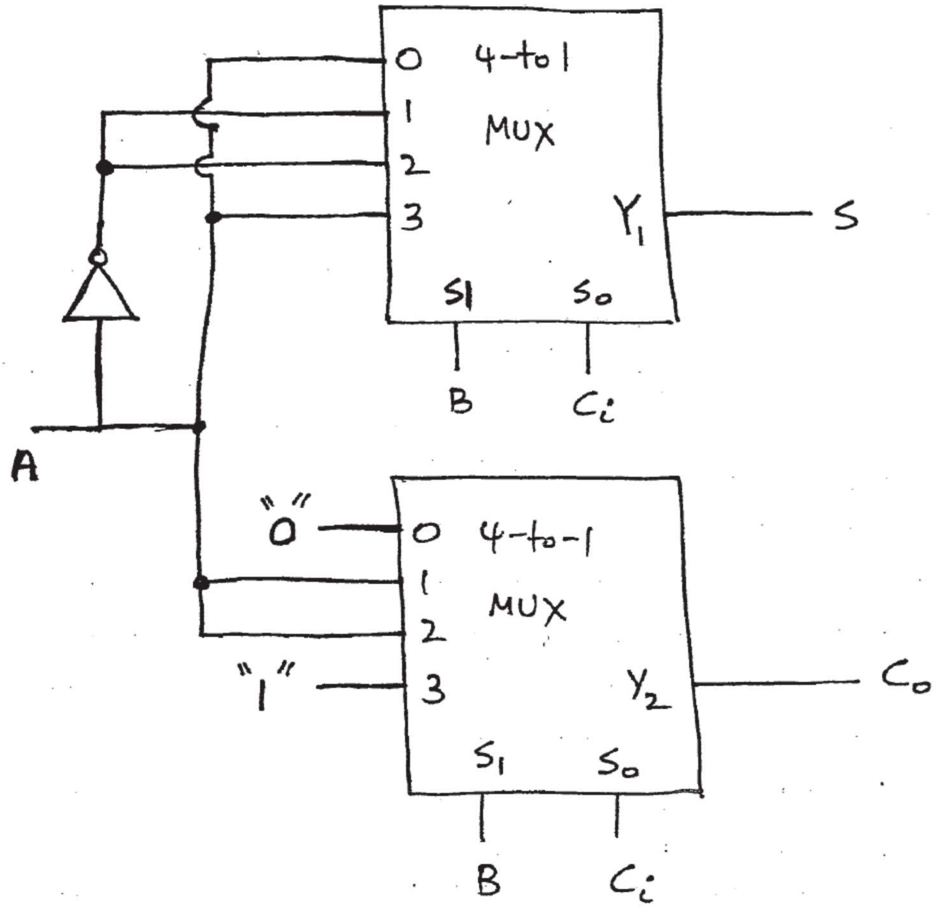


For a Full adder,

$$S(A,B,C_i) = \sum m\,(1,2,4,7)$$

$$C_o(A,B,C_i) = \sum m\,(3,5,6,7)$$

m	A	B	C_i	S	$I = BC_i$ SUM	C_o	$I = BC_i$ CARRY
0	0	0	0	0	$I_0 = A$	0	$I_0 = 0$
1	0	0	1	1	$I_1 = \bar{A}$	0	$I_1 = A$
2	0	1	0	1	$I_2 = \bar{A}$	0	$I_2 = A$
3	0	1	1	0	$I_3 = A$	1	$I_3 = 1$
4	1	0	0	1	$I_0 = A$	0	$I_0 = 0$
5	1	0	1	0	$I_1 = \bar{A}$	1	$I_1 = A$
6	1	1	0	0	$I_2 = \bar{A}$	1	$I_2 = A$
7	1	1	1	1	$I_3 = A$	1	$I_3 = 1$


0
1
2
3
4-to1
MUX
Y1
S
S1
So
B
Ci
A
"0"
"1"
0
1
2
3
4-to-1
MUX
Y2
Co
S1
So
B
Ci

Example 3

A	B	C	D	F	
0	0	0	0	0	I_0
0	0	0	1	0	I_0
0	0	1	0	1	I_0
0	0	1	1	1	I_0
0	1	0	0	0	I_1
0	1	0	1	0	I_1
0	1	1	0	0	I_1
0	1	1	1	0	I_1
1	0	0	0	1	I_2
1	0	0	1	0	I_2
1	0	1	0	1	I_2
1	0	1	1	0	I_2
1	1	0	0	0	I_3
1	1	0	1	1	I_3
1	1	1	0	1	I_3
1	1	1	1	0	I_3

$I_0 = C$

$I_1 = 0$

$I_2 = \overline{D}$

$I_3 = C \oplus D$

can only use inverters and 2-input NOR gates

$$I_3 = C \oplus D = \overline{C}D + C\overline{D}$$
$$= \overline{\overline{\left(\overline{C + \overline{D}}\right) + \left(\overline{\overline{C} + D}\right)}}$$ using De Morgan Theorem
$$= \left(\overline{C+\overline{D}}\right) + \left(\overline{\overline{C}+D}\right)$$