点亮LED灯

```
module led(
        input   clk,//开发板晶振频率50MHz
        input   rst_n,//复位下绛沿有效
        output  reg     ld //led灯
);
reg [25:0]      cnt; //时钟寄存器

//计时器模块
always@(negedge rst_n or posedge clk)begin
        if(!rst_n)begin
                cnt <= 26'd0;//初始化计时器为0
                ld <= 1'b1;//初始化led灯，高电平有效
        end
        else if(cnt == 26'd50_000_000-1)begin
                cnt <= 26'd0;
                ld <= ~ld;//1s钟led取反
        end
        else begin
                cnt <= cnt + 26'd1;
                ld <= ld;//其他时刻，led等于其自身
        end
end
endmodule
```