

PROJECT S.A.I.C

Hancis Bogdan

Group 2331

Cuprins:

- 1. Specificatii individuale. Specificatii generale.
- 2. Etaj 1 Amplifier
- 3. Etaj 2 Filters
- 4. Etaj 3 PGA
- 5. Etaj 4 Rectifier
- 6. Block Diagram

1. Specificatii individuale:

	Etaj 1						Etaj 2				Etaj 3					Etaj 4		AO	
Sursa semnal	amplitudi ne minima (pt castig maxim PGA)	ine maxima	unitate	Tip Etaj 1	Castig etaj 1 (liniar)	tip Etaj 2	H0 castig liniar in banda de trecere	Rintrare minim	Banda	ď	tip Etaj 3	castig minim [dB]	rezolutie (pas minim) [dB]	nr pasi	castig maxim [dB]	Rintrare minim	tip Etaj 4	Castig etaj 4 (liniar)	Tip AO
2	6.29E-03	2.51E-02	V (differe	4	10	8	depinde d	2.00E+03	2.00E+03	1.41	6	6	3	5	18		10	2	12

Specificatii generale :

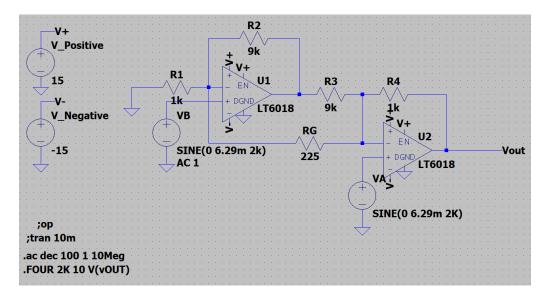
	Etaj 1 - amplificator													
Sursa sem nr.	nal	nr	semi	nal Intrare		semn iesir		tip		Castig (liniar) [V/V I/V, V/I]	, Rin_min [Ohms]	reglaj Out_DC	banda*	liniaritate
	2	4	tensiune			tensiu	Amplif instrur ne neinve	nentatie	cu 2 AO	spec individ	ual		> fin_max	fara distorsiuni la fin_max pt ampl_in*castig (SR, THD<1%)
										_	Etaj 2 - Filtru			
				semnal			H0 castig in banda de trecer	e						
Etaj 1	nr		semnal Intrare	iesire	tip functie de transfer	topologie	[V/V sau I/V]	Rin_min	BW	f0	frecventa centrala filtru trec	e-banda	Q	liniaritate
1,2,3,4,5,6,7,10		8 tensiune		tensiune	trece-banda BPF	Rauch	depinde de Q	2.00E+03	spec individu	ial BW*Q				amplitudinea de la iesire = (amplitudinea de la intrare)X(castigul in banda de trecere) pentru un semnal armonic cu frecventa = frecventa centrala BPF

		Et	aj 3 - PGA					
			rezolutie					
			(pas					
		contract of the files	minim)		castig maxim			11 -1 - 11 - 1 -
Nr	tip	castig minim [dB]	[dB]	numar pasi	[dB]	Rin_min [Ohms]	banda	liniaritate
								fara distorsiuni
								la fin_max pt
								ampl_in_min*c
								astig_max_PGA
								si
								ampli_in_max*
	neinversor,		spec					castig_min_PG
	comutatoare in							Α
	_	spec	individua	spec	spec			(THD<1%)
		individual		individual	individual		> Fin_max	

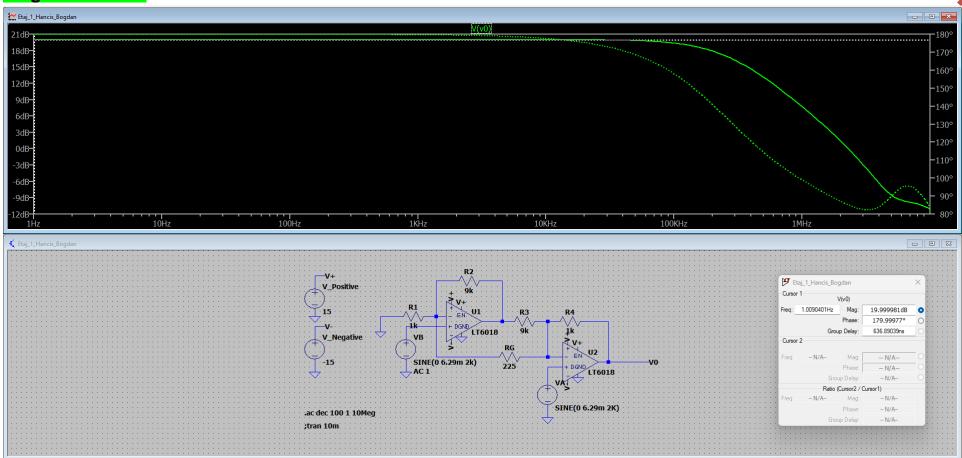
Etaj 4 - Redresor/Convertor AC-DC/Detector de varf									
tip	castig [V/V] semnal mare - circuitul are functia dorita pe domeniul=								
Redresor									
dubla									
alternanta									
FWR v10	spec individual	vin_max*castig							

Tip Amplificator Operational AO							
LT6018	+/-15V						

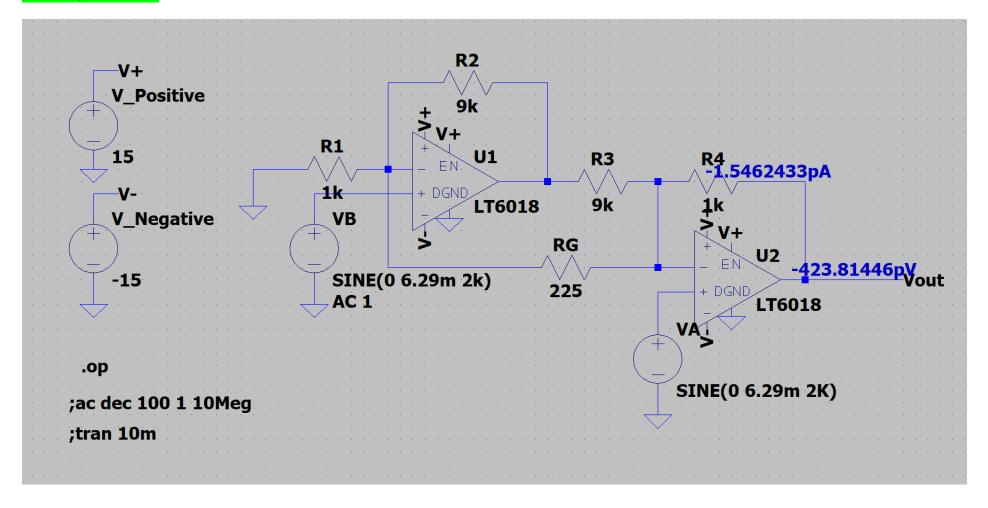
2. Etaj 1 - Amplifier



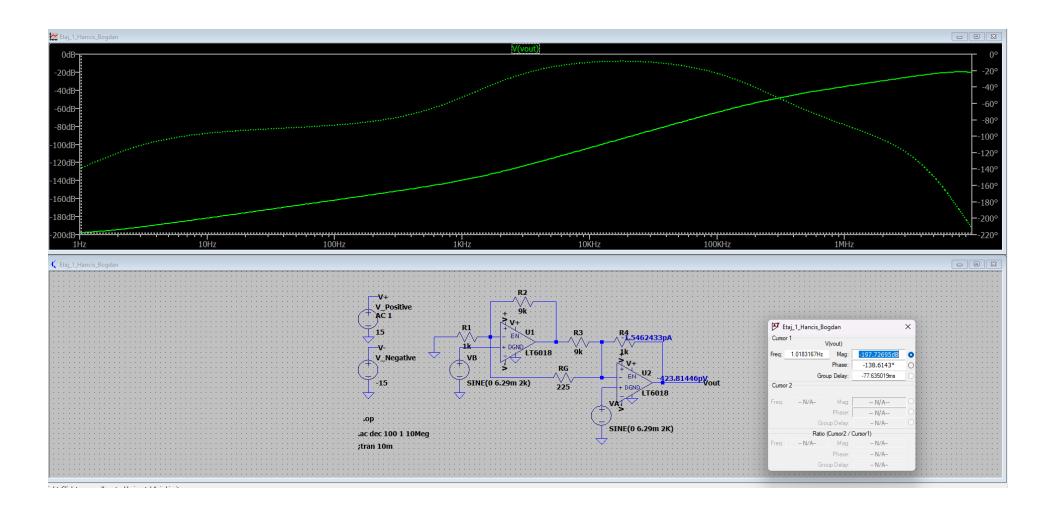
Original circuit:



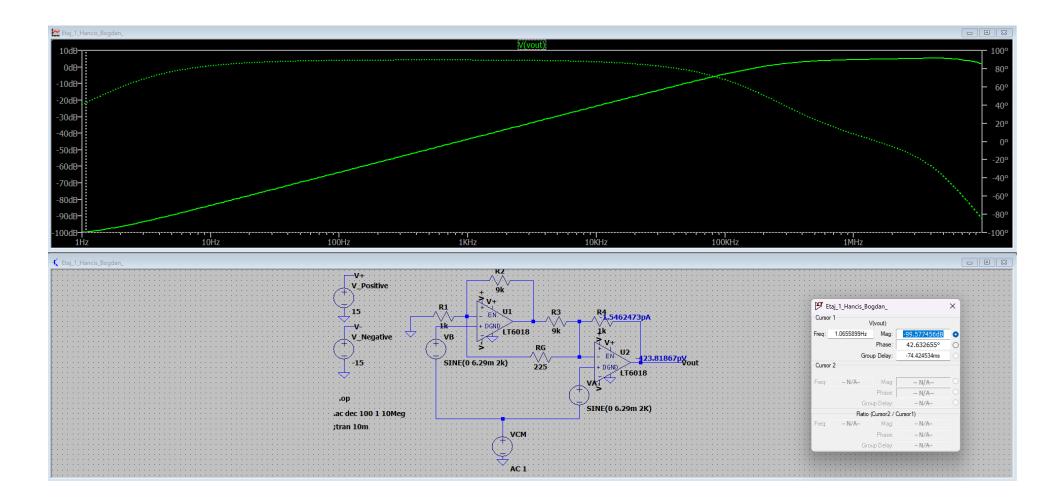
->compensarea



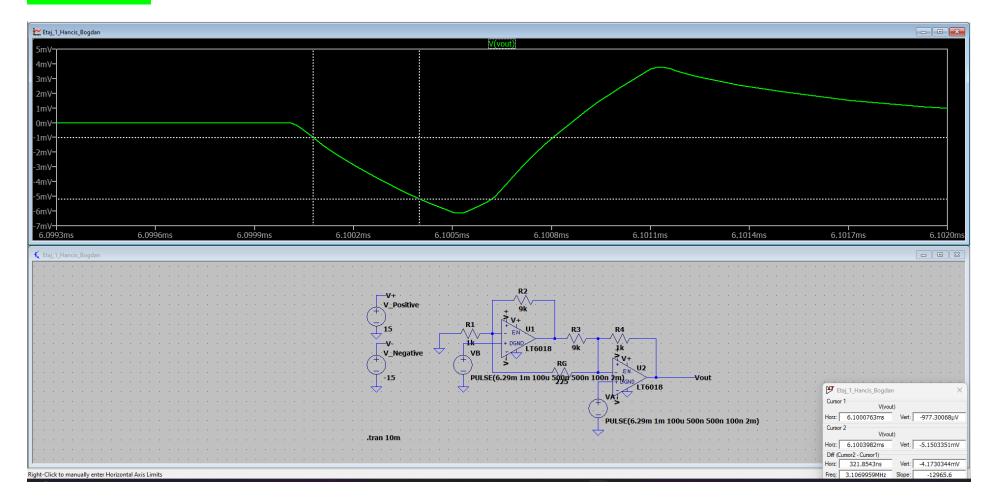
→PSRR=20dB-aps



→CMRR

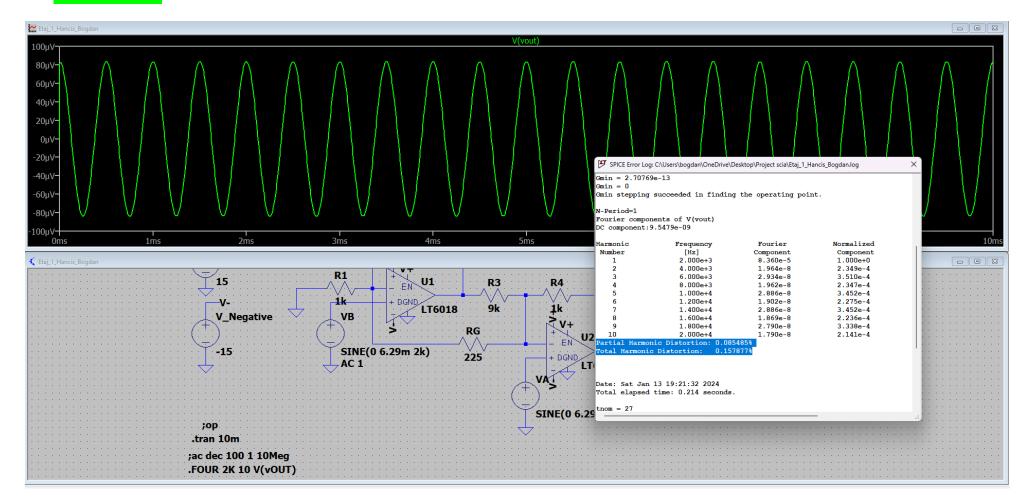


→Slew-Rate



For this circuit from "Etaj 1" we need to add a Voltage Source as Pulse , with specific parameters .

→ THD < 1%



3. Etaj 2 - Filter

→ Parameters :

$$Q = 1.41$$

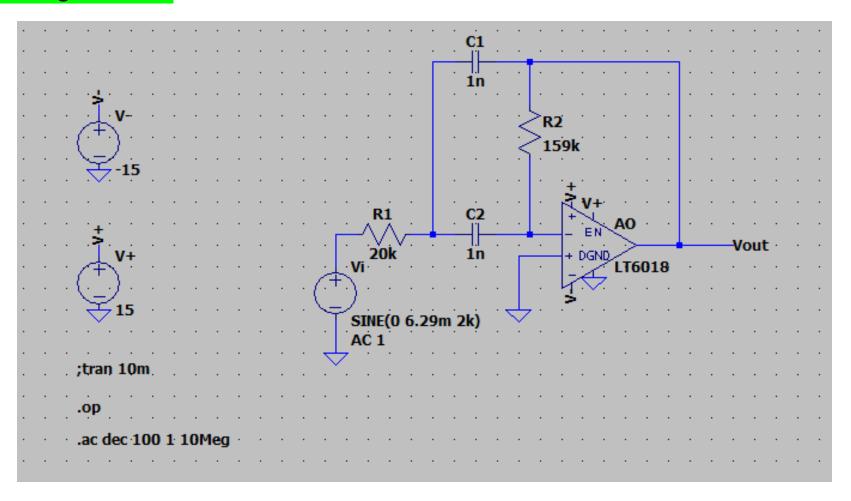
$$\omega_0$$
= 2 * π * F0 => ω_0 = 17709,6 rad/s

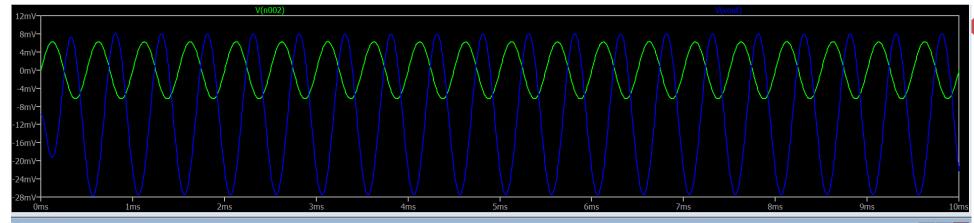
$$H_0 < 2 * Q^2 => H_0 < -3.97$$

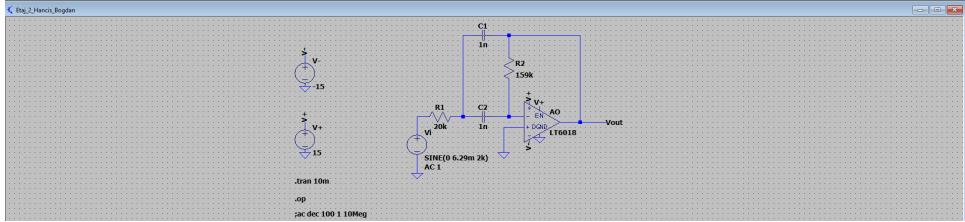
$$R1 = \frac{1}{2*\omega_0*Q*C}$$
 => R1 = 20k

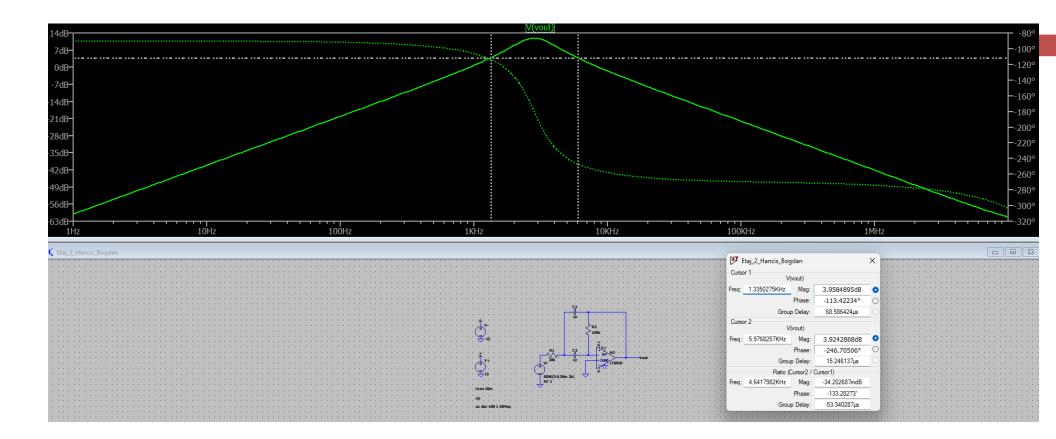
$$R2 = \frac{2*Q}{\omega_0*C}$$
 => R2 = 159k

→ Original circuit



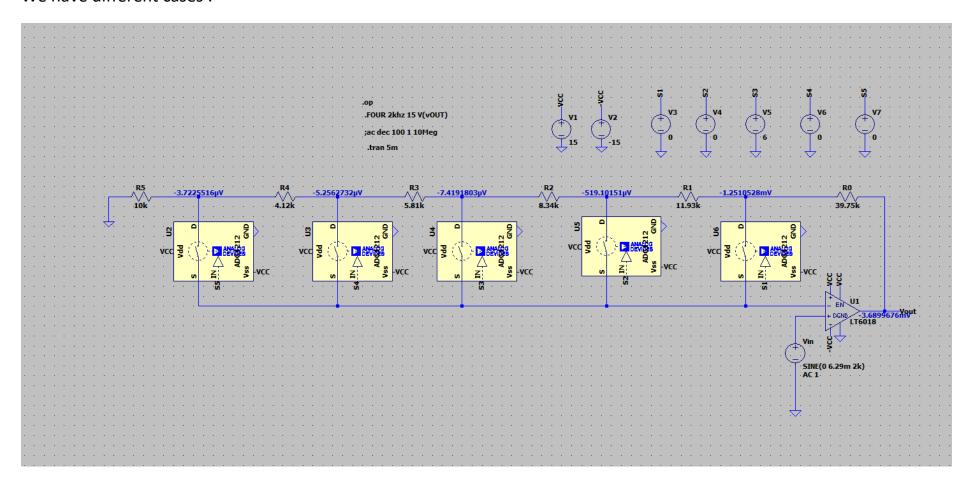




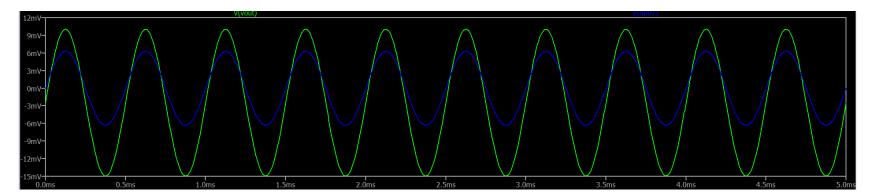


3. <u>Etaj 3 - PGA</u>

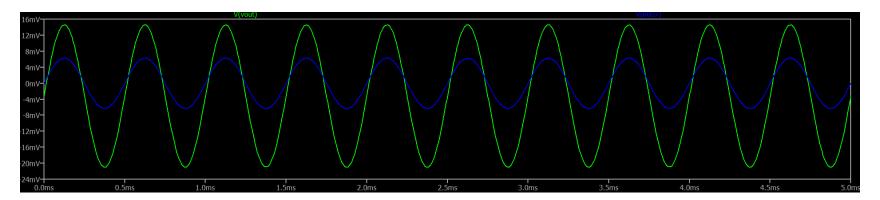
We have different cases :



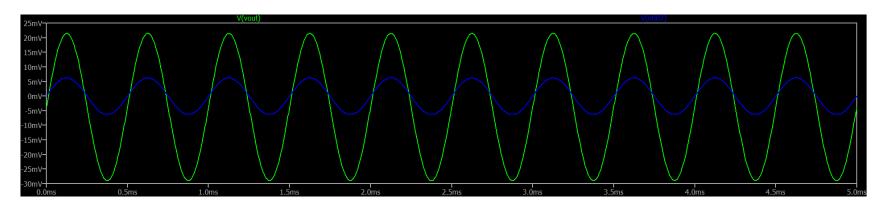
First switch open:



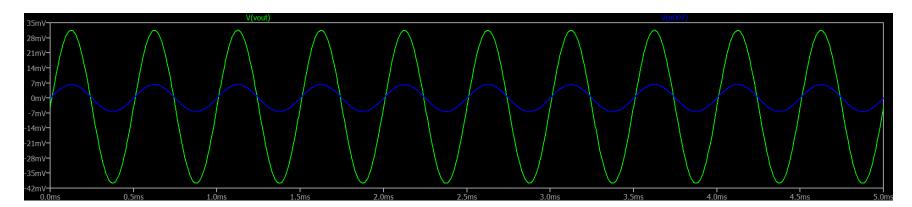
Second switch:



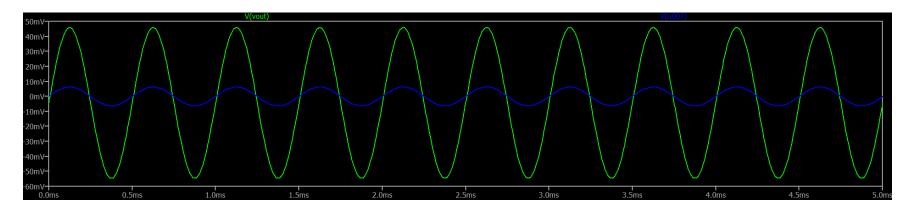
Third Switch:

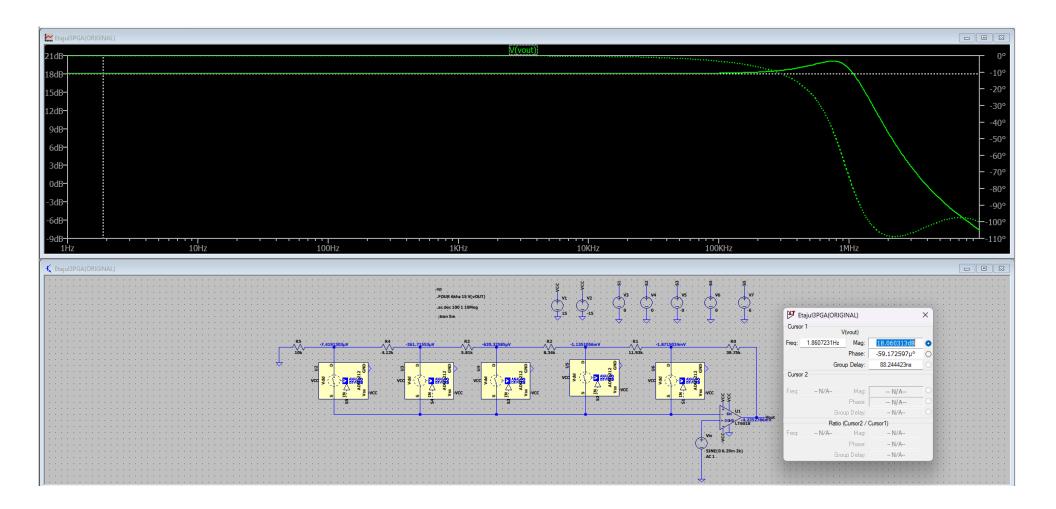


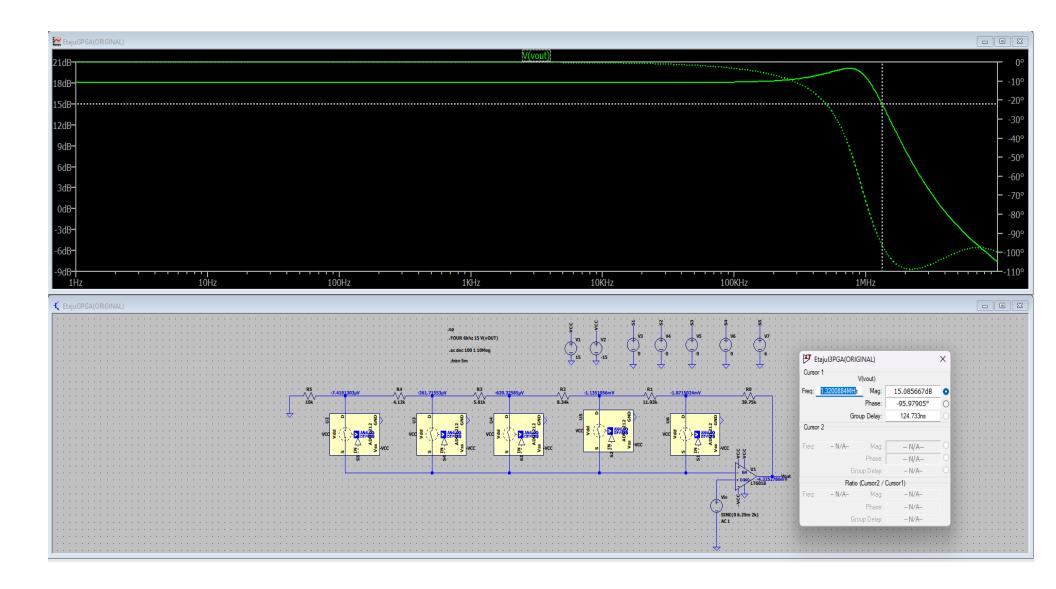
Fourth Switch:



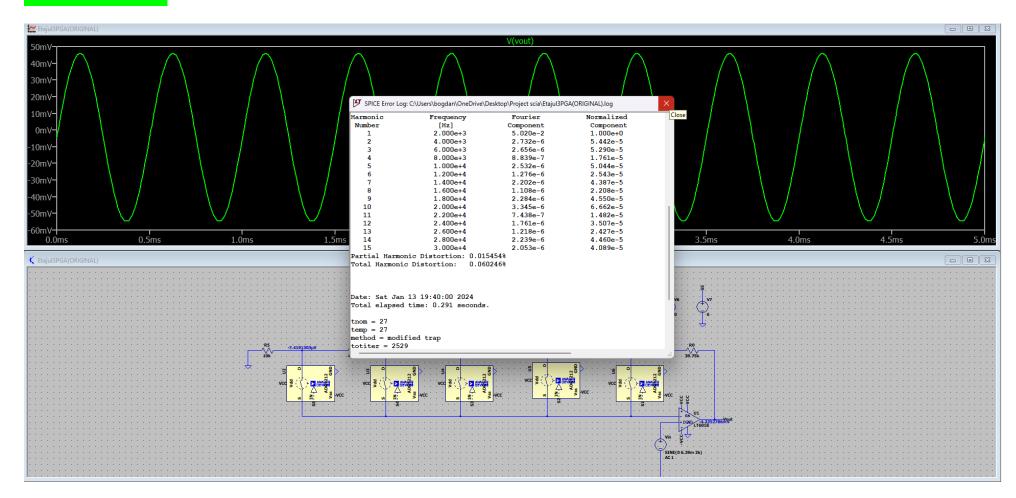
Fifth Switch:



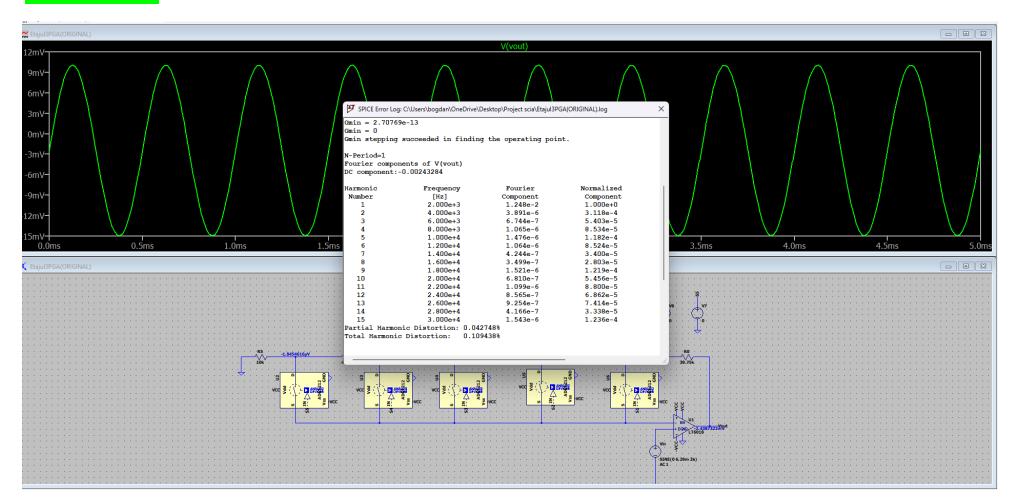




→ Switch max

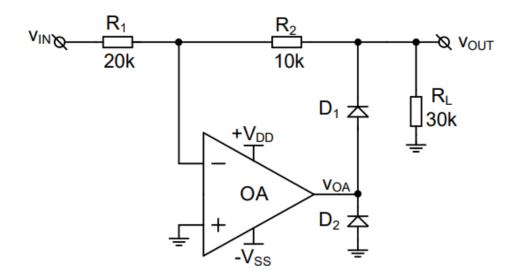


→Switch min



4. Etaj 4 - Rectifier

Full-Wave Rectifiers Implemented with OAs and Diodes single-OA implementation: Analysis



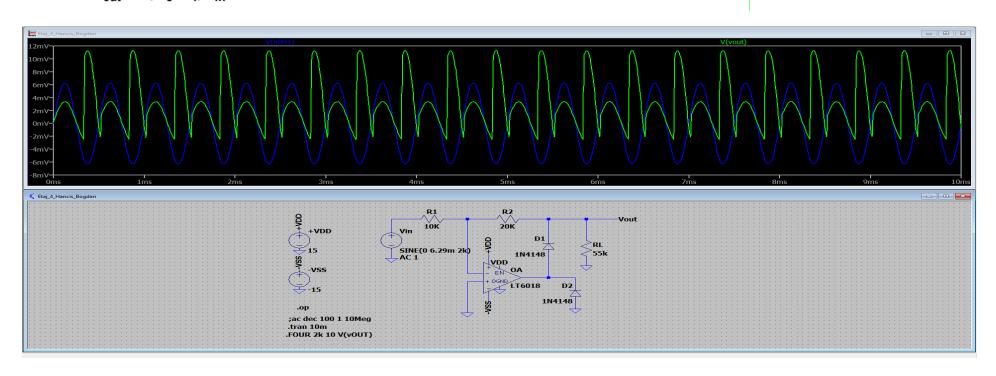
Vin>0

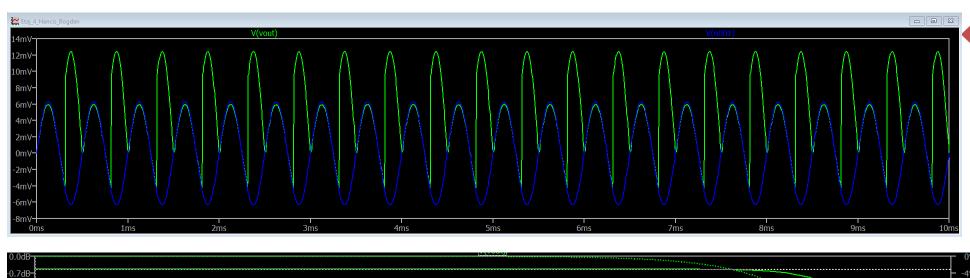
Assume D₁, D₂ = OFF $V_1^+ = 0$; $V_1^- > 0 \Rightarrow V_{OA1} \supset V_{OL} \Rightarrow D_1 = ON$; D₂ = OFF AO1 has negative feedback thru D1 $V_1^- = V_1^+ = 0$ $V_1^- = V_2^- \Rightarrow \text{ no current through R}_2 \text{ and R}_3$ $V_0^- = V_0^- = -(R_5/R_4)V_{in}$

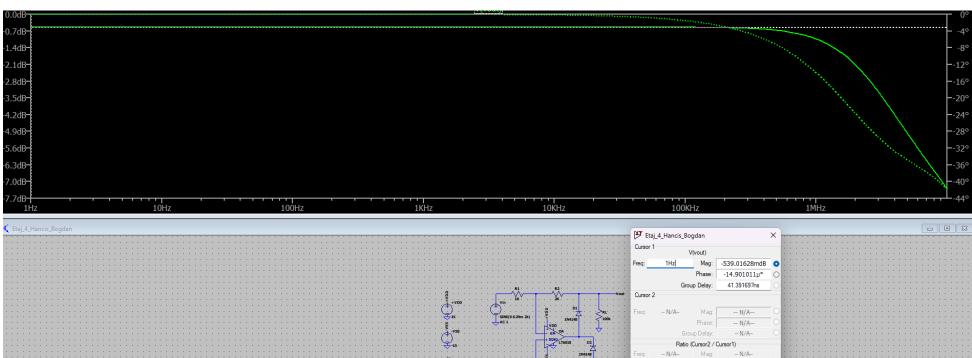
Vin<0

Assume D_1 , $D_2 = OFF$ $V_1^+ = 0$; $V_1^- < 0 \Rightarrow V_{OA1} \nearrow V_{OH}$ $=> D_1 = OFF$; $D_2 = ON$

AO1 implements an Inverting Amplifier => $V_{01} = -R_2/R_1Vin$







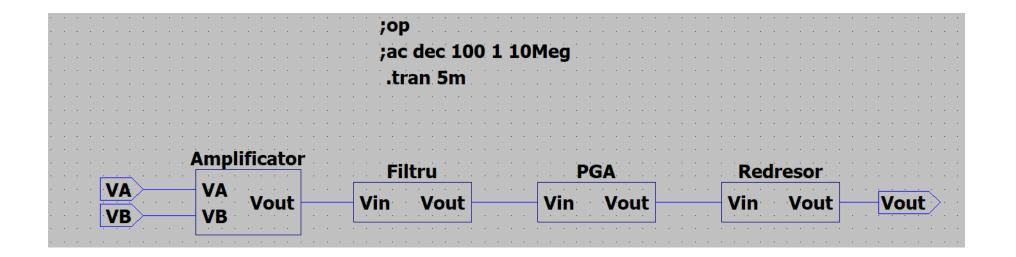
- N/A-- N/A-

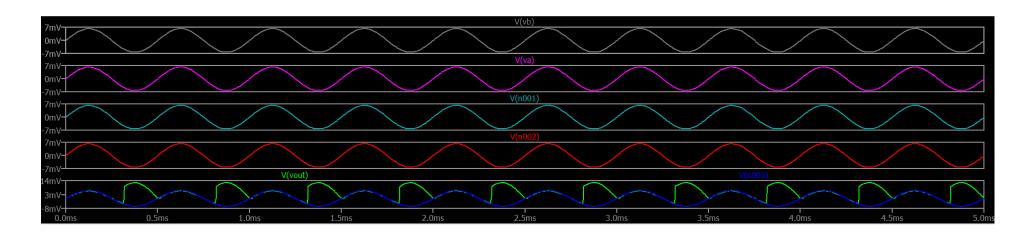
-- N/A--

Phase: Group Delay:

5. <u>Block diagram :</u>

In this section, we will show a block diagram containing all circuits we used:





6. Bibliography:

- 2022-23 SwAIC4 MNeag ContinuousTimeFilters.pdf
- 2022-23_SwAIC6_MNeag_InstrumentAmplifiers.pdf
- 2022-23 SwAIC7 MNeag NonlinearCircuitsWithOpAmps.pdf
- 2022-23 SwAIC9 MNeag SignalGenerators.pdf