**Problem Set 1: Hardware Design Using VHDL**

Graphical user interface, text, application

Description automatically generated

Diagram, schematic

Description automatically generated

Table

Description automatically generated

|  |  |  |  |
| --- | --- | --- | --- |
| **b signal** | **ALMs** | **ALUTs** | **dedicated logic registers** |
|  |
| signal | 9 | 17 | 0 |  |
| "000…001" | 8 | 16 | 0 |  |
| "00…1…00" | 5 | 9 | 0 |  |
| "100…000" | 0 | 0 | 0 |  |
| "1010…10" | 8 | 15 | 0 |  |

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1. Unsigned 31 < 2^5 then 6 bit is too much, then 5 bits.
2. Unsigned 57 < 2^6 then 7 bit is too much, then 6 bits.
3. Signed . 57 with 0 at MSB, then 6 bits only for positive. And one bit in MSB for negative. Then 7 bits is required.
4. Signed. 2020 with 0 at MSB , then considering that 2^11 > 2020 then 12 bits too much. Then 11 bits only for positive part, with MSB 0. Considering that – 1986 is also < 2^11 and > 2^10 then for negative is ok 11 bits that we have for positive. So only 1 bit more is required for twos complement negative part . So finally is required 12 bits.
5. Unsigned . 68719476736 . Lets divide repeatedly this number by two. The remainder repeatedly goes in each column from right side. 68719476736 / 2 = 34 359 738 368 so 0 goes in the 1-st column. So on …

68719476736 / 2 = 34 359 738 368 0

34 359 738 368 / 2 = 17 179 869 184 0

17 179 869 184 / 2 = 8 589 934 592 0

8 589 934 592 / 2 = 4 294 967 296 0

4 294 967 296 is 2 ^ 32 so 33 bits plus 4 are required. 37 bits

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Text

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Text

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See the project folder.