Bohan Hu

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EDUCATION

Georgia Institute of Technology (Gatech) **Shenzhen, China & Atlanta, GA**
Master of Electrical and Computer Engineering, **GPA:** 4.0/4.0 08/2021 - 08/2022
Courses: Advanced Computer Architecture, Advanced Programming Techniques, Digital System Test

Harbin Institute of Technology (HIT) **Shenzhen, China**
Bachelor of Engineering in Computer Science, **GPA:** 89/100 09/2017 - 07/2021
Courses: C Programming, Computer Architecture, Compiling Theory, Digital Circuit, Deep Learning Architecture

University of California, Berkeley **Berkeley, CA, USA**
Summer School, **GPA:** 4.0/4.0 06/2019 - 08/2019
Courses: Machine Structures, Academic English Reading and Writing

RESEARCH EXPERIENCE

Hardware-Accelerated Binary Translation, Pengcheng National Laboratory **Shenzhen, China**
Research Intern 05/2021 - 09/2021
- Built a heterogeneous SoC with 2 different CPU cores using Chisel, based on Tilelink interconnection
- Co-designed the SoC with NEMU (NJU-EMU, a QEMU-like binary translator) software
- Introduced a separate controller to make binary translation acceleration hardware transparent to other hardware
- Implemented the inter-core communication with RoCC interface, interruption and MMIO

Proof-of-Concept for RISC-V Virtual Memory Extension, Chinese Academy of Sciences **Beijing, China**
Participant, Advised by RISC-V Virtual Memory Task Group 04/2021 - 05/2021
- The *Zsa* extension drafted by RISC-V foundation aims at resolving the difficulty in maintaining the coherence when implementing the hardware-managed page table entry policy
- Implemented the hardware part of the extension on Rocket Core by modifying the memory management unit
- Support the designated modified address translation algorithm. Capable of booting Linux
- The technical report is accepted by *RISC-V World Conference, China, 2021*

Floating-Point Reciprocal & Reciprocal Square Root Unit Optimization, Chinese Academy of Sciences **Beijing, China**
Awarded *Outstanding Undergraduate Thesis of Harbin Institute of Technology, 2021*
Research Assistant, Advisor: Dr. Wenxiang Wang, Institute of Computing Technology 09/2020 - 04/2021
- Analyzed the performance of floating-point reciprocal and reciprocal square root algorithm and improved the throughput by 30x by modifying the architecture of FP reciprocal and reciprocal square root unit from non-pipelined to pipelined fashion
- Modelled the pipelined algorithm using C language and verified the functionality of instruction with QEMU
- Reduced latency while maintaining a reasonable precision: from 30 non-pipelined cycles with 23-bit precision to 4 pipelined cycles with 14-bit precision
- Applied hardware-efficient Newton-Raphson iteration method for higher accuracy output with only additional 15 pipelined cycles, which reaches higher ILP (Instruction Level Parallelism) in software loops on Out-of-Order processors
- Use a hardware/software codesign approach, modify the GCC compiler to enable iterations for higher accuracy
- RTL design using Verilog, simulation using VCS and Verilator, synthesis using Design Compiler
- Target frequency of 3.5GHz on 14nm technology node

ACADEMIC PROJECTS

MIPS Out-of-Order Superscalar Processor on FPGA, HIT **Shenzhen, China**
Team Lead, Advisor: Prof. Hongpeng Wang 07/2020 - 08/2020
- Self-learned micro-processor design and implemented a 10-stage Out-of-Order superscalar processor, with 2-way fetch, 2-way dispatch, 4-way issue, 2-way commit
- Implemented features: (1) GShare / TAGE overriding branch predictor, with a 256-entry Branch Target Buffer and a 16-entry Next Line Predictor; (2) Pipeline flushing on branch misprediction and precise exception handling; (3) 2 integer units, 1 pipelined multiplication and division unit and 1 pipelined load/store unit, with grouped bypass network; (4) 4KiB 4-way instruction cache with Pseudo-LRU replacement policy and 16KiB non-blocking data cache to avoid stalling the load/store pipeline on cache misses; (5) Use ROB to force the MMIO access seen in order; (6) Explicit register renaming to handle WAW, WAR hazards
- Considered area-timing trade-off to improve the timing on issue unit, reorder buffer and instruction queue, and improved the frequency by 15 MHz using canonical diagrams, multi-selector path optimization, and redundant logic elimination
- Exceeded the 40x IPC than Loongson GS132 (single-issue, 3-stage pipeline) on crc32, select sort, 30x on sha, stream copy
- RTL design using Verilog, synthesis and implementation using Vivado, with target frequency 88 MHz on Artix-7 FPGA
- Implemented AXI interface and integrated the processor in a SoC with LCD, UART and DDR, capable of running RTOS
- Project code, design document and slide: https://github.com/Superscalar-HIT-Core/Superscalar-HIT-Core-NSCSCC2020

MIPS 6-stage In-order Processor on FPGA, HIT **Shenzhen, China**
Team Lead, Advisor: Prof. Hongpeng Wang 07/2019 - 08/2019

- Designed micro-architecture, implemented RTL, optimized performance of an MIPS in-order processor and achieved a synthesis frequency of 110MHz on Xilinx Artix-7 FPGA
- Implemented an SRAM-based, direct-mapped L1 data cache with write-back and write-allocate policy and a 2-way L1 instruction cache to reduce the latency of DDR memory access
- Inserted a new pipeline stage dedicated for cache accessing based on the classic MIPS 5-stage pipeline architecture to hide the 1-cycle latency of SRAM-based cache access and improved the IPC by 40%
- Implemented a 2-bit branch predictor and improved the IPC by 10% with the MIPS delay slot technique

A RISC-V Processor Core running Linux, Chinese Academy of Sciences **Beijing, China**
"One Chip Per Student" Participant, Advisor: Prof. Yungang Bao, Institute of Computing Technology 10/2020 - 12/2020

- Designed a minimal die-area but fully functional core capable of running Linux operating system
- Self-implemented the processor core from scratch
- Designed a 3-stage pipeline including (1) instruction fetch, (2) decode & execute and (3) commit & exception handling
- Implemented Translation Lookaside Buffer and hardware Page Table Walker to support hardware virtual memory management
- Implemented AXI interface to integrate the core into SoC that work with peripherals (DDR controllers, Ethernet, etc.)
- Taped-out on Dec. 29th with SMIC 110nm technology node

HLS-Based Deep Learning Accelerator **Shenzhen, China**
Hardware Engineer 09/2019 - 12/2019

- Optimized C language-based neural network implementations in loops, data structure and data type to utilize parallelism
- Improved performance by pipelining, loop unrolling, and array splitting and accelerated the inference of existing CNN, DNN and RNN networks by ~10x on PYNQ platform compared to ARM-only solution

TEACHING EXPERIENCE

Computer Architecture
Principles of Computer Organization
Computer Design Practice **Shenzhen, China**
Teaching Assistant, HIT 04/2021 - 08/2021

- Introduced a dynamic RISC-V CPU verification framework to course labs
- Developed an automated building and testing system to help student evaluate their design

Principles of Computer Organization
Computer Design Practice **Shenzhen, China**
Teaching Assistant, HIT 03/2020 - 07/2020

- Designed and improved lab instructions for the two courses and answered students' questions
- Built automated test platform with Docker running Vivado and Icarus Verilog simulator, wrote scripts for grading homework
- Designed training programs for National Student Computer System Capability Challenge (NSCSCC) and delivered lectures
- Wrote the lab instruction of cache, bus, and microcontroller for the course website: http://comp2008.gitee.io/archived/

AWARDS

- Merit-Based Scholarship at Georgia Tech – Shenzhen Campus 2022
- Outstanding Undergraduate Thesis of HIT (Ranking: 1/121) 2021
- Third Prize of NSCSCC 2020 (Ranking: preliminary 12/82, final 10/31) 2020
- HIT Merit Scholarship 2020 (Annual GPA top 15%) 2020
- HIT Merit Scholarship 2019 (Annual GPA top 25%) 2019
- Second Prize of NSCSCC 2019 (Ranking: preliminary 4/150, final 6/22) 2019
- Academic Scholarship for Exchange Abroad (GPA 4.0/4.0 at UC Berkeley) 2019
- First Prize of Lanqiao Cup Programming Contest 2019, Guangdong Province (Top 10%) 2019

SKILLS

Programming Skills: C/C++, Verilog HDL, Chisel, Python, x86/MIPS/RISC-V ISA & Assembly, Linux, FPGA, LaTeX
Language: Mandarin (Native); English (Proficient, TOEFL:109, GRE: Verbal 155, Quantitative 166)