

Bohuslavstola / Digital-electronics-1

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main

Digital-electronics-1 / Labs / 03-vivado /

Bohuslavstola LAB3 17 hours ago History

..

comparator_2bit

5 days ago

images

5 days ago

mux_2bit_4to1

17 hours ago

README.md

17 hours ago

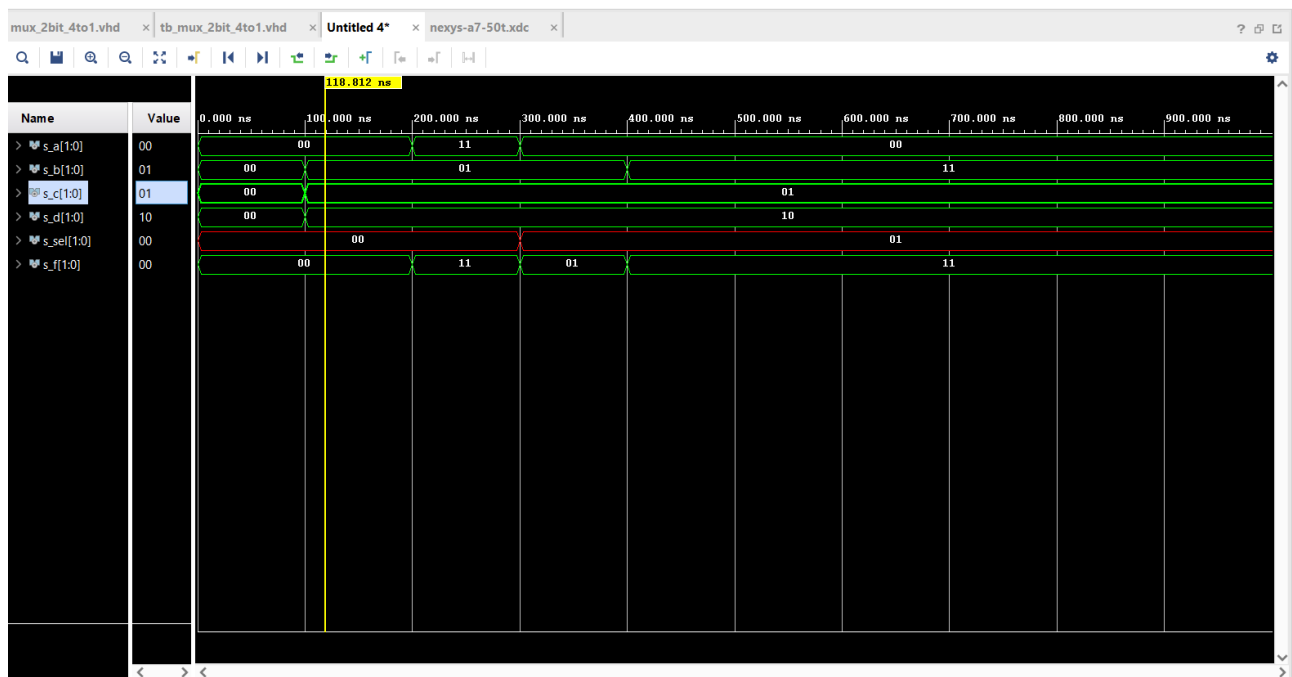
README.md

První úkol

LED	Connection	Switch	Connection
LED0	H17	SW0	J15
LED1	K15	SW1	L16
LED2	J13	SW2	M13
LED3	N14	SW3	R15
LED4	R18	SW4	R17
LED5	V17	SW5	T18
LED6	U17	SW6	U18

LED	Connection	Switch	Connection
LED7	U16	SW7	R13
LED8	V16	SW8	T8
LED9	T15	SW9	U8
LED10	U14	SW10	R16
LED11	T16	SW11	T13
LED12	V15	SW12	H6
LED13	V14	SW13	U12
LED14	V12	SW14	U11
LED15	V11	SW15	V10

Druhý úkol



mux_2bit_4to1

```

architecture Behavioral of mux_2bit_4to1 is
begin
    f_0 <= a_i when (sel_i="00")else
        b_i when (sel_i="01")else
        c_i when (sel_i="10")else
        d_i;
end architecture Behavioral;

```

```
-- WRITE "GREATER" AND "EQUALS" ASSIGNMENTS HERE
```

```
end architecture Behavioral;
```

tb_mux_2bit_4to1

```
p_stimulus : process
begin
    -- Report a note at the beginning of stimulus process
    report "Stimulus process started" severity note;

    -- First test values
    s_d <= "00"; s_c <= "00"; s_b <= "00"; s_a <= "00" ;
    s_sel <="00";wait for 100ns;

    s_d <= "10"; s_c <= "01";s_b <= "01"; s_a <= "00" ;
    s_sel <="00";wait for 100ns;

    s_d <= "10"; s_c <= "01";s_b <= "01"; s_a <= "11" ;
    s_sel <="00";wait for 100ns;

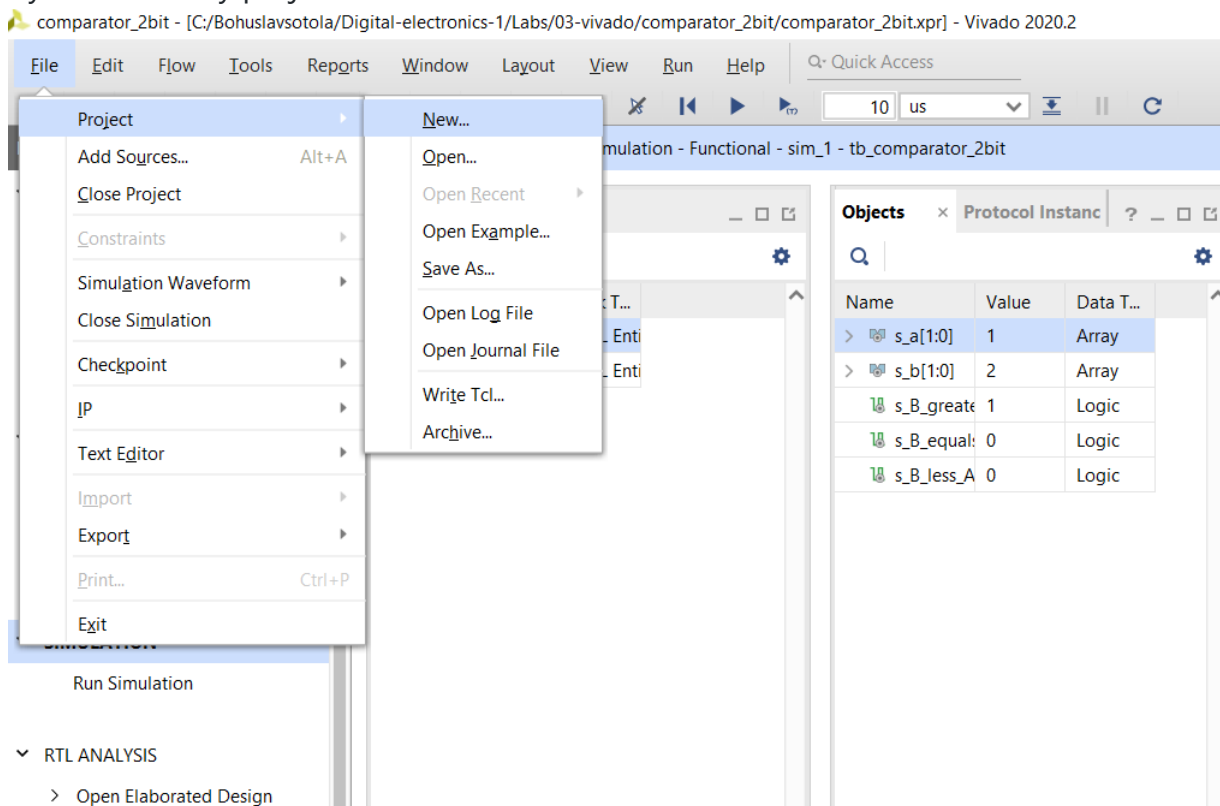
    s_d <= "10"; s_c <= "01";s_b <= "01"; s_a <= "00" ;
    s_sel <="01";wait for 100ns;

    s_d <= "10"; s_c <= "01";s_b <= "11"; s_a <= "00" ;
    s_sel <="01";wait for 100ns;

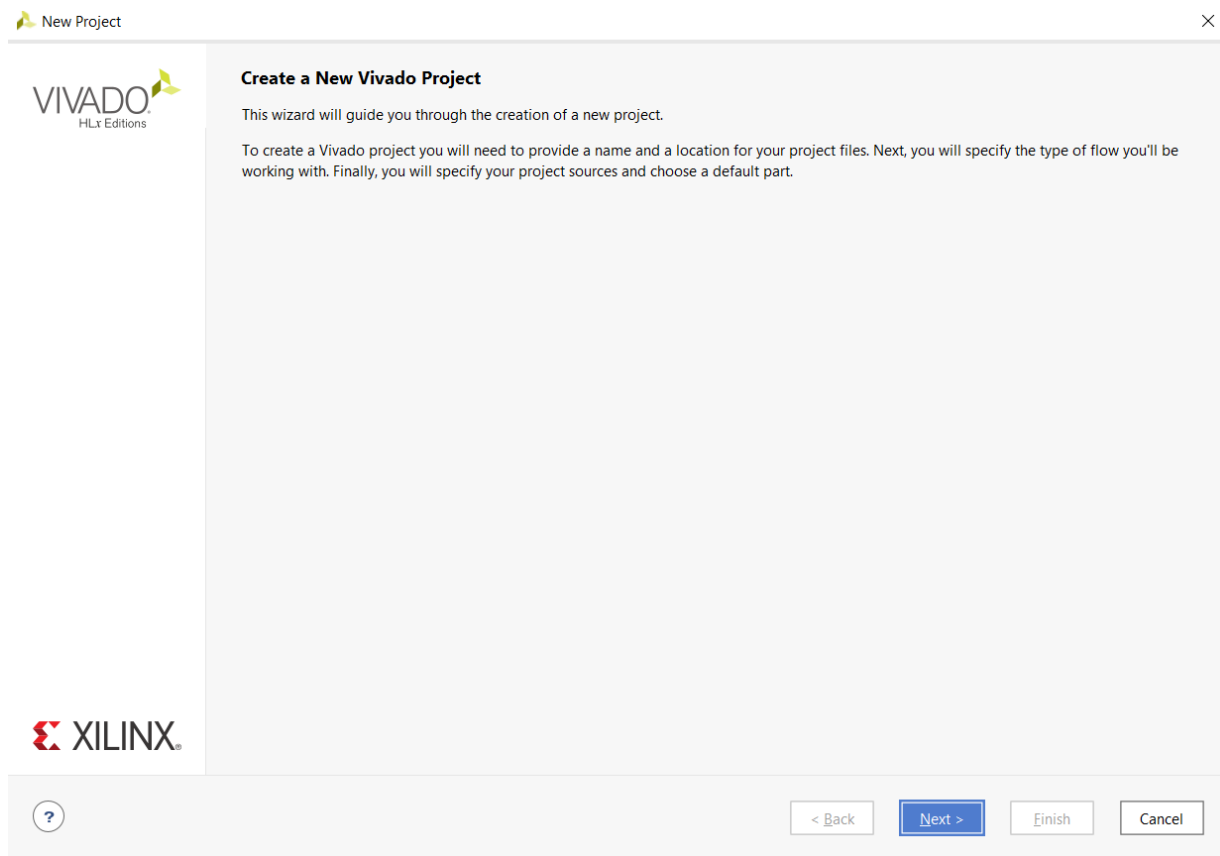
    -- Report a note at the end of stimulus process
    report "Stimulus process finished" severity note;
    wait;
end process p_stimulus;
```

Třetí úkol - tutoriál

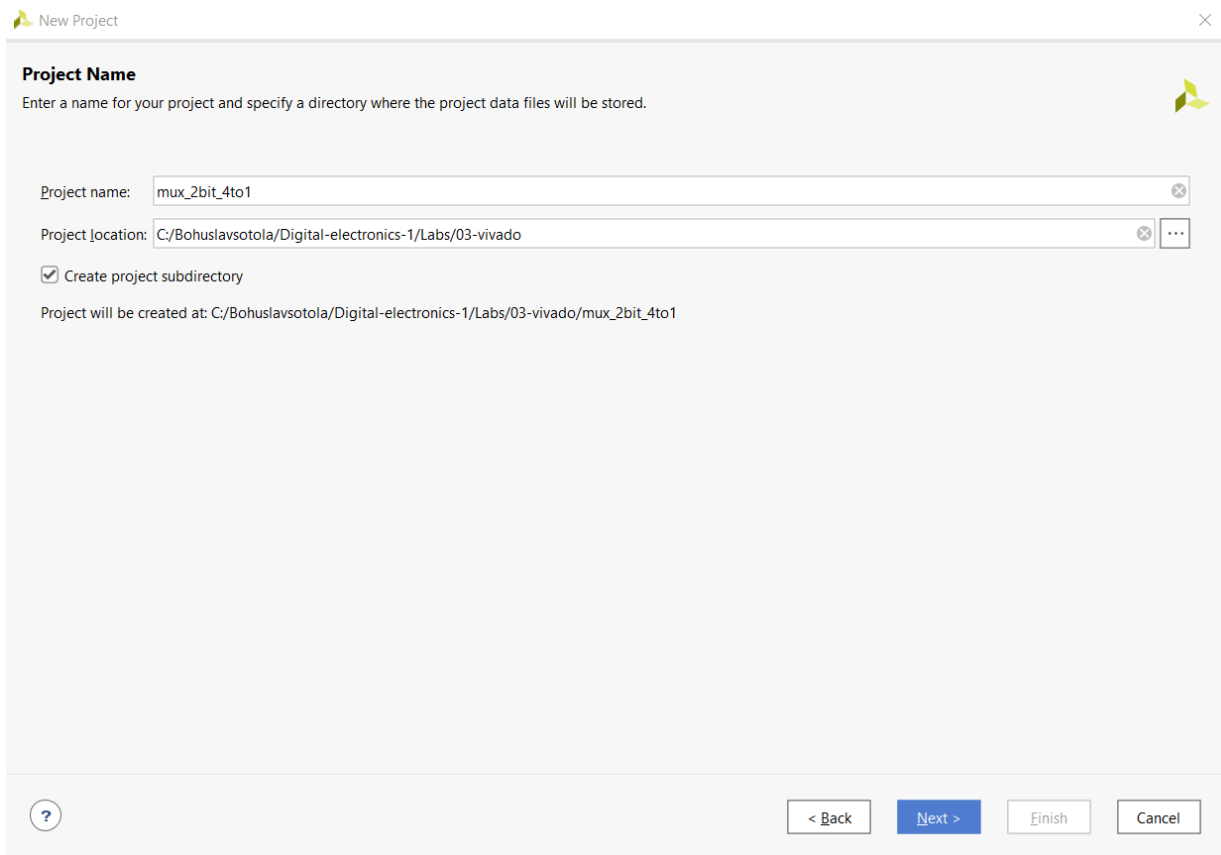
1. Vytvoříme Nový projekt



2. Klikneme na tlačítko next



3. Zadáme Project name



New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

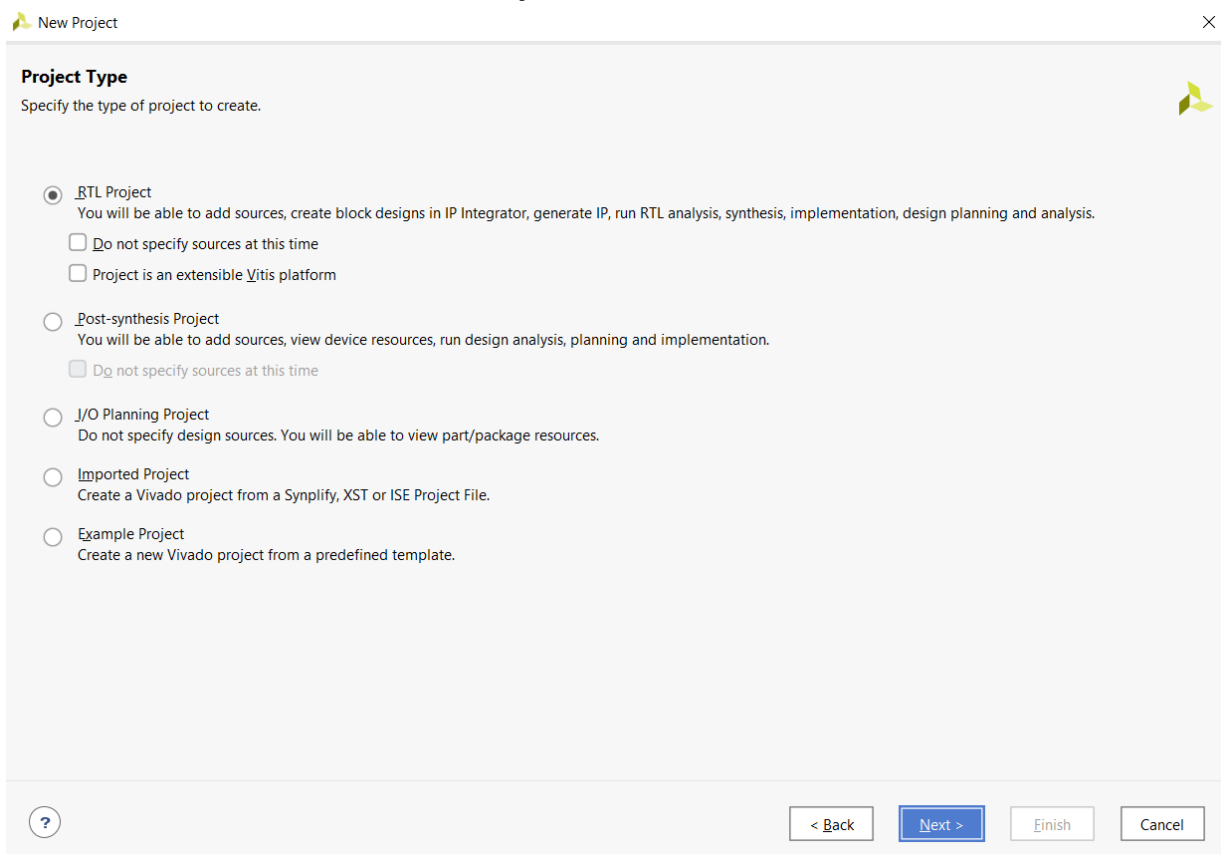
Project name:

Project location:

☒ Create project subdirectory

Project will be created at: C:/Bohuslavsotola/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

4. Necháme zaškrknutou volbu RTL Project



New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

☐ Project is an extensible Vitis platform

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.

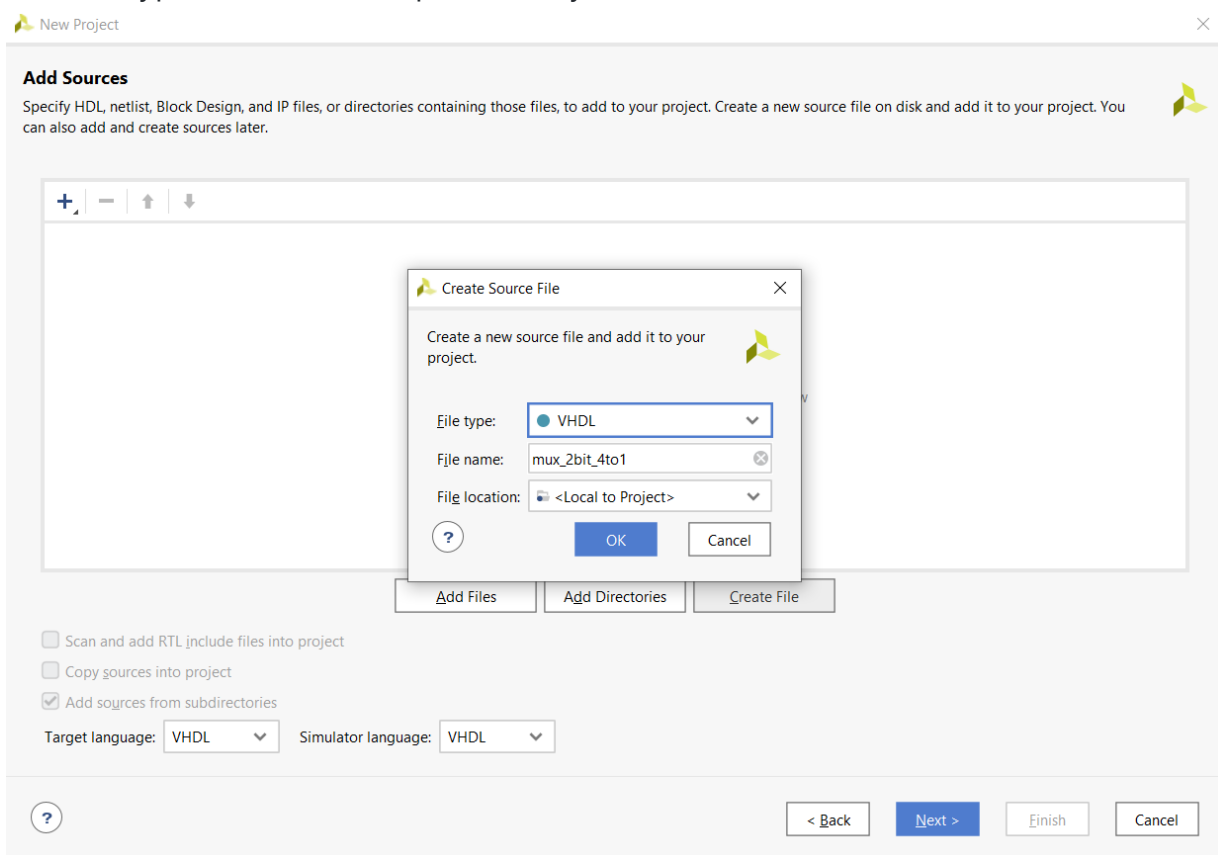
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

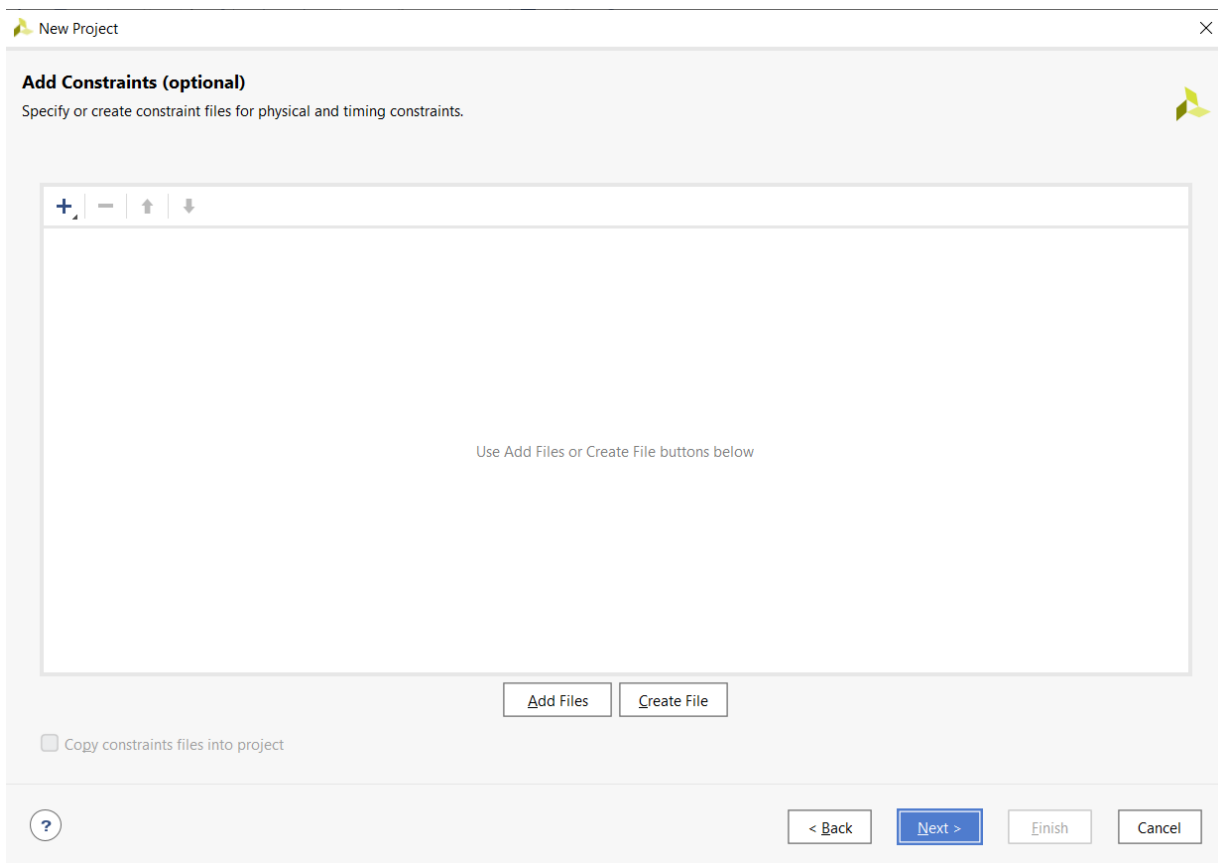
☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

5. Zadáme typ VHDL a zadáme požadovaný File name



6. Klikneme na Next



7. Zadáme Board Nexys A7-50T

New Project ×

Default Part
Choose a default Xilinx part or board for your project.

Parts | **Boards**

[Reset All Filters](#) Install/Update Boards

Vendor: Name: Board Rev:

Search: (5 matches)

Display Name	Preview	Vendor	File Version	Part	I/O Pin Count	Board Rev	Available IOBs	LUT Elements
Nexys A7-100T		digilentinc.com	1.0	xc7a100tcsq324-1	324	D.0	210	63400
Nexys A7-50T		digilentinc.com	1.0	xc7a50tcsq324-1L	324	D.0	210	32600
Nexys4		digilentinc.com	1.1	xc7a100tcsq324-1	324	B.1	210	63400
Nexys4 DDR		digilentinc.com	1.1	xc7a100tcsq324-1	324	C.1	210	63400
Nexys Video		digilentinc.com	1.1	xc7a200tsbg484-1	484	A.0	285	134600

? < Back Next > Finish Cancel

8. Klikneme na tlačítko Finish

New Project ×

VIVADO
HLx Editions

New Project Summary

- A new RTL project named 'mux_2bit_4to1' will be created.
- 1 source file will be added.
- No constraints files will be added. Use Add Sources to add them later.
- The default part and product family for the new project:
 Default Board: Nexys A7-50T
 Default Part: xc7a50tcsq324-1L
 Product: Artix-7
 Family: Artix-7
 Package: csg324
 Speed Grade: -1L

XILINX

To create the project, click Finish

? < Back Next > Finish Cancel

9. Zadáme Entity name



Define Module



Define a module and specify I/O Ports to add to your source file.

For each port specified:

MSB and LSB values will be ignored unless its Bus column is checked.

Ports with blank names will not be written.

**Module Definition**

Entity name:

mux_2bit_4to1



Architecture name:

Behavioral

**I/O Port Definitions**

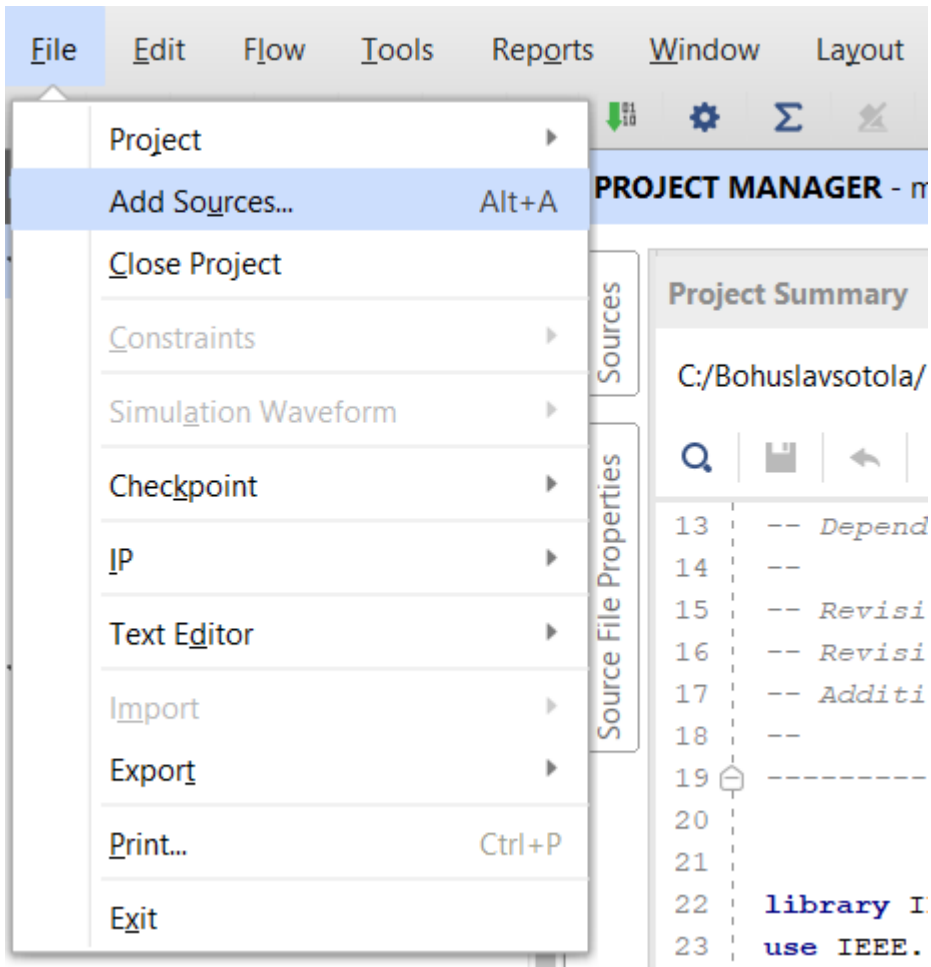
Port Name	Direction	Bus	MSB	LSB	
	in	<input type="checkbox"/>	0	0	



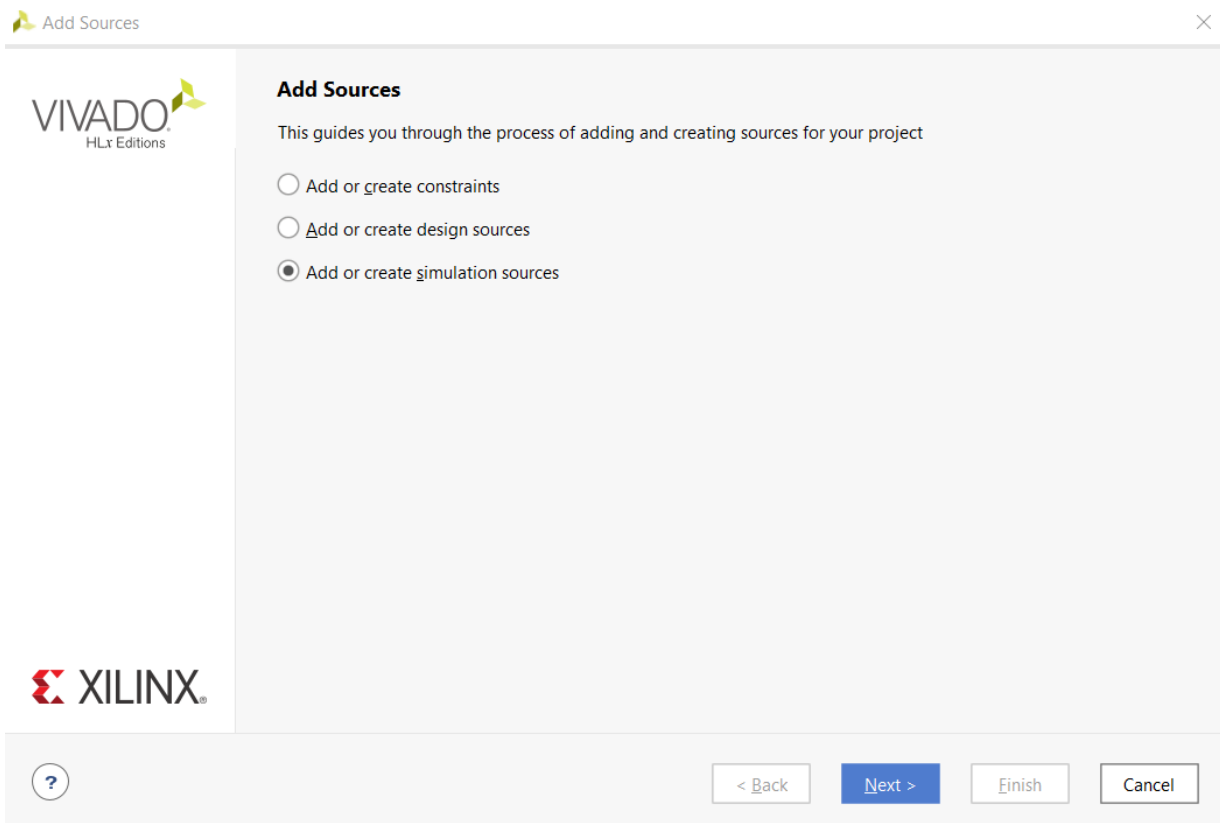
OK

Cancel

10. Klikneme na File - Add Sources



11. Vybereme položku Add or create simulation sources



12. Klikneme na Create file, dále vybereme File typ: VHDL a zadáme File name

