燕博南 博士，北京大学人工智能研究院助理教授

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研究特色

- 研究方向：智能体认知芯片、通用人工智能处理器设计、存储器芯片设计
- 在研项目：超大规模智能体博弈计算芯片、单智能体认知架构与决策芯片
- 交叉学科：集成电路科学与工程、计算机科学、人工智能、认知科学

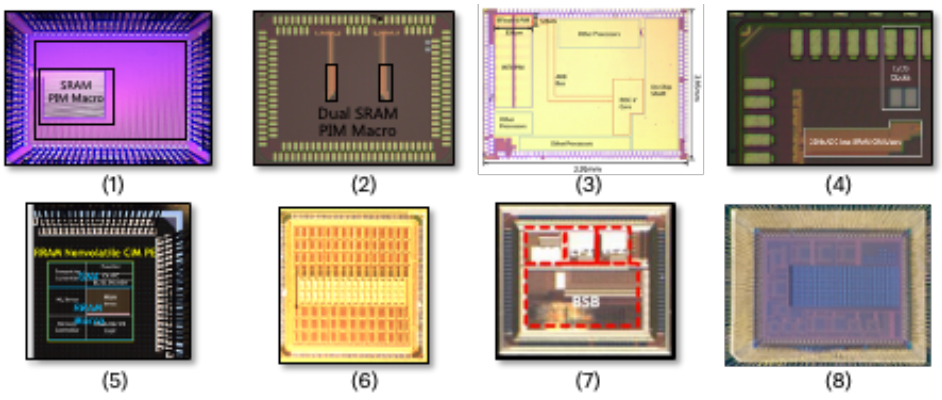
工作经历

- 北京大学，人工智能研究院 — 助理教授 2020.11-今
- NeoNexus Group — 首席科学家 2020.5-2020.11

教育经历

- Duke University, USA — 电子与计算机工程, 哲学博士（Ph.D.） 2017-2020
- University of Pittsburgh, USA — 电子工程, 理学硕士（M.S.） 2014-2017
- 北京航空航天大学，中国 — 电子信息工程, 工学学士 2010-2014

芯片成果



(1) 单核模拟型SRAM存内计算深度学习网络加速器芯片
(2) 双核SRAM存内计算深度学习网络加速器芯片
(3) RISC-V+SRAM数字型存内计算片上系统芯片
(4) 数字型SRAM存内计算深度学习网络加速器芯片
(5) 脉冲型150nm 忆阻器类脑存内计算加速核芯片
(6) 多层感知机RRAM存内计算芯片
(7) 基于忆阻器的Brain-State-in-a-Box (BSB)认知芯片
(8) 40nm先进工艺忆阻器存储器芯片

任教课程

- 人工智能芯片：设计与实践 — 研究生，秋季学期 @ 北京大学
- 人工智能与芯片设计 — 本科生，秋季学期 @ 北京大学
- 数字系统原理与设计（实验班） — 本科生，春季学期 @ 北京大学
- ICisC芯片设计暑期课程，2021 & 2022 @ 南京集成电路培训基地NICT

科研项目

- 国家自然科学基金委员会,原创探索计划项目, 认知处理器智能芯片与生物灵活决策交叉研究, 2024-01-01 至 2026-12-13, 299万元, 获批, 主持
- 国家自然科学基金委员会, 重大研究计划, 92264201, 单片三维集成的存算一体混合架构与芯片研究, 2023-01-01 至 2026-12-31, 300万元, 在研, 参与（负责子课题经费90万元）
- 北京苹芯科技有限公司, 横向课题, 8410102577, 面向AI的计算加速硬件设计, 2021-05 至 2023-05, 15万元, 结题, 主持
- 美国空军实验室, BAA-RIK-14-05, FA8750-18-2-0121, 忆阻器控制器集成电路设计, 2018-03 至 2020-02, 50万元, 结题, 参与

学术成果

会议:

[C1] ISSCC'22（集成电路领域全世界最高级别学术会议）: **Bonan Yan**, Jeng-Long Hsu, Pang-Cheng Yu, Chia-Chi Lee, Yaojun Zhang, Wenshuo Yue, Guoqiang Mei et al. "A 1.041-Mb/MM 2 27.38-TOPS/W signed-INT8 dynamic-logic-based ADC-less SRAM compute-in-memory macro in 28nm with reconfigurable bitwise operation for AI and embedded applications." In 2022 IEEE International Solid-State Circuits Conference (ISSCC), vol. 65, pp. 188-190. IEEE, 2022.

[C2] VLSI-TSA'2020: **Bonan Yan**, Ziru Li, Brady Taylor, Hai Li, and Yiran Chen. "Neuromorphic Computing Systems with Emerging Nonvolatile Memories: A Circuits and Systems Perspective." In 2020 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), pp. 122-123. IEEE, 2020.

[C3] IEDM'19: **Bonan Yan**, Mengyun Liu, Krishnendu Chakarabarty, Yiran Chen and Hai Li. "On Designing Low-Power and Reliable Nonvolatile Memory-based Computing-In-Memory Accelerators." IEEE International Electron Devices Meeting (IEDM), 2019.

[C4] VLSI'19: **Bonan Yan**, Qing Yang, Wei-Hao Chen, Kung-Tang Chang, Jian-Wei Su, Chien-Hua Hsu, Sih-Han Li, Heng-Yuan Lee, Shyh-Shyuan Sheu, Mon-Shu Ho, Qing Wu, Meng-Fan Chang, Yiran Chen and Hai Li. "RRAM-based Spiking Nonvolatile Computing-In-Memory Processing Engine with Precision-Configurable In Situ Nonlinear Activation." IEEE Symposium on VLSI Technology, pp. T86-T87, 2019.

[C5] DAC'18: **Bonan Yan**, Xiong Cao, and Hai Li. "A neuromorphic design using chaotic Mott memristor with relaxation oscillation." Design Automation Conference (DAC), pp. 1-6. 2018.

[C6] DATE'18: **Bonan Yan**, Fan Chen, Yaojun Zhang, Chang Song, Hai Li, and Yiran Chen. "Exploring the opportunity of implementing neuromorphic computing systems with spintronic devices." Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 109-112. 2018.

[C7] IEDM'17: **Bonan Yan**, Chenchen Liu, Xiaoxiao Liu, Yiran Chen, and Hai Li. "Understanding the trade-offs of device, circuit and application in ReRAM-based neuromorphic computing systems." IEEE International Electron Devices Meeting (IEDM), pp. 11-4. 2017.

[C8] ICCAD'17: **Bonan Yan**, Jianhua Yang, Qing Wu, Yiran Chen, and Hai Li. "A closed-loop design to enhance weight stability of memristor based neural network chips." International Conference on Computer-Aided Design (ICCAD), pp. 541-548. 2017.

[C9] ISCAS'16: **Bonan Yan**, Amr Mahmoud Mahmoud, Jianhua Joshua Yang, Qing Wu, Yiran Chen, and Hai Li. "A neuromorphic ASIC design using one-selector-one-memristor crossbar." IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1390-1393. 2016.

[C10] NVMTS'16: **Bonan Yan**, Zheng Li, Yiran Chen, and Hai Li. "RAM and TCAM designs by using STT-MRAM." Non-Volatile Memory Technology Symposium (NVMTS), pp. 1-5. IEEE, 2016.

[C11] ASICON'15: **Bonan Yan**, Yaojun Zhang, Enes Eken, Wujie Wen, Weisheng Zhao, and Yiran Chen. "Recent progresses of STT memory design and applications." IEEE International Conference on ASIC (ASICON), pp. 1-4. 2015.

[C12] GLVLSI'15: **Bonan Yan**, Zheng Li, Yaojun Zhang, Jianlei Yang, Hai Li, Weisheng Zhao, and Pierre Chor-Fung Chia. "A High-Speed Robust NVM-TCAM Design Using Body Bias Feedback." Great Lakes Symposium on VLSI (GLVLSI), pp. 69-74. 2015.

[C13] FPGA'2023: Lei Cai, Jing Wang, Lianfeng Yu, **Bonan Yan**, Yaoyu Tao, and Yuchao Yang. "Accelerating Neural-ODE Inference on FPGAs with Two-Stage Structured Pruning and History-based Stepsize Search." In Proceedings of the 2023 ACM/SIGDA International Symposium on Field Programmable Gate Arrays, pp. 177-183. 2023.

[C14] Ziru Li, Qilin Zheng, **Bonan Yan**, Ru Huang, Bing Li, and Yiran Chen. "ASTERS: adaptable threshold spike-timing neuromorphic design with twin-column ReRAM synapses." In Proceedings of the 59th ACM/IEEE Design Automation Conference, pp. 1099-1104. 2022.

[C15] ASP-DAC'22: Kangyi Qiu, Yaojun Zhang, **Bonan Yan**, and Ru Huang. "Heterogeneous Memory Architecture Accommodating Processing-in-Memory on SoC for AIoT Applications." In 2022 27th Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 383-388. IEEE, 2022.

[C16] IEDM'2021: Longhao Yan, Xi Li, Yihang Zhu, **Bonan Yan**, Yingming Lu, Teng Zhang, Yuchao Yang, Zhitang Song, and Ru Huang. "Uncertainty Quantification Based on Multilevel Conductance and Stochasticity of Heater Size Dependent C-doped Ge2Sb2Te5 PCM Chip." In 2021 IEEE International Electron Devices Meeting (IEDM), pp. 28-2. IEEE, 2021.

[C17] ICCAD'20: Xiaoxuan Yang, **Bonan Yan**, Hai Li, and Yiran Chen. "ReTransformer: ReRAM-based processing-in-memory architecture for transformer acceleration." In Proceedings of the 39th International Conference on Computer-Aided Design, pp. 1-9. 2020.

[C18] DAC'20: Qilin Zheng, Zishun Feng, **Bonan Yan**, Zongwei Wang, Yimao Cai, Ru Huang, Yiran Chen, Chia-Lin Yang and Hai (Helen) Li. "Lattice: An ADC/DAC-less ReRAM-based Processing-In-Memory Architecture for Accelerating Deep Convolution Neural Networks." Design Automation Conference (DAC), 2020.

[C19] DAC'20: Ziru Li, **Bonan Yan**, and Hai Li. "ReSiPE: ReRAM-based Single-Spiking Processing-In-Memory Engine." Design Automation Conference (DAC), 2020.

[C20] ITC'19: Arjun Chaudhuri, **Bonan Yan**, Yiran Chen and Krishnendu Chakrabarty, "Hardware Fault Tolerance for Binary RRAM Crossbars." IEEE International Test Conference (ITC), 2019

[C21] ASP-DAC'19: Bing Li, **Bonan Yan**, Chenchen Liu, and Hai Li. "Build reliable and efficient neuromorphic design with memristor technology." Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 224-229. 2019.

[C22] ASP-DAC'17: Shihui Yin, Deepak Kadetotad, **Bonan Yan**, Chang Song, Yiran Chen, Chaitali Chakrabarti, and Jae-sun Seo. "Low-power neuromorphic speech recognition engine with coarse-grain sparsity." Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 111-114. 2017.

[C23] DAC'15: Chenchen Liu, **Bonan Yan**, Chaofei Yang, Linghao Song, Zheng Li, Beiye Liu, Yiran Chen, Hai Li, Qing Wu, and Hao Jiang. "A spiking neuromorphic design with resistive crossbar." Design Automation Conference (DAC), pp. 14. 2015.

[C24] ISCAS'15: Zheng Li, **Bonan Yan**, Lun Yang, Weisheng Zhao, Yiran Chen, and Hai Li. "A new self-reference sensing scheme for TLC MRAM." IEEE International Symposium on Circuits and Systems (ISCAS), pp. 593-596. 2015.

[C25] DATE'15: Yaojun Zhang, **Bonan Yan**, Wenqing Wu, Hai Li, and Yiran Chen. "Giant spin hall effect (GSHE) logic design for low power application." Design Automation & Test in Europe Conference & Exhibition (DATE), pp. 1000-1005. 2015.

[C26] VLSI-SoC'15: Zheng Li, Chenchen Liu, Yandan Wang, **Bonan Yan**, Chaofei Yang, Jianlei Yang, and Hai Li. "An overview on memristor crossbar based neuromorphic circuit and architecture." IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), pp. 52-56. 2015.

[C27] ISVLSI'16: Chenchen Liu, Qing Yang, **Bonan Yan**, Jianlei Yang, Xiaocong Du, Weijie Zhu, Hao Jiang, Qing Wu, Mark Barnell, and Hai Li. "A Memristor Crossbar Based Computing Engine Optimized for High Speed and Accuracy." IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 110-115. 2016.

期刊及专著：

[J1] Anjunyi Fan, Yihan Fu, Yaoyu Tao, Zhonghua Jin, Haiyue Han, Huiyu Liu, Yaojun Zhang, **Bonan Yan***, Yuchao Yang*, and Ru Huang*. "Hadamard product-based in-memory computing design for floating point neural network training." Neuromorphic Computing and Engineering (2023).

[J2] Zhaokun Jing, **Bonan Yan**, Yuchao Yang, and Ru Huang. "VSDCA: A Voltage Sensing Differential Column Architecture Based on 1T2R RRAM Array for Computing-in-Memory Accelerators." IEEE Transactions on Circuits and Systems I: Regular Papers 69, no. 10 (2022): 4028-4041.

[J3] Bingjie Dang, Ling Lv, Hong Wang, Lei Cai, **Bonan Yan**, Keqin Liu, Liying Xu, Yue Hao, Ru Huang, and Yuchao Yang. "1-HEMT-1-Memristor With Hardware Encryptor for Privacy-Preserving Image Processing." IEEE Electron Device Letters 43, no. 8 (2022): 1223-1226.

[J4] Xiao, Zhuojian, **Bonan Yan**, Teng Zhang, Ru Huang, and Yuchao Yang. "Memristive devices based hardware for unlabeled data processing." Neuromorphic Computing and Engineering (2022).

[J5] Yingming Lu , Xi Li, **Bonan Yan**, Longhao Yan, Teng Zhang, Zhitang Song, Ru Huang, and Yuchao Yang. "In-memory realization of eligibility traces based on conductance drift of phase change memory for energy-efficient reinforcement learning." Advanced Materials 34, no. 6 (2022): 2107811.

[J6] **Bonan Yan**, Bing Li, Ximing Qiao, Cheng-Xin Xue, Meng-Fan Chang, Yiran Chen and Hai Li. "RRAM Based In-Memory Computing: From Device and Large-Scale Integration System Perspectives." Advanced Intelligent Systems. 1900068 (2019).

[J7] **Bonan Yan**, Yiran Chen, and Hai Li. "Challenges of memristor based neuromorphic computing system." Science China Information Sciences (SCIS). 61, no. 6 (2018): 060425.

[J8] Qing Yang, **Bonan Yan**, and Hai Li. "Sensing of Resistive RAM." Sensing of Non-Volatile Memory Demystified. Springer, 2019. 31-45.

[J9] Yaojun Zhang, **Bonan Yan**, Xiaobin Wang, and Yiran Chen. "Persistent and Non-Persistent Error Optimization for STT-RAM Cell Design." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). 36, no. 7 (2017): 1181-1192.

[J10] Enes Ekens, Ismail Bayram, Yaojun Zhang, **Bonan Yan**, Wenqing Wu, Hai Li, and Yiran Chen. "Giant Spin-Hall assisted STT-RAM and logic design." Integration 58 (2017): 253-261.

[J11] Yue Zhang, **Bonan Yan**, Wang Kang, Yuanqing Cheng, Jacques-Olivier Klein, Youguang Zhang, Yiran Chen, and Weisheng Zhao. "Compact model of subvolume MTJ and its design application at nanoscale technology nodes." IEEE Transactions on Electron Devices (T-ED). 62, no. 6 (2015): 2048-2055.

专利：

- 杨玉超; 荆兆坤; 燕博南; 黄如 ; 一种基于1T2R阻变存储器阵列的存内计算加速器及其应用, 2022- 08-26, 中国, CN202210702639.9
- 李政; 郭玮; 康旺; 燕博南; 赵巍胜 ; 一种磁逻辑器件的并联编程电路, 2014-11-5, 中国, CN201410339998.8

指导学生

博士研究生

岳文硕（二年级），范安骏逸（一年级），史代璟（一年级）

硕士研究生

李嘉怡（一年级），杨知雨（二年级）

本科研究助理

邱康怡（已毕业），符一涵（四年级），赵洪宵（四年级），吴秋平（三年级），周钜宸（三年级），李铁铮（二年级）

社会服务

- 中国能源研究会电力传感和智能分析专业委员会（第一届）委员
- 技术委员会（TPC）委员：
  - 2022 Design Automation Conference (DAC)
  - 2023 Design Automation Conference (DAC)
  - 2022 IEEE Electron Devices Technology and Manufacturing Conference (EDTM)
  - 2023 IEEE Electron Devices Technology and Manufacturing Conference (EDTM)
  - 2023 IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)
- 学术会议/期刊审稿：
  - IEEE JSSC, IEEE TCAS-I, IEEE TCAS-II, IEEE Embedded Letters, IEEE D&T, ACM JETC, Nano Select, Advanced Intelligent Systems等

获奖情况

- 北京大学第二十二届青年教师教学基本功比赛
  - 理工科类二等奖
  - 最佳教学演示奖
- CCF-华为胡杨林基金-存储领域专项优秀方案奖

邀请报告

2020.12, 北京大学微纳电子系青年教师论坛，北京
2020.12, 清华大学，邀请人：尹首一教授，北京
2021.1, 京区青年学者“后摩尔时期的计算形态与设计自动化”论坛，北京
2021.4, 电子信息技术年会，西安
2021.7, 全国半导体物理学术会议，重庆
2021.8, 北京航空航天大学，邀请人：赵巍胜教授，北京
2021.9, DJI 大疆创新，深圳
2021.10, 阿里巴巴云栖大会，杭州
2021.11, 智源人工智能研究院青源会，北京
2021.12, CCF-Sys，北京
2022.3, 清华大学，邀请人：刘厚方助理教授，北京
2022.5, 复旦新型存储器件及其创新应用论坛，上海
2022.5, 中国移动信息产业链创新大会，北京
2022.10, 青源会具身智能研讨会，北京
2022.2, 北京大学哲学系，新工科交叉研讨会，邀请人：王彦晶副教授，北京
2022.3, 多样性算力产业峰会，北京