BONAN YAN

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RESEARCH INTERESTS

- Circuit design for emerging nonvolatile memories
- Brain-inspired computing systems
- Hardware/software co-design for machine learning acceleration

Research highlights:

- 24 publications (12 as first authors) in competitive conferences and journals/book chapters across the fields of solid-state circuits, circuits and systems (CAS) and electronic design automation (EDA), including Symposium on VLSI Technology, IEDM (2 times), DAC (2 times), ICCAD, GLVLSI, ISVLSI, ISCAS, Advanced Intelligent Systems, IEEE Transactions on Electron Devices, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, etc.
- 203 citations (h-index: 7, i10-index: 6) since my first paper published in 2015

EDUCATION

Duke University — Durham, NC
Ph.D., Electrical and Computer Engineering — 2017-Expect 2020

University of Pittsburgh — Pittsburgh, PA
M.S., Electrical and Computer Engineering — 2014-2017

Beihang University — Beijing, China
B.S., Electrical and Computer Engineering (with honor) — 2010-2014

INTEGRATED CIRCUIT (IC) TAPEOUT EXPERIENCE

RRAM Based Modular NN Accelerator Controller — submitted in 05/2019

- TSMC 65nm CMOS, standalone 3-bit 1T1R/binary 1S1R RRAM array

RRAM Based Dot-Product Engine Controller — submitted in 02/2017

- GlobalFoundries 130nm CMOS, standalone 3-bit 1T1R/binary 1S1R RRAM array
- Demonstration video: https://www.youtube.com/watch?v=H7hu4F1tlaw&t=3s

RRAM Based Spiking Computing-In-Memory Processing Engine — submitted in 10/2016

- TSMC 150nm CMOS, embedded 64Kb 1T1R RRAM array
- Demonstration video: https://www.youtube.com/watch?v=gIZZWXTF2gg

RRAM Based Brain-State-In-A-Box (BSB) Controller — submitted in 05/2016

- GlobalFoundries 130nm CMOS, standalone 3-bit 1T1R RRAM array

RRAM Based Feedforward Perceptron Controller submitted in 08/2015

- GlobalFoundries 130nm CMOS, standalone 3-bit 1T1R RRAM array

1T1R RRAM Memory submitted in 04/2015

- HHNEC 130nm CMOS, embedded binary 4Kb 1T1R RRAM array

RESEARCH PROJECTS

Graduate Researcher at Duke University Durham, NC
Advisor: Prof. Hai Li, Prof. Yiran Chen 2017-Present

- Design efficient neuron circuit and integrate with the embedded 1T1R macro
- Build real-time demonstration of RRAM based computing-in-memory processing core
- Develop EDA method to tolerate RRAM non-ideal behaviors

Visiting Scholar at University of Massachusetts, Amherst Amherst, MA
Advisor: Prof. Jianhua (Joshua) Yang 11/2017-12/2017

- Build RRAM/CMOS hybrid hardware demonstration for MNIST recognition

Visiting Research Fellow at HP labs Palo Alto, CA
Advisor: Dr. Miao Hu 05/2015-08/2015

- Build Fast EDA Tool to Emulate Nonlinearity of Multi-Level RRAM based on Jacobian matrix method

Graduate Researcher at University of Pittsburgh Pittsburgh, PA
Advisor: Prof. Hai Li, Prof. Yiran Chen 2014-2017

- Design reliable write/read circuit for 1T1R RRAM crossbar array
- Develop emerging STT-MRAM based TCAM using body effect

Undergraduate Researcher at Beihang University Beijing, China
Advisor: Dr. Weisheng Zhao 2013-2014

- Macromodeling of STT p-MTJ under 40nm and Verilog-A coding

Awards

Princeton Pathway into the Academy Grant
2019 Symposium on VLSI Technology Student Travel Grant
Ph.D. Forum at DAC Travel Grant
2019 Duke University Pratt School of Engineering Travel Grant
2018 Duke University Pratt School of Engineering Travel Grant

TEACHING EXPERIENCE

Teaching Assistant at Duke University

- ECE566 Enterprise Storage Architecture 2019

Graduate Teaching Fellow at University of Pittsburgh 2014-2016

- ECE132: Digital Logic
- ECE1192: Introduction to VLSI Design
- ECE1193: Advanced VLSI Design
- COE147: Computer Organization and Assembly Language

PUBLICATIONS

Conferences:

[C1] **IEDM'19: Bonan Yan**, Mengyun Liu, Krishnendu Chakarabarty, Yiran Chen and Hai Li, " On Designing Low-Power and Reliable Nonvolatile Memory-based Computing-In-Memory Accelerators." IEEE International Electron Devices Meeting (IEDM), to appear 2019.

[C2] **VLSI'19: Bonan Yan**, Qing Yang, Wei-Hao Chen, Kung-Tang Chang, Jian-Wei Su, Chien-Hua Hsu, Sih-Han Li, Heng-Yuan Lee, Shyh-Shyuan Sheu, Mon-Shu Ho, Qing Wu, Meng-Fan Chang, Yiran Chen and Hai Li, "RRAM-based Spiking Nonvolatile Computing-In-Memory Processing Engine with Precision-Configurable In Situ Nonlinear Activation", IEEE Symposium on VLSI Technology, pp. T86-T87, 2019.

[C3] **DAC'18: Bonan Yan**, Xiong Cao, and Hai Li, "A neuromorphic design using chaotic Mott memristor with relaxation oscillation", Design Automation Conference (DAC), pp. 1-6. 2018.

[C4] **DATE'18: Bonan Yan**, Fan Chen, Yaojun Zhang, Chang Song, Hai Li, and Yiran Chen. "Exploring the opportunity of implementing neuromorphic computing systems with spintronic devices." Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 109-112. 2018.

[C5] **IEDM'17: Bonan Yan**, Chenchen Liu, Xiaoxiao Liu, Yiran Chen, and Hai Li. "Understanding the trade-offs of device, circuit and application in ReRAM-based neuromorphic computing systems." IEEE International Electron Devices Meeting (IEDM), pp. 11-4. 2017.

[C6] **ICCAD'17: Bonan Yan**, Jianhua Yang, Qing Wu, Yiran Chen, and Hai Li. "A closed-loop design to enhance weight stability of memristor based neural network chips." International Conference on Computer-Aided Design (ICCAD), pp. 541-548. 2017.

[C7] **ISCAS'16: Bonan Yan**, Amr Mahmoud Mahmoud, Jianhua Joshua Yang, Qing Wu, Yiran Chen, and Hai Li. "A neuromorphic ASIC design using one-selector-one-memristor crossbar." IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1390-1393. 2016.

[C8] **NVMTS'16: Bonan Yan**, Zheng Li, Yiran Chen, and Hai Li. "RAM and TCAM designs by using STT-MRAM." Non-Volatile Memory Technology Symposium (NVMTS), pp. 1-5. IEEE, 2016.

[C9] **ASICON'15: Bonan Yan**, Yaojun Zhang, Enes Eken, Wujie Wen, Weisheng Zhao, and Yiran Chen. "Recent progresses of STT memory design and applications." IEEE 11th International Conference on ASIC (ASICON), pp. 1-4. 2015.

[C10] **GLVLSI'15: Bonan Yan**, Zheng Li, Yaojun Zhang, Jianlei Yang, Hai Li, Weisheng Zhao, and Pierre Chor-Fung Chia. "A High-Speed Robust NVM-TCAM Design Using Body Bias Feedback." Great Lakes Symposium on VLSI (GLVLSI), pp. 69-74. 2015.

[C11] **ITC'19:** Arjun Chaudhuri, **Bonan Yan**, Yiran Chen and Krishnendu Chakrabarty, "Hardware Fault Tolerance for Binary RRAM Crossbars", to appear in IEEE International Test Conference (ITC), 2019

[C12] **ASP-DAC'19:** Bing Li, **Bonan Yan**, Chenchen Liu, and Hai Li. "Build reliable and efficient neuromorphic design with memristor technology." Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 224-229. 2019.

[C13] **ASP-DAC'17:** Shihui Yin, Deepak Kadetotad, **Bonan Yan**, Chang Song, Yiran Chen, Chaitali Chakrabarti, and Jae-sun Seo. "Low-power neuromorphic speech recognition engine with coarse-grain sparsity." Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 111-114. 2017.

[C14] **DAC'15:** Chenchen Liu, **Bonan Yan**, Chaofei Yang, Linghao Song, Zheng Li, Beiye Liu, Yiran Chen, Hai Li, Qing Wu, and Hao Jiang. "A spiking neuromorphic design with resistive crossbar." Design Automation Conference (DAC), pp. 14. 2015.

[C15] **ISCAS'15:** Zheng Li, **Bonan Yan**, Lun Yang, Weisheng Zhao, Yiran Chen, and Hai Li. "A new self-reference sensing scheme for TLC MRAM." IEEE International Symposium on Circuits and Systems (ISCAS), pp. 593-596. 2015.

[C16] **DATE'15:** Yaojun Zhang, **Bonan Yan**, Wenqing Wu, Hai Li, and Yiran Chen. "Giant spin hall effect (GSHE) logic design for low power application." Design Automation & Test in Europe Conference & Exhibition (DATE), pp. 1000-1005. 2015.

[C17] **VLSI-SoC'15:** Zheng Li, Chenchen Liu, Yandan Wang, **Bonan Yan**, Chaofei Yang, Jianlei Yang, and Hai Li. "An overview on memristor crossbar based neuromorphic circuit and architecture." IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), pp. 52-56. 2015.

[C18] **ISVLSI'16:** Chenchen Liu, Qing Yang, **Bonan Yan**, Jianlei Yang, Xiaocong Du, Weijie Zhu, Hao Jiang, Qing Wu, Mark Barnell, and Hai Li. "A Memristor Crossbar Based Computing Engine Optimized for High Speed and Accuracy." IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 110-115. 2016.

Journals & Book Chapters:

[J1] **Bonan Yan**, Bing Li, Ximing Qiao, Cheng-Xin Xue, Meng-Fan Chang, Yiran Chen and Hai Li. "RRAM Based In-Memory Computing: From Device and Large-Scale Integration System Perspectives." Accepted by Advanced Intelligent Systems. 1900068 (2019).

[J2] **Bonan Yan**, Yiran Chen, and Hai Li. "Challenges of memristor based neuromorphic computing system." Science China Information Sciences (SCIS). 61, no. 6 (2018): 060425.

[J3] Qing Yang, **Bonan Yan**, and Hai Li. "Sensing of Resistive RAM." Sensing of Non-Volatile Memory Demystified. Springer, 2019. 31-45.

[J4] Yaojun Zhang, **Bonan Yan**, Xiaobin Wang, and Yiran Chen. "Persistent and Non-Persistent Error Optimization for STT-RAM Cell Design." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). 36, no. 7 (2017): 1181-1192.

[J5] Enes Ekens, Ismail Bayram, Yaojun Zhang, **Bonan Yan**, Wenqing Wu, Hai Li, and Yiran Chen. "Giant Spin-Hall assisted STT-RAM and logic design." Integration 58 (2017): 253-261.

[J6] Yue Zhang, **Bonan Yan**, Wang Kang, Yuanqing Cheng, Jacques-Olivier Klein, Youguang Zhang, Yiran Chen, and Weisheng Zhao. "Compact model of subvolume MTJ and its design application at nanoscale technology nodes." IEEE Transactions on Electron Devices (T-ED). 62, no. 6 (2015): 2048-2055.

REVIEWER

Journals:

IEEE Transactions on Electron Devices (T-ED)
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
ACM Journal on Emerging Technologies in Computing (JETC)
Elsevier Neurocomputing

Conferences:

IEEE International Symposium on Circuits and Systems (ISCAS)