BONAN YAN

701 W Main St Suite 400 bonan.yan@duke.edu
Durham, NC 27701 USA +1(412) 944-8877

CURRENT APPOINTMENT

Ph.D. Student at Duke University
Research interests:

- Computing-in-memory design with emerging nonvolatile memory technologies
- Emerging nonvolatile memory design
- Reliability for emerging nonvolatile memories

EDUCATION

Duke University — Durham, NC
Ph.D., Electrical and Computer Engineering, GPA: 3.84/4.0 — Expected 2020

University of Pittsburgh — Pittsburgh, PA
M.S., Electrical and Computer Engineering, GPA: 4.0/4.0 — 2014-2017

Beihang University — Beijing, China
B.S., Electrical and Computer Engineering (with honor) — 2010-2014
GPA: 3.84/4.0, Ranking: 2/267

RESEARCH EXPERIENCE

Duke University — Durham, NC
Graduate Researcher; Advisor: Dr. Hai Li, Dr. Yiran Chen — 2017-Present
RRAM Based Neuromorphic Accelerator Design

- Design efficient neuron circuit and integrate with the embedded 1T1R macro
- Build real-time demonstration of RRAM based computing-in-memory processing core
- Develop EDA method to tolerate RRAM non-ideal behaviors

University of Massachusetts, Amherst — Amherst, MA
Visiting Scholar; Advisor: Dr. Jianhua (Joshua) Yang — 11/2017-12/2017
Demonstration of RRAM Array for Neuromorphic Computing Acceleration

- Build RRAM/CMOS hybrid hardware demonstration for MNIST recognition

HP labs — Palo Alto, CA
Visiting Research Fellow; Advisor: Dr. Miao Hu — 05/2015-08/2015
Fast EDA Tool To Emulate Nonlinearity of Multi-Level RRAM

- Fit experimental RRAM (memristor) data into nonlinear differential model
- Build crossbar array level MATLAB simulator based on Jacobian matrix method

University of Pittsburgh — Pittsburgh, PA
Graduate Researcher; Advisor: Dr. Hai Li, Dr. Yiran Chen — 2014-2017
Emerging Memory Design

- Design reliable write/read circuit for 1T1R RRAM crossbar array
- Develop emerging STT-MRAM based TCAM using body effect

Beihang University Beijing, China
Undergraduate Researcher; Advisor: Dr. Weisheng Zhao 2013-2014
Compact Modeling of STT p-MTJ under 40nm

- Modeling the interface impact in MTJ for high spin-torque efficiency and Verilog-A coding

IC TAPEOUT EXPERIENCE

RRAM Based Modular NN Accelerator Controller submitted in 05/2019

- Technology: TSMC 65nm CMOS
- Target nonvolatile memory device: standalone 3-bit 1T1R/binary 1S1R RRAM array

RRAM Based Dot-Product Engine Controller submitted in 02/2017

- Technology: GlobalFoundries 130nm CMOS
- Target nonvolatile memory device: standalone 3-bit 1T1R/binary 1S1R RRAM array

RRAM Based Spiking Computing-In-Memory Processing Engine submitted in 10/2016

- Technology: TSMC 150nm CMOS
- Target nonvolatile memory device: embedded 64Kb 1T1R RRAM array

RRAM Based Brain-State-In-A-Box (BSB) Controller submitted in 05/2016

- Technology: GlobalFoundries 130nm CMOS
- Target nonvolatile memory device: standalone 3-bit 1T1R RRAM array

RRAM Based Feedforward Perceptron Controller submitted in 08/2015

- Technology: GlobalFoundries 130nm CMOS
- Target nonvolatile memory device: standalone 3-bit 1T1R RRAM array

1T1R RRAM Memory submitted in 04/2015

- Technology: HHNEC 130nm CMOS
- Target nonvolatile memory device: embedded binary 4Kb 1T1R RRAM array

TEACHING EXPERIENCE

University of Pittsburgh Pittsburgh, PA
Graduate Teaching Fellow 2014-2016
Course Teaching:

- ECE132: Digital Logic
- ECE1192: Introduction to VLSI Design
- ECE1193: Advanced VLSI Design
- COE147: Computer Organization and Assembly Language

PUBLICATIONS

Conferences:

[C1] **Bonan Yan**, Qing Yang, Wei-Hao Chen, Kung-Tang Chang, Jian-Wei Su, Chien-Hua Hsu, Sih-Han Li, Heng-Yuan Lee, Shyh-Shyuan Sheu, Mon-Shu Ho, Qing Wu, Meng-Fan Chang, Yiran Chen and Hai Li, “RRAM-based Spiking Nonvolatile Computing-In-Memory Processing Engine with Precision-Configurable In Situ Nonlinear Activation”, IEEE

Symposium on VLSI Technology, pp. T86-T87, 2019.

[C2] **Bonan Yan**, Xiong Cao, and Hai Li, “A neuromorphic design using chaotic Mott memristor with relaxation oscillation”, Design Automation Conference (DAC), pp. 1-6. 2018.

[C3] **Bonan Yan**, Fan Chen, Yaojun Zhang, Chang Song, Hai Li, and Yiran Chen. "Exploring the opportunity of implementing neuromorphic computing systems with spintronic devices." Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 109-112. 2018.

[C4] **Bonan Yan**, Chenchen Liu, Xiaoxiao Liu, Yiran Chen, and Hai Li. "Understanding the trade-offs of device, circuit and application in ReRAM-based neuromorphic computing systems." IEEE International Electron Devices Meeting (IEDM), pp. 11-4. 2017.

[C5] **Bonan Yan**, Jianhua Yang, Qing Wu, Yiran Chen, and Hai Li. "A closed-loop design to enhance weight stability of memristor based neural network chips." International Conference on Computer-Aided Design (ICCAD), pp. 541-548. 2017.

[C6] **Bonan Yan**, Amr Mahmoud Mahmoud, Jianhua Joshua Yang, Qing Wu, Yiran Chen, and Hai Li. "A neuromorphic ASIC design using one-selector-one-memristor crossbar." IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1390-1393. 2016.

[C7] **Bonan Yan**, Zheng Li, Yiran Chen, and Hai Li. "RAM and TCAM designs by using STT-MRAM." Non-Volatile Memory Technology Symposium (NVMTS), pp. 1-5. IEEE, 2016.

[C8] **Bonan Yan**, Yaojun Zhang, Enes Eken, Wujie Wen, Weisheng Zhao, and Yiran Chen. "Recent progresses of STT memory design and applications." IEEE 11th International Conference on ASIC (ASICON), pp. 1-4. 2015.

[C9] **Bonan Yan**, Zheng Li, Yaojun Zhang, Jianlei Yang, Hai Li, Weisheng Zhao, and Pierre Chor-Fung Chia. "A High-Speed Robust NVM-TCAM Design Using Body Bias Feedback." Great Lakes Symposium on VLSI (GLVLSI), pp. 69-74. 2015.

[C10] Arjun Chaudhuri, **Bonan Yan**, Yiran Chen and Krishnendu Chakrabarty, “Hardware Fault Tolerance for Binary RRAM Crossbars”, to appear in IEEE International Test Conference (ITC), 2019

[C11] Bing Li, **Bonan Yan**, Chenchen Liu, and Hai Li. "Build reliable and efficient neuromorphic design with memristor technology." Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 224-229. 2019.

[C12] Shihui Yin, Deepak Kadetotad, **Bonan Yan**, Chang Song, Yiran Chen, Chaitali Chakrabarti, and Jae-sun Seo. "Low-power neuromorphic speech recognition engine with coarse-grain sparsity." Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 111-114. 2017.

[C13] Chenchen Liu, **Bonan Yan**, Chaofei Yang, Linghao Song, Zheng Li, Beiye Liu, Yiran Chen, Hai Li, Qing Wu, and Hao Jiang. "A spiking neuromorphic design with resistive crossbar." Design Automation Conference (DAC), pp. 14. 2015.

[C14] Zheng Li, **Bonan Yan**, Lun Yang, Weisheng Zhao, Yiran Chen, and Hai Li. "A new self-reference sensing scheme for TLC MRAM." IEEE International Symposium on Circuits and Systems (ISCAS), pp. 593-596. 2015.

[C15] Yaojun Zhang, **Bonan Yan**, Wenqing Wu, Hai Li, and Yiran Chen. "Giant spin hall effect (GSHE) logic design for low power application." Design Automation & Test in Europe Conference & Exhibition (DATE), pp. 1000-1005. 2015.

[C16] Zheng Li, Chenchen Liu, Yandan Wang, **Bonan Yan**, Chaofei Yang, Jianlei Yang, and Hai Li. "An overview on memristor crossbar based neuromorphic circuit and architecture." IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), pp. 52-56. 2015.

[C17] Chenchen Liu, Qing Yang, **Bonan Yan**, Jianlei Yang, Xiaocong Du, Weijie Zhu, Hao Jiang, Qing Wu, Mark Barnell, and Hai Li. "A Memristor Crossbar Based Computing Engine Optimized for High Speed and Accuracy." IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 110-115. 2016.

Journals & Book Chapters:

[J1] **Bonan Yan**, Bing Li, Ximing Qiao, Cheng-Xin Xue, Meng-Fan Chang, Yiran Chen and Hai Li. “RRAM Based In-Memory Computing: From Device and Large-Scale Integration System Perspectives.” Accepted by Advanced Intelligent Systems, to appear August 2019.

[J2] **Bonan Yan**, Yiran Chen, and Hai Li. "Challenges of memristor based neuromorphic computing system." Science China Information Sciences (SCIS). 61, no. 6 (2018): 060425.

[J3] Qing Yang, **Bonan Yan**, and Hai Li. "Sensing of Resistive RAM." Sensing of Non-Volatile Memory Demystified. Springer, 2019. 31-45.

[J4] Yaojun Zhang, **Bonan Yan**, Xiaobin Wang, and Yiran Chen. "Persistent and Non-Persistent Error Optimization for STT-RAM Cell Design." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). 36, no. 7 (2017): 1181-1192.

[J5] Enes Ekens, Ismail Bayram, Yaojun Zhang, **Bonan Yan**, Wenqing Wu, Hai Li, and Yiran Chen. "Giant Spin-Hall assisted STT-RAM and logic design." Integration 58 (2017): 253-261.

[J6] Yue Zhang, **Bonan Yan**, Wang Kang, Yuanqing Cheng, Jacques-Olivier Klein, Youguang Zhang, Yiran Chen, and Weisheng Zhao. "Compact model of subvolume MTJ and its design application at nanoscale technology nodes." IEEE Transactions on Electron Devices (T-ED). 62, no. 6 (2015): 2048-2055.

REVIEWER

Journals:

IEEE Transactions on Electron Devices (T-ED)
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)
ACM Journal on Emerging Technologies in Computing (JETC)
Elsevier Neurocomputing

Conferences:

Design Automation Conference (DAC)
IEEE International Symposium on Circuits and Systems (ISCAS)