BONAN YAN

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RESEARCH INTERESTS

- Integrated circuit design with emerging nonvolatile memories
  - High-performance resistive or magnetic random access memories (ReRAM/MRAM)
  - In-Memory Computing interface and controller circuits
- Circuit and systems for brain-inspired computing systems
  - Spiking-based machine learning accelerator architectures and design automation
  - Computer-aided design for reliability enhancement

EDUCATION

Duke University Aug. 2017 - Expected May 2020
PhD Candidate in Electrical & Computer Engineering Advisor: Prof. Hai "Helen" Li, Prof. Yiran Chen

University of Pittsburgh Aug. 2014 - Jul. 2017
M.S. in Electrical & Computer Engineering Advisor: Prof. Hai "Helen" Li, Prof. Yiran Chen

Beihang University Sep. 2010 - Jul. 2014
B.S. in Electrical and Computer Engineering (with honor)

INTEGRATED CIRCUIT (IC) TAPE-OUT PROJECTS

RRAM Based Modular NN Accelerator Controller submitted in 05/2019
- TSMC 65nm CMOS, standalone 3-bit 1T1R/binary 1S1R RRAM array

RRAM Based Dot-Product Engine Controller submitted in 02/2017
- GlobalFoundries 130nm CMOS, standalone 3-bit 1T1R/binary 1S1R RRAM array
- Demonstration video: http://bit.ly/2IE3o85

RRAM Based Spiking Computing-In-Memory Processing Engine submitted in 10/2016
- TSMC 150nm CMOS, embedded 64Kb 1T1R RRAM array
- Demonstration video: http://bit.ly/AICHIP

RRAM Based Brain-State-In-A-Box (BSB) Controller submitted in 05/2016
- GlobalFoundries 130nm CMOS, standalone 3-bit 1T1R RRAM array

RRAM Based Feedforward Perceptron Controller submitted in 08/2015
- GlobalFoundries 130nm CMOS, standalone 3-bit 1T1R RRAM array

1T1R RRAM Memory submitted in 04/2015
- HHNEC 130nm CMOS, embedded binary 4Kb 1T1R RRAM array

PUBLICATIONS

CONFERENCE

1. **[IEDM'19]** Bonan Yan, Mengyun Liu, Yiran Chen, Krishnendu Chakarabarty and Hai Li. "On Designing Low-Power and Reliable Nonvolatile Memory-based Computing-In-Memory Accelerators." *IEEE International Electron Devices Meeting (IEDM)*, 2019.

2. **[VLSI'19]** Bonan Yan, Qing Yang, Wei-Hao Chen, Kung-Tang Chang, Jian-Wei Su, Chien-Hua Hsu, Sih-Han Li, Heng-Yuan Lee, Shyh-Shyuan Sheu, Mon-Shu Ho, Qing Wu, Meng-Fan Chang, Yiran Chen and Hai Li. "RRAM-based Spiking Nonvolatile Computing-In-Memory Processing Engine with Precision-Configurable In Situ Nonlinear Activation." *IEEE VLSI Symposium on Technology*, 2019.

3. **[DAC'18]** Bonan Yan, Xiong Cao, and Hai Li. "A neuromorphic design using chaotic Mott memristor with relaxation oscillation." *Design Automation Conference (DAC)*, 2018.

4. **[DATE'18]** Bonan Yan, Fan Chen, Yaojun Zhang, Chang Song, Hai Li, and Yiran Chen. "Exploring the opportunity of implementing neuromorphic computing systems with spintronic devices." *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2018.

5. **[IEDM'17]** Bonan Yan, Chenchen Liu, Xiaoxiao Liu, Yiran Chen, and Hai Li. "Understanding the trade-offs of device, circuit and application in ReRAM-based neuromorphic computing systems." *IEEE International Electron Devices Meeting (IEDM)*, 2017.

6. **[ICCAD'17]** Bonan Yan, Jianhua Yang, Qing Wu, Yiran Chen, and Hai Li. "A closed-loop design to enhance weight stability of memristor based neural network chips." *International Conference on Computer-Aided Design (ICCAD)*, 2017.

7. **[ISCAS'16]** Bonan Yan, Amr Mahmoud Mahmoud, Jianhua Joshua Yang, Qing Wu, Yiran Chen, and Hai Li. "A neuromorphic ASIC design using one-selector-one-memristor crossbar." *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016.

8. **[NVMTS'16]** Bonan Yan, Zheng Li, Yiran Chen, and Hai Li. "RAM and TCAM designs by using STT-MRAM." *Non-Volatile Memory Technology Symposium (NVMTS)*, 2016.

9. **[ASICON'15]** Bonan Yan, Yaojun Zhang, Enes Eken, Wujie Wen, Weisheng Zhao, and Yiran Chen. "Recent progresses of STT memory design and applications." *IEEE 11th International Conference on ASIC (ASICON)*, 2015.

10. **[GLSVLSI'15]** Bonan Yan, Zheng Li, Yaojun Zhang, Jianlei Yang, Hai Li, Weisheng Zhao, and Pierre Chor-Fung Chia. "A High-Speed Robust NVM-TCAM Design Using Body Bias Feedback." *Great Lakes Symposium on VLSI (GLVLSI)*, 2015.

11. **[DAC'20]** Qilin Zheng, Zishun Feng, Bonan Yan, Zongwei Wang, Yimao Cai, Ru Huang, Yiran Chen, Chia-Lin Yang and Hai (Helen) Li. "An ADC/DAC-less ReRAM-based Processing-In-Memory Architecture for Accelerating Deep Convolution Neural Networks." *Design Automation Conference (DAC)*, 2020 (accepted).

12. **[DAC'20]** Ziru Li, Bonan Yan, and Hai Li. "ReSiPE: ReRAM-based Single-Spiking Processing-In-Memory Engine." *Design Automation Conference (DAC)*, 2020 (accepted).

13. **[SPIE'20]** Brady Taylor, Ziru Li, Bonan Yan, Hai Li, Yiran Chen. "Highly efficient neuromorphic computing systems with emerging nonvolatile memories." *Proc. SPIE 11324, Novel Patterning Technologies for Semiconductors, MEMS/NEMS and MOEMS 2020*, 113240V (23 March 2020).

14. **[ITC'19]** Arjun Chaudhuri, Bonan Yan, Yiran Chen and Krishnendu Chakrabarty. "Hardware Fault Tolerance for Binary RRAM Crossbars." *IEEE International Test Conference (ITC)*, 2019.

15. **[ASP-DAC'19]** Bing Li, Bonan Yan, Chenchen Liu, and Hai Li. "Build reliable and efficient neuromorphic design with memristor technology." *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2019.

16. **[ASP-DAC'17]** Shihui Yin, Deepak Kadetotad, Bonan Yan, Chang Song, Yiran Chen, Chaitali Chakrabarti, and Jae-sun Seo. "Low-power neuromorphic speech recognition engine with coarse-grain sparsity." *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2017.

17. **[ISVLSI'16]** Chenchen Liu, Qing Yang, Bonan Yan, Jianlei Yang, Xiaocong Du, Weijie Zhu, Hao Jiang, Qing Wu, Mark Barnell, and Hai Li. "A Memristor Crossbar Based Computing Engine Optimized for High Speed and Accuracy." *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2016.

18. **[DAC'15]** Chenchen Liu, Bonan Yan, Chaofei Yang, Linghao Song, Zheng Li, Beiye Liu, Yiran Chen, Hai Li, Qing Wu, and Hao Jiang. "A spiking neuromorphic design with resistive crossbar." *Design Automation Conference (DAC)*, 2015.

19. **[ISCAS'15]** Zheng Li, Bonan Yan, Lun Yang, Weisheng Zhao, Yiran Chen, and Hai Li. "A new self-reference sensing scheme for TLC MRAM." *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015.

20. **[DATE'15]** Yaojun Zhang, Bonan Yan, Wenqing Wu, Hai Li, and Yiran Chen. "Giant spin hall effect (GSHE) logic design for low power application." *Design Automation & Test in Europe Conference & Exhibition (DATE)*, 2015.

21. **[VLSI-SoC'15]** Zheng Li, Chenchen Liu, Yandan Wang, Bonan Yan, Chaofei Yang, Jianlei Yang, and Hai Li. "An overview on memristor crossbar based neuromorphic circuit and architecture." *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 2015.

JOURNAL

22. **[Advanced Intelligent Systems]** Bonan Yan, Bing Li, Ximing Qiao, Cheng-Xin Xue, Meng-Fan Chang, Yiran Chen and Hai Li. "RRAM Based In-Memory Computing: From Device and Large-Scale Integration System Perspectives." *Advanced Intelligent Systems*, 1900068 (2019).

23. **[SCIS]** Bonan Yan, Yiran Chen, and Hai Li. "Challenges of memristor based neuromorphic computing system." *Science China Information Sciences (SCIS)*, 61, no. 6 (2018): 060425.

24. **[TCAD]** Yaojun Zhang, Bonan Yan, Xiaobin Wang, and Yiran Chen. "Persistent and Non-Persistent Error Optimization for STT-RAM Cell Design." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 36, no. 7 (2017): 1181-1192.

25. **[Integration]** Enes Ekens, Ismail Bayram, Yaojun Zhang, Bonan Yan, Wenqing Wu, Hai Li, and Yiran Chen. "Giant Spin-Hall assisted STT-RAM and logic design." *Integration* , 58 (2017): 253-261.

26. **[T-ED]** Yue Zhang, Bonan Yan, Wang Kang, Yuanqing Cheng, Jacques-Olivier Klein, Youguang Zhang, Yiran Chen, and Weisheng Zhao. "Compact model of subvolume MTJ and its design application at nanoscale technology nodes." *IEEE Transactions on Electron Devices (T-ED)*, 62, no. 6 (2015): 2048-2055.

BOOK CHAPTER

27. Qing Yang, Bonan Yan, and Hai Li. ""Sensing of Resistive RAM." Sensing of Non-Volatile Memory Demystified." *Springer*, 2019. 31-45.

TALKS & PRESENTATIONS

Conference Talks:

2019 IEEE Symposium on VLSI Technology	06/2019
2018 Design Automation Conference (DAC)	06/2018
2017 International Conference On Computer Aided Design (ICCAD)	11/2017

Posters:

2019 DAC PhD Forum 06/2019

2019 tinyML Summit @ Google 03/2019

Duke Center for Alternative Sustainable and Intelligent Computing (ASIC) 02/2019

AFRL/RI Neuromorphic Computing Workshop 05/2018

HONORS AND AWARDS

2019 IEEE Symposium on VLSI Technology Student Travel Grant

2019 DAC PhD Forum

2019 Duke University Pratt School of Engineering Travel Grant

2018 Duke University Pratt School of Engineering Travel Grant

2014 Outstanding Undergraduate Dissertation in Beihang University

TEACHING & MENTORING

Teaching Fellow/Assistant:

- Teaching Assistant at Duke University 2019
  - ECE566: Enterprise Storage Architecture
- Graduate Teaching Fellow at University of Pittsburgh 2014-2016
  - ECE132: Digital Logic
  - ECE1192/2192: Introduction to VLSI Design
  - ECE1193: Advanced VLSI Design
  - COE147: Computer Organization and Assembly Language

ACADEMIC SERVICES

Workshop Organizer

- ICCAD Workshop on Hardware and Algorithms for Learning On-a-chip (HALO) 2019
- Non-Volatile Memory Technology Symposium 2019

Reviewer

Journal:

- IEEE Transactions on Electron Devices (T-ED)
- IEEE Magnetics Letters
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Circuits and Systems I (TCAS-I)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Embedded Systems Letters (ESL)
- ACM Journal on Emerging Technologies in Computing (JETC)
- Elsevier Neurocomputing
- Elsevier Integration, the VLSI Journal
- Springer Journal of Electronic Testing: Theory and Applications (JETTA)

Conference:

- Design Automation Conference (DAC)
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)
- IEEE International Symposium on Circuits and Systems (ISCAS)