Homework 4

CDA 4102 / CDA 5155: Fall 2025

Due: November 18, 2025 at **11:30 pm** **Total Points:** 20 points

You are not allowed to take or give help in completing this assignment. Submit the PDF version of the submission in e-learning before the deadline. Late submission (email the PDF to parvath.harikris@ufl.edu) is allowed (up to 24 hours) with a 20% penalty (irrespective of whether it is late for 10 minutes or 10 hours). No grades for late submissions after 24 hours from the deadline. Handwritten (scanned PDF) submissions will NOT be accepted. Please write it in LaTeX or Microsoft Word and convert it to PDF. Please do not take any help from LLM (e.g., ChatGPT) or any other sources. Please do not include the questions in your solution (PDF) since it affects the plagiarism checker. Please include the following sentence on top of your submission (PDF):

I have neither given nor received any unauthorized aid on this assignment.

Problem 1 [6+6 points]

Answer the following questions about cache coherence protocol in a multiprocessor system. Assume that the memory locations (addresses) A1 and A2 has values 1 and 2, respectively. A1 and A2 are uncached initially. A1 and A2 are different blocks and are mapped to the same cache set in each cache and therefore A2 replaces A1 (and vice versa). Assume that the caches follow the writeback policy. Consider the following sequence of memory operations:

P1: Write A1=3

P1: Read A2

P2: Write A2=4

P1: Read A1

P2: Read A1

P1: Write A2=5

P2: Read A2

Simulate the cache coherence activities similar to the example given in the lecture slides (21-26 and 64-69 in multiprocessor.pptx) using the following table. Please add more rows for each operation (if needed). Please show all the events (exact order is not important).

a. Using the Snoopy Bus protocol:

	P1			P2			Bus				Memory
Step	State	Addr	Value	State	Addr	Value	Action	Proc	Addr	Value	Value
P1: Write A1=3	**E**	**A1**	**3**				**Write Miss**	**P1**	**A1**		A1 = 1 A2 = 2
P1: Read A2							**Read Miss**	**P1**	**A2**		
							Write Back	**P1**	**A1**	**3**	**A1 = 3** A2 = 2
	S	**A2**	**2**				**Read Data**	**P1**	**A2**	**2**	
P2: Write A2=4											
P1: Read A1											
P2: Read A1											
P1: Write A2=5											
P2: Read A2											

b. Using the directory protocol:

	P1			P2			Bus				Directory			Memory
Step	State	Addr	Value	State	Addr	Value	Action	Proc	Addr	Value	Addr	State	{Proc}	Value
P1: Write A1=3							**Write Miss**	**P1**	**A1**		**A1**	**E**	**{P1}**	A1 = 1 A2 = 2
	E	**A1**	**3**											
P1: Read A2							**Read Miss**	**P1**	**A2**					
							Write Back	**P1**	**A1**	**3**	**A1**	**U**	**{}**	**A1 = 3** A2 = 2
	S	**A2**	**2**				**Data Value Reply**	**P1**	**A2**	**2**	**A2**	**S**	**{P1}**	
P2: Write A2=4														
P1: Read A1														
P2: Read A1														
P1: Write A2=5														
P2: Read A2														

2. **[8]** Consider a snooping-bus based cache-coherent system with 2 processors (P1, P2). Each processor is equipped with a single-level cache. It is a direct cache design with two cache blocks. Each block has two words and each word is one byte. In other words, the cache size = 2x2x1 bytes. Note that, if an address is 1101, the rightmost bit ('1') is block offset, the next bit ('0') is index, and therefore, the leftmost two bits ('11') are tag bits.

   Complete the table below with both **cache content** (use alphabets) and **hit/miss** information (no explanation needed). In case of a miss, identify the primary **type of the miss**. Assume that the requests are issued from left to right; 2 words (since block size is 2) are read/written at a time. Use the following code for hit/misses.

   0 – Hit, 1 – Compulsory, 2 – Capacity, 3 – Conflict, 4 – True coherence, 5 – False Coherence

   We have 16 words in main memory from addresses 0000 to 1111, they are named using alphabets i.e.,

   A=0000, B=0001, C=0010, D=0011, E=0100, F=0101, G=0110, H=0111,

   I= 1000, J=1001, K=1010, L=1011, M=1100, N=1101, O=1110, P=1111

Proc.	**P1**	**P2**	**P1**	**P2**	**P1**	**P1**	**P2**	**P1**	**P1**	**P1**	**P2**
Request	Read	Write	Write	Read	Read	Read	Read	Read	Read	Write	Write
Address	**A**	**B**	**A**	**A**	**M**	**A**	**C**	**D**	**O**	**A**	**A**
P1 block0	AB										
P1 block 1											
P2 block0		AB									
P2 block 1											
Hit/Miss	**1**	**1**									