Digitizing and Modernizing a HP141 Display

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> When you ask God for a gift, be thankful if he sends not diamonds, pearls, or riches but the love of real, true friends.
>
> —*Muhammad Ali*

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To the Almighty God and my mother, thank you for applying the patience that was required to mould me into the person that I am today.

Abstract

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Abbreviations

ADC **A**nalog-to-**D**igital **C**onverter

AvM **A**verage **M**ode

BLE **B**luetooth-**L**ow **E**nergy

CRT **C**athode **R**ay **T**ube

DC **D**irect **C**urrent

DFT **D**igital **F**ourier **T**ransform

DSI **D**isplay **S**erial **I**nterface

DVI **D**igital **V**ideo **I**nterface

EDA **E**lectronic **D**esign **A**utomation

FFT **F**ast **F**ourier **T**ransform

FIFO **F**irst **I**n **F**irst **O**ut

FPGA **F**ield **P**rogrammable **G**ate **A**rray

HDL **H**ardware **D**escription **L**anguage

HDMI **H**igh **D**efinition **M**ultimedia **I**interface

HP **H**ewlett-**P**ackard Company

IF **I**ntermediate **F**requency

LCD **L**iquid **C**rystal **D**isplay

LO **L**ocal **O**scillator

MCU **M**icro**c**ontroller **U**nit

MSPS **M**ega **S**amples Per **S**econd

OLED **O**rganic **L**ight-**E**mitting **D**iode

OS **O**perating **S**ystem

PHM **P**eak **H**old **M**ode

RAM **R**andon **A**ccess **M**emory

RBW **R**esolution **B**andwidth

RF **R**adio **F**requency

RGB **R**ed **B**lue **G**reen

RTL **R**egister **T**ransfer **L**evel

RTSA **R**adio-**T**ime Spectrum Analayzer

RwM **R**a**w** **M**ode

SA **S**ignal/**S**pectrum **A**nalyzer

SBC **S**ingle-**B**oard **C**omputer

SDK **S**oftware **D**evelopment **K**it

SNR **S**ignal-to-**N**oise **R**atio

SPI **S**erial Peripheral **I**nterface

SPS **S**amples Per **S**econd

TFT **T**hin-**F**ilm **T**ransistor

UI **U**ser **I**nterface

USB **U**niversal-**S**erial **B**us

VSA **V**ector **S**pectrum **A**nalyzer

Chapter 1

Introduction

1.1 Background

Designed and patented in the 1970s, Hewlett-Packard Company's (HP) high performance plug-in model 8552B and 8555A spectrum analyzers (SA), equipped with the 141T display, remain powerful tools for characterising signals in the frequency domain. The 8552B is particularly convenient for measuring spectra in a wide frequency range between 20 Hz to 40 GHz. Another advantage of these spectrum analysers is that a user can broaden frequency requirements by increasing the number of tuning sections. Additionally, the 141T features absolute calibration of amplitude as well as high resolution, sensitivity and a simple display output.

The shortcoming of the spectrum analyzer, however, is that it uses a cathode ray tube (CRT) display which is prone to degradation after extended periods of usage and is outdated compared to the display on most modern devices. In this project, a single board computer and a liquid crystal display (LCD) touch screen is interfaced with the 141T display unit, thereby, replacing the outdated CRT technology. This allows users to continue to exploit the advantageous capabilities of the spectrum analyzer, such as the wide frequency bandwidth, despite damage to the CRT display. In addition, interfacing a single board computer with the 141T offers improved software-based features for performing frequency analysis.

Specifically, this project aims to develop a new display for the high resolution 8552B intermediate frequency (IF) section equipped with the 8555A spectrum analyzer radio frequency (RF) section which can make frequency domain measurements from 10 MHz to 18 GHz. The broad scanning frequency bandwidth of this model makes it suitable for frequency domain analyses in engineering applications such as mechanical vibrations and EMC field strength analysis with a calibrated antenna [1].

The CRT display subsystem consists of a post-accelerator storage tube with a 9 kV accelerating potential and aluminized P31 phosphor for producing high trace brightness. When calibrated, the CRT screen can display frequency bandwidths of up to 2 GHz wide. To display the full frequency range with a maximum of 18 GHz, the CRT can be calibrated in 10 frequency bands using internal mixing. One of advantage of the 141T over other displays that were manufactured during that time is that more detail can be observed in the spectrum by progressively narrowing frequency width from 100 Hz/division to 2 kHz/division. Overall, the 141T consists of a CRT graticule which can plot the frequency domain representation of a signal on a 2D plane with 8 x 10 divisions.

For this project, the 141T is powered by a 220 V single-phase source at 60 Hz, requiring less than

225 W even when plug-ins are connected. To achieve the 9 kV accelerating potential for deflecting electron beams in producing the CRT display, the device uses a step-up transformer and transistorized oscillator. The main disadvantage of having to increase the accelerating potential in a CRT display system is that the performance of electronic voltage regulation components such as capacitors, diodes and resistors can degrade over time.

Another challenge of using a phosphor CRT display is the effect of persistence on the saccadic information transfer which can lead to bias in experimental results [2]. This effect of persistence on experimental results is of particular interest to frequency domain analysis since displayed signals include noise from the environment which can make it difficult to extract accurate frequency information from plots. For the Model 141T, the persistence varies from the natural persistence of P31 phosphor (0.1 s) to a maximum of 15 s when the device is operating in the maximum writing rate mode. Therefore, phosphor persistence in the CRT display can significantly affect the amount of time to acquire measurements as well as the precision of the data extracted from the display.

1.2 Objectives

The aim of this project is to design a new display with full functionality and computer-aided signal processing features such as signal normalization. The digital display has to be compatible with the voltage outputs that enable analog signals to be plotted by the 141T. The aim of digitizing the signals is to interface measures from the spectrum analyzer with a computer that can perform tasks and store data accordingly. Therefore, a survey of the 8555A RF section and 8552B IF section outputs and available single board computer and touch screen options must be conducted. Furthermore, the project aims to investigate basic XYZ replicas, performing digital signal processing algorithms, how to correctly display signal data on annotated axes depending on available instrument settings.

This report aims to provide:

- Characterization of the HP141 display inputs from the 8555A RF section and 8552B IF section
- Available options for single-board computer and touchscreens options and the most suitable selection for interfacing with the two spectrum analyzer sections
- A design and simulation of interface between the single-board computer which includes analog converter for digitizing outputs from the RF and IF sections
- Algorithms for processing the digital signals and performing operations on displayed spectra
- Results on the construction, unit tests and integration tests of the improved system for spectral analysis

1.3 Project Requirements

Before detailing system requirements, user requirements were used to scope the project in terms of objectives that are not related to functions and performance. In designing the upgraded or 'new' SA, selection of hardware components was conducted with the aim of formulating specifications that

successfully fulfill user requirements. Table 1.1 summarises the user requirements and gives a short description of the objective.

Table 1.1: User requirements.

ID	Requirement Description
UR01	Display of the new SA must behave like the display of newer generations of SAs, such as the FieldFox. That is, the new SA must achieve more or less the same number data points as the FieldFox (801 points).
UR02	The SA must have the following display modes: (a) Peak hold mode (PHM) which displays the largest value seen and updated at each scan. (b) Average mode (AvM) in which each frequency bin's average is updated at each scan. (c) Raw mode (RwM) where the latest value is displayed until the next scan and overwriting each value during a scan event.
UR03	SA unit must have a suitable vertical resolution based on a 10 dB/division in the logarithmic scale.
UR04	Linear display mode must have low priority.
UR05	SA display subsystem must have setting markers, similar to the FieldFox analyzer.
UR06	Design must be capable of storing and recalling traces.
UR07	Users must be able to change modes by touching the screen and must be able to enter data using a keyboard.
UR08	All software must load on power up.
UR09	SA unit must use a single wall wart power source for the display subsystem.
UR10	Project must develop an HP141T display emulator of horizontal sweep, vertical sawtooth and pen lift state.

Table 1.2 details system requirements in terms of functions and performance. These requirements were developed after a review of the scope through the formalization of the user requirements in table 1.1 above.

Table 1.2: System requirements.

ID	Requirement Description
SR01	The system must digitize analog outputs from an HP141T 8555A model which performs frequency domain measurements between 20 Hz and 18 GHz.
SR02	Digitized outputs must be interfaced with a single board computer for performing signal processing tasks.
SR03	The system must include a signal conditioning box for debugging purposes and replicating the outputs of the spectrum analyzer during testing.
SR04	The system must be simulated using software.
SR05	The display must include new annotations that take instrument and operator manual inputs into account.
SR06	The system must include appropriate documentation such as tutorials and operational instructions when using the signal processor and screen.

In addition to the above mentioned system requirements, the project considers the basic configuration parameters that signal analyzers typically provide such as:

- Setting the minimum and maximum frequencies to be displayed based on a given center frequency

- Setting the reference amplitude for frequency responses and a span that is suitable for the spectrum analyzer
- Setting the frequency resolution according to the passband of the IF filter
- Setting the sweep time required to record the full frequency spectrum that is of interest

1.4 Scope & Limitations

The focus of this report is in the design and implementation of a digitized display for the HP141T that interfaces with a single board computer for storing and manipulating signal data from the oscilloscope. The scope is limited to selection of electronics that are suitable for converting the analog signals from the HP141T that are responsible for displaying signals. The scope only includes a survey of the HP141T circuits and outputs that directly affect how a spectrum is generated with respect to time domain and frequency domain analyses. The paper is not concerned with changing or improving the operational design of the device with respect to its power, amplification and filtering circuitry.

1.5 Report Outline

Chapter 2 initiates the report by establishing the general history and theoretical framework for the design and applications of spectrum analyzers in engineering. The same chapter details the previous techniques for converting the output of a SA to digital values that can be manipulated by a processor. Finally, designs of displays are explored in literature to establish an approach to representing the processor output on a LCD screen.

Chapter 2

Literature Review

The aim of this chapter is to conceptualize the operation of spectrum analyzers and establish a theoretical foundation for the frequency analysis techniques applied to produce the correct output. This conceptualization is then integrated with a broader review of digitizing and modernizing the display of spectrum analyzers.

In circumventing design limitations of spectrum analyzer displays, it is prudent to survey the most suitable hardware components. This is particularly true for the case where electronic components are required to perform in a broad frequency bandwidth. For example, for high frequency signals, the Nyquist theorem indicates that the ADC is required to have a sample at a frequency that is more than double the frequency of the output signal. Furthermore, the challenge of presenting signals in the frequency domain using electronics exists due to the fact the input signal to the ADC holds information about frequency in the time domain. Therefore, the investigation of literature that is presented in this chapter aims to provide a motivation for the design decisions taken in digitizing and modernizing the HP141T display.

The chapter begins with an evaluation of the frequency domain analysis theory that is applied in the operation of signal analyzers. Then, the different principles that distinguish different types of analyzers are explored to form the basis understanding the expected behaviour of a spectrum analyzer with specific settings. Following descriptions of the operation of spectrum analyzers from literature, the chapter includes a review of the investigation into different techniques for digitizing analyzer displays. This also includes a review of the different electronic components and techniques for digitizing frequency information in order to survey available hardware options that can be selected for a cost effective implementation. Finally, a broad discussion is included on different types of displays for analyzers in literature and a critique of the literature is provided to outline the purpose of the proposed design.

2.1 History and Fundamentals of Spectrum Analysis

2.1.1 Brief History of Spectrum Analyzers

2.1.2 Frequency Domain Analysis of Signals

2.1.3 Classifications of Spectrum Analyzers

2.2 Digitizing Spectrum Analyzer Outputs

2.2.1 Output Voltage Regulation and Preparation for Frequency Analysis

2.2.2 Transforming Spectrum Analyzer Output Signals to Digital Frequency Domain

2.2.3 Interfacing Computers with Spectrum Analyzers

2.3 Modern Spectrum Analyzer Displays

2.3.1 Configurations and Displayed Data in Modern Spectrum Analyzer Displays

2.3.2 Technological Developments in Signal Analyzer Displays

Chapter 3

Methodology

3.1 Methodology Outline

This chapter details the design process and approach employed in achieving the aim of the project which is to digitize and modernize the HP141T display by replacing the CRT monitor with a LCD touchscreen display that offers different functions and modes of operation. Design decision are also documented here, showing the considerations that were made based on the operation and outputs of the HP141T spectrum analyzer and ensuring that the newly integrated display is compatible with the device's hardware. For example, the design required selection of the digital hardware for processing the analog voltage signals from the SA. The selection of the digital processor made from single-board computers such as the Raspberry Pi 4 Model B, microcontrollers like the STM32F4 boards, FPGA such as the Artix-7 from Xilinix, or a heterogeneous digital processor which consists of a combination of these options.

Other considerations were made regarding the electronic circuits for converting the auxiliary output voltages from the HP141T to the appropriate voltage level for the operation of ADC. This chapter describes how together, the ADC and digital processor form a crucial part of the system. Additionally, the chapter details the software development kit (SDK) and associated coding language that was used. The selection of the development framework depended on the choice of processor and digital processing algorithms that were required to fulfil the project requirements. For example, assuming that a FPGA is the chosen digital processor, the SDK would include tools such as the AMD Vivado and electronic design automation (EDA) software and the choice of coding language between Verilog, VHDL, and SystemVerilog would depend on how comfortable the developer is in representing digital processing algorithms, such the DFT, using the chosen language.

Overall, this chapter documents an overview of the design methodology and different phases in the design process. The design process followed a variation of V-Model in which a series of iterative phases was implemented with a process checking mechanism. The chapter begins by highlighting the design stages and modularization of the system. Thereafter, the chapter includes an assessment of the project requirements detailed in introductory section. Finally, the chapter describes the use of findings from the review of requirements in informing the design decisions and specifications.

3.2 Phases in the Design Process

The design process was decomposed into four iterative stages as illustrated in Figure ?? below. The first stage documented the digitization requirements and listed examples of modern SAs in order to define the requirements for modernization. As shown in the methodology overview diagram, the first stage also included thorough investigation into methods that have been implemented in literature for upgrading the functions and performance of SAs. A theoretical framework for relevant information about signal processing was also formulated based on the literature to ensure that the display modes and functions were consistent with the mathematically derived expected outputs in the system.

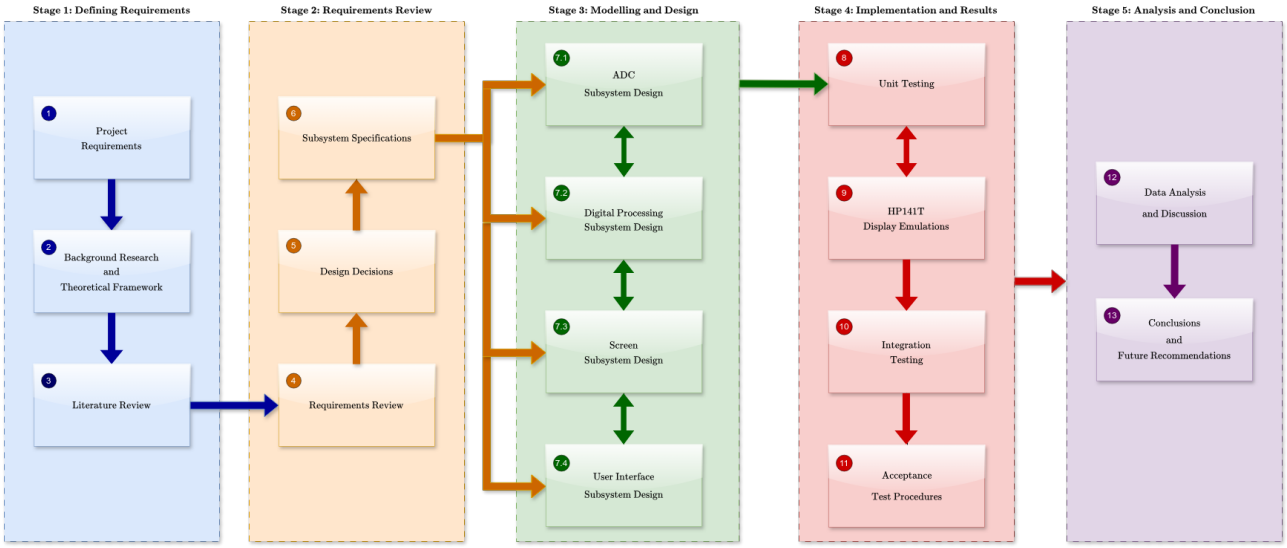

Figure 3.1: Methodology overview showing different stages in the iterative design process that was applied as a variation of the V-Model.

The second stage in the design process involved a review of the user requirements specifications detailed in chapter 1. The aim of this step in the methodology was to clarify the desired functions of the upgraded spectrum analyzer and to inform the design decisions with respect to the digital hardware and software development for digital signal processing. Additionally, the requirements review was employed in modularizing the design into four subsystems including, the Analog-to-Digital Conversion, Digital Processing, Screen and User Interface subsystems.

Stage 3 of the design process dealt with the design specifications of each of these subsystems by further decomposing each module into smaller hardware and software components. Each function is tested against a requirement in Stage 4 where each design specification was verified and the operation of the integrated system was tested to ensure that the interfaces between the subsystems was configured correctly.

In general, implementation of the design process adhered to the following design steps detailed in the project brief and are associated with the user requirement specifications:

1. Surveying the HP141T display and other outputs.
2. Surveying single-board computers and touchscreen options.

3. Phase One: establish a basic XYZ replica or HP141T emulator.
4. Phase Two: implement averaging and peak hold options.
5. Phase Three: annotate display axes.
6. Phase Four: determine the appropriate instrument settings.
7. Phase Five: design new annotations for display taking instrument or operator manual inputs into account.
8. Phase Six: include more tutorial and operational instructions using.

In finalizing the design process of the upgraded SA, results from acceptance tests were assimilated and a conclusion was drawn. Then, based on the outcomes of the project, future recommendations were made for future iterations of the upgrade SA system. Overall, the stages of the methodology included:

- Stage 1: Defining Requirements
- Stage 2: Requirements Review and System Overview
- Stage 3: Modelling and Design
- Stage 4: Implementation and Results
- Stage 5: Analysis and Conclusion

The first four stages of the design process were performed iteratively as a variation of the V-Model in which risk analysis was performed at each step, similar to the Spiral Model for design processes. Each iteration aimed at producing a new version of the upgraded HP141T display and a single conclusion was made when a satisfactory prototype was established.

3.3 Requirements Review

This section aims to clarify the scope of the project and produce a technical formalization of the user requirements specifications. The section begins by giving context to the term modernization by investigating the properties of modern SAs. Then, the section breaks down the user requirements into categories relating data acquisition, processing and display. Finally, the section concludes with a review of the requirement for developing a HP141T emulator.

3.3.1 Comparing the HP141T System to Modern Spectrum Analyzers

The first user requirement deals with the modernization of the HP141T system. The aim of this section is to review this requirement and to give clarification on the context of the use of 'modernization' in this project. To achieve this objective, the section begins with a description of the HP141T system and the functions that differ from 'modern' spectrum analyzers, such as the range of hand-held SAs by FieldFox, and the N9000B CXA SA manufactured by Keysight®. The section concludes with a summary table comparing the features of the HP141T system and modern spectrum analyzers.

The HP141T system is equipped with three plug-ins, namely the 8555A RF section which operates in the microwave region of the electromagnetic spectrum, the 8552B IF section and the Model 141T display which includes the CRT monitor. The three plug-ins operate in unison to electronically scan signals in the time-domain and provide a visual representation of the input signal's amplitude in the frequency domain on the CRT monitor [3]. Amplitude can be represented on a logarithmic (dB m) or linear scale (mV).

The 8555A and 8552B plug-ins apply principles of heterodyning spectroscopy, allows high frequency input signals with frequencies in the K-band of the microwave portion of the electromagnetic spectrum (i.e. 18 MHz) [4]. As noted from literature in the previous chapter, spectrum analyzers which rely on the FFT by sampling the continuous input signal and performing the Fourier transform on N total samples typically deal with signals that have lower frequencies. This is because SAs that employ the super-heterodyne principle like the HP141T determine the spectrum directly by analysis in the frequency domain and not from the time-dependent characteristics of the input signal. This is achieved by using a super-heterodyne receiver comprised of a mixer and tunable local oscillator (LO) which convert the input signal to an intermediate frequency as illustrated in figure ?? [5].

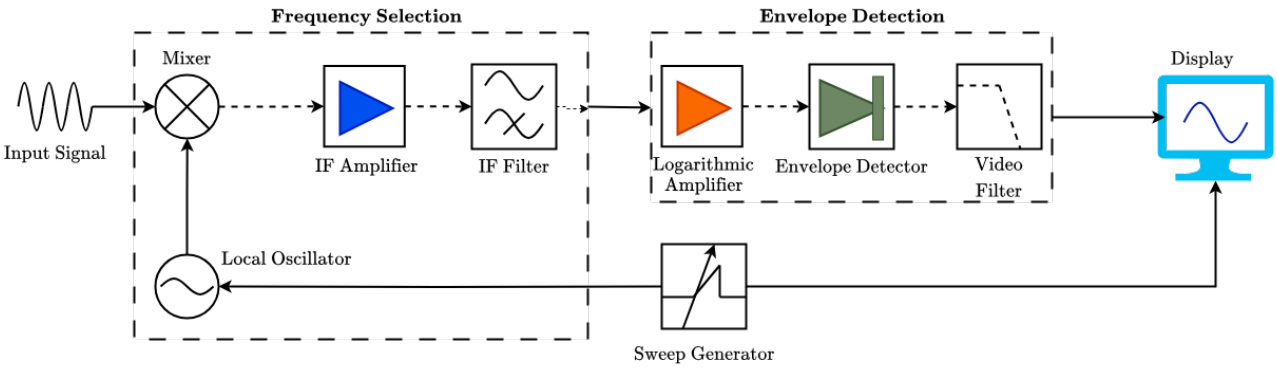

Figure 3.2: Heterodyne Spectrum Analyzer Block Diagram.

As noted in the literature review, most modern SAs are real-time spectrum analyzers RTSA which are a special case of vector spectrum analyzers (VSA) that use the super-heterodyne principle but digitize the input signal at the intermediate frequency, as shown in Figure ??, using a bandpass filter which can behave like a pre-select filter to limit distortions that arise from the mixer and shows the result in real-time. The advantage of digitizing the output of the IF section is that it enables large a input range of up to 50 MHz which can be analyzed in the time and frequency domain using digital signal processing techniques [6]. Much like FFT analyzers, vector analyzers are limited by the minimum and maximum sampling rate at which the ADC can operate. Additionally, exceedingly high sampling rates can lead to aliasing which causes frequencies outside of the bandwidth to fold into the frequency band [6].

Examples of modern real-time analyzers include:

- Tektronix RSA2208A which can scan input signals with frequencies of up to 8 GHz.
- Rohde & Schwarz FSP13 which operates within a 9 GHz to 30 GHz RBW.

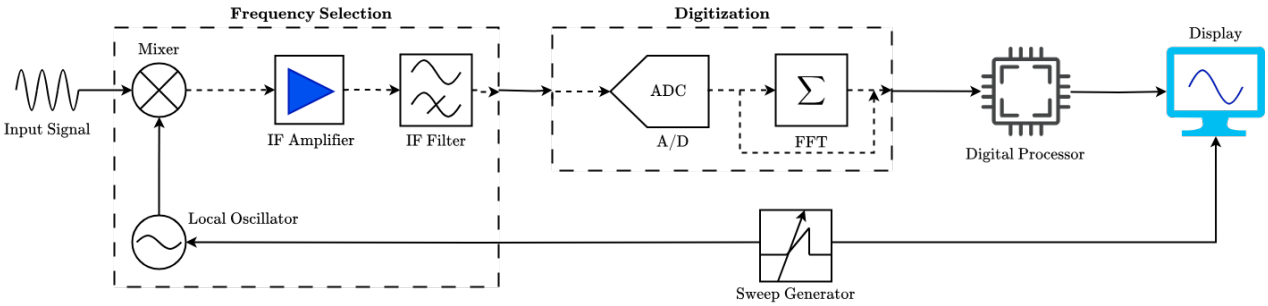

Figure 3.3: Vector analyzer block diagram showing digitization of the IF frequency.

- Agilent E4445A which offer frequency analysis up to 13.2 GHz.
- FieldFox RTSA which covers 5 kHz up to 50 GHz.

In modern RTSAs, IF analog output is transferred to the ADC through an anti-aliasing filter before being stored in memory [7]. This is in contrast to older heterodyne SAs such as the HP141T which takes the IF output through a video filter is essentially an averaging low-pass filter which smooths the IF output and reduces the effects of internal noise before the signal is channelled to the display [5]. HP141T video filters may select 10 Hz, 100 Hz, 10 kHz or OFF section of the low-pass filter for the detected video.

In the HP141T, the output of the video filter is transmitted to the vertical deflection of the CRT display [1]. For the horizontal deflection of the electron beam in the CRT display, a sawtooth signal from the sweep generator governs the horizontal scaling of the output frequency as electrons impinge on the phosphorescent screen. Modern SAs retrieve data from memory through high speed data lines to display information about the digital signal from the ADC. Digital display technologies include:

- LCD - most commonly used digital display which represents signal data with a sharp image and has low power consumption
- OLED - typically used in high performance SAs for displaying color coded spectrograms
- TFT - offer good visual quality and response time for sharper imagery when analyzing high frequency signals.

Displays in modern SA architectures offer more options for displaying frequency domain data. This is enabled by the processor, which is typically hosted on microcontroller board with high clock speed for performing digital signal processing algorithms. For example, RTSAs display the spectrogram as a color coded function of the amplitude of the signal [8]. In addition, digital displays generally consume less physical space compared to CRT displays with the same screen dimensions. This has allowed spectrum analyzers to become smaller as they entire system can fit into smaller packaging. For example, the FieldFox is an hand-held RTSA which despite its size, offers improved performance over the HP141T.

The comparison table in 3.1 below summarizes the differences between the HP141T analyzer (equipped with the 8555A and 8552B plug-ins) and modern RTSAs.

Table 3.1 shows that RTSAs also have connectivity abilities. For example, data can be transferred

Feature	HP141T	Real-Time Spectrum Analyzer
Operation	Heterodyne	FFT-based real-time processing
Frequency Range	10 GHz - 40 GHz	DC to 54 GHz
Scan Speed	0.1 ms/div - 10 s/div	Real-time GHz bandwidth capture with no losses
Dynamic Range	High but limited by analog filters	Very high due to digital signal processing
Resolution Bandwidth	Adjustable limited by analog filters	As low as 1 Hz
Real-time Capture	No. Displays active signals and struggles with pulsed signals	Yes. Captures transient and pulsed signals with ease
Signal Processing	Analog signal processing with IF filters and logarithmic amplifiers	Digital signal processing from ADC-sampled signal
FFT Capability	-	Built-in FFT
Display Type	CRT	LCD/OLED/TFT
Trace Storage	No memory.	Digital data storage
Connectivity	None	USB, Wi-Fi, Bluetooth, BLE
Size & Portability	Large and mountable on a rack	Compact and portable
Settings & Configuration	Manual tuning and calibration	Automated measurements, presets, user-friendly

Table 3.1: Comparing the features of the HP141T system to the modern RTSAs.

serially from on-board memory to an external device through the USB transfer protocol or through the BLE transfer protocol.

Features shown in the comparison formulated the modernization criteria to give context to the user requirement specification. Following sections expand on the features which can provide the functionality for associated requirements.

3.3.2 Data Acquisition in Digitizing the HP141T

As seen in the previous section, a primary criteria for modernizing HP141T is the translation of continuous analog input signals from the time domain to a digital signal that can be assessed using a digital processor such as a single-board computer, FPGA, or microcontroller. Selecting the point at which the conversion occurs in the pipeline of the HP141T super-heterodyne system plays a crucial role in the performance of the modernized system. The following project aimed to fulfil the signal conversion criteria by sampling the input signal at the intermediate frequency in a similar manner to the technique implemented by a modern RTSA and vector analyzers. In addition, user requirement UR01 states that the system needs to sample 801 points which is a standard for modern signal analyzers.

The following section reviews the user requirements to inform decisions about the data acquisition subsystem of the digitized HP141T subsystem. One of the most crucial parts in the design of the data acquisition subsystem is the selection of the ADC which samples signals and transmits them to the digital processor to store or manipulate signals in real-time. The section describes the limitations of this central part of the system and proposes solutions that can be implemented to fulfil the user requirements.

ADC Constraints

Table ?? shows constraints that influence the selection of the ADC and a solution for circumventing the limitation. For example, the operating voltage range of the ADC is a constraint which can be circumvented by including a signal conditioning circuit.

Constraint	Problem	Solution
Operating Voltage	Limited input voltage range of 0 V to 3.3 V or 5.0 V. The HP141T produces incompatible auxiliary output voltages	Signal conditioning circuit for scaling and shifting signals for compatibility with ADC operating voltages
Sample Rate	Required minimum of 801 points	Select an ADC with a high sampling rate (at 1 MSPS)
Resolution	Higher resolution is required for finer amplitude accuracy	Use an ADC with a minimum resolution of 16-bits
Number of Channels	The HP141T has 3 auxiliary outputs that are related to the frequency vs amplitude plot	Use an ADC with at least 3 channels
Latency	High latency can introduce delays in rendering signal data in real-time	Choose an ADC with SPI for low latency
SNR	ADC with a low SNR are more susceptible to noise and fluctuations in the amplitude	Use an ADC with a high SNR

Table 3.2: ADC selection constraints and solutions.

Conditioning HP141T Output Voltages to Match the ADC Operating Voltages

To satisfy the modernization requirement, an ADC with at least three channels is required to sample the three auxiliary analog output signals from the HP141T system that are shown in Table ?? below.

Label	Name	Range	Description
ν_{pen}	Pen-Lift	0 V to 14 V	Triggers the CRT display. The pen-lift output is 0 V during scanning
ν_v	Vertical Output	0 V to -0.8 V	Detected video output proportional to the vertical deflection on the CRT, corresponding to the amplitude of the signal in the frequency domain. Voltage range is scaled for full vertical deflection of the electron beam in 8 divisions of the CRT display
ν_h	Horizontal Output	-5 V to 5 V	Sawtooth signal for representing scaling frequency across 10 divisions of the horizontal deflection on the CRT display. The HP141T uses this output to control the trace of the spectrum across the screen.

Table 3.3: Auxiliary voltages of the HP141T that must be sampled to digitize the system.

Since the operating voltage of most ADCs is in the range between 0 V and 3.3 V or $\pm$5 V, the auxiliary outputs listed in table ?? need to be scaled and shift to be within the operating voltage range. To scale the signal, an op-amp with appropriate gain A can be used between the auxiliary outputs of the

HP141T and the input channels of the ADC. To shift the output voltages, a logic level-shifter can be used to translate the signals to be within the operating voltage domain.

Sampling Limitations in the Data Acquisition and Data Processing Subsystems

Among the constraints in the selection of the ADC is the requirement of the data acquisition subsystem to sample 801 points. Given that the 8552B has 16 internal scan rates from 0.1 ms/div to 10 s/div in a 1, 2, 5 sequence and given that the data acquisition subsystem needs to store 801 points per scan, the fastest scan rate, corresponding to 0.1 ms/div, can be achieved using an ADC with a sampling rate of

$$\frac{801\text{samples}}{0.1\,\text{ms}} = 8.01\ \textbf{MSPS}$$

Similarly, for the slowest scan rate corresponding to 10 s/div, the required minimum sampling rate of the ADC is 80.1 SPS.

In addition to the sample rate of the ADC, the design must take several factors into account regarding the integration of the ADC with a digital processor such as a SBC, MCU, or FPGA. Table 3.4 shows the considerations that need to be made in selecting a digital processor that is compatible with the operation of the ADC and high sampling rate.

Digital Processor Type	Consideration	Feature
MCU	Communication Interface	Supports I^2C and SPI
	Data Transfer Rate	Up to hundreds of MHz
	Synchronization and Timing	Can use interrupts and FIFO buffers
SBC	Communication interface	Supports I^2C and SPI
	Data Transfer Rate	Suited for low sampling rates
	Synchronization and Timing	Requires buffering and introduces operating system relating delays
FPGA	Communication Interface	Supports SPI and high-speed parallel interfaces
	Data Transfer Rate	Can handle sampling rates at hundreds of MHz to GHz speeds.
	Synchronization and Timing	Uses parallel data pipelines suitable for high-speed sampling rates for real-time spectral analysis applications.

Table 3.4: Digital processor selection based on ADC interface considerations.

Table 3.4 indicates that to fulfil the requirement for sampling 801 points per scan, the design that can deliver the highest performance in real-time data acquisition should include an ADC which can perform 8.01 MSPS and a FPGA with multiple pipelines for storing and processing rapidly sampled data in parallel. Alternatively, a heterogeneous digital processor can be implemented using a suitable combination of the available options listed in the table. For example, a Xilinx Artix-7 FPGA can be used for high-speed data acquisition while a Raspberry Pi SBC is used to process and display data. MCUs can also be daisy-chained to perform different tasks in the data acquisition subsystem.

Further Design Considerations in Digital Processor Selection

While FPGAs offer superior speeds in data acquisition and processing, one of the shortcomings of selecting it as the primary digital processor is that the overall development time is typically longer than the design time for MCUs and SBCs. This is because FPGA development has a structured design flow which includes details of the register-transfer level (RTL) using a hardware description language (HDL), validation, synthesis and implementation. Although tools like AMD Vivado exist to significantly reduce FPGA development times, the other available options offer significantly shorter development times.

Table ?? gives a comparison between the available digital processor options to highlight the most suitable option for fulfilling the requirements of this project.

Design Aspect	MCU	SBC	FPGA
Development Time	Short	Moderate	Long
Processing Speed	Medium	Moderate to High	High
Programming Language	C/C++	Python or C/C++	VHDL or Verilog
On-board Memory and RAM	Very Low	High	Low
Power consumption	Low	High	Moderate to High
Scalability	High	Moderate	High
Cost	Low	Moderate to High	High

Table 3.5: A structure comparison of the available digital processor options.

The different benefits of choosing a certain digital processor can be deduced from Table 3.4 and ??. Other considerations need to made regarding the memory capacity of the chosen processor, however, the primary objective is to satisfy UR06 which requires the data acquisition subsystem to be capable of storing and recalling traces. Due to the high sampling rate, the device must have a sufficient large memory capacity for storing signal frequency and amplitude related information at high-speeds. Specifically, given that a minimum sampling rate of 8.01 MSPS is required and supposing that the resolution of the ADC is 16-bit, the device must be able to store

$$8.01\text{MSPS} \times 16\,\text{bit} = 128\,160\,000\,\text{bit}\,\text{s}^{-1}$$

In other words, the device must be able to store $16.02\,\text{MB}\,\text{s}^{-1}$, which equates to approximately 1 GB per minutes. Thus, the selected digital processor must include efficient memory management algorithms to ensure that data is not lost or corrupted. The table indicates that the MCU has the most limited capability with respect to memory. This is because MCUs typically have few KB to MB of RAM and require external memory. Similarly, FPGAs offer limited memory capabilities since they typically use a small embedded RAM and require external memory for large data buffers.

In summary, the MCU is most suitable for its low cost, low power consumption, good real-time capabilities and short development time. However, the MCU is only suitable for moderate-speed sampling, which is not ideal for the high sampling rates that are needed to fulfil the requirements. While SBCs offer intermediate performs and features that combine the moderate capabilities of MCUs

and FPGAs, their primary shortcoming is poor real-time capabilities due to OS delays and overall low latency. Finally, the best option for this application is the FPGA due to its ability to perform real-time high-speed data processing and ADC synchronization, however, the biggest shortcomings are the development time and high cost.

3.3.3 Design Considerations in Satisfying Display Requirements

The choice of display depends on the selected processor type. The display hardware must satisfy multiple user requirements including UR03, UR07 and UR09 which are related to resolution, functionality and power. Further considerations have to be made for the display to satisfy requirements relating to the user interface (UI). The following section breaks down these requirements separately to evaluate the design choices that need to be made in modernizing the HP141T display.

Display Hardware Considerations for a MCU-Based System

Table 3.6 assimilates the design considerations for a MCU-based system. Overall, the design needs to consider factors such as clock and I/O speed, memory, power consumption and the display interface.

Key Consideration	Aspects	Description
Processor	Clock Speed	Clock speed of at least 100 MHz for rendering 801 points per scan to the display
	Architecture	A 32-bit ARM Cortex-M series MCU is preferred for good balance between power efficiency and speed
	I/O Speed	ADC waveform samples need to be rendered at high speeds. SPI is recommended for improving latency
Memory	RAM	At least 128 kB of RAM required for real-time display rendering
	Flash Memory	Required for storing firmware and display configurations which need to be loaded during power-up.
Interface	Compatibility	Should support the same communication interfaces as the display screen.
	Resources	Modern displays include internal frame buffers which can reduce the effect of memory and data transfer bottlenecks.
Power	Compatibility	System must be powered by a single wall wart power supply.
	Efficiency	Low-power and standby modes can reduce energy consumption when the display is idle.

Table 3.6: Key considerations for the display subsystem for a MCU-based system.

Display Hardware Considerations for a SBC-Based System

If the chosen digital processor is a single-board computer such as the Raspberry Pi 4B, similar considerations need to be made regarding its compatibility of the display unit. Differences arise from the hardware capabilities that the SBC offers. Table 3.7 summarizes the design considerations that need to be made for the interface between SBC and the display unit.

Key Consideration	Aspects	Description
Resolution	1080p at 60Hz	Recommended for smooth spectrum rendering; higher resolutions.
	HDMI 2.0	A high-speed HDMI 2.0-compatible display is required for the best display quality.
HDMI	HDMI Version Support	Older monitors may only support HDMI 1.2, which could limit resolution and refresh rates
	Data Handling	Improper extended display identification data detection may require manual configuration
	Adapter	Micro-HDMI to HDMI adapters are required. Faulty adapters may introduce noise
Touch	Touch Display	Dedicated SBC touchscreens can be used
	DSI	Raspberry Pi touchscreen connect via the DSI (Display Serial Interface) without required HDMI
	Power	Dedicated screen can be powered by the SBC
Monitor	Compatibility	Selected display must support the required resolution and refresh rate for clear visualization of digitized spectra.
	Over-scanning	Display adjustments may be required for screens that crop spectrum visualizations.
Software	OS Support	Dedicated OS recommended for compatibility with built-in display drivers and utilities.
	Settings	Used to adjust display resolution, rotation, and other settings for the most suitable spectrum visualization.

Table 3.7: Display considerations for screen integration with a SBC-based system.

Display Hardware Considerations for a FPGA-Based System

Although FPGAs offer the best performance with respect to sampling rates and data processing speeds, they are not as suitable for processing display data compared to SBCs. However, the real-time capabilities of the FPGA-based system can provide a seamless user experience by rendering spectrum displays at a high frame rate. Table 3.8 lists the design considerations for the display of a FPGA-based system.

Display User Interface

User requirements relating to the aspects of the display that the user can interact with include UR02, UR04, UR05 and UR07. The primary objective of the project is to display a plot of the amplitude vs frequency for the input signal, in real-time. To achieve this objective, spectrum data needs to be organized and easily accessible from RAM or flash memory, depending on the architecture of the system that is centred around the ADC and digital processor. For example, STM microcontrollers have a dedicated LCD-TFT display controller with a frame buffer that can be located either in on-chip memory or in an external memory, depending on the resolution. Using external memory can increase latency which decreases the real-time performance of the system.

In addition, data needs to be scaled while considering the effects of windowing, so that all spectrum data can be translated to a grid with 8 divisions of the amplitude, on the vertical axis, and 10 divisions of the frequency, on the horizontal axis. This is also to ensure that the appearance of the CRT display,

Key Consideration	Aspects	Description
Video Output	HDMI Support	Different FPGAs feature built-in HDMI, DVI transmitters or external serializer chips. The chosen FPGA must support high-speed video output
	Parallel	For parallel RGB inputs, the FPGA must generate compatible timing signals for proper synchronization
	Buffering	Additional external memory may be required for storing video frames before display
Synchronization	Pixel Clock	Display's resolution and refresh rate requirements must be compatible with a stable FPGA pixel clock
	Fabric Speed	Spectrum updates can be rendered rapidly using the high-speed fabric which ensure low-latency
Interface	Protocols	The display must be able to interface with the available hardware on the FPGA
	Controller	Display must be compatible with FPGA IP cores for developing display functionality more easily
	Resources	Optimization is needed to balance consumption of FPGA logic, memory block and I/O pins by the display unit
Memory	RAM	External DDR memory may be necessary for extending limited on-chip RAM capacity
	Storage	Efficient memory management is essential to prevent bottlenecks
Power	Delivery	Some high-speed video interfaces require additional power regulators
	Heating	FPGA video processing generates heat which may require cooling to prevent damage to components of the FPGA
Software	Drivers	Display drivers must be implemented using HDL or software cores
	Updates	Updates must occur in real-time and support different display modes

Table 3.8: Display considerations for an FPGA-based HP141T modernization system.

as shown in Figure 3.4, is maintained.

Secondary objectives include digitizing the operations that were previously executed by physical knobs such as horizontal and vertical scaling of the waveform. This objective can be as functions in a program that can be called to perform similar task. The choice of coding language and available development tools for the program that runs the display is a critical part of the UI subsystem.

An alternative approach to handling data acquisition and display functions on the same board would be to use a single-board computer for the display. Spectrum data can be retrieved from memory and displayed to the user in a Python, C/C++ or Java program. Knobs can be replaced by programmatic buttons with functions that users can access by touching the screen. This can allow other features such as averaging and displaying maxima and minima to be easily accessible to the user. For this project, UI must enable users to select between different display modes, including the PHM, AvM and RwM.

Figure 3.4: HP141T CRT display section.

The UI must enable users to switch between these modes seamlessly and allow for back them to return to previous screens using a back button in the program.

Overall, the project aims to adhere to Nielsen's heuristic design principles which includes:

1. Match between the system and the HP141T - the program should use the language and current features of the HP141T that users are familiar with
2. User control and freedom - the UI must support undo, redo and exit points
3. Aesthetics and minimalist design - the most relevant information that must be displayed is related to the frequency plot of the input signals as well as configurations and settings of the data acquisition and digital processing units that give context to the current display
4. Flexibility and efficiency of use - the UI interface of the modernized HP141T must be optimized for difference experience levels through suitable shortcuts and frequent actions such as averaging and showing maxima and minima of the input signal.
5. Help and documentation - documentation of the modernized HP141T display must correspond to current documentations of the entire system and must be easy to read
6. Error prevention - the UI must protect users from deleting stored traces and signal information
7. Visibility - a user must always know what is happening within the program and current state of their actions

8. Consistency and standards - the appearance of the UI must follow the conventions of modern spectrum analyzer displays through consistent words, situations and actions.

9. Help user to recognize, diagnose and recover from errors such as closing windows with information about pulses or signal noise

10. Recognition rather than recall - minimize users' memory load by making program features that are related to the most accessed signal data easy to access

3.3.4 Equipment for Debugging and Testing

The following section gives a review of the project requirement which necessitates the development of an HP141T display emulator of the three auxiliary outputs as shown in ??. Additionally, the section describes software-based simulation tools that can be used in the development for debugging and obtaining an idea about the expected behaviour individual hardware components and overall system.

Emulating HP141T Auxiliary Outputs

The sawtooth signal can be generated using a 555-timer circuit which produces a ramp voltage with adjustable frequency to mimic the adjustable scan time, and a fixed peak-to-peak voltage of 10 V with no DC offset. This is to ensure that the horizontal sawtooth output range between -5 V and $+5$ V is maintained.

To emulate the vertical output which swings between 0 V and -0.8 V, a simple voltage biasing circuit can be built with appropriate resistor values and input voltage. To control this level, a potentiometer can be used to manually adjust the voltage level within that range. Similarly, the pen-lift output can be produced using a biasing circuit with a potentiometer that allows the voltage to swing between 0 V and 14 V.

Lastly, the HP141T display emulator circuit needs to interface with the signal conditioning circuit that prepares the signal voltages to match the operating range of the ADC. Therefore, to avoid the development of multiple circuits, the output cables of the display emulator must be the same as the output cables that take the auxiliary outputs from the HP141T to the signal conditioning circuit.

Software-Based Simulation Tools

To optimize the selection and configuration of the data acquisition subsystem, ADCs can be simulated in MATLAB using Simulink to understand the behaviour of the sawtooth input from the HP141T or emulating hardware. Additionally, Simulink provides visualizations of the spectrum of the ADC output which can be used to determine the expected values from sampling signals. Simulink also allows users to add impairments to the ADC for introducing a layer of non-linearity that may be seen for signals with frequencies that are close the edges of the RBW or intermediate frequency.

Electronic circuits, such as the signal conditioning circuits with op-amps and level-shifters, can be simulated using LTSpice to predict the expected behaviour. Output values from LTSpice simulations can be used to simulate the behaviour of the system using Simulink with MATLAB.

3.4 System Design

Design decisions in formulating the specifications were informed by the requirement review in the previous section. This section aims to give a full description of the system and the interfaces between the different subsystems. The section begins with a visual representation of the system using a block diagram. Following the visual representation of the design, the section includes specifications and concludes with acceptance and integration tests.

3.4.1 System Block Diagram

The system block diagram is shown in Figure 3.5 below. The diagram shows that the modernized HP141T maintains the basic analog signal processing functionality, similar to modern RTSAs. The main difference between the architecture of vector analyzers and the proposed system is that this system includes a signal conditioning circuit and memory to store ADC values during each scan.

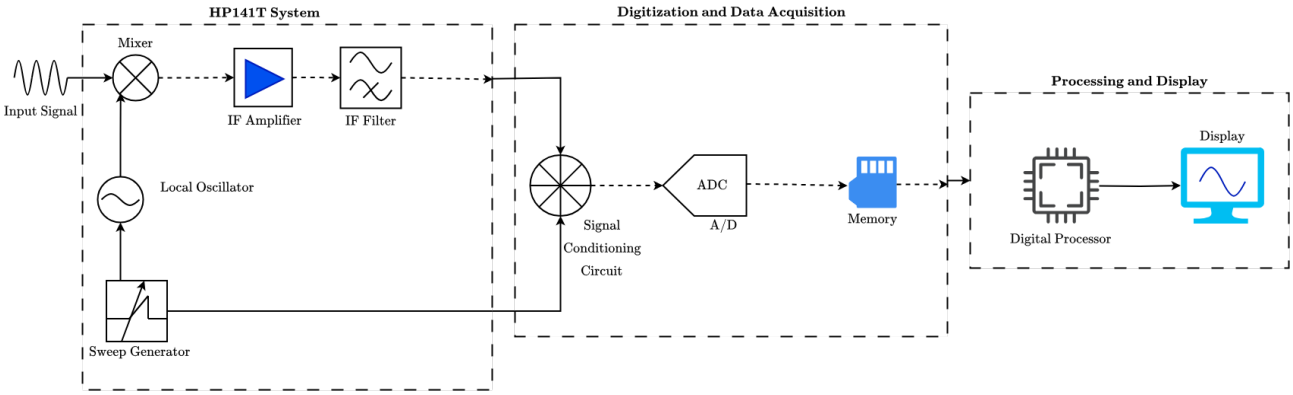

Figure 3.5: Proposed system diagram which includes the HP141T plugin sections.

Chapter 4

Results

Chapter 5

Discussion

Chapter 6

Conclusions

> The same rule holds for us now, of course: we choose our next world through what we learn in this one. Learn nothing, and the next world is the same as this one.
>
> —*Richard Bach, Jonathan Livingston Seagull*

The purpose of this project was to...

This report began with...

The literature review was followed in Chapter...

The bulk of the work for this project followed next, in Chapter...

In Chapter...

Finally, Chapter... attempted to...

In summary, the project achieved the goals that were set out, by designing and demonstrating...

Chapter 7

Recommendations

> It is for us the living, rather, to be dedicated here to the unfinished work which they who fought here have thus far so nobly advanced.
>
> —*Abraham Lincoln*

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