Digitizing and Modernizing an HP141-display

Bonga Njamela, University of Cape Town, South Africa

Supervised by: Dr Stephen Paine & Professor Emeritus Michael Inggs

Background

The HP141T display, introduced in the 1970s, employs the HP8555A and HP8552B spectrum analyzers to achieve a wide frequency range of 20 Hz to 40 GHz with absolute amplitude calibration and high resolution. However, the CRT display suffers from degradation, persistence effects, and outdated technology which limits its modern applicability. The primary objective of this project is to replace the CRT with a digital LCD touchscreen while ensuring compatibility with the 8555A/8552B plug-ins over a 10 MHz to 18 GHz bandwidth.

Methodology

The methodology implemented a modular system design to digitize the HP141T. The Signal Conditioning Subsystem (SCS) scaled analog outputs (to a 0 V to 3.3 V range) using op-amps, while the Data Acquisition Subsystem (DAS) digitized signals with the Picoscope 2204A as a substitute for the planned STM32H723ZG (7.2 MSPS), targeting 801 points per scan.

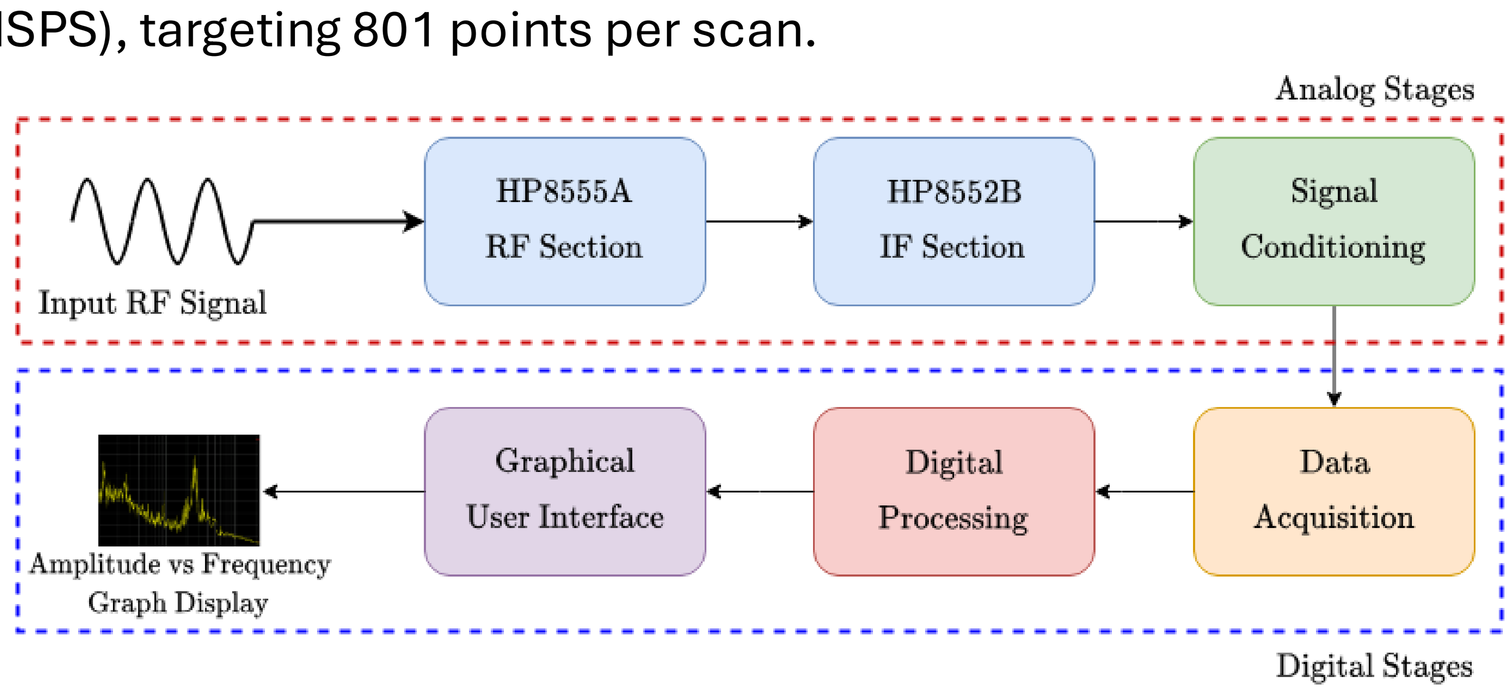

Figure 1: Overall System Diagram.

The Digital Processing Subsystem (DPS) on a Raspberry Pi 4B processed data for Peak Hold Mode (PHM), Average Mode (AVM), and Raw Mode (RWM), and the Graphical User Interface Subsystem (GUIS) rendered results on a 7-inch TFT touchscreen (800x480) using matplotlib and tkinter with an 8x10 grid.

Testing utilized the Siglent SDG1010 and HP-E3630A, with unit, integration, and acceptance tests (UR01-UR10, SR01-SR06) conducted via Picoscope 7 software on a Linux Dell Inspiron 15.

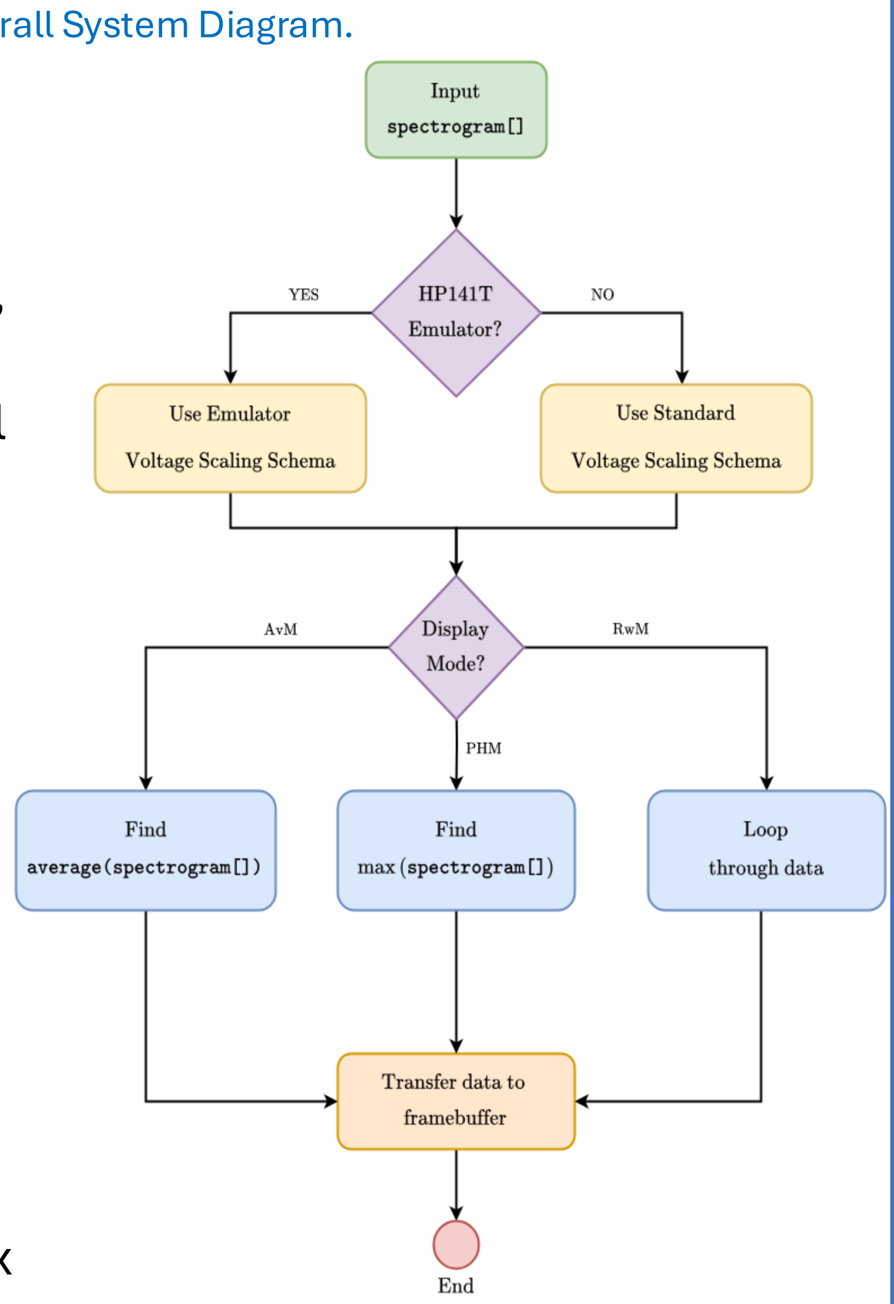

Figure 2: DPS flow diagram.

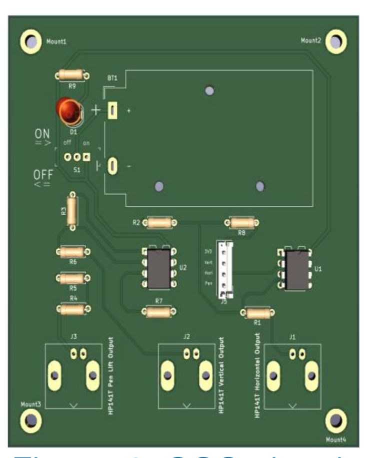

Figure 3: SCS circuit.

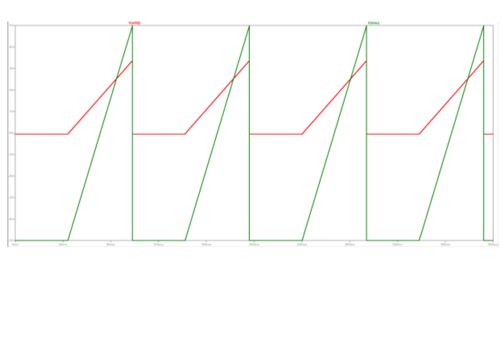

Figure 4: Simulated results.

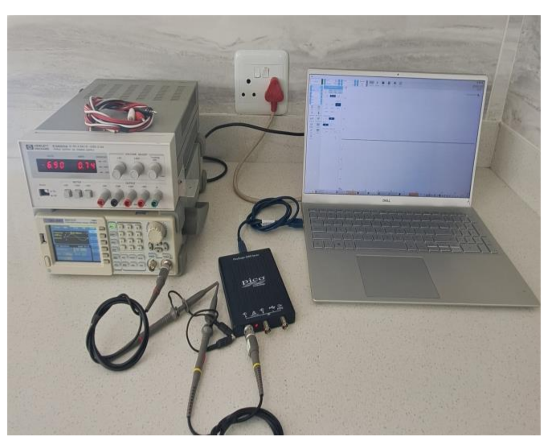

Figure 5: Test Environment.

Results

Testing revealed mixed outcomes for the digitized HP141T system. The HP141T system tests approximated the vertical output with a 10% deviation and successfully mimicked 300 kHz fluctuations using Gaussian noise (σ = 136.2 mV, μ = -0.200 mV), but horizontal and pen-lift emulation failed due to waveform shape mismatches and voltage limits (±7 V vs. 0 to 14 V).

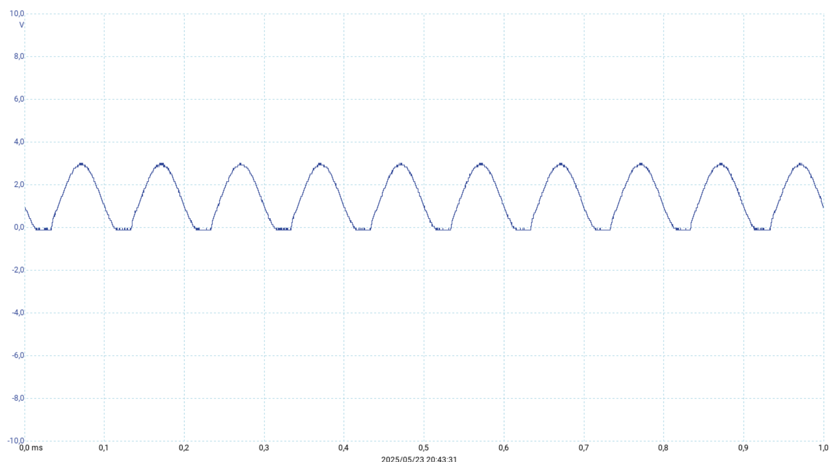

Figure 6: SCS output for Vy = –0.8 V at 10 kHz.

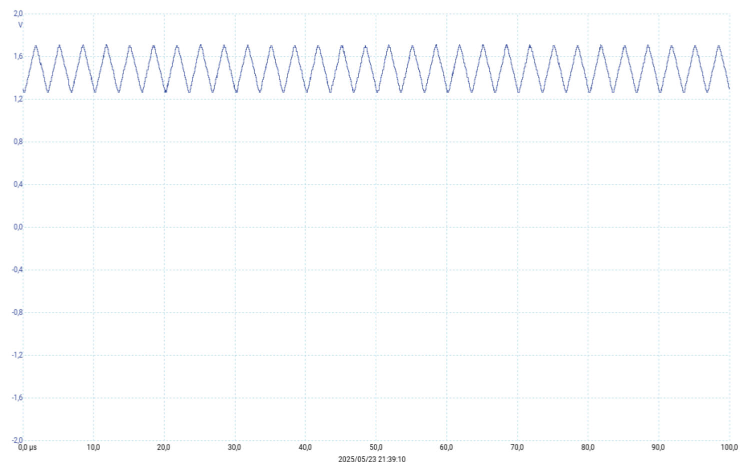

Figure 7: SCS output for Vy = –0.8 V at 300 kHz.

The SCS effectively scaled inputs (e.g., -0.2 Vpp to 0.7 V), handled noise, but exhibited clipping at -0.8 Vpp, which improved at 300 kHz. The DAS captured 6257 points at 3.3 kHz, exceeding requirements, while the DPS and GUIS met all tests, delivering 50-100 ms updates and accurate PHM/AVM/RWM displays.

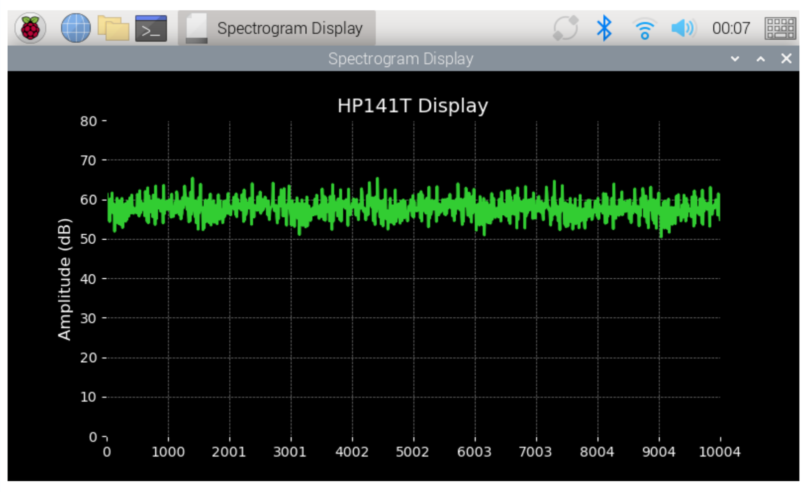

Figure 8: RWM samples of a noisy Vy on the digitized HP141-display.

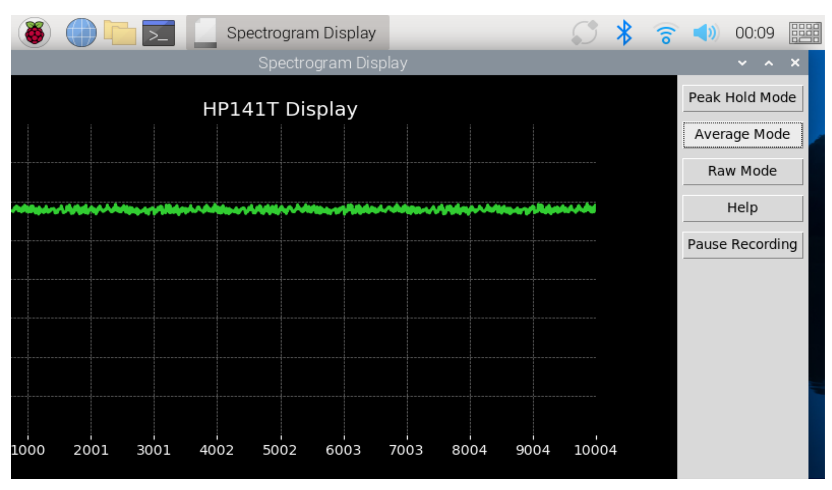

Figure 9: AVM applied to the noisy Vy with μ = -0.200 mV.

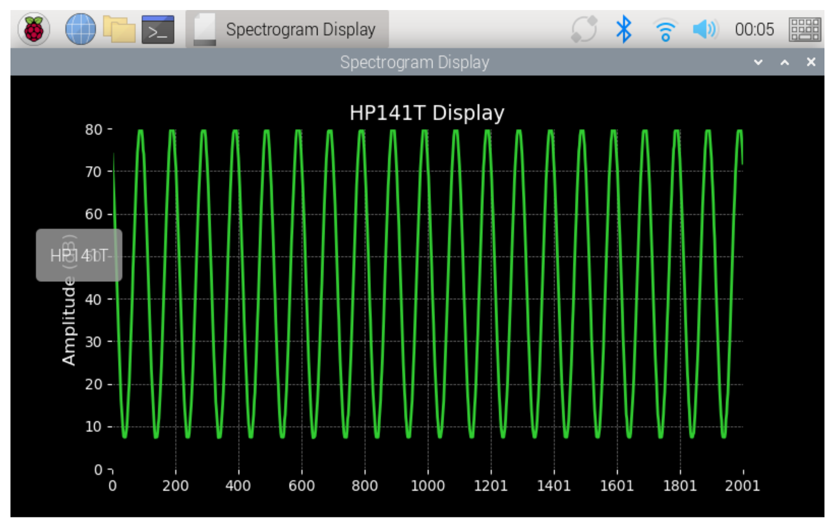

Figure 10: Sinusoidal RWM samples of Vy on the digitized HP141-display.

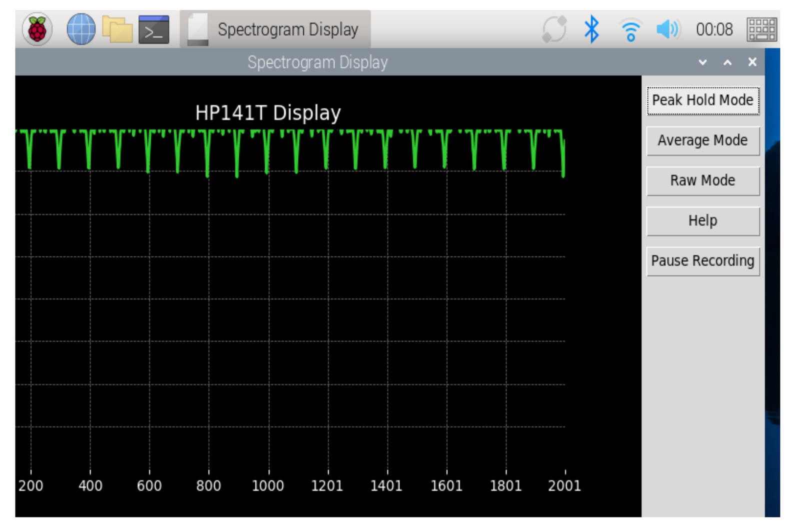

Figure 11: PHM applied to sinusoidal wave for displaying the maximum of Vy.

Conclusion

The digitized HP141T system successfully emulated the vertical output with a ~10% deviation, using the SDG1010, and implemented the signal conditioning (SCS) that scaled -0.8 V to 0 V into 0 V to 3.3 V, alongside a fully functional DPS and GUIS with 50-100 ms latency and support for PHM, AVM, and RWM modes. This project demonstrates the feasibility of digitizing the HP141T, with strong software and signal conditioning performance, but hardware emulation requires further development. The system is functional but incomplete, needing refinement to fully meet requirements. For the DAS, early procurement of the STM32H723ZG is critical, and a capacitor should be added near the ADC pins on the STM32H746ZG to improve settling time. The DPS should consider FPGA implementation for better performance.