Digital IC-Project and Verification

Power Analysis

Joachim Rodrigues
Linag Liu
Masoud Nouripayam

Outline

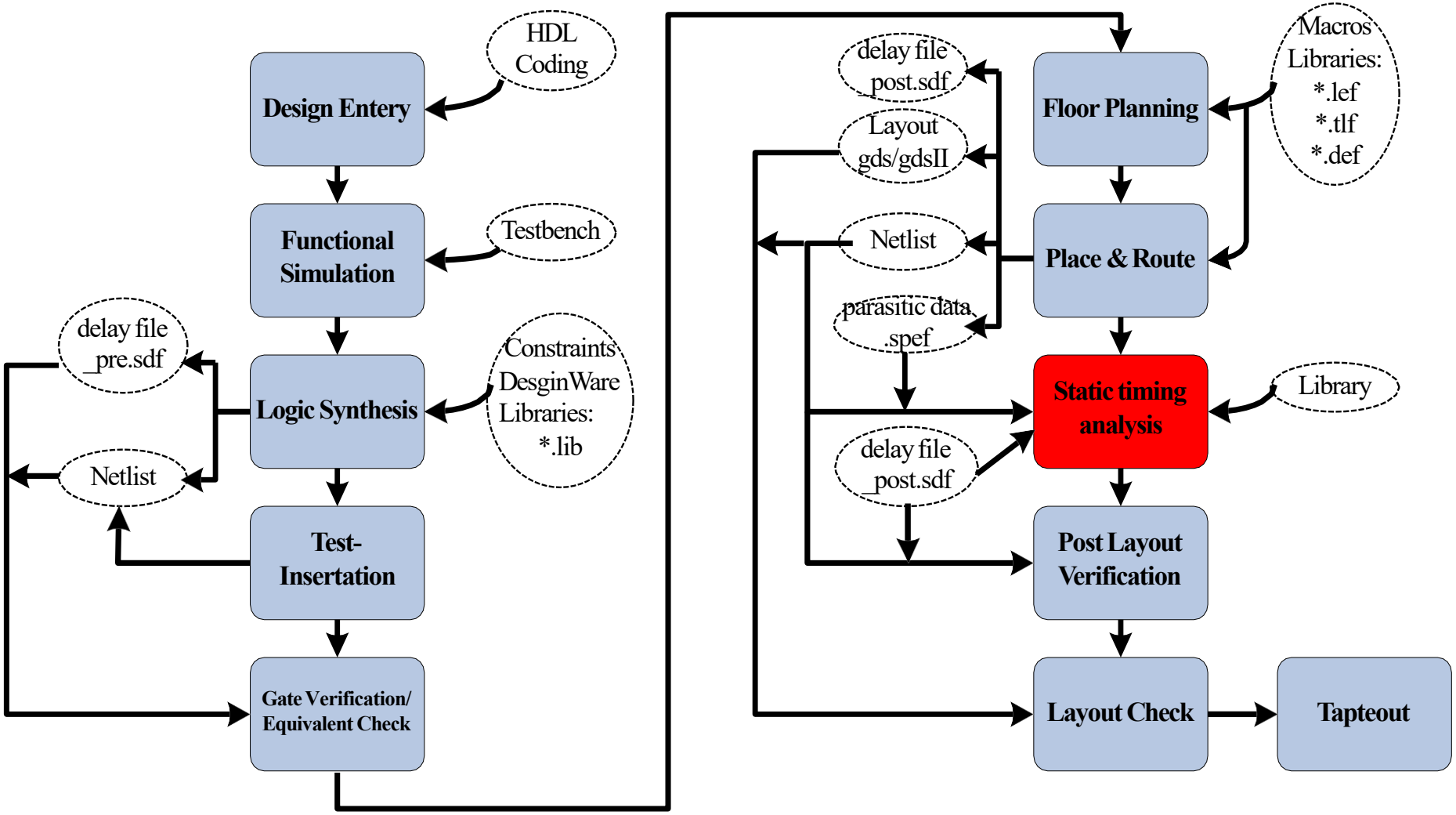
- STA & PrimeTime Overview
- STA Using PrimeTime
  - Basic Concepts
  - PrimeTime Flow
- Suggestions

Static Timing Analysis

- What's STA
  - STA is a method of validating the timing performance of a design by checking all possible paths for timing violations.

- Different with dynamical timing analysis
  - ***Full coverage***: removes the possibility that not all critical paths are identified
  - ***Higher speed***: especially for large complex designs
  - Slightly **pessimistic estimation**: e.g., wire load model

Static Timing Analysis

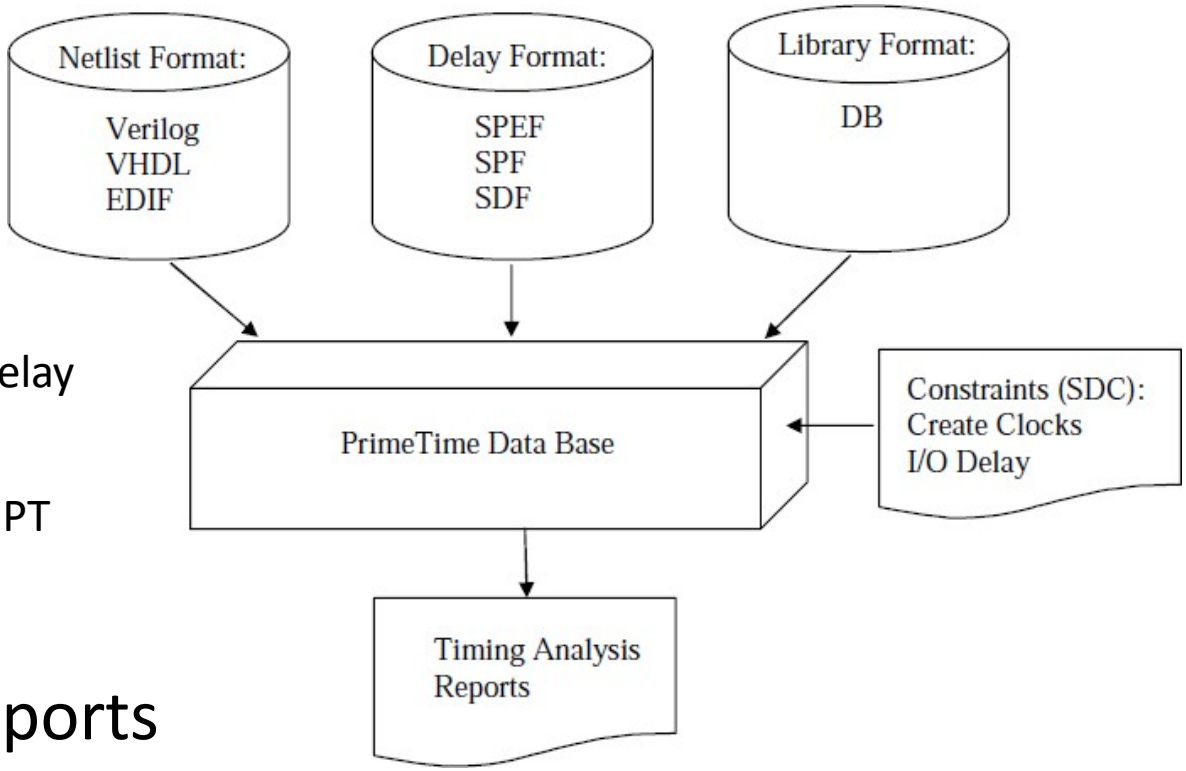


PrimeTime - Overview

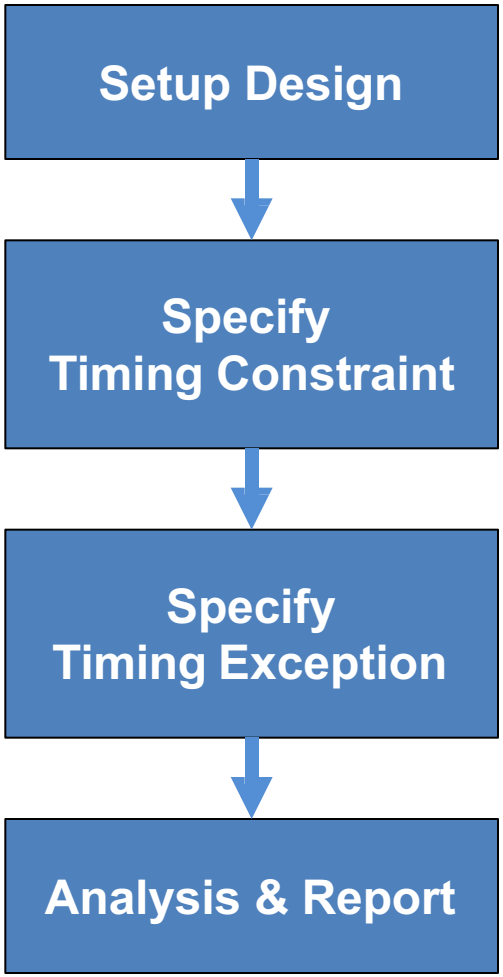
- PrimeTime is the ***Synopsys*** stand-alone full chip, gate-level static timing analyzer
- Widely-adopted in industry and academia, sign-off tools
- Controlled by Tool command language (TCL) compatible with DC

PrimeTime - Input/Output

- Inputs:
  - Netlist file
    - Verilog/VHDL/EDIF
  - Delay format:
    - SPEF/SPF/SDF
  - Database file (DB):
    - Determine the cell delay
  - SDC file:
    - Define the design to PT
- Outputs:
  - Timing Analysis Reports



PrimeTime - STA Flow



To start PrimeTime

- Change to the folder where you want to run PrimeTime, and execute

  inittde dicp21

  (more info @: www.eit.lth.se/cadsys)
- Initializes the environment and copies some setup files (if required)
- CAD tools initialization script creates several directories

  (good directory structure for project management)
  - /Desktop/project_name
  - netlists (.v, .sdf, .spef, .sdc)
  - reports (setup.rpt, hold.rpt, violate.rpt, skew.rpt)
  - scripts (.tcl, .run)
  - Readme.txt
- Execute the following command in the same terminal as inittde was executed

  primetime
- Start_gui

PrimeTime - Setup Design

- Remove extra design

```
remove_design –all
```

- Set the search path and the link path

```
set search_path “lib path”
set link_path “* design.db”
```

- Read the design and the libraries

```
read_verilog top_level.v
current_design “top_level”
```

- Link the top design

```
current_design TOP_ENTITY_NAME
link_design –force
```

PrimeTime - Timing Constraint

- Timing Violations
  - Setup violations happen when data changes less than t_{Setup} before the rising edge of the clock.
    - The ***maximum*** data path is used to check setup violations
  - Hold violations are similar to setup violations but data changes less than t_{Hold} after the rising edge of the clock.
    - The ***minimum*** data path is used to check hold violations

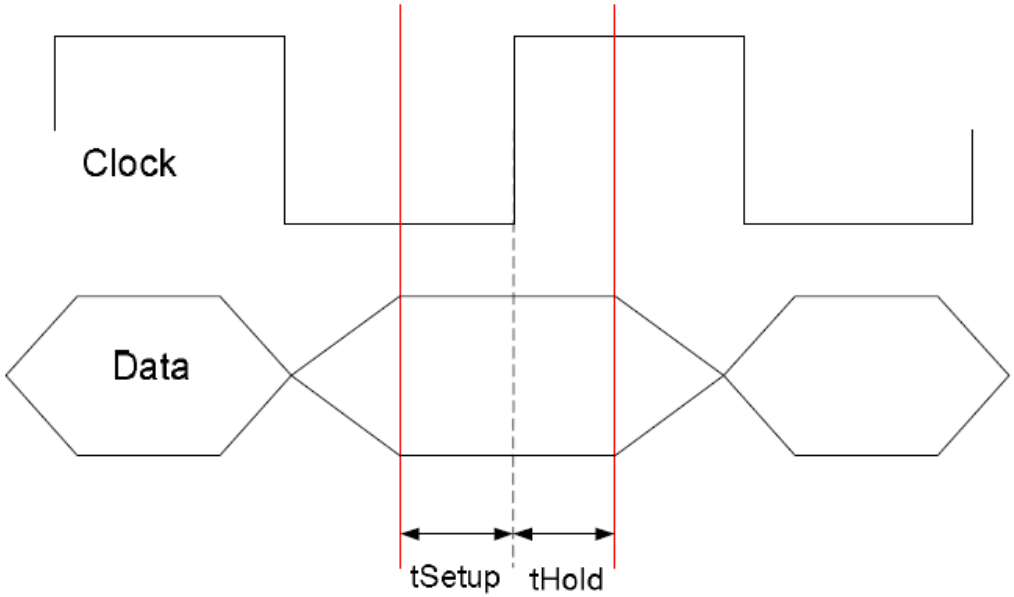
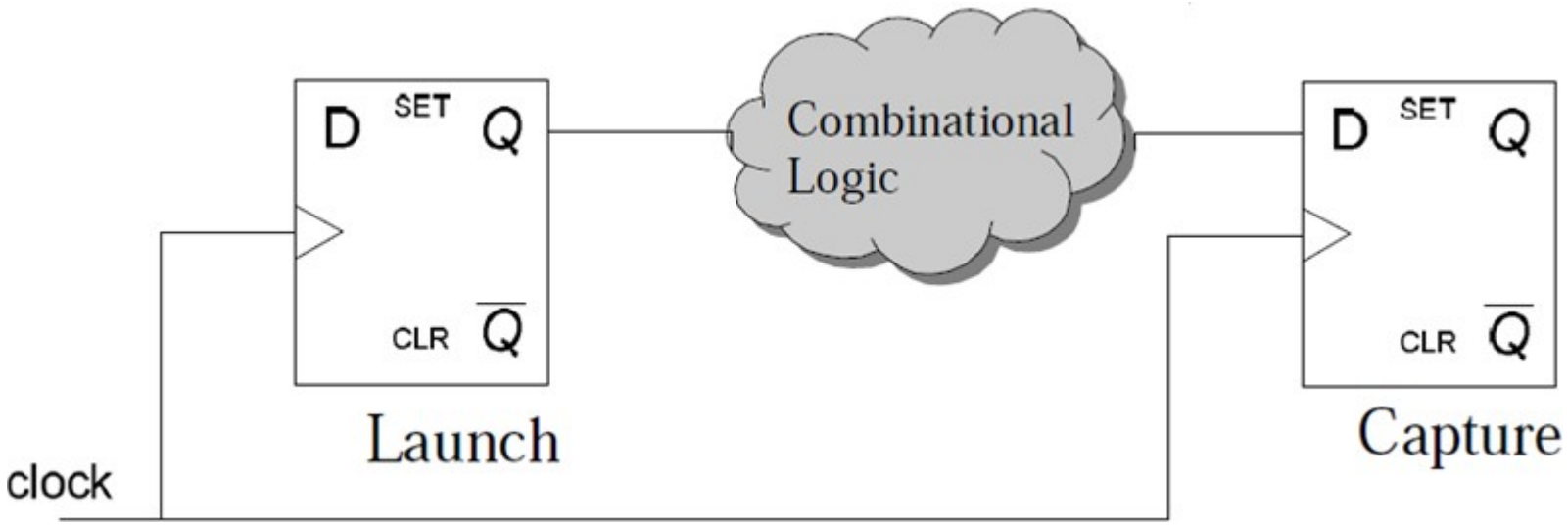


Figure from reference "PrimeTimeStatic Timing Analysis Tool", *George Michael*, 2006

PrimeTime - Timing Constraint

- Clock Period Constraint



$T_{Combinational\ logic} + FF_{lauch}(clk \rightarrow Q) < Clock\ Period - FF_{tSetup} - Clock\ Uncertainty$

$T_{Combinational\ logic} + FF_{lauch}(clk \rightarrow Q) > FF_{tHold} + Clock\ Uncertainty$

PrimeTime - Timing Constraint

To setup the timing constraints, perform one of the followings:

- Set clock constraints manually
- Read the SDC file

PrimeTime - Timing Constraint – Read SDC

Read the SDC file

```
read_sdc SDC_FILE.sdc
```

This SDC file can be:

- output of PnR step from encounter(innovus)
- output of Synthesis from Genus (or design_vision from synopsys)

PrimeTime - Timing Constraints Setup

Set clock constraints manually

```
create_clock -period 2 [get_ports clk_in]
```

define a clock with a frequency of 500 MHz or 2ns period in PrimeTime

```
set_clock_uncertainty # [get_clocks clk_in]
```

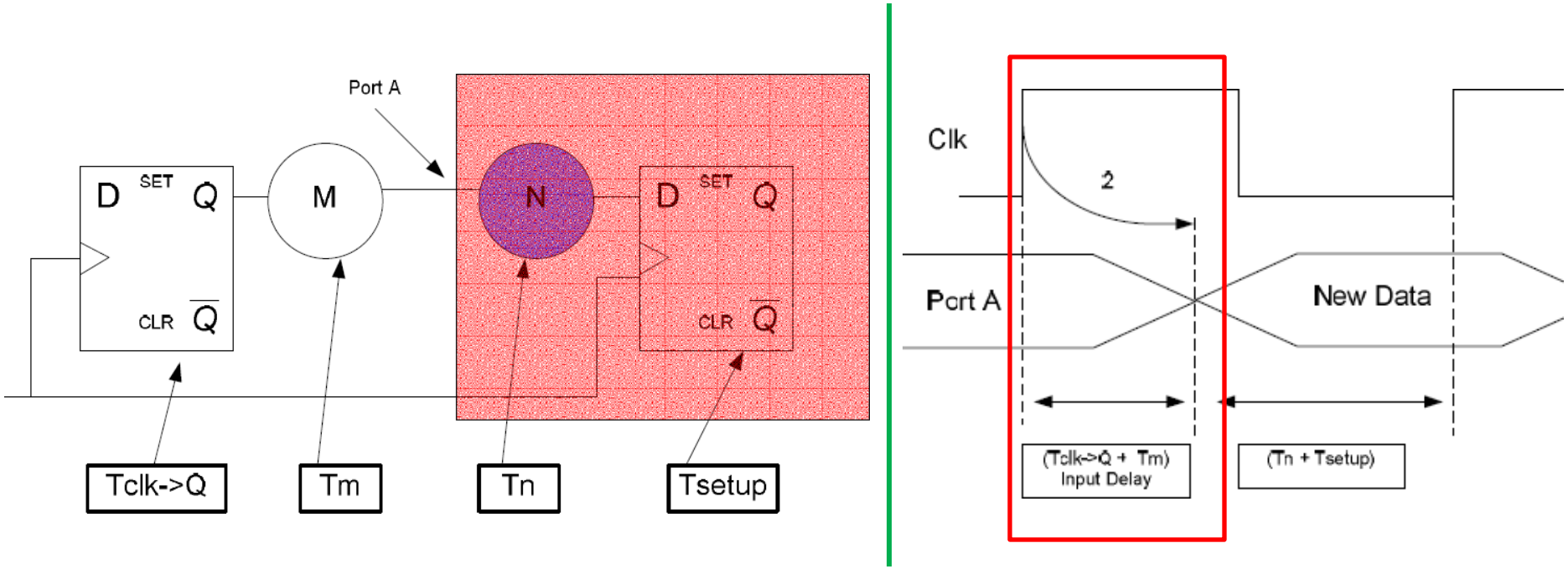
define delay between the clock branches (skew). For pre-layout

```
set_propagated_clock [all_clocks]
```

specifies that PrimeTime realized the latency for each clock path. This command should be used during post route analysis.

PrimeTime - Timing Constraints Setup

- Input Delay
  - Specify the delay of external logic driving current design



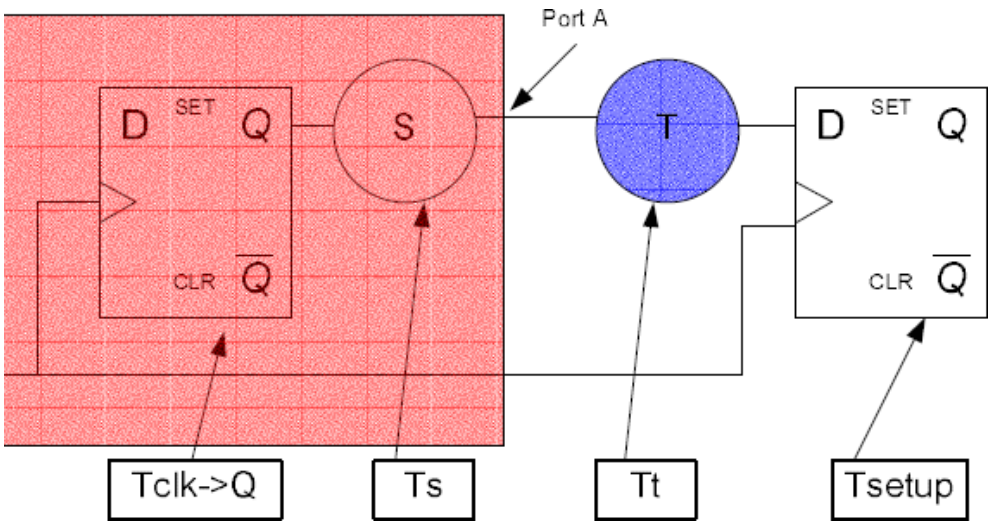
Script:

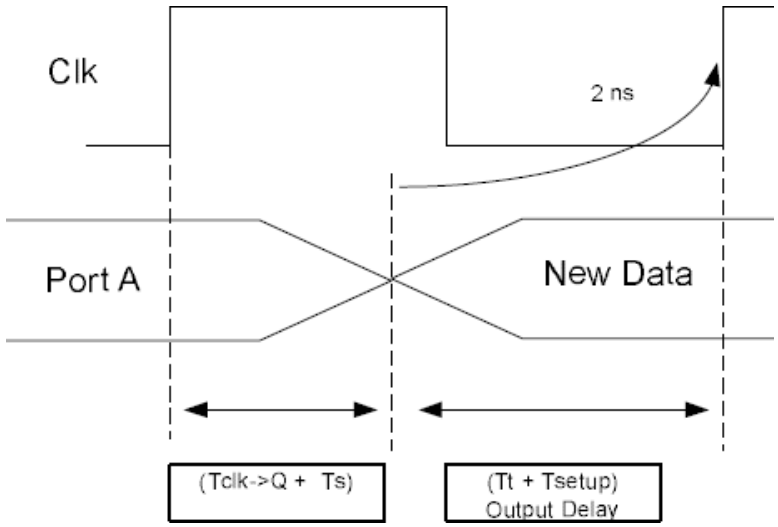
```
set_input_delay -clock clk_in -max #[get_ports i_*]
```

Figure from reference “PrimeTimeStatic Timing Analysis Tool”, *George Michael*, 2006

PrimeTime - Timing Constraints Setup

- Output Delay
  - Specify the delay of external logic driven by current design





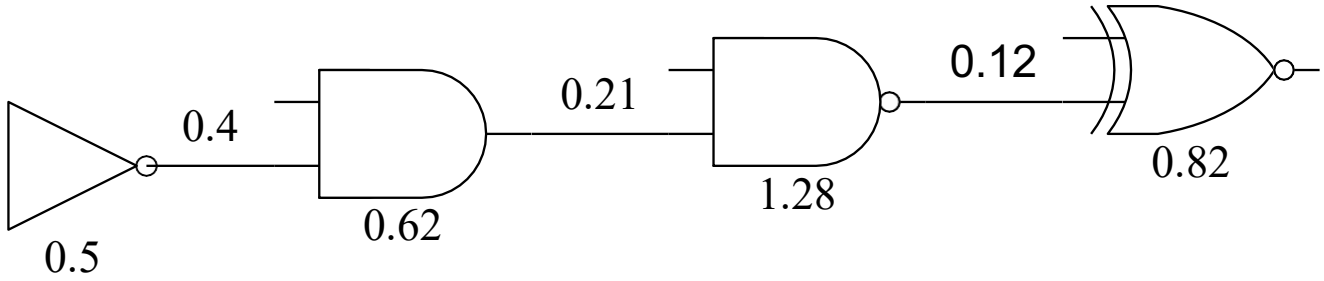
Script:

```
set_output_delay -clock clk_in -max #[get_ports O_*]
```

Figure from reference “PrimeTimeStatic Timing Analysis Tool”, *George Michael*, 2006

PrimeTime - Path Delay Calculation

- path delay = cell delay + net delay



Path Delay = 0.5+0.4+0.62+0.21+1.28+0.12+0.82=3.95 ns

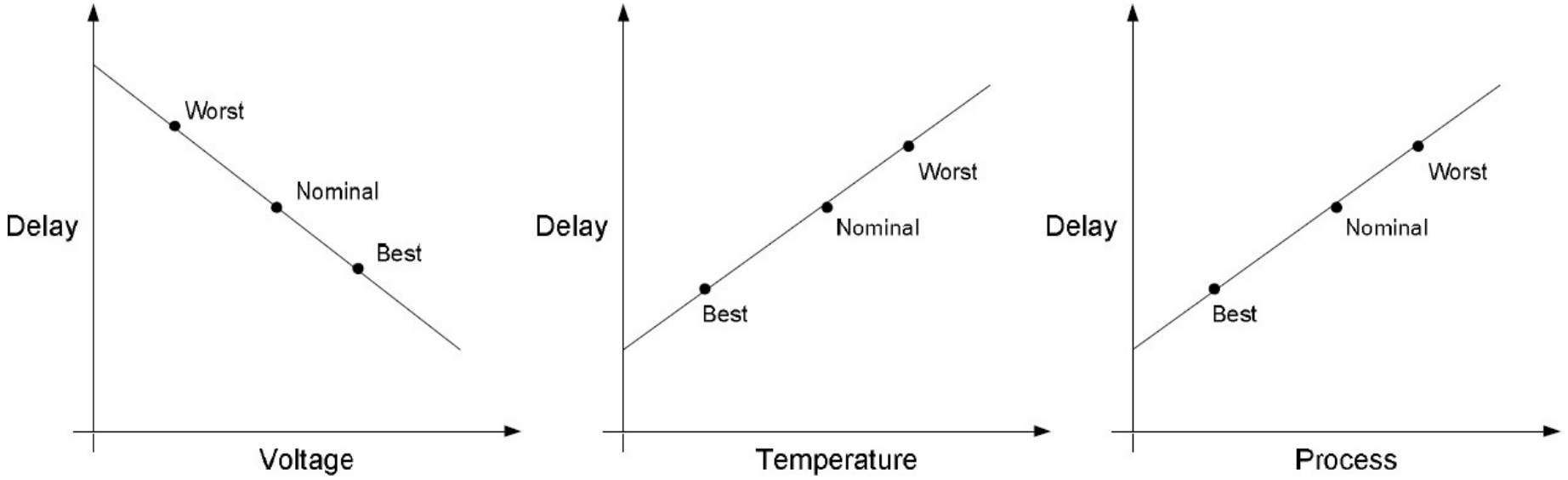
- Cell delay is stored in files called Synopsys database files or db files. Database files are read into PrimeTime by the link_path variable
- Net delay is stored in sdf file (post-layout) or calculated by PrimeTime by an internal delay calculator (pre-layout).

Script:

```
set link_library "*.db"
read_parasitics -format SPEF top_level.spef.gz
read_sdf top_level.sdf
```

PrimeTime - Working Condition

- Best Case v.s. Worst Case



  - Use the worst case delay when testing for setup violations
  - Use the best case delay when testing for hold violations

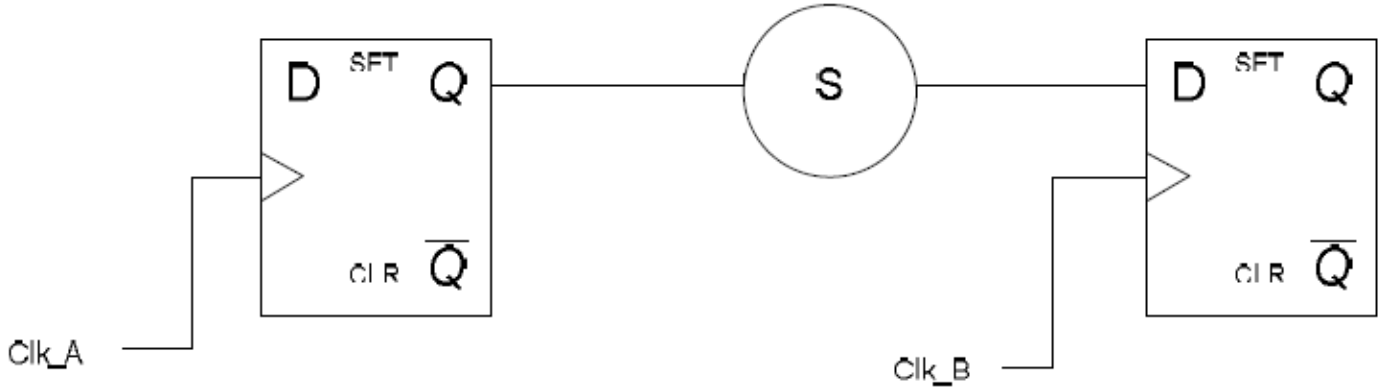
Script:

```
set_operating_conditions <worst/best-case>
```

Operating condition is defined in library

PrimeTime - Timing Exception

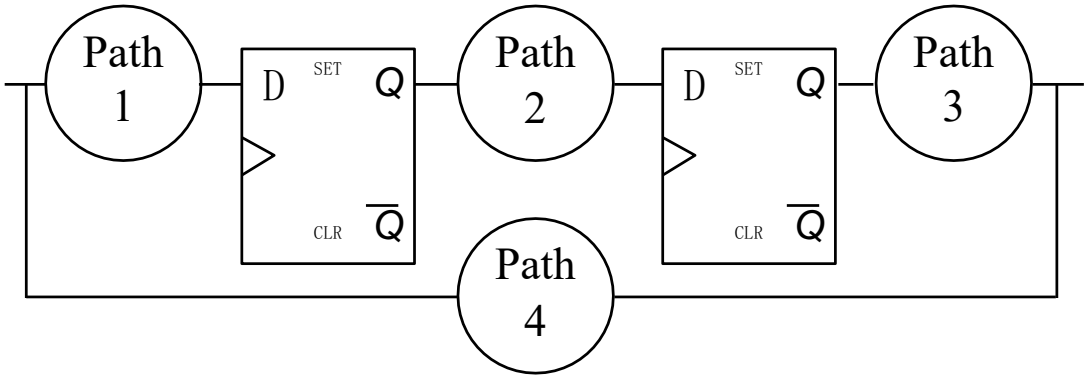
- False Path
  - paths in a design were a designer would not want the timing arcs to be calculated
    - Paths not relevant to functional operation of the circuit
    - paths which are impossible to exercise
    - Paths cross different clock domains




```
set_false_path -from clk_a -to clk_b
set_false_path -from clk_b -to clk_a
```

PrimeTime - Generating Reports

- Report Timing
  - To reduce the size and complexity of the PrimeTime reports, it is recommended to break the design into groups



P1: input to reg
P2: reg to reg
P3: reg to output
P4: input to output

```
report_timing   -from [all_registers -clock_pins]
                      [all_inputs]
                -to   [all_registers -data_pins]
                      [all_outputs]
```

PrimeTime - Generating Reports

- Report Timing (continued)

```
report_timing   -from -to
```

If this commands is not used PrimeTime will default to the longest path (critical path) in the design

```
-path full_path
```

This option reports not only the data path but the launching and capturing clock path. `Set_propagated_clocks` must be set for this option to properly report the clock paths.

```
-delay {max|min}
```

max: PrimeTime reports setup time/min: PrimeTime reports hold time

```
-max_paths
```

This variable states the total number of paths to be reported per group. The default is one.

PrimeTime - Generating Reports

- Report Violation

```
report_constraints -all_violators
```

This command generates a summary of all paths that are violation setup and hold times as well as and any cells that violation a design rule such as fanout, capacitance, and transition. Viewing this one report will tell you if changes will need to be made to your design.

PrimeTime - Generating Reports

- Report Clock Timing

```
report_clock_timing -type skew -verbose
```

This command will report clock skew, the difference between the longest and shortest clock insertion time, and allow the design to evaluate whether or not the clock tree must be re-synthesized. This is a powerful command can save the designer from numerous timing closure spins.

PrimeTime - setup Reports

Point	Incr	Path	
clock tck (rise edge)	0.00	0.00	
clock network delay (ideal)	0.00	0.00	
input external delay	15.00	15.00	r
tdi (in)	0.00	15.00	r
pads/tdi (pads)	0.00	15.00	r
pads/tdi_pad/Z (PAD1X)	1.32	16.32	r
pads/tdi_signal (pads)	0.00	16.32	r
ir_block/tdi (ir_block)	0.00	16.32	r
ir_block/U1/Z (AND2D4)	0.28	16.60	r
ir_block/U2/ZN (INV0D2)	0.33	16.93	f
ir_block/U1234/Z (OR2D0)	1.82	18.75	f
ir_block/U156/ZN(NOR3D2)	1.05	19.80	r
ir_block/ir_reg0/D (DFF1X)	0.00	19.80	r
data arrival time		19.80	

clock tck (rise edge)	30.00	30.00	
clock network delay (ideal)	2.50	32.50	
ir_block/ir_reg0/CP (DFF1X)		32.50	r
library setup time	–0.76	31.74	
data required time		31.74	
data required time		31.74	
data arrival time		–19.80	
slack (MET)		11.94	

PrimeTime - hold Reports

Point	Incr	Path	
clock tck (rise edge)	0.00	0.00	
clock network delay (propagated)	1.92	1.92	
state_block/st_reg9/CP (DFF1X)	0.00	1.92	r
state_block/st_reg9/Q (DFF1X)	0.18	2.10	r
state_block/U15/Z (BUFF4X)	0.04*	2.14	r
state_block/bp_reg2/D (DFF1X)	0.06*	2.20	r
data arrival time		2.20	
clock tck (rise edge)	0.00	0.00	
clock network delay (propagated)	1.54	1.54	
state_block/bp_reg2/CP (DFF1X)		1.54	r
library hold time	0.50	2.04	
data required time		2.04	
data required time		2.04	
data arrival time		–2.20	
slack (MET)		0.16	

Some suggestions

- Notes/comments are even more important

```
//_____________________________________
// Design      : CARRIER SENSE
// File Name   : CARRIER_SENSE.v
// Purpose     : Model of CARRIER SENSE process in PCS (IEEE Std 802.3)
// Limitation  : none
// Errors      : none known
// Include Files: none
// Author      : Liang Liu, liang.liu@eit.lth.se, Lund University
// Simulator   : ModelSim 6.5
//_____________________________________
// Revision List:
//+_______+_____________+___________+_____________________+
//| Version  | Author          | Date         | Changes              |
//+_______+_____________+___________+_____________________+
//|1.0       |      Liang Liu    | 2001/08/03  | original created           |
//| 1.0      |      Liang Liu    | 2002/01/04  |disable TX_EN to CRS      |
//|          |                   |             |in repeater mode          |
//+_______+_____________+___________+_____________________+
```

Some suggestions

- Name the files/signals

File name:

module file starts with “m_”, test bench starts with “tb_”

e.g., netlist name “syn_” for DC out, “pr_” for Encounter out

Signals:

inputs starts with “i_”

outputs starts with “o_”

clocks starts with “clk_”

resets starts with “rst_”

register out put ends with “_r”

low-valid signal ends with “_n”, e.g., rst_n

Some suggestions

- Pre-/Post layout design

Getting experienced by comparing pre- and post- layout design

Set reasonable timing margin to avoid **LARGE** loop in design flow, e.g.,

- clock_uncertainty : justify the value with post-layout report

-clock_period: post-layout period= pre-layout period+margin, depending on process technology

Meet timing requirement as early as possible

-keep in mind the delay information when design the circuits, e.g., pipeline schedule, parallel, et. al.

- set reasonable constraint for synthesis

- optimize the design at early stage of P&R