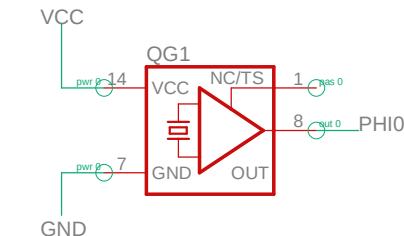
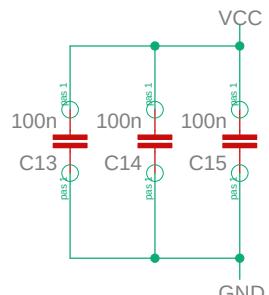
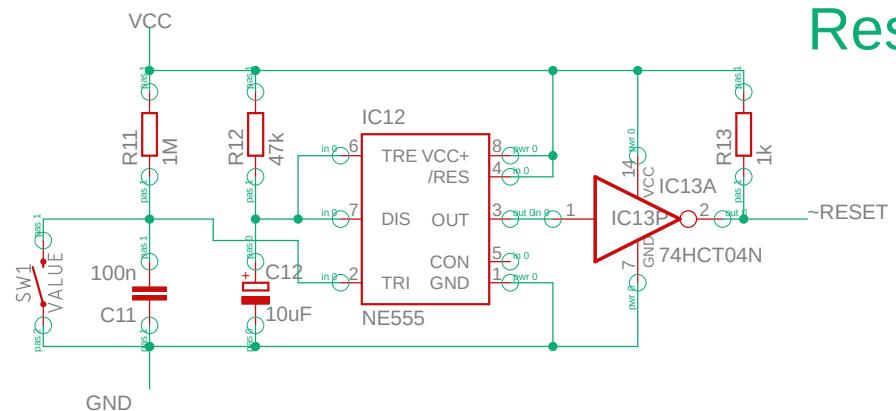
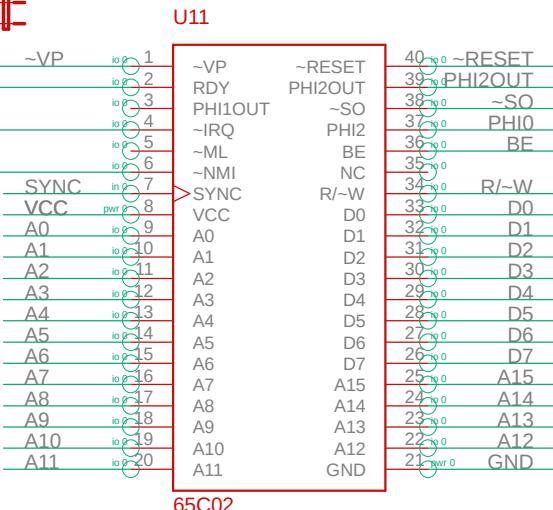
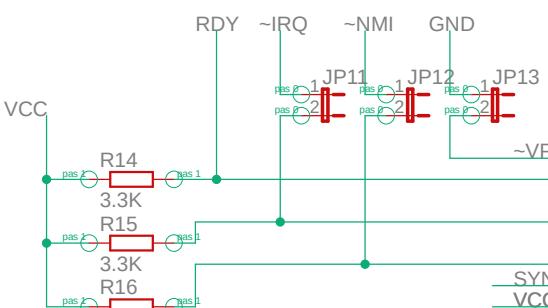
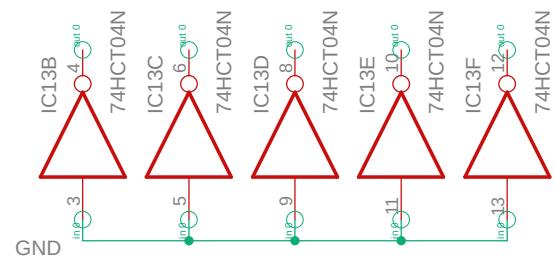


# CPU & RESET

## Reset



# Clock



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1

2

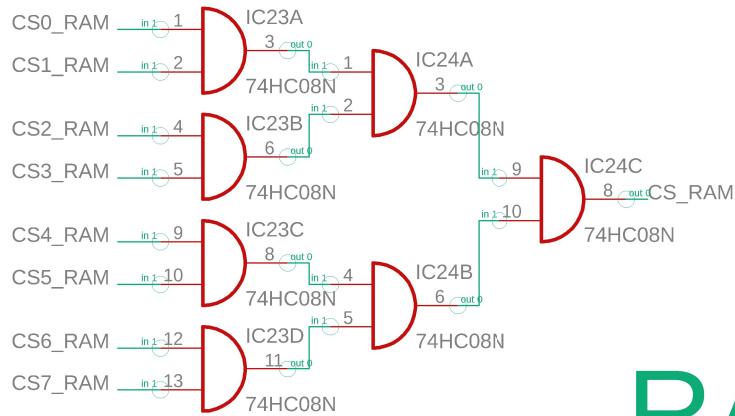
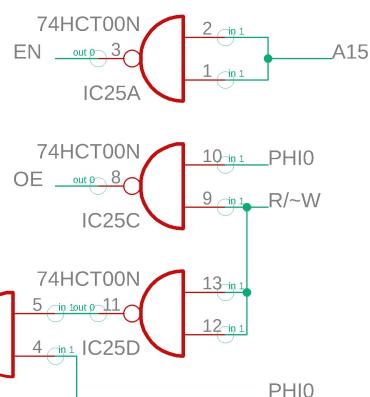
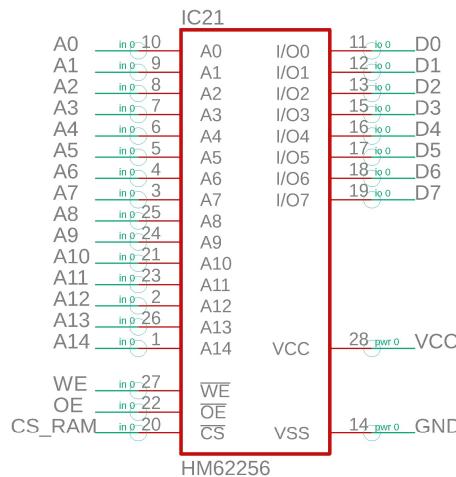
3

4

5

6

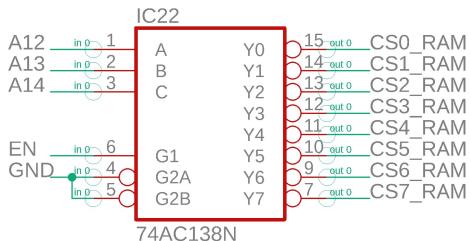
A



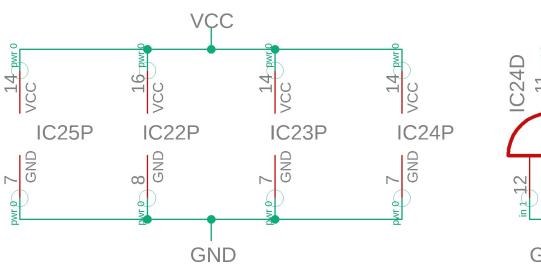
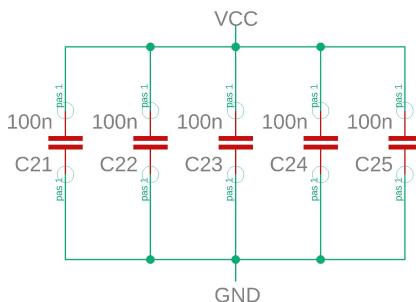
# RAM

AVAILABLE  
ADDRESS:  
0000 - 0FFF

B



C



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1

2

3

4

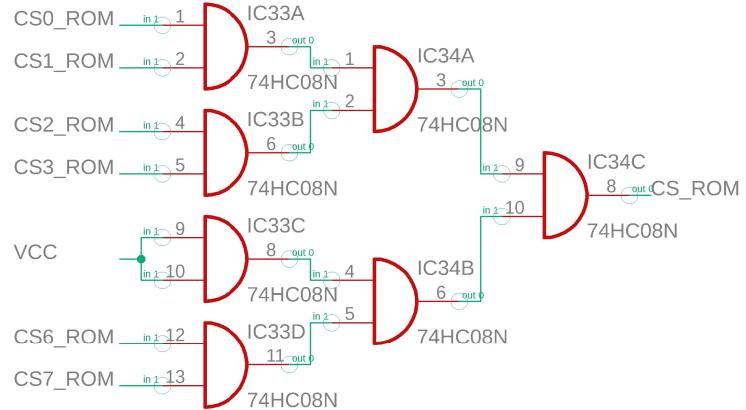
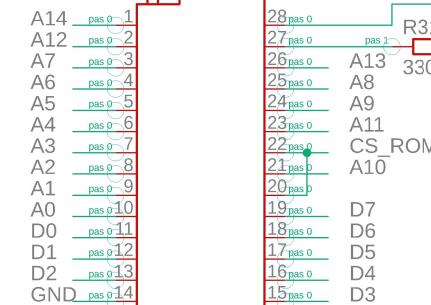
5

6

D

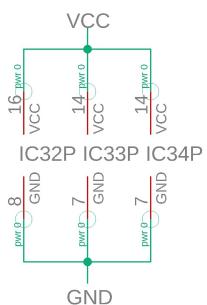
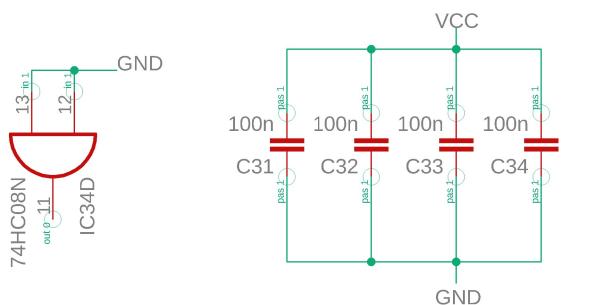
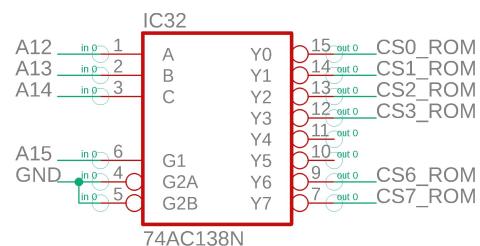
D

1 2 3 4 5 6



AVAILABLE ADDRESS:  
1000 - BFFF  
E000 - FFFF

# ROM



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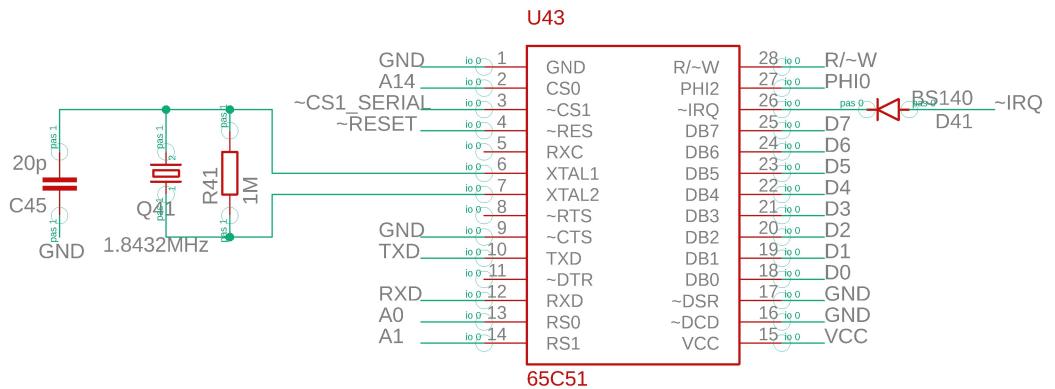
1 2 3 4 5 6

# SERIAL

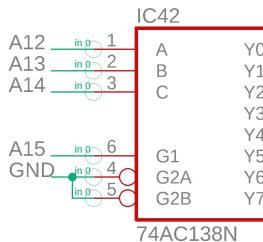
## CXXX

ENABLE FOR  
CXXX  
1100 XXXX XXXX

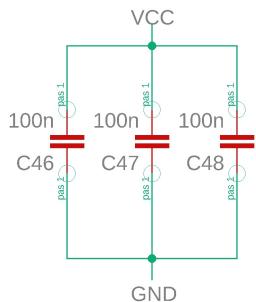
A



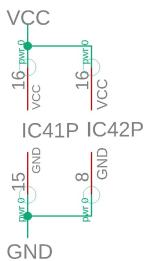
B



C



D



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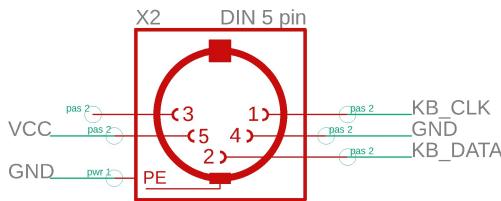
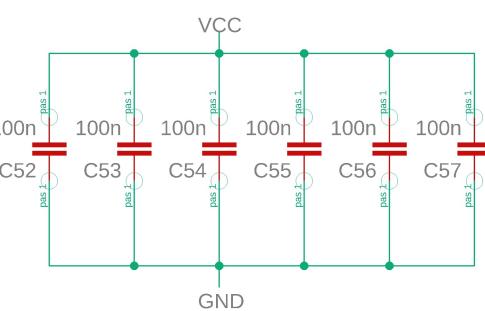
1 2 3 4 5 6

1 2 3 4 5 6

# KEYBOARD

## D18X

ENABLE FOR  
D18X  
1101 0001 1000 XXXX



ENABLE FOR  
D18X  
1101 0001 1000

GND	io 0_1	GND	CA1	40 io 0 KB_INT
PA05	io 0_2	PA0	CA2	39 io 0
PA15	io 0_3	PA1	RS0	38 io 0 A0
PA25	io 0_4	PA2	RS1	37 io 0 A1
PA35	io 0_5	PA3	RS2	36 io 0 A2
PA45	io 0_6	PA4	RS3	35 io 0 A3
PA55	io 0_7	PA5		34 io 0 ~RESET
PA65	io 0_8	PA6	D0	33 io 0 D0
PA75	io 0_9	PA7	D1	32 io 0 D1
	io 1_10	PB0	D2	31 io 0 D2
	io 1_11	PB1	D3	30 io u D3
	io 0_12	PB2	D4	29 io 0 D4
	io 0_13	PB3	D5	28 io 0 D5
	io 0_14	PB4	D6	27 io 0 D6
	io 0_15	PB5	D7	26 io 0 D7
	io 0_16	PB6	PHI2	25 io 0 PHI0
	io 0_17	PB7	CS1	24 io 0 A12
	io 0_18	CB1	~CS2	23 io 0 ~CS2_KEYB
VCC	io 0_19	CB2	R/W	22 io 0 R/W
	io 0_20		~IRQ	21 io 0 pas 0 SB140

Pinout diagram for IC55 (74AC138N) showing connections from pins A11, A10, A9, A8, YH5, and YL5 to inputs A, B, C, G1, G2A, and G2B. The outputs Y0 through Y7 are shown on the right, with Y0 being the active-low output.

 Boogs B06502

VCC

16 pins  
VCC

14 pins  
VCC

IC55P IC55P IC54P IC53P IC52P IC57P

GND

8  
GND

8  
GND

8  
GND

8  
GND

8  
GND

7  
GND

avr 0

avr 0

avr 0

avr 0

avr 0

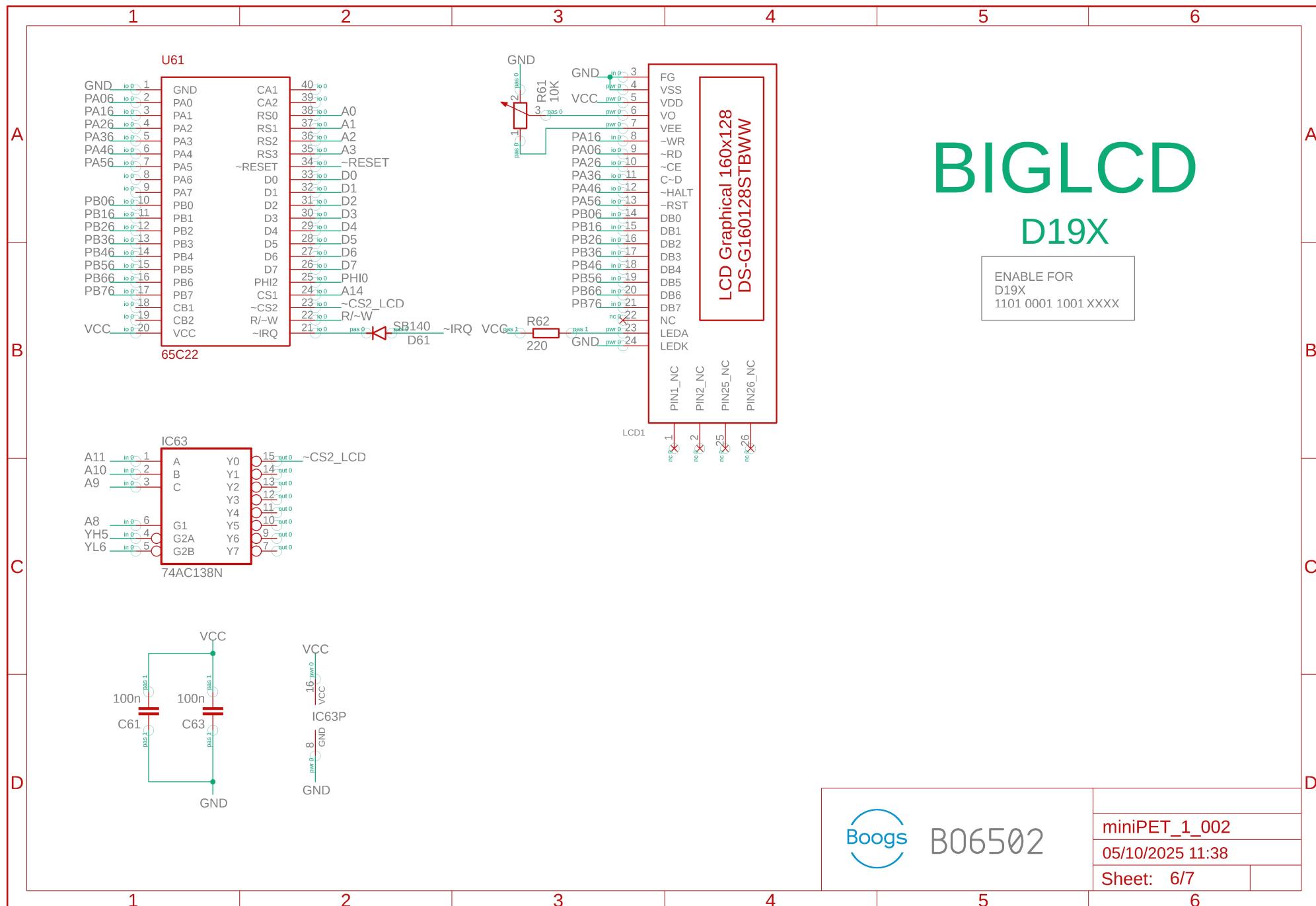
avr 0

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# BIGLCD

## D19X

ENABLE FOR  
D19X  
1101 0001 1001 XXXX



1 2 3 4 5 6

A

B

C

D

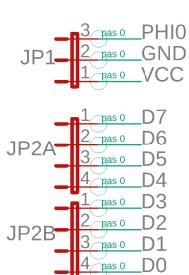
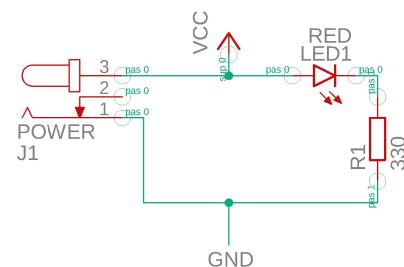
A

B

C

D

# POWER



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1 2 3 4 5 6