

1.0 到 9999bcd 計數器:

The image displays two screenshots of the Quartus II 64-bit software interface, showing the compilation process of a 1.0 to 9999bcd counter.

Top Screenshot: c09.vhd

The top window shows the VHDL code for the counter. The code defines a 4-bit counter (c) and a 4-bit divider (d). The counter is implemented using a process (rst, flag) that resets the counter to 0 when rst is 0. The divider is implemented using a process (rst, flag) that resets the divider to 0 when rst is 0. The counter is then incremented by the divider output (d) when the divider output is 1.

```
30 signal c: std_logic_vector(3 downto 0);
31 signal d: std_logic_vector(3 downto 0);
32 begin
33
34   clk_div port map (clk, rst, flag);
35
36   process (rst, flag)
37   variable m0: std_logic_vector(3 downto 0) := "0000";
38   variable m1: std_logic_vector(3 downto 0) := "0000";
39   variable m2: std_logic_vector(3 downto 0) := "0000";
40   variable m3: std_logic_vector(3 downto 0) := "0000";
41
42   begin
43
44   if rst='0' then
45     m0:="0000";
46     m1:="0000";
47     m2:="0000";
48     m3:="0000";
49   elsif flag'event and flag='1' then
50     a<=m0;
51     b<=m1;
52     c<=m2;
53     d<=m3;
54   if m0 /= "1001" then
55     m0:= m0 + 1;
56   elsif m0="1001" and m1 /= "1001" then
57     m0:="0000";
58     m1:= m1 + 1;
59   elsif m1="1001" and m2 /= "1001" and m0="1001" then
60     m1:="0000";
61     m0:="0000";
62     m2:= m2 + 1;
63   elsif m2="1001" and m3/= "1001" and m0="1001" and m1="1001" then
64     m1:="0000";
65     m0:="0000";
66     m2 := "0000";
67     m3 := m3 + 1;
68   elsif m3="1001" then
69     m0:="0000";
70     m1:="0000";
71     m2:="0000";
72     m3:="0000";
73   end if;
74   end if;
75   end process;
76
77   z0: segd port map (a,op0);
78   z1: segd port map (b,op1);
79   z2: segd port map (c,op2);
80   z3: segd port map (d,op3);
81
82   end count;
83
```

Bottom Screenshot: Quartus II 64-bit - C:/altera/clk component/clk_div - clk_div

The bottom window shows the compilation progress and messages. The compilation is complete, and the messages indicate that the design is not fully constrained for some timing analysis.

Compilation Progress:

Task	Time
Compile Design	00:00:12
Analysis & Synthesis	00:00:02
Fitter (Place & Route)	00:00:06
Assembler (Generate programming files)	00:00:02
TimeQuest Timing Analysis	00:00:02
EDA Netlist Writer	
Program Device (Open Programmer)	

Messages:

- 332140 No Recovery paths to report
- 332140 No Removal paths to report
- 332146 Worst-case minimum pulse width slack
- 332102 Design is not fully constrained for
- 332102 Design is not fully constrained for
- Quartus II 64-Bit TimeQuest Timing
- 293000 Quartus II Full Compilation was suc

