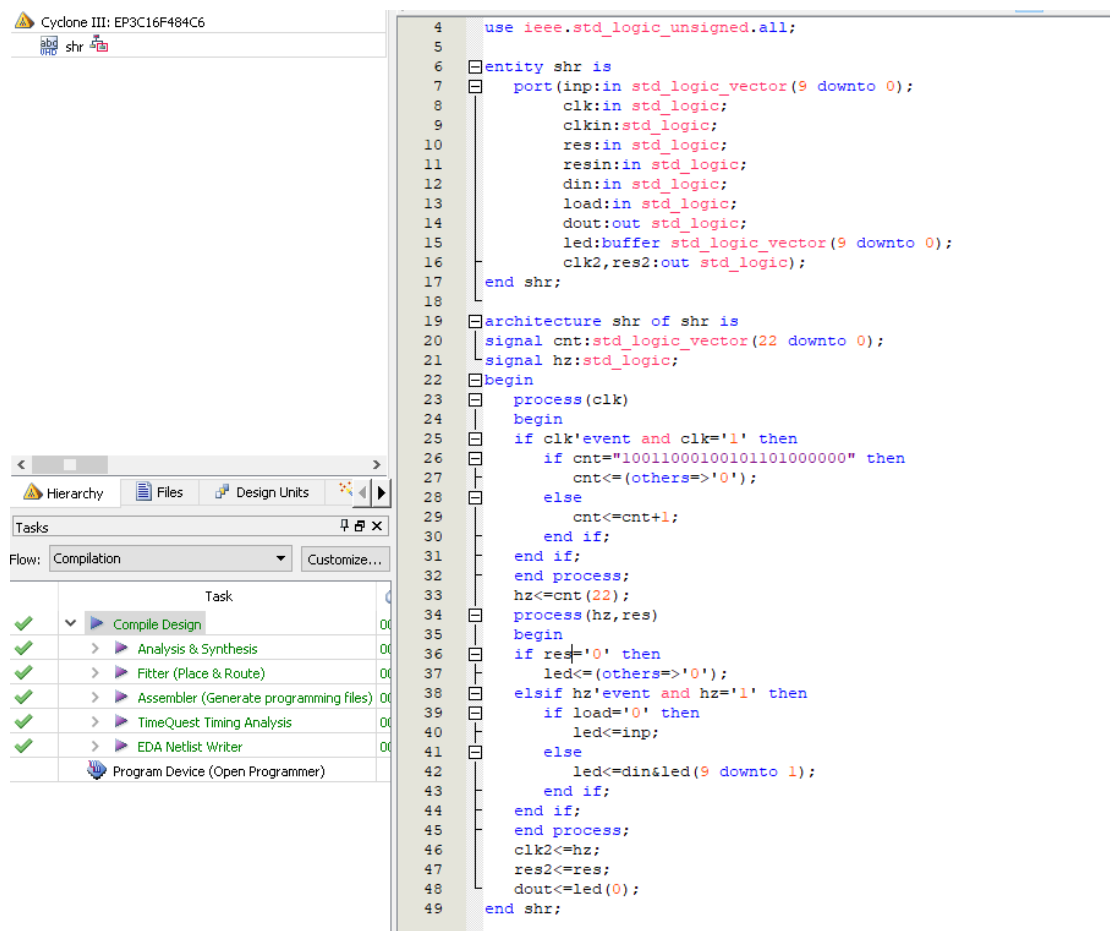


## 1. led shift register(main):



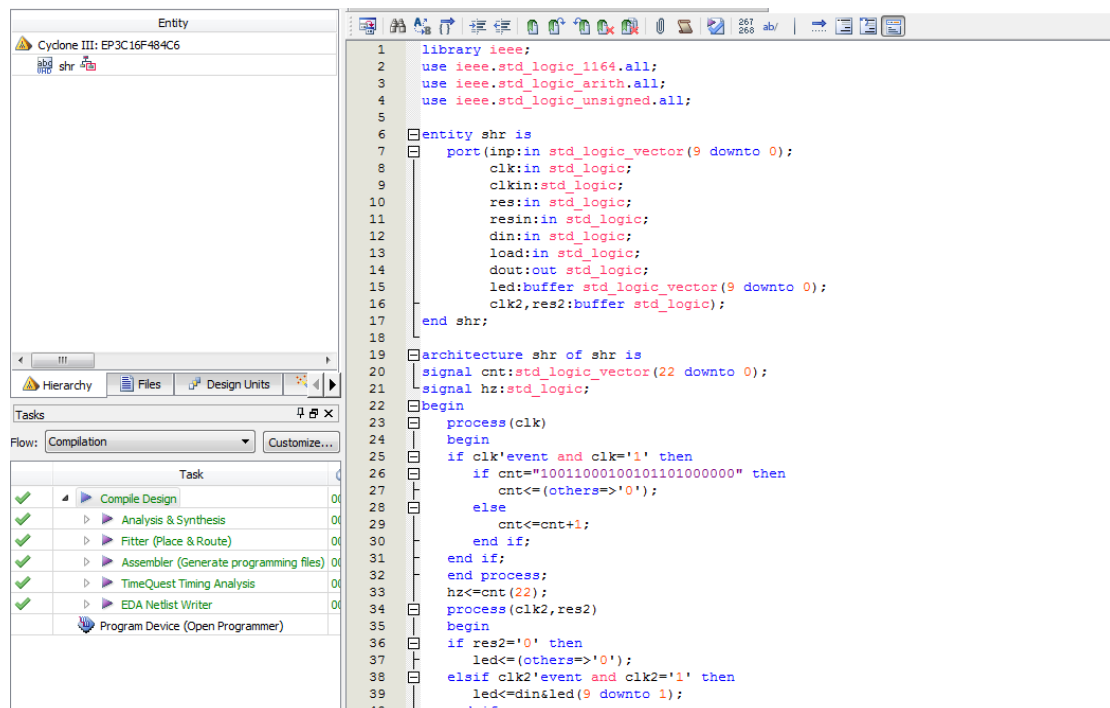
The screenshot shows the Quartus II IDE with the main VHDL code for the 'shr' entity. The left pane displays the project hierarchy and a task list. The main editor shows the following code:

```

4  use ieee.std_logic_unsigned.all;
5
6  entity shr is
7  port (inp:in std_logic_vector(9 downto 0);
8        clk:in std_logic;
9        clk2:in std_logic;
10       res:in std_logic;
11       resin:in std_logic;
12       din:in std_logic;
13       load:in std_logic;
14       dout:out std_logic;
15       led:buffer std_logic_vector(9 downto 0);
16       clk2,res2:out std_logic);
17 end shr;
18
19 architecture shr of shr is
20 signal cnt:std_logic_vector(22 downto 0);
21 signal hz:std_logic;
22 begin
23 process(clk)
24 begin
25 if clk'event and clk='1' then
26 if cnt="10011000100101101000000" then
27 cnt<=(others=>'0');
28 else
29 cnt<=cnt+1;
30 end if;
31 end if;
32 end process;
33 hz<=cnt(22);
34 process(hz,res)
35 begin
36 if res='0' then
37 led<=(others=>'0');
38 elsif hz'event and hz='1' then
39 if load='0' then
40 led<=inp;
41 else
42 led<=din&led(9 downto 1);
43 end if;
44 end if;
45 end process;
46 clk2<=hz;
47 res2<=res;
48 dout<=led(0);
49 end shr;

```

## 2. (vice):



The screenshot shows the Quartus II IDE with the 'vice' VHDL code for the 'shr' entity. The left pane displays the project hierarchy and a task list. The main editor shows the following code:

```

1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_arith.all;
4  use ieee.std_logic_unsigned.all;
5
6  entity shr is
7  port (inp:in std_logic_vector(9 downto 0);
8        clk:in std_logic;
9        clk2:in std_logic;
10       res:in std_logic;
11       resin:in std_logic;
12       din:in std_logic;
13       load:in std_logic;
14       dout:out std_logic;
15       led:buffer std_logic_vector(9 downto 0);
16       clk2,res2:buffer std_logic);
17 end shr;
18
19 architecture shr of shr is
20 signal cnt:std_logic_vector(22 downto 0);
21 signal hz:std_logic;
22 begin
23 process(clk)
24 begin
25 if clk'event and clk='1' then
26 if cnt="10011000100101101000000" then
27 cnt<=(others=>'0');
28 else
29 cnt<=cnt+1;
30 end if;
31 end if;
32 end process;
33 hz<=cnt(22);
34 process(clk2,res2)
35 begin
36 if res2='0' then
37 led<=(others=>'0');
38 elsif clk2'event and clk2='1' then
39 led<=din&led(9 downto 1);
40 end if;

```

```
41     end process;  
42     clk2<=hz;  
43     res2<=res;  
44     dout<=led(0);  
45 end shr;
```