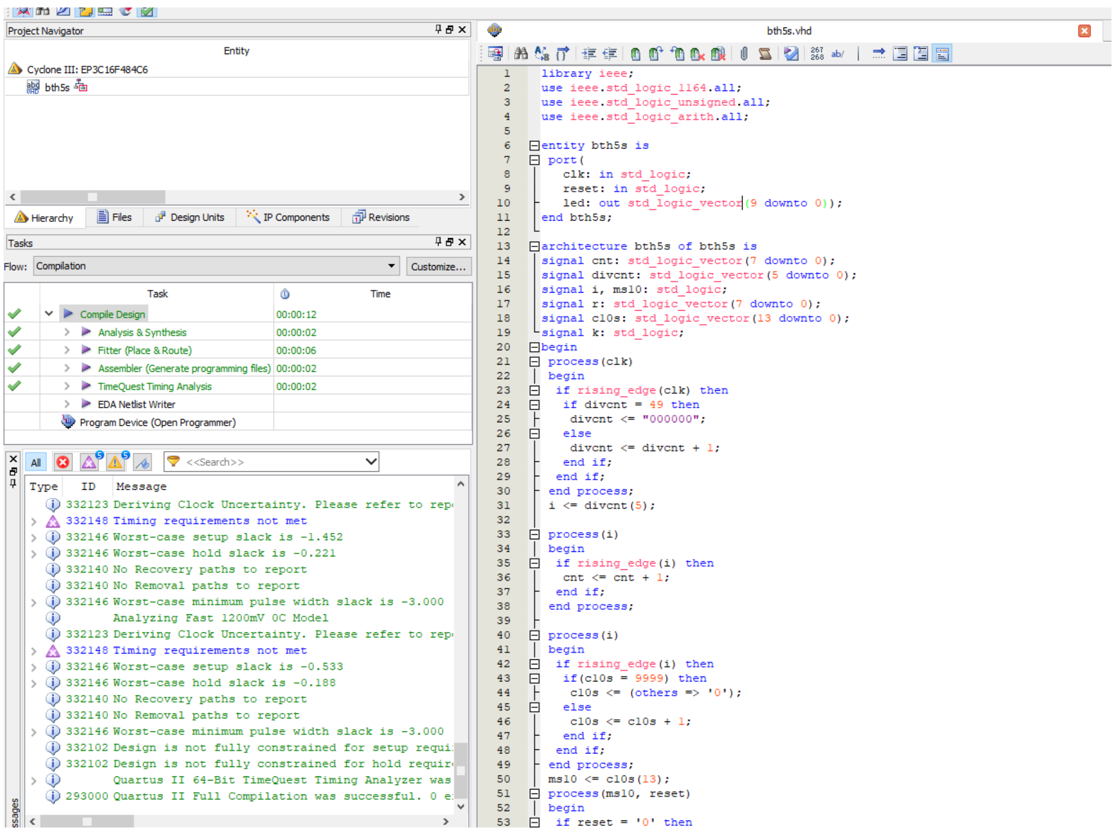
1.5 second breathing light:


Project Navigator

Entity

Cyclone III: EP3C16F484C6

bth5s

Tasks

Flow: Compilation

	Task	Time
✓	Compile Design	00:00:12
✓	Analysis & Synthesis	00:00:02
✓	Fitter (Place & Route)	00:00:06
✓	Assembler (Generate programming files)	00:00:02
✓	TimeQuest Timing Analysis	00:00:02
	EDA Netlist Writer	
	Program Device (Open Programmer)	

```
Type  ID     Message
      332123 Deriving Clock Uncertainty. Please refer to rep
      332148 Timing requirements not met
      332146 Worst-case setup slack is -1.452
      332146 Worst-case hold slack is -0.221
      332140 No Recovery paths to report
      332140 No Removal paths to report
      332146 Worst-case minimum pulse width slack is -3.000
                    Analyzing Fast 1200mV 0C Model
      332123 Deriving Clock Uncertainty. Please refer to rep
      332148 Timing requirements not met
      332146 Worst-case setup slack is -0.533
      332146 Worst-case hold slack is -0.188
      332140 No Recovery paths to report
      332140 No Removal paths to report
      332146 Worst-case minimum pulse width slack is -3.000
      332102 Design is not fully constrained for setup requi
      332102 Design is not fully constrained for hold requir
                    Quartus II 64-Bit TimeQuest Timing Analyzer was
      293000 Quartus II Full Compilation was successful. 0 e
```

bth5s.vhd

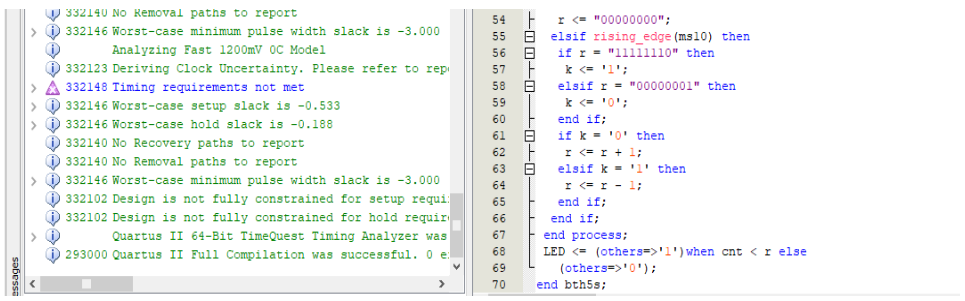
```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity bth5s is
 port(
   clk: in std_logic;
   reset: in std_logic;
   led: out std_logic_vector(9 downto 0));
end bth5s;

architecture bth5s of bth5s is
signal cnt: std_logic_vector(7 downto 0);
signal divcnt: std_logic_vector(5 downto 0);
signal i, ms10: std_logic;
signal r: std_logic_vector(7 downto 0);
signal c10s: std_logic_vector(13 downto 0);
signal k: std_logic;
begin
 process(clk)
 begin
  if rising_edge(clk) then
   if divcnt = 49 then
    divcnt <= "000000";
   else
    divcnt <= divcnt + 1;
   end if;
  end if;
 end process;
 i <= divcnt(5);

 process(i)
 begin
  if rising_edge(i) then
   cnt <= cnt + 1;
  end if;
 end process;

 process(i)
 begin
  if rising_edge(i) then
   if(c10s = 9999) then
    c10s <= (others => '0');
   else
    c10s <= c10s + 1;
   end if;
  end if;
 end process;
 ms10 <= c10s(13);
 process(ms10, reset)
 begin
  if reset = '0' then
```


```
      332140 No Removal paths to report
      332146 Worst-case minimum pulse width slack is -3.000
                    Analyzing Fast 1200mV 0C Model
      332123 Deriving Clock Uncertainty. Please refer to rep
      332148 Timing requirements not met
      332146 Worst-case setup slack is -0.533
      332146 Worst-case hold slack is -0.188
      332140 No Recovery paths to report
      332140 No Removal paths to report
      332146 Worst-case minimum pulse width slack is -3.000
      332102 Design is not fully constrained for setup requi
      332102 Design is not fully constrained for hold requir
                    Quartus II 64-Bit TimeQuest Timing Analyzer was
      293000 Quartus II Full Compilation was successful. 0 e
```

```vhdl
   r <= "00000000";
  elsif rising_edge(ms10) then
   if r = "11111110" then
    k <= '1';
   elsif r = "00000001" then
    k <= '0';
   end if;
   if k = '0' then
    r <= r + 1;
   elsif k = '1' then
    r <= r - 1;
   end if;
  end if;
 end process;
 LED <= (others=>'1')when cnt < r else
   (others=>'0');
end bth5s;
```