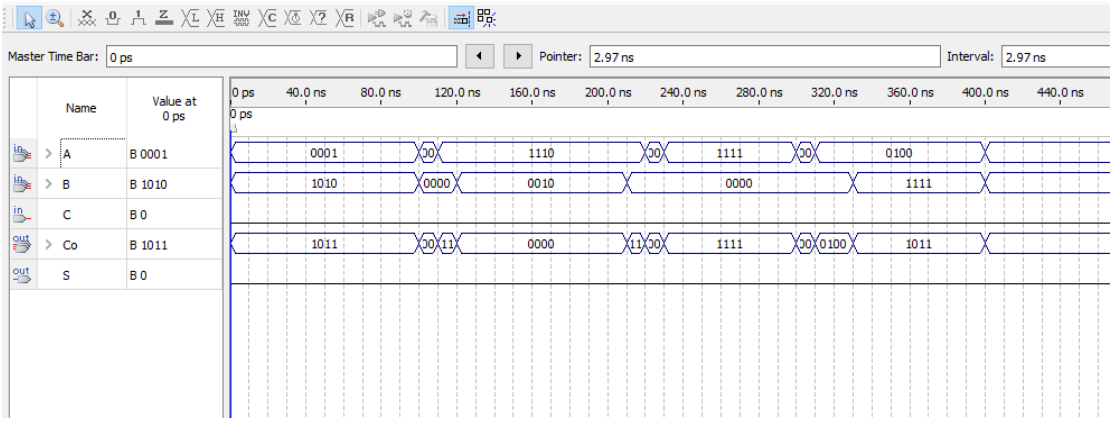
2-1 用 process 做 4bit 加法器

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6  entity proc is
7      Port(A:in STD_LOGIC_VECTOR(3 downto 0);
8           B:in STD_LOGIC_VECTOR(3 downto 0);
9           C:in std_LOGIC;
10          Co:out STD_LOGIC_VECTOR(3 downto 0);
11          S:out STD_LOGIC
12          );
13 end proc;
14
15 architecture proc of proc is
16 signal temp:std_LOGIC_VECTOR(4 downto 0);
17 begin
18    fir:process(A(0),B(0))
19          begin
20          Co(0)<=A(0) XOR B(0);
21          temp(0)<=A(0) AND B(0);
22          end process fir;
23    sec:process(A(0),B(0))
24          begin
25          Co(1)<=A(1) XOR (B(1) OR temp(0));
26          temp(1)<=A(1) AND (B(1) XOR temp(0));
27          end process sec;
28    thi:process(A(0),B(0))
29          begin
30          Co(2)<=A(2) XOR (B(2) OR temp(1));
31          temp(2)<=A(2) AND (B(2) XOR temp(1));
32          end process thi;
33    frt:process(A(0),B(0))
34          begin
35          Co(3)<=A(1) XOR (B(3) OR temp(2));
36          temp(3)<=A(3) AND (B(3) XOR temp(2));
37          end process frt;
38 end proc;
```



2-2.8bit 上下數器:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity dcou is
    Port(
    clk: in std_logic;
    reset: in std_logic;
    m:in std_logic;
    Q: out std_LOGIC_VECTOR(7 downto 0));
end dcou ;

architecture dcuo of dcou is
signal temp:std_LOGIC_VECTOR(7 downto 0);
begin
   process (clk,reset,m):
   begin
      if reset ='0' then
         reg<=(others =>'0');
      elseif clk'event and clk ='1' then
         if m='0' then
            if reg=x'160' then
               reg<=x'20';
            else
            reg<=reg+1;
            end if;
         else
            if reg=x'20' then
               reg<=x'160';
            else
            reg<=reg-1;
            end if;
         end if;
      Q<=reg;
   end process;
end dcou;
```

2-3.三位數 bcd 計數器

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity dcou is
    Port(
    clk: in std_logic;
    reset: in std_logic;
    Q: out std_LOGIC_VECTOR(10 downto 0));
end dcou ;

architecture dcuo of dcou is
signal temp:std_LOGIC_VECTOR(10 downto 0);
begin
   process (clk,reset,m):
   begin
      if reset ='0' then
         temp<=(others =>'0');
      elseif clk'event and clk ='1' then
            if temp='111110011' then
               temp<='001100100';
            else
            temp<=temp+1;
            end if;
      Q<=temp;
   end process;
end dcou;
```