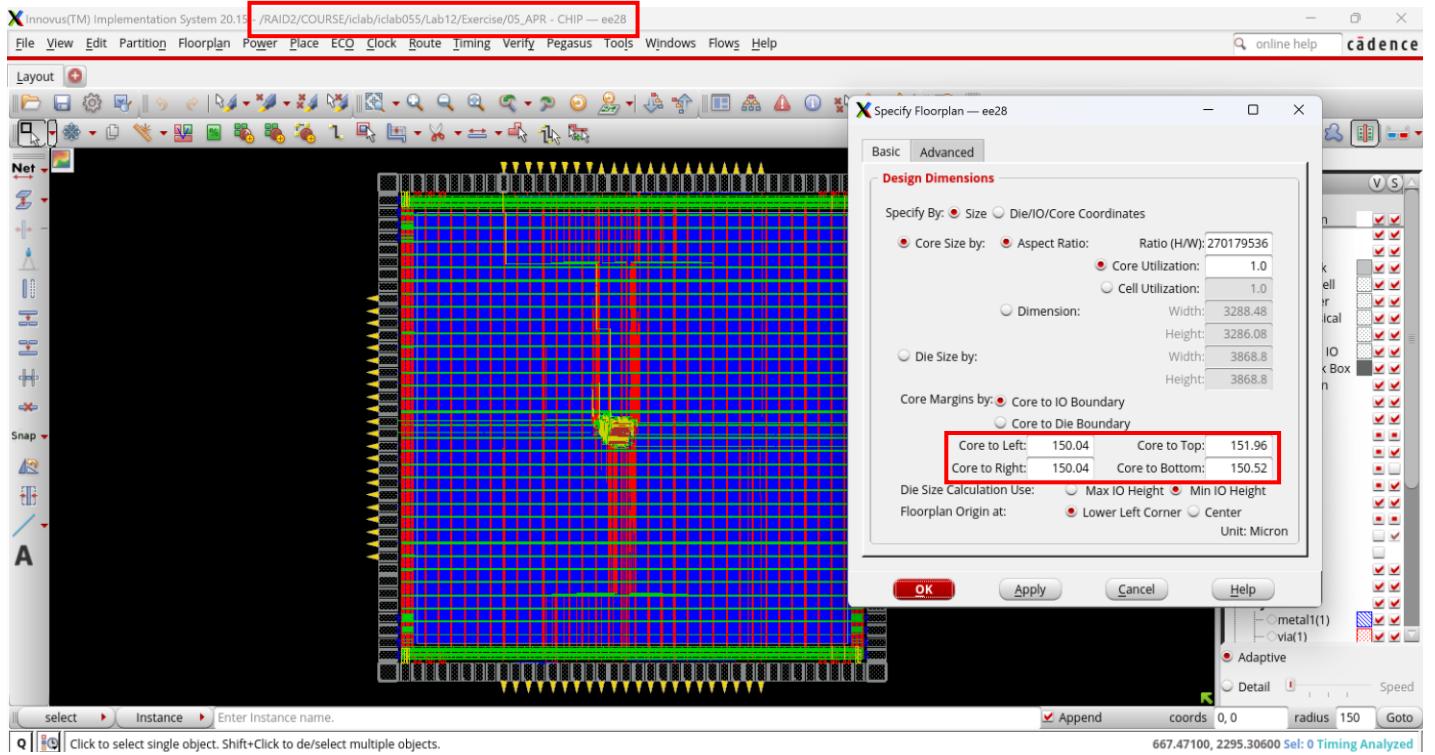


Report

IEE 313510162 陳柏淳

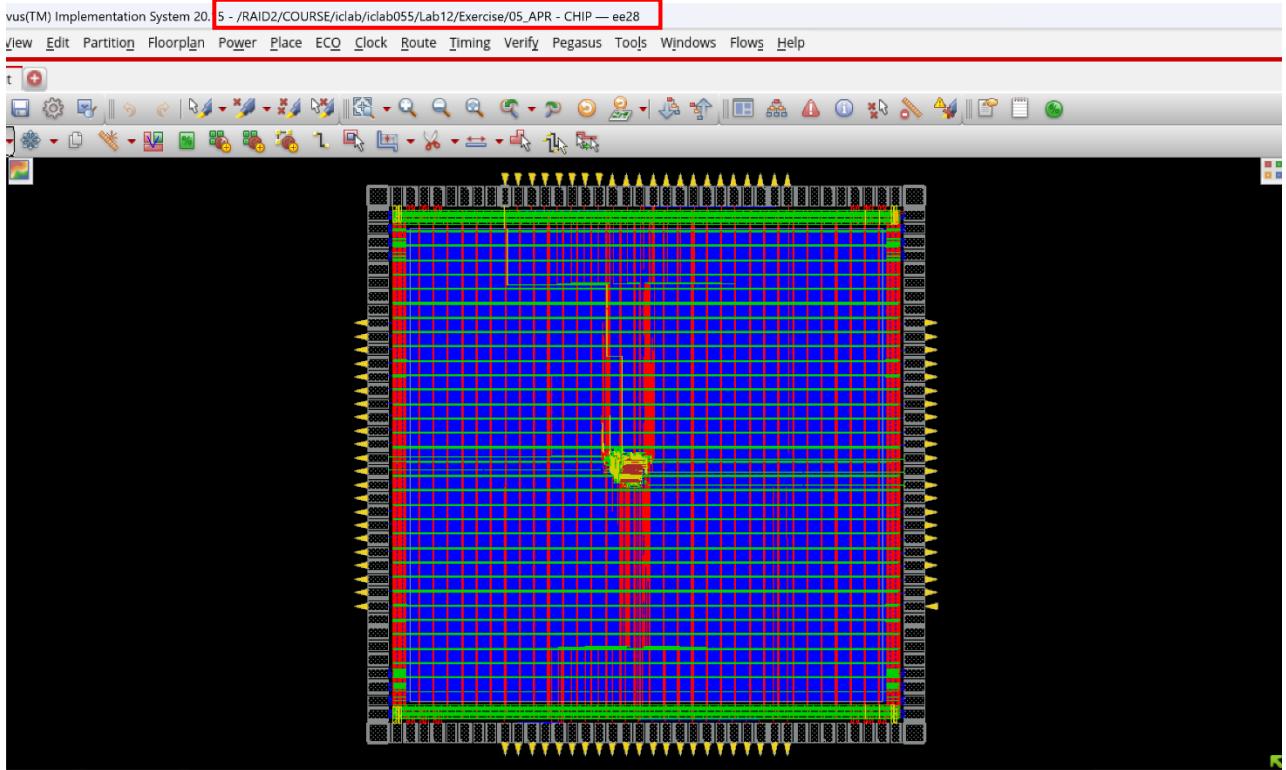
1. Core to IO boundary :



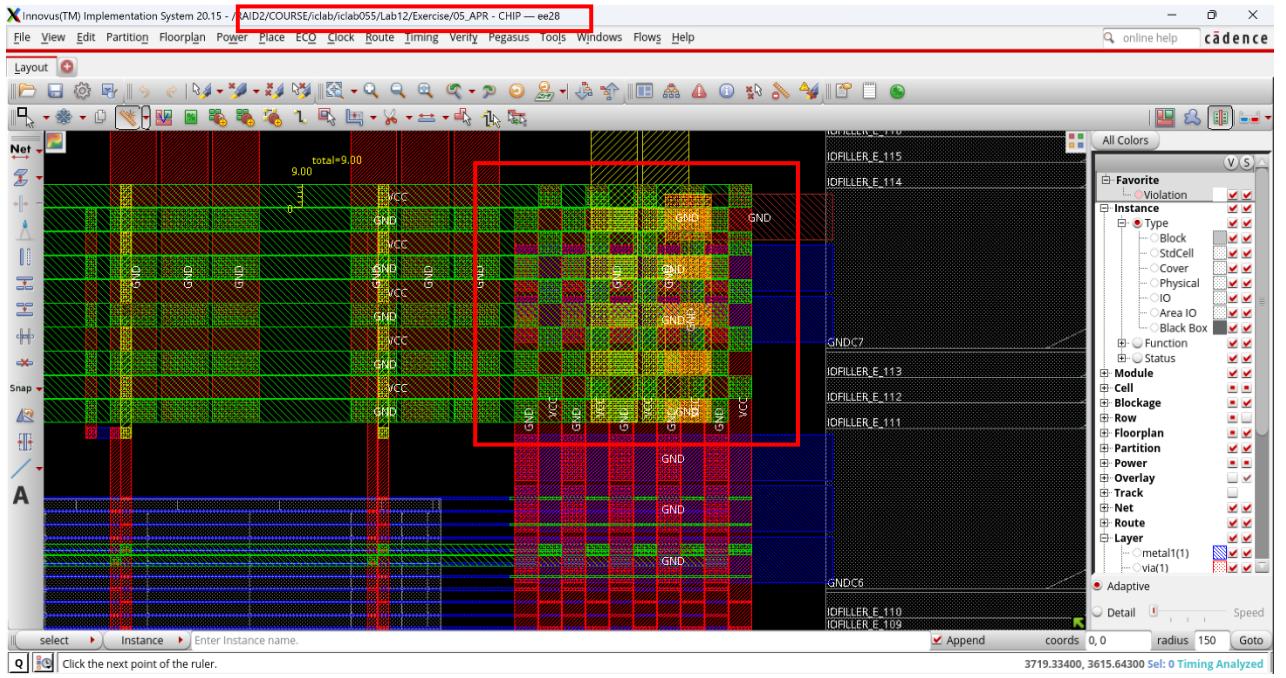
✓ Core to IO boundary: 150

2. Core Ring :

a. Layout :

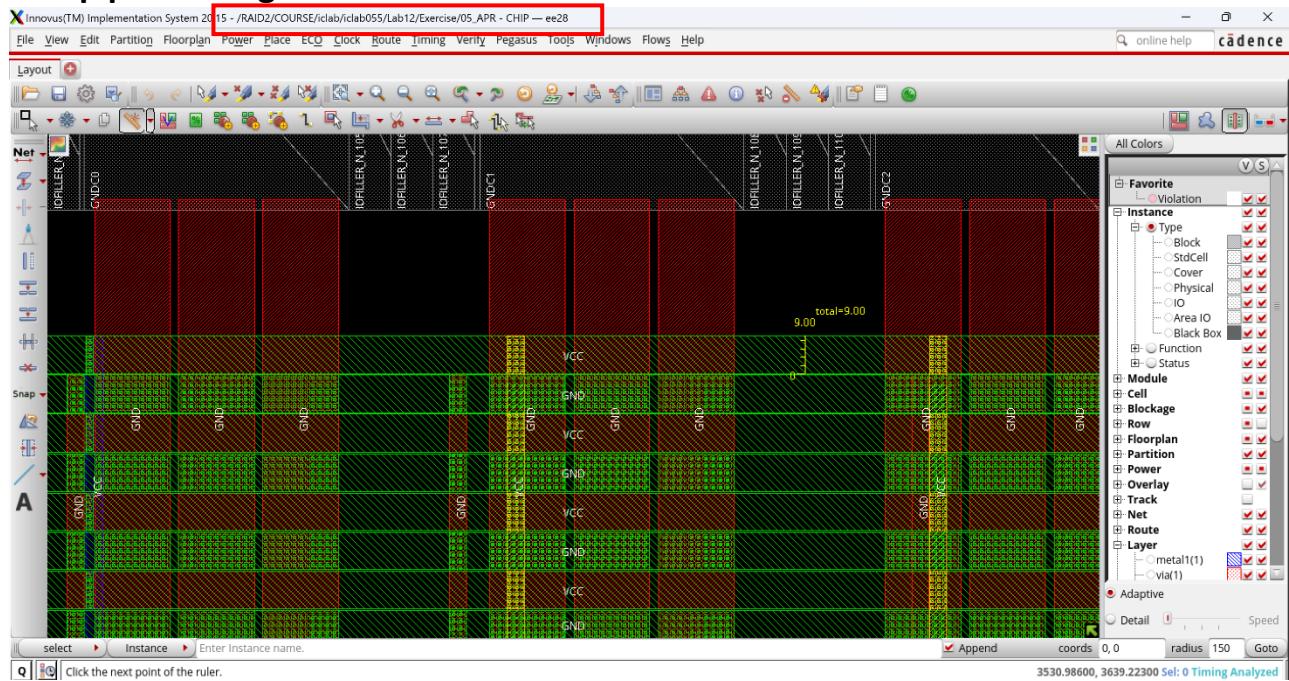


b. Power ring

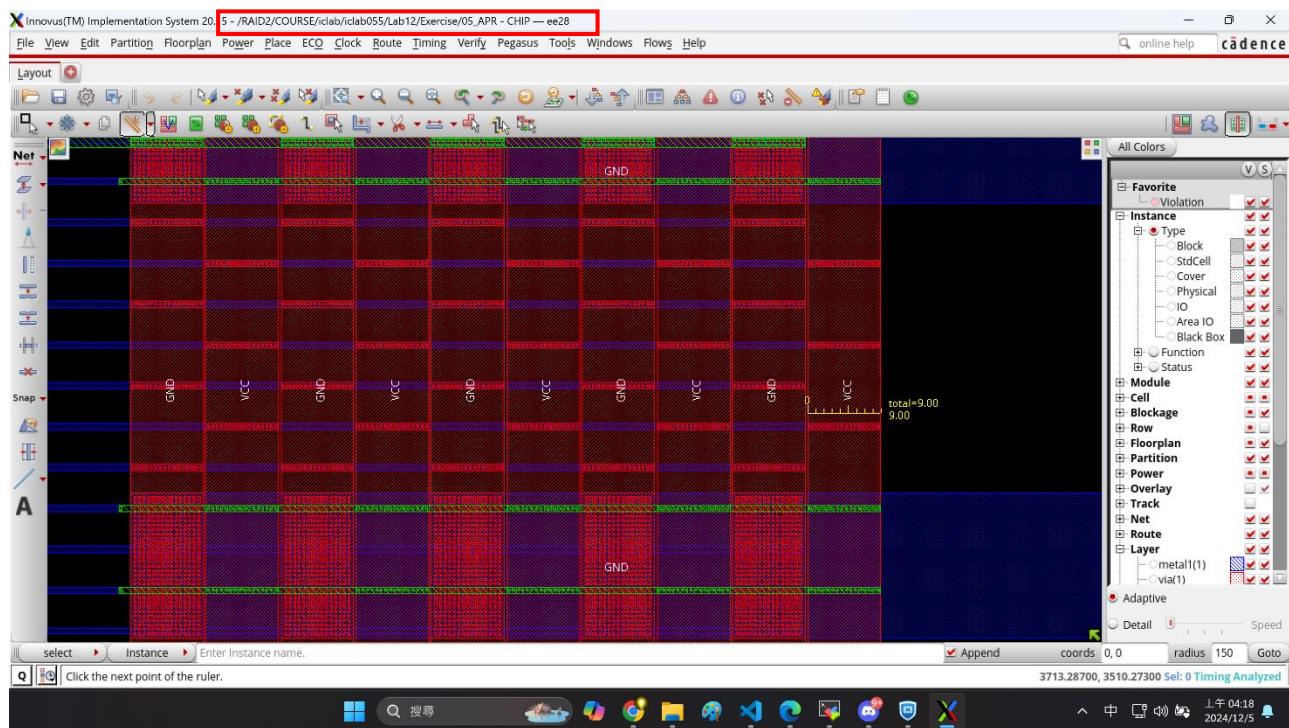


- ✓ wire group
- ✓ interleaving
- ✓ 5 pairs

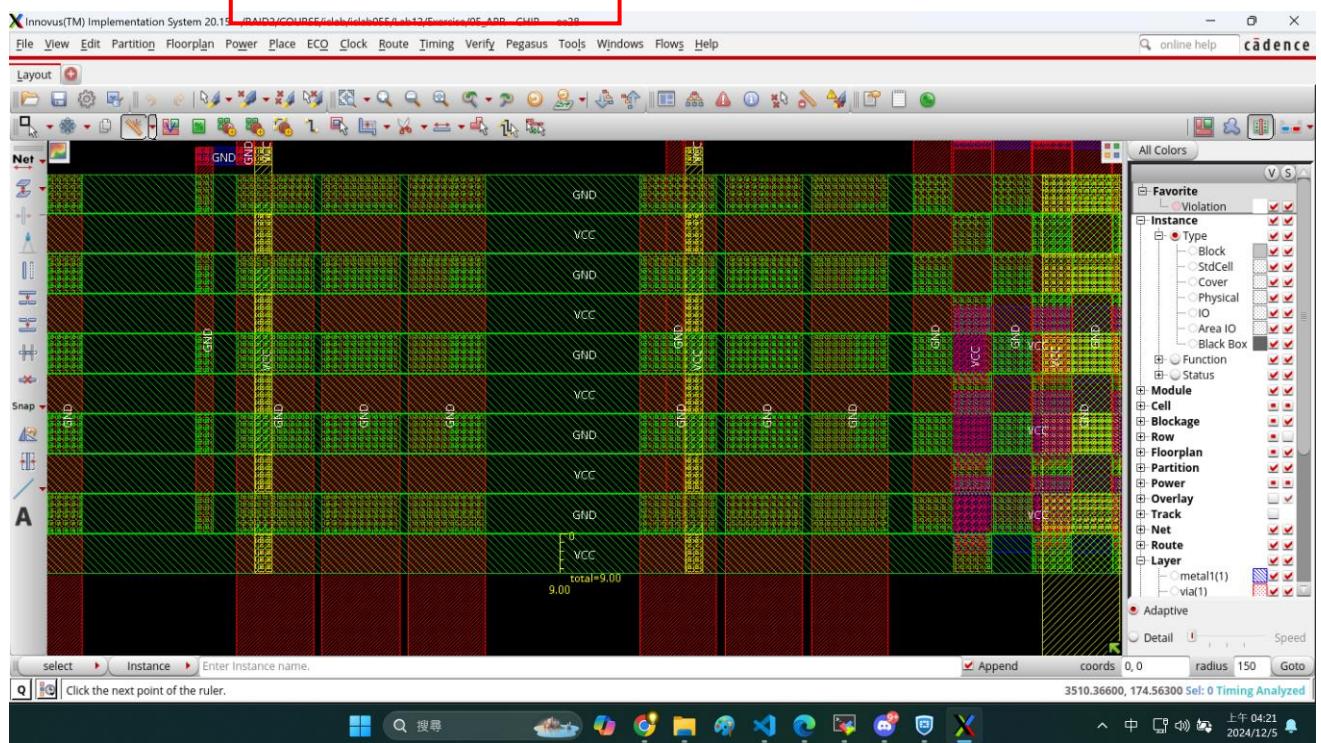
c. Top power ring



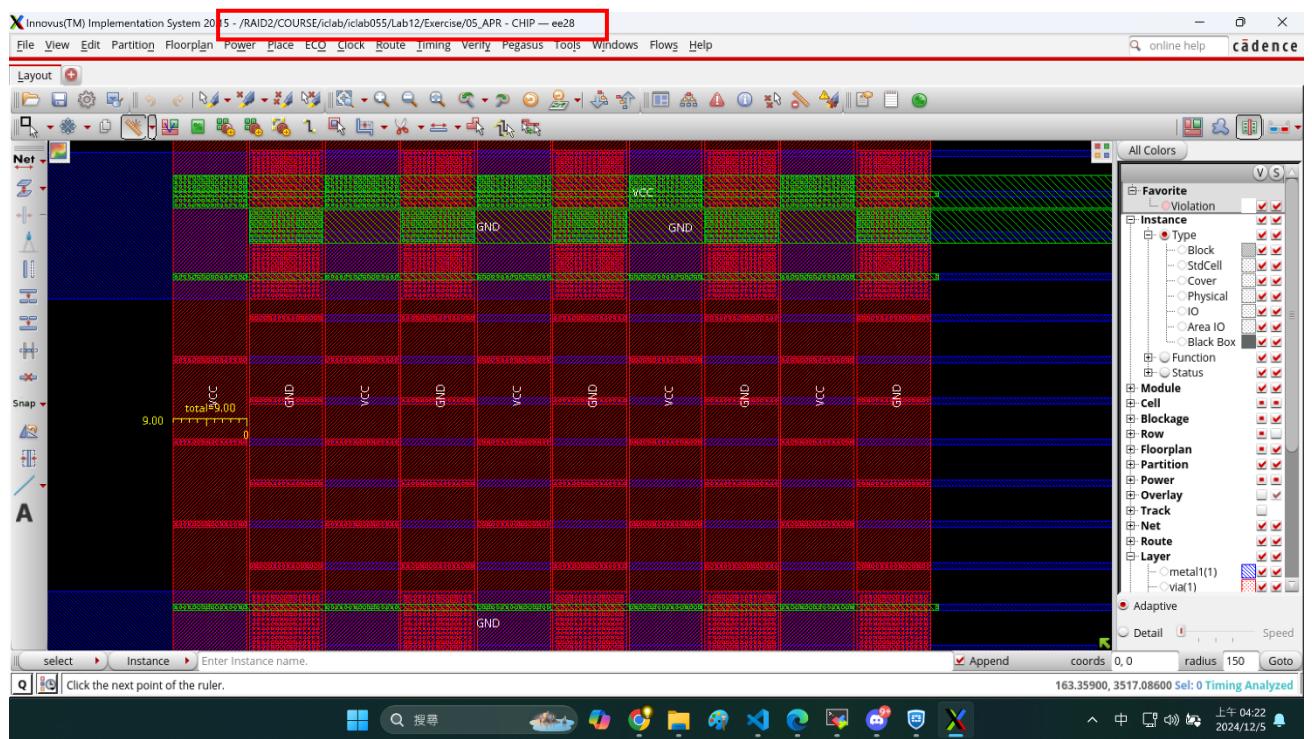
d. Right power ring



e. Bottom power ring



f. Left power ring



- ✓ Top & Bottom: metal layer must be odd and width is fixed to 9.
- ✓ Left & Right: metal layer must be even and width is fixed to 9.

3. Post-Route setup time analysis :

```

ee28.si2.iee.ncu.edu.tw (iclab055)
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
12. ee28.si2.iee.ncu.edu.tw (iclab055) 10. ee28.si2.iee.ncu.edu.tw (iclab055)

timeDesign Summary

Setup views included:
av_func_mode_max

+-----+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns):| 13.503 | 31.345 | 13.503 |
| TNS (ns):| 0.000 | 0.000 | 0.000 |
| Violating Paths:| 0 | 0 | 0 |
| All Paths:| 595 | 247 | 366 |
+-----+-----+-----+-----+

+-----+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+
| max_cap | Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+

Density: 0.357%
(126.921% with Fillers)
Total number of glitch violations: 0
Reported timing to dir timingReports
Total CPU time: 0.63 sec
Total Real time: 2.0 sec
Total Memory Usage: 3622.101562 Mbytes
Reset AAE Options
*** timeDesign #8 [finish] : cpu/real = 0:00:00.6/0:00:02.3 (0.3), totSession cpu/real = 0:05:51.4/0:34:15.2 (0.2), mem = 3622.1M
0
innovus 32>

```

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4. Post-Route hold time analysis :

```

ee28.si2.iee.ncu.edu.tw (iclab055)
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
12. ee28.si2.iee.ncu.edu.tw (iclab055) 10. ee28.si2.iee.ncu.edu.tw (iclab055)

Add other clocks and setup CTE to AAE Clock Mapping during iter 1
Loading CTE Timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 3647.9M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=3612.97)
Glitch Analysis: View av_func_mode_mtn -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_mtn -- Total Number of Nets Analyzed = 1385.
Total number of fetched objects 1385
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-018: Total number of nets in the design is 1348, 0.1 percent of the nets selected for SI analysis
End delay calculation. (MEM=3652.14 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=3652.14 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.7 real=0:00:01.0 totSessionCpu=0:05:53 mem=3652.1M)

timeDesign Summary

Hold views included:
av_func_mode_mtn

+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns):| 0.233 | 0.233 | 19.767 |
| TNS (ns):| 0.000 | 0.000 | 0.000 |
| Violating Paths:| 0 | 0 | 0 |
| All Paths:| 595 | 247 | 366 |
+-----+-----+-----+-----+

Density: 0.357%
(126.921% with Fillers)
Reported timing to dir timingReports
Total CPU time: 1.17 sec
Total Real time: 1.0 sec
Total Memory Usage: 3583.402344 Mbytes
Reset AAE Options
*** timeDesign #9 [finish] : cpu/real = 0:00:01.2/0:00:01.5 (0.8), totSession cpu/real = 0:05:53.3/0:34:31.3 (0.2), mem = 3583.4M
0
innovus 33>

```

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- ✓ NO negative slacks after setup/hold time analysis (**Post-Route stage**)
- ✓ The DRV of (fanout, cap, tran) should be all 0 after setup/hold time analysis

5. DRC result :

The screenshot shows a terminal window titled "ee28.s12.iee.nycu.edu.tw (iclab055)". The terminal content displays the results of a DRC verification process. A red box highlights the final message: "Verification Complete : 0 Viols." Below this, the command "*** End Verify DRC (CPU: 0:00:01.0 ELAPSED TIME: 1.00 MEM: 0.0M) ***" is shown. At the bottom of the terminal, the prompt "innovus 31>" is visible.

```
VERIFY DRC ..... Sub-Area : 209 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3655.680 3394.560 3868.800 3655.680} 210 of 225
VERIFY DRC ..... Sub-Area : 210 complete 0 Viols.
VERIFY DRC ..... Sub-Area : {0.000 3655.680 261.120 3868.800} 211 of 225
VERIFY DRC ..... Sub-Area : 211 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {261.120 3655.680 522.240 3868.800} 212 of 225
VERIFY DRC ..... Sub-Area : 212 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {522.240 3655.680 783.360 3868.800} 213 of 225
VERIFY DRC ..... Sub-Area : 213 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {783.360 3655.680 1044.480 3868.800} 214 of 225
VERIFY DRC ..... Sub-Area : 214 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1044.480 3655.680 1305.600 3868.800} 215 of 225
VERIFY DRC ..... Sub-Area : 215 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1305.600 3655.680 1566.720 3868.800} 216 of 225
VERIFY DRC ..... Sub-Area : 216 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1566.720 3655.680 1827.840 3868.800} 217 of 225
VERIFY DRC ..... Sub-Area : 217 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1827.840 3655.680 2088.960 3868.800} 218 of 225
VERIFY DRC ..... Sub-Area : 218 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2088.960 3655.680 2350.080 3868.800} 219 of 225
VERIFY DRC ..... Sub-Area : 219 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2350.080 3655.680 2611.200 3868.800} 220 of 225
VERIFY DRC ..... Sub-Area : 220 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2611.200 3655.680 2872.320 3868.800} 221 of 225
VERIFY DRC ..... Sub-Area : 221 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2872.320 3655.680 3133.440 3868.800} 222 of 225
VERIFY DRC ..... Sub-Area : 222 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3133.440 3655.680 3394.560 3868.800} 223 of 225
VERIFY DRC ..... Sub-Area : 223 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3394.560 3655.680 3655.680 3868.800} 224 of 225
VERIFY DRC ..... Sub-Area : 224 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3655.680 3655.680 3868.800 3868.800} 225 of 225
VERIFY DRC ..... Sub-Area : 225 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.0 ELAPSED TIME: 1.00 MEM: 0.0M) **

1 innovus 31>
```

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6. LVS result :

The screenshot shows a terminal window titled "ee28.s12.iee.nycu.edu.tw (iclab055)". The terminal content displays the results of an LVS verification process. A red box highlights the final message: "Verification Complete : 0 Viols., 0 Wrngs. (CPU Time: 0:00:00.2 MEM: 0.00M)". The command "source ./cmd/my_script/final_LVS.cmd" was run before the verification. At the bottom of the terminal, the prompt "innovus 30>" is visible.

```
**WARN: (IMPCTE-291): FILLER_T_1_512 is a physical only instance and is ignored. This indicates that the instance is physical only (e.g. a filler/decap cell) and is in the database, but not in timing graph since physical cells do not have timing information. Verify the instance is a physical only cell to confirm that this warning can be ignored.
Type 'man IMPCTE-291' for more detail.
**WARN: (EMS-27): Message (IMPCTE-291) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.
innovus 29> set_power_rail_display -plot none
innovus 29> set_power_rail_display -plot ir
innovus 29>
innovus 29> set_power_rail_display -plot none
innovus 29>
innovus 29> source ./cmd/my_script/final_LVS.cmd
VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Thu Dec 5 04:14:04 2024

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (3868.8000, 3868.8000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Thu Dec 5 04:14:04 2024
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols., 0 Wrngs.
(CPU Time: 0:00:00.2 MEM: 0.00M)

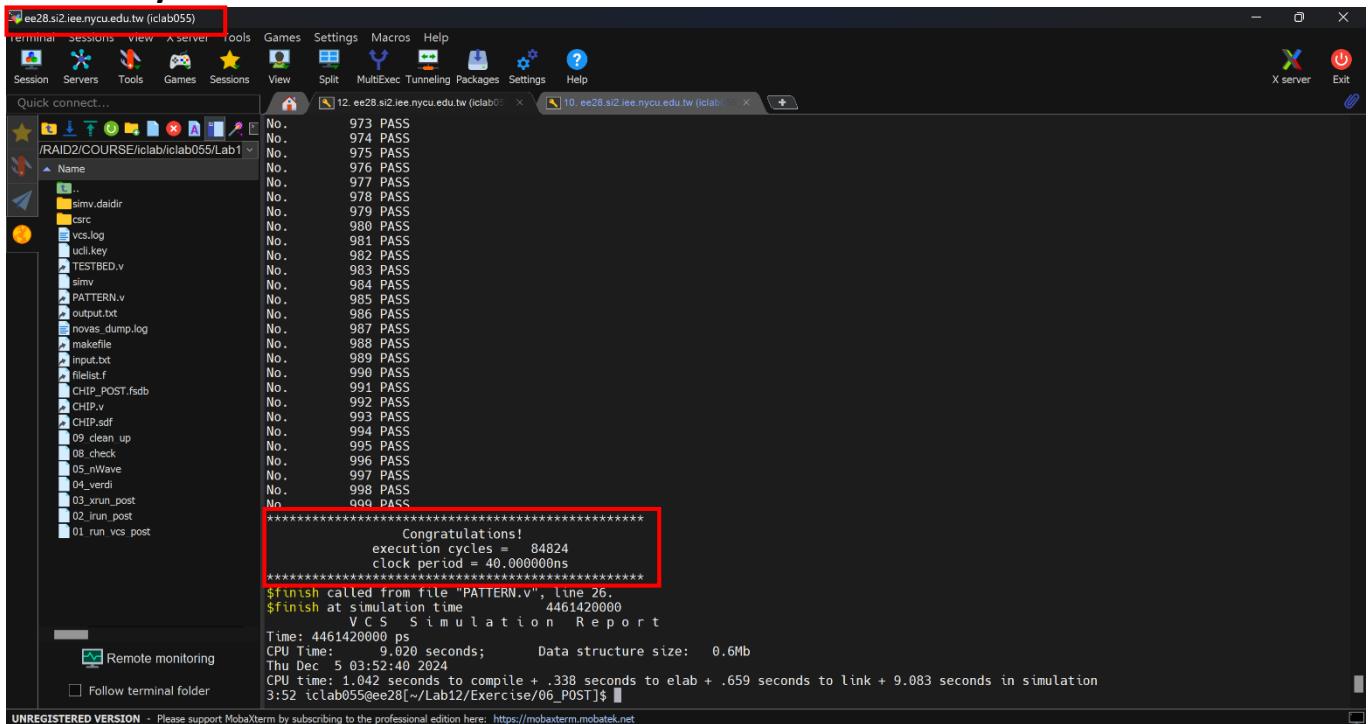
1 innovus 30>
```

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✓ **LVS : No LVS violations after “verify connectivity”**

✓ **DRC : No DRC violations after “verify DRC”**

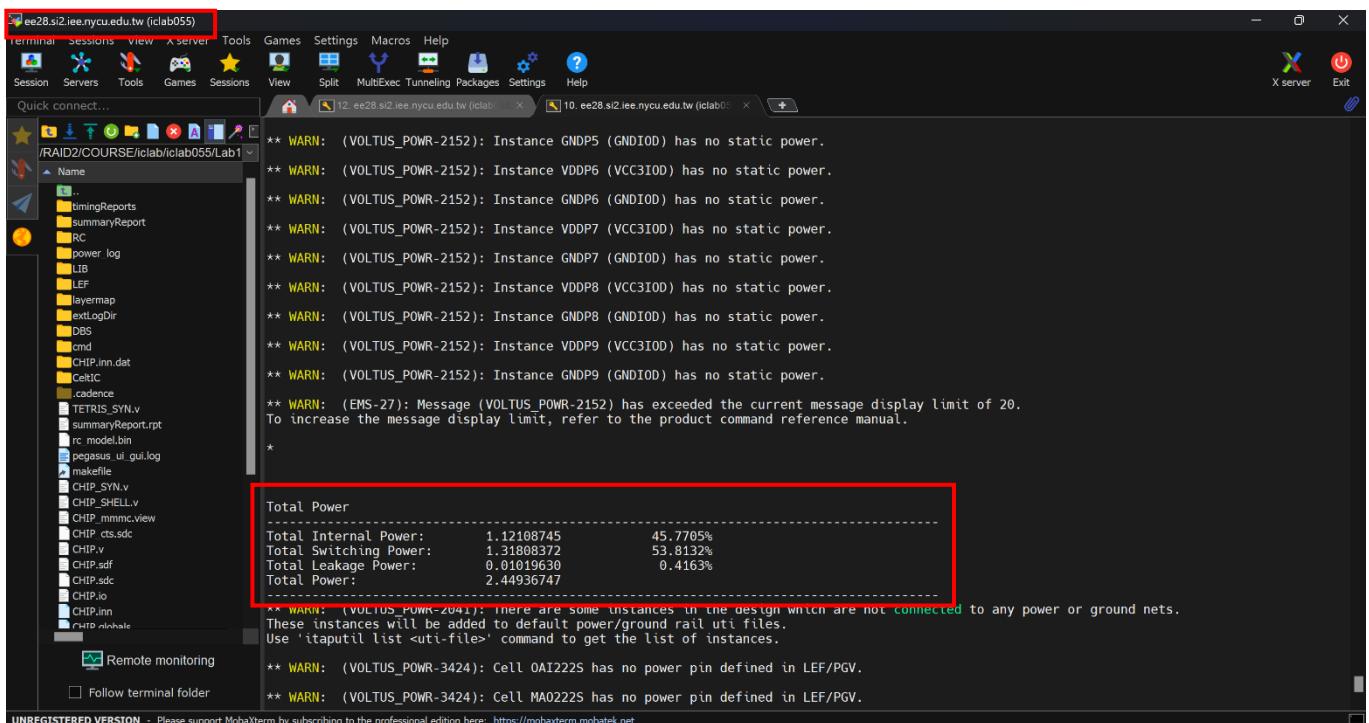
7. Post Layout simulation result :



```
ee28.si2.iee.nycu.edu.tw (iclab055)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect... 12. ee28.si2.iee.nycu.edu.tw (iclab055) 10. ee28.si2.iee.nycu.edu.tw (iclab055)
No. 973 PASS
No. 974 PASS
No. 975 PASS
No. 976 PASS
No. 977 PASS
No. 978 PASS
No. 979 PASS
No. 980 PASS
No. 981 PASS
No. 982 PASS
No. 983 PASS
No. 984 PASS
No. 985 PASS
No. 986 PASS
No. 987 PASS
No. 988 PASS
No. 989 PASS
No. 990 PASS
No. 991 PASS
No. 992 PASS
No. 993 PASS
No. 994 PASS
No. 995 PASS
No. 996 PASS
No. 997 PASS
No. 998 PASS
No. 999 PASS
*****
Congratulations!
execution cycles 84924
clock period 40.00000ns
*****
$finish called from file "PATTERN.v", line 26.
$finish at simulation time 44614206000
VCS Simulation Report
Time: 4461420600 ps
CPU Time: 9.020 seconds; Data structure size: 0.6Mb
Thu Dec 5 03:52:40 2024
CPU time: 1.042 seconds to compile + .338 seconds to elab + .659 seconds to link + 9.083 seconds in simulation
3:52 iclab055@ee28:~/Lab12/Exercise/06_POST]$
```

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8. Power result :

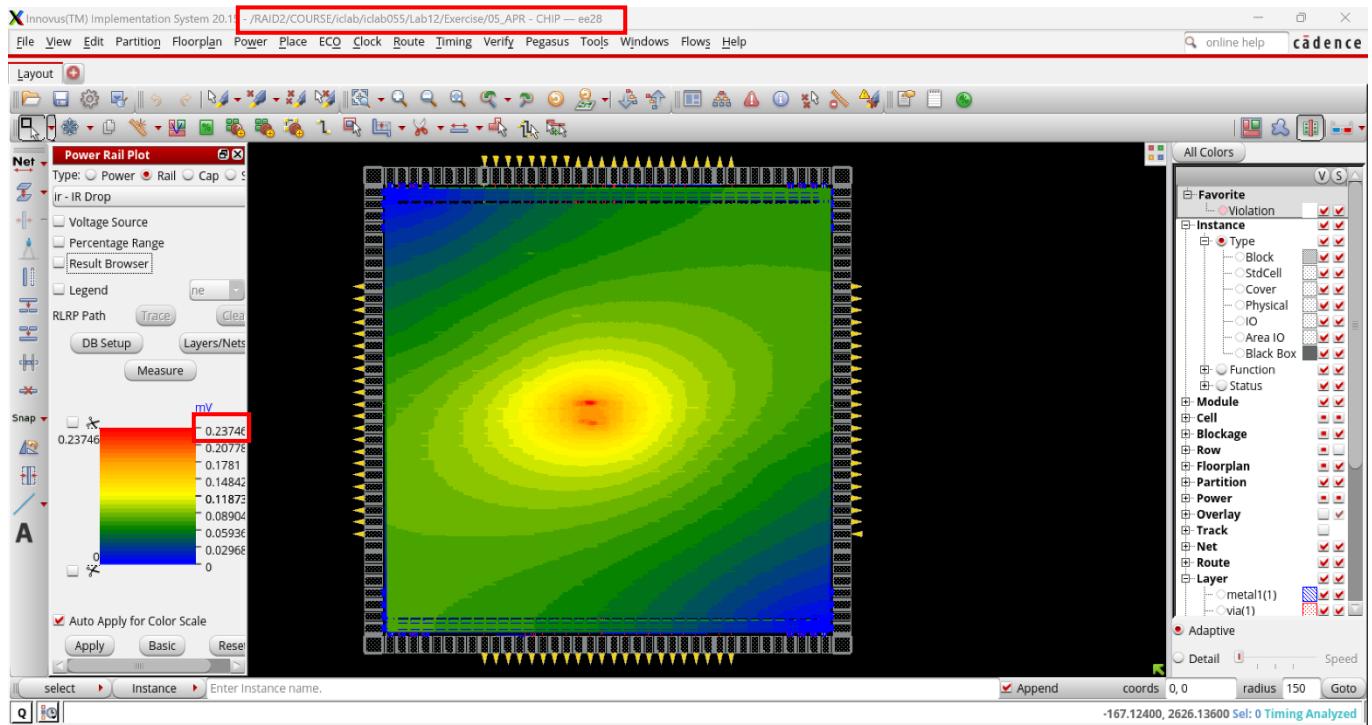


```
ee28.si2.iee.nycu.edu.tw (iclab055)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect... 12. ee28.si2.iee.nycu.edu.tw (iclab055) 10. ee28.si2.iee.nycu.edu.tw (iclab055)
** WARN: (VOLTUS_POWR-2152): Instance GNDP5 (GNDIOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDP6 (VCC3IOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDP6 (GNDIOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDP7 (VCC3IOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDP7 (GNDIOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDP8 (VCC3IOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDP8 (GNDIOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDP9 (VCC3IOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDP9 (GNDIOD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDP10 (VCC3IOD) has no static power.
** WARN: (EMS-27): Message (VOLTUS_POWR-2152) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.
*
Total Power
-----
Total Internal Power: 1.12108745 45.7705%
Total Switching Power: 1.31808372 53.8132%
Total Leakage Power: 0.01019630 0.4163%
Total Power: 2.44936747
-----
** WARN: (VOLTUS_POWR-2041): There are some instances in the design which are not connected to any power or ground nets.
These instances will be added to default power/ground rail uti files.
Use 'itaputl list <uti-file>' command to get the list of instances.
**
** WARN: (VOLTUS_POWR-3424): Cell OA122S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell MA022S has no power pin defined in LEF/PGV.
```

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9. IR Drop Results :

a.



The maximum IR drop : **0.237 mV**

Strategies to reduce IR Drop issue :

To mitigate the issue of IR drop, I implemented **16 sets of core power pads** and reduced the spacing between power stripes to make them more compact. Additionally, I ensured an equal number of pads on each side of the chip's perimeter, **maintaining a square chip shape**. This design evenly distributes power in both vertical and horizontal directions, effectively reducing the extent of IR drop.