CPU Architecture

Final Project

Entropy Filter and Histogram

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1. Aim of the Assignment

- Design, synthesize and analyze a digital filter.
- Understanding t FPGA memory structure

2. Definition and prior knowledge

The aim of this laboratory is to design a Real Time entropy detection filter for an image received from a camera. The histogram of the image must be calculated. Further information will be given below.

3. Assignment definition

You must design an entropy filter and image histogram. Connect both modules to MIPS MCU, which was designed in previous work.

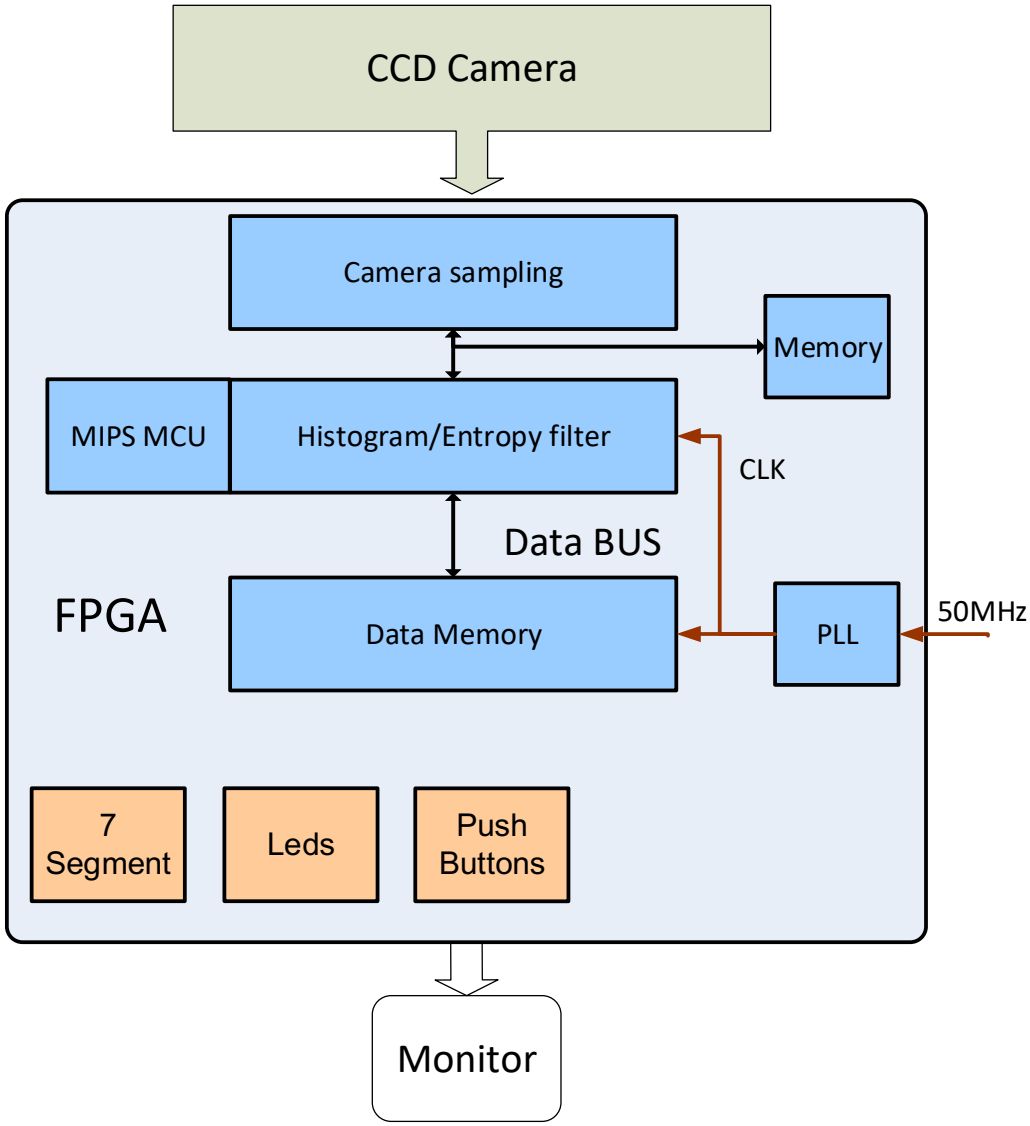

Figure 1 : System architecture

While performing the RT image processing the MIPS CPU must continue to work (run a program). The PLL [2] is used to make a higher frequency from the 50MHz clock and is used in FPGA compilation only.

You have to do the following tasks:

- Modelsim Simulation with maximal coverage
- Quartus Compilation
- Find the maximum operating clock
- Analyze the critical path, and explain what is the main reason
- Analyze the logic usage, and optimize it for FPGA
- Load the design into the FPGA and verify the simulation results

The following must be presented in the report.

- RTL Viewer results for each logic block
- Logic usage for each block (Combinational and Flip-Flops)
- Critical path for each logic block and overall system critical path
- Optimizations performed on the code for the FPGA
- Logic usage report from Quartus II

4. Test

As a test bench, you will have to perform an entropy filter [1],[6] on the image taken from camera. The size of the filter will be 6x6. In addition to the filtering process, the image histogram [5] will be calculated. Switches will allow to select the image presented on the monitor (original, filtered or histogram). A general diagram of the processing is shown in figure 2.

The test will be in the following steps:

- Capture image from camera, convert to gray scale.
- MCU Receive interrupt from the camera when a frame is saved into memory.
- Send command to hardware to perform the filtering or histogram calculation.
- Receive interrupt when hardware done and filtered frame saved into memory
- An original image, filtered image or histogram will be presented on monitor depending on switches.
- MCU must run counter in main loop and print to 7S the time in resolution of seconds.

You must compare processing time of entropy filter and histogram in hardware design vs implementation in MIPS from lab3 (theoretically) and provide an estimation of the speedup. If necessary, instructions can be added to your MIPS design.

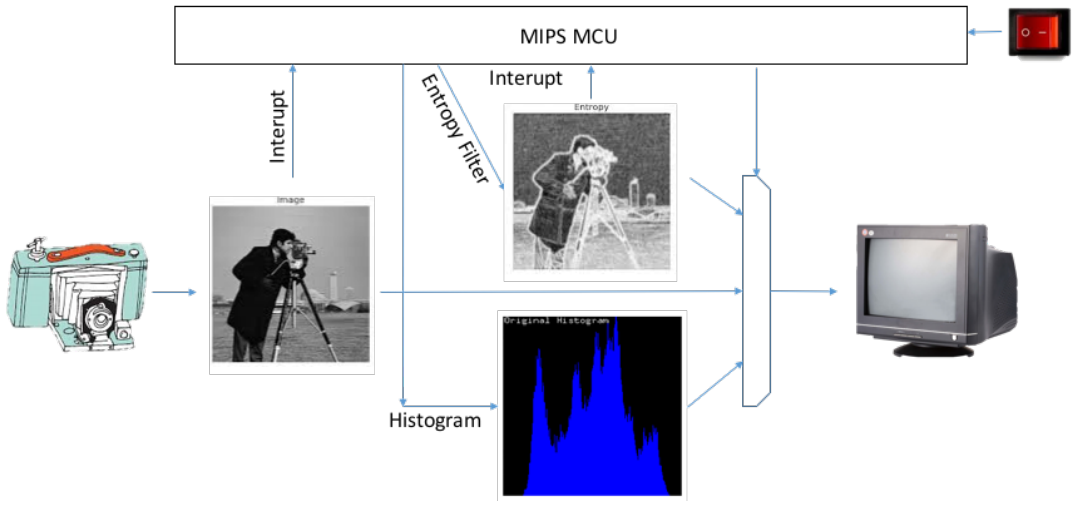

Figure 2 : Processing Diagram

5. Requirements

You have to do the following tasks:

- Modelsim Simulation with maximal coverage
- Analyze the critical path , explain where is it in the VHDL file and design and Find the maximal operating clock
- Load the design into the FPGA and verify the simulation results

The following must be presented in the report.

1. Top level block review diagram of your design.
2. For each block in the top level design:
   - RTL Viewer results
   - Logic usage for each block (Combinational and Flip-Flops)
   - Graphical description (a square with ports going in and out).
   - Port Table (direction, size, functionality).
   - Short description.

3. Maximum(Critical) path of your design – explain where it is in the code and how it is possible to optimize it if you would have more time. What is the maximum clock frequency.
4. Minimum path analysis.
5. Style - Contents with page numbers, Images and tables will be numbered. The caption of an images and tables below the images or tables.
6. Elaborated analysis and wave forms:
   - Test bench description –
   - Regular cases that were checked.
   - Extreme cases that were checked
   - Forbidden cases that were not checked.
   - Maximal Frequency and critical paths from Timing Analyzer
   - Proof of work using Signal Tap
   - **One** basic waveform to explain the system timing.
7. Maximal frequency analysis
8. Conclusions and future work (how can the system be improved if you'd had more time)

Design requirements:

1. The design must be well commented.
2. The system must work from only one clock.
3. Resets in the system must be synchronous except the main system asynchronous reset.
4. Do not use latches.

A zip file form of id1_id2.zip where id1 and id2 are the identification number of the submitters, and id1 < id2 will be submitted to borisbr@bgu.ac.il mail. The file will contain:

- The full *.doc or *.pdf report file, with operation manual of the watch.
- Modelsim simulations
- **Quartus project including the VHDL files and the project itself**
- The SignalTap files used in project debug
- Quartus Project SOF file
- The ZIP must not contain temporary files ("db" and "db_incremental" and "work" directories).
-
- The ZIP file directory structure must be arranged according to Table 3.

- After organizing the ZIP file, verify compilation and that no files are missing.

Directory	Contains	Comments
VHDL	Project VHDL files	Only VHDL files , excluding test bench
TB	VHDL files that are used for test bench	
SIM	Modelsim project ".mpf" and waveform ".do" files	Do not place files that are not relevant for compilation or is a result of compilation
DOC	Project documentation	Readme.txt and PDF report file
Quartus	Quartus Project files	Do not place files that are not relevant for compilation or is a result of compilation
CODE	The assembly source code	

Table 1 : Directory Structure

6. Grading policy

Weight	Task	Description
30%	Requirements	The entire list of requirements in the assignment paper
20%	Documentation	The "clear" way in which you presented the requirements and the analysis
20%	Design	The overall system design, code styling, comments, logic usage and code/files organization.
20%	Analysis and Test	The correct analysis of the system and test bench coverage
10%	Conclusions	Asserted conclusions on the work you've done

Table 2 Grading

Under the above policies you'll be also evaluated using common sense:

- Your files will be compiled and checked, the system must work.
- Your design and architecture must be intelligent, effective and well organized.
- The design must be well commented

The preliminary project presentation will be on lecture (10.6.18).

Final presentation on date 21/6/2018 in the lab between 16-18 and submission to the borisbr@post.bgu.ac.il

For a late submission the penalty is 2^{days}.
For early submission the reward is 2*days (up to 3 days).

7. References

[1]. http://www.mathworks.com/help/images/ref/entropyfilt.html
[2]. ALTPLL User Guide: http://www.altera.com/literature/ug/ug_altpll.pdf
[3]. Altera RAM user guide: http://www.altera.com/literature/ug/ug_ram_rom.pdf
[4]. Altera Megafunction User Guide:
www.altera.com/literature/ug/ug_intro_to_megafunctions.pdf
[5]. http://en.wikipedia.org/wiki/Image_histogram
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stuttgart.de/~maucher/Python/MMCodecs/html/basicFunctions.html