Host FPGA-Memory Interface

The host memory interface is based on an Altera control panel and is used to initialize the board memory content and perform dump from the board memory.

Setting up the Host Memory Interface

Setting up the host memory involves the following actions:

- Adding the host interface logic to your design
- Compile the design
- Set up the hardware
- Configure the FPGA
- Start the Control Panel

Adding the host interface logic to the design

The easiest way to add the host interface to your design is to insert your design logic into a template located in the archive. To do that, instantiate your logic in the ***top_level.vhd*** file and connect your CPU program and data busses to the ***port_a*** of ***rogram_memory*** and ***data_memory*** instances. Make sure to connect your CPU clock to ***clock_a*** inputs.
If you don't want to use the template, you must copy all the required logic located in ***top_level.vhd*** to your top-level design and to add pins related to debug interface (TDI, TDO, TCK, and TCS) to your top-level. Also you are required to add lines located at the beginning of ***top_level.vhd*** file to your project QSF file.

Hardware Setup

- Ensure that the development board has powered up and is operating normally
- Check that the USB-Blaster cable connects the host computer to the the development board.
- Check that the 7.5 V DC adapter connects the development board to a power source.
- Set the **RUN/PROG** switch to the RUN position.
- Turn the power on by depressing the **ON/OFF** switch on the development board.

FPGA Configuration

Before using the Host Interface, you must first download the compiled design (with host interface logic) to Cyclone II FPGA by downloading the **top_level.sof** configuration file.

Control Panel Start

To start the Control Panel, perform the following steps:

- Run the CII_Starter_control_panel.exe program found in the archive.
- Select **Open** to list all USB ports connected to development boards.
- Select **Open USB Port 0.** This step places the Control Panel in control of the development board. The Control Panel occupies the USB port. Quartus II can not download a configuration file into the FPGA while the Control Panel occupies the USB port. Closing the Control Panel GUI releases the port.
- Experiment by setting the value of some 7-segment display and observing the result on the development board.

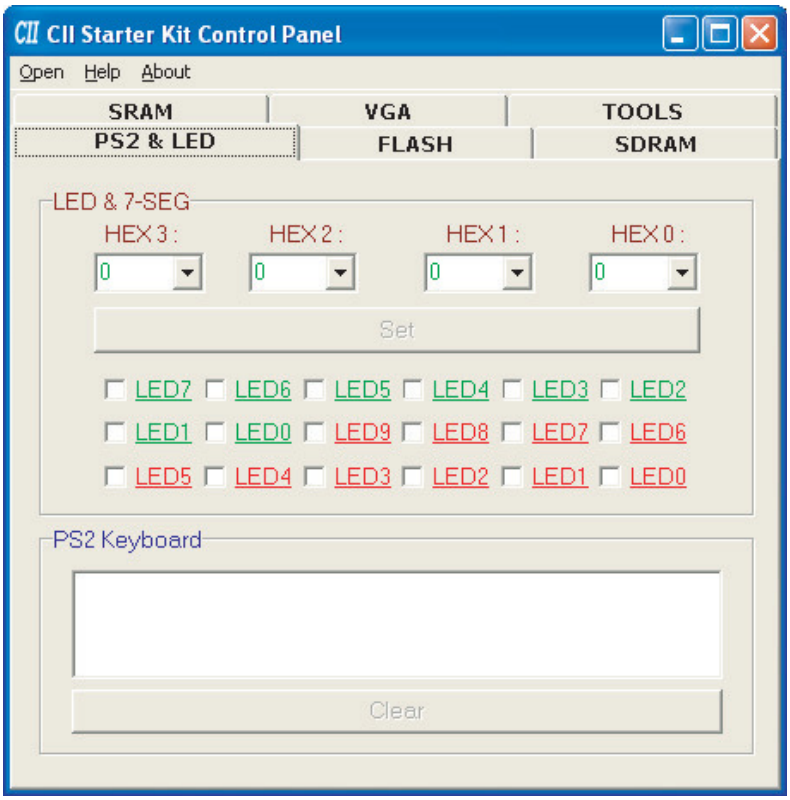

Figure 1 : Control Panel Window

Using the Host memory Interface

The host memory Interface is based on modified Altera control panel and can't perform all the functions of it. The only options that can be controlled are:

- LEDs
- Seven Segment
- Writing and reading Internal FPGA SRAM (program and data) through SRAM control panel interface

Accessing internal FPGA memory

The main purpose of the host interface is to allow access to your CPU program and data memory from a host computer. This operation is uses an SRAM part of the control panel.

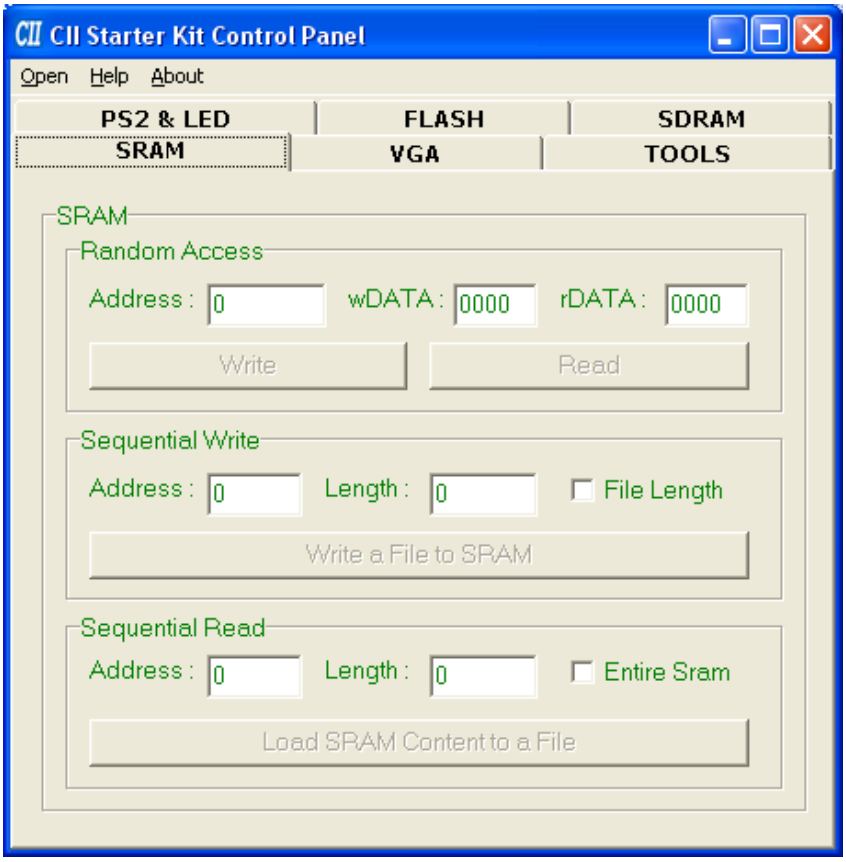

Figure 2 : Memory Access

In order to write data to the program or data memory perform the following:

- Open a SRAM tap of the control panel
- In the sequential Write , specify Address (0 for data memory , 20000 for program memory)
- Mark “File Length”
- Click “Write a File to SRAM” and select a file

In order to read data from the program or data memory perform the following:

- Open a SRAM tap of the control panel
- In the sequential Read , specify Address (0 for data memory , 20000 for program memory)
- Specify the Length of data you want to read
- Click “Load SRAM Contents to a File” and select a file

In order to Read/Write one word from a program or data memory use the “Random Access” , note that you need to make two consecutive writes/reads to two addresses in order to access one memory word (X*2 and X*2+1) where X is a address of the memory word. For example if you want to read word 5, you must read word 10 and 11.

For more information see “Using Control Panel” chapter in the Altera FPGA board user manual.