DESIGN OF A MICROWAVE POWER DETECTOR USING A SCHOTTKY BARRIER DIODE

- **Components:**

  - Metal: **Copper**
    - Conductivity: 58000000 Siemens/m
    - Relative Permittivity (εr): 1
  - Substrate: **Rogers RO4003C**
    - Relative Permittivity **(**εr): 3.55
    - Dielectric Loss Tangent ($tan\delta$): 0.0027

- **Design Specifications:**

  - Substrate Thickness = 0.508mm
  - Metal Thickness = 0.017mm

- **Design Criteria:**

  Operating Frequency: 7.8 GHz

- **Block Diagram:**

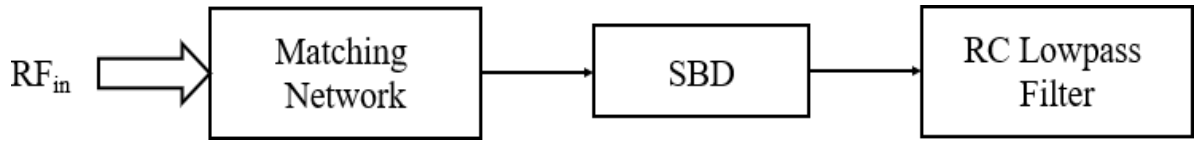

Fig.1. Block diagram of detector design

Fig.1 shows the block diagram of the microwave power detector. It consists of a matching network followed by a Schottky barrier diode (SBD) and an RC lowpass filter.

- **Design Steps:**

  To design the specified microwave power detector, we have followed a few steps.

  (i) Design of RC low pass filter.

(ii) Diode attachment to the low pass filter and measurement of input impedance of the diode.

(iii) Design of the matching network.

(iv) Attachment of the matching network to the diode and low pass filter to complete the circuit.

❖ The diode used here is Schottky diode, as it has the least junction capacitance and least forward voltage. The principle of diode detection relies on rectifying the signal (AC component) through a diode and generating voltage as DC component. The detection makes use of nonlinear characteristics of Schottky diode. So, bias circuit is not necessary. The Schematic implementation of the diode is shown in the fig. 2

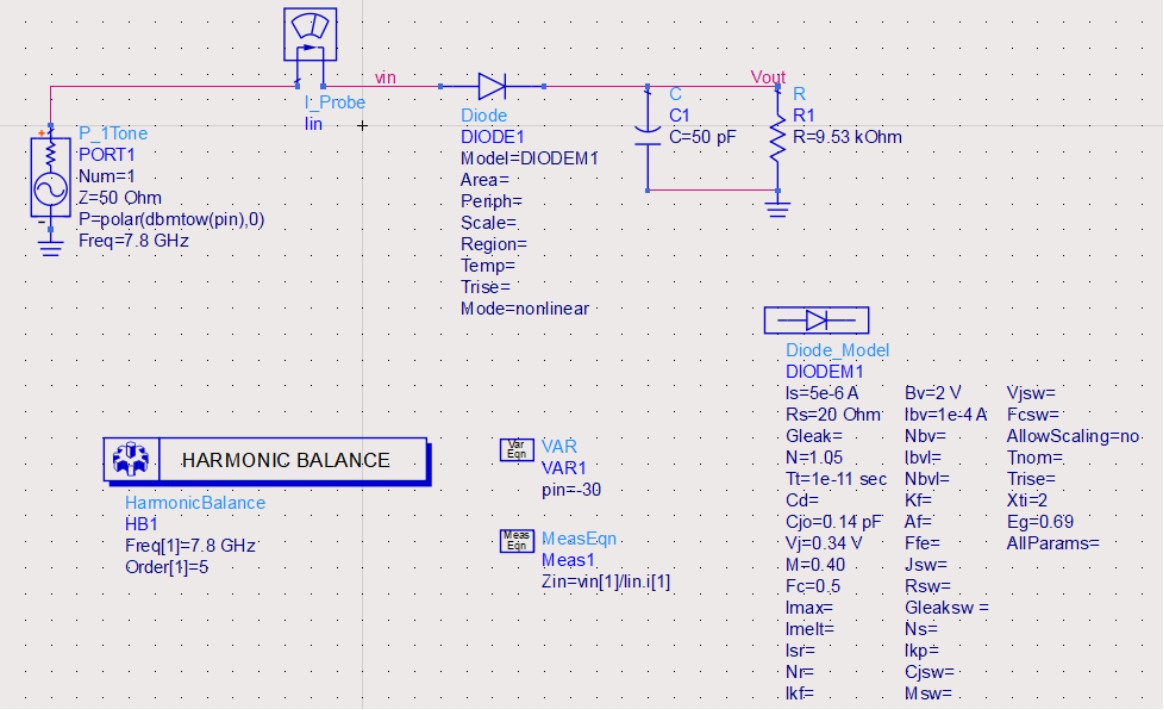

Fig.2. Schematic circuit of SBD Detector

❖ The RC network forms low pass filter as represented in the fig. 2. The exact frequency response of the filter depends on the choice of R and C in RC network. In this design R = 9.53 kΩ and C=50 pF. The impedance looking into RC network at the RF design frequency f_o should be negligibly small. Impedance at harmonic frequency nf_o where n=2, 3… is approximately zero. Higher harmonics are reflected by RC circuit and forced to pass through diode. Harmonic components further contribute to dc improvement of the detector sensitivity.

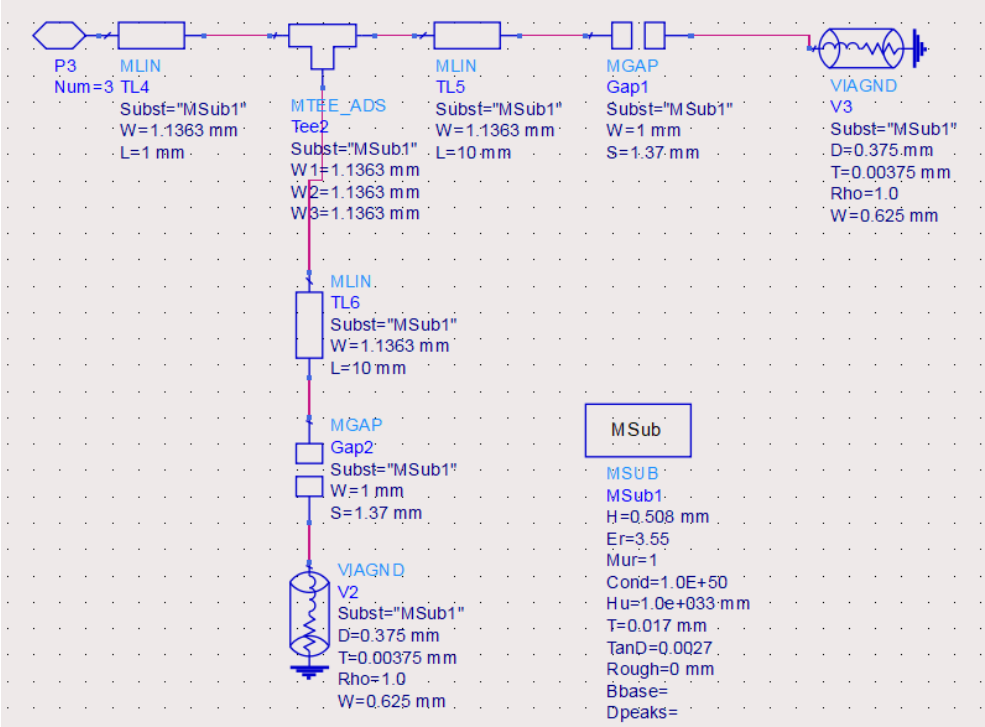

Fig. 3. Schematic of RC Network.

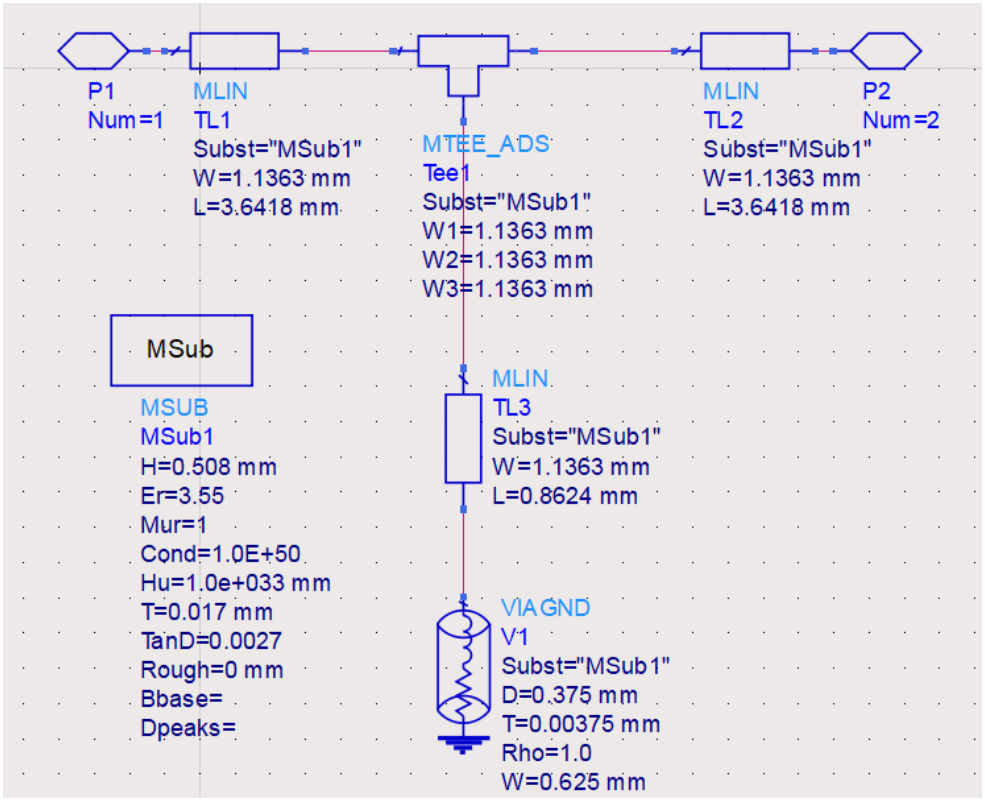

Fig. 4. Schematic of Matching Network.

- ❖ Matching network consists of shunt and series stub. Here, for detector design, three MLIN and a TEE have been used and width and length of MLIN have been optimized to get the desired output at 7.8 GHz and Harmonic balance analysis gives the required harmonic response for the detector.

  Fig.3 and Fig.4 show the schematics of the RC network and the matching network respectively along with various parameters.

Fig.4 shows the substrate design with various parameters and Fig.5 shows the layout of the RC network. The RC network consists of two VIAGNDs, one for capacitor and the other for resistor. The value of resistor is R = 9.53 kΩ and capacitor C= 50 pF.

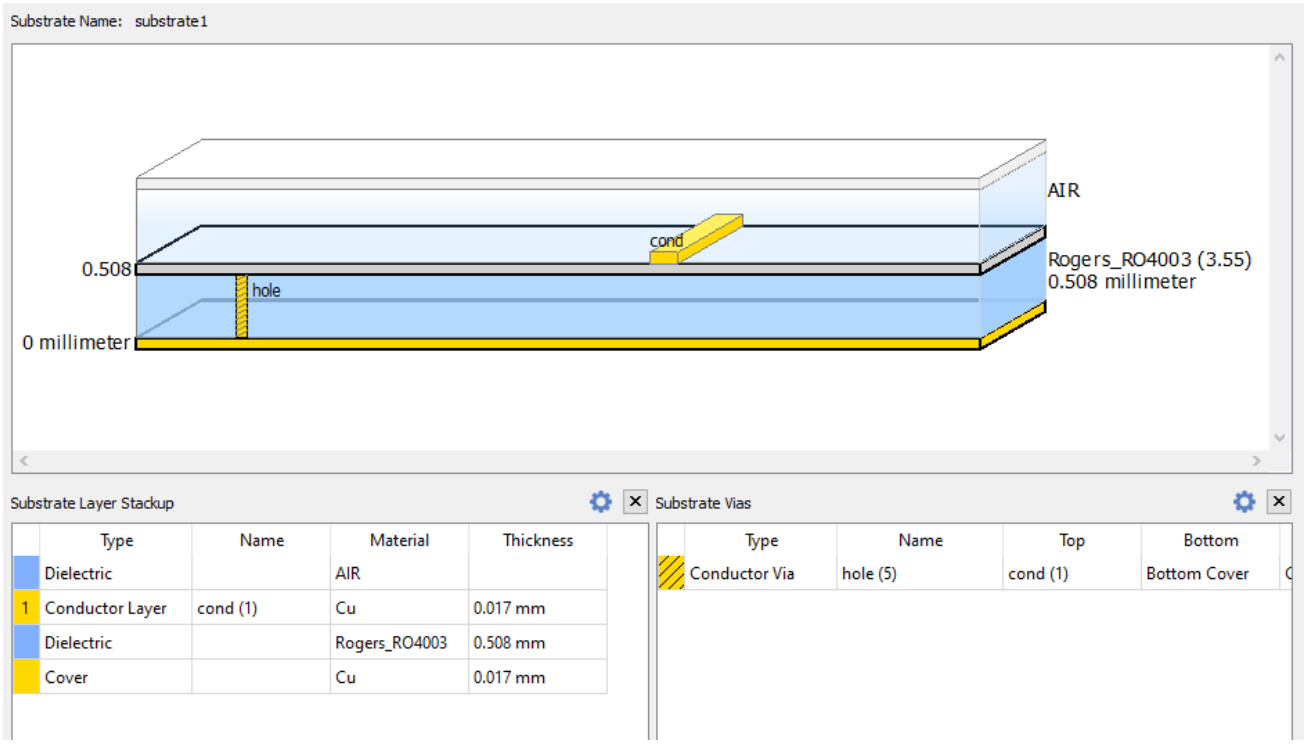

Fig. 5. Diagram of Substrate (Rogers RO4003C, Dielectric constant of 3.55, Frequency of 7.8 GHz)

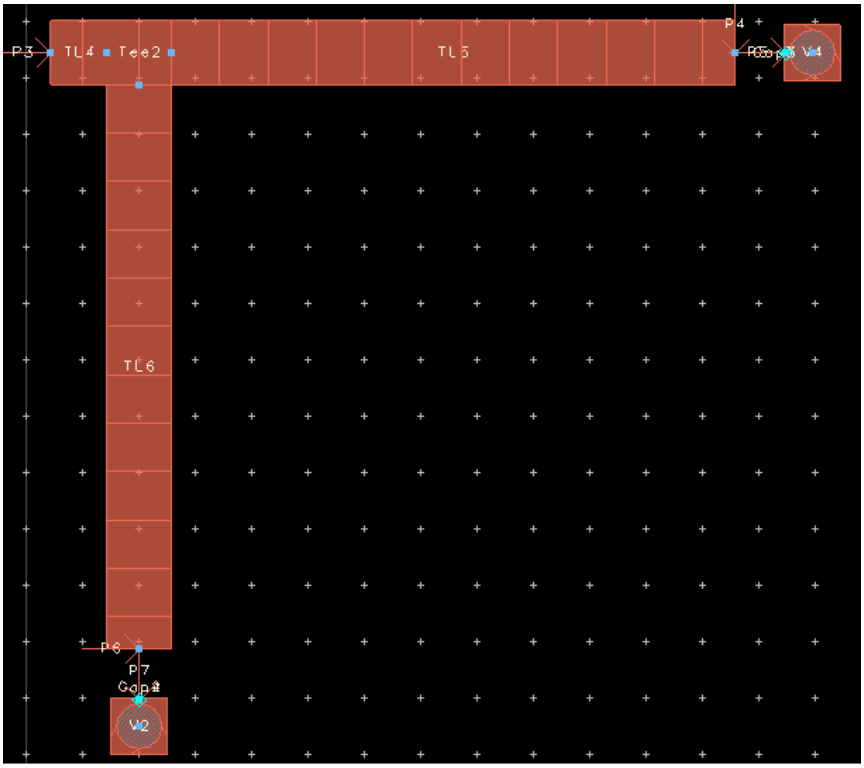

Fig. 6. Layout of the RC network.

After the design of RC along with diode pad, we get Z_{in} = (25.076-j*143.926) Ω as shown in Fig.6.

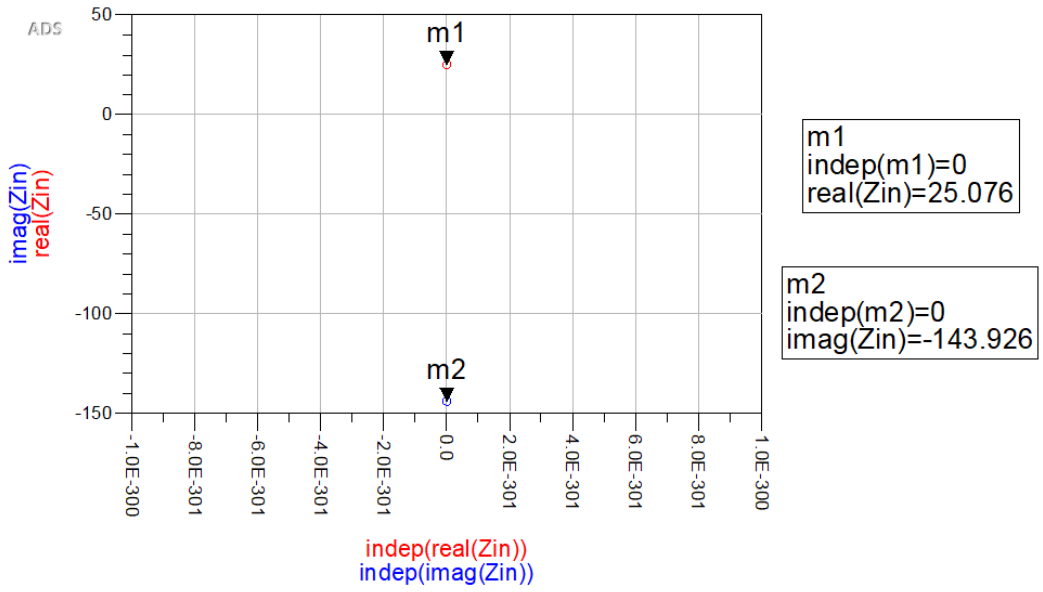

Fig. 6. Value of Zin at Pin of -30 dBm.

Fig.7 shows the layout of the matching network. The input of the matching network consists of 50 Ω impedance and the output consists of Z_{in}. A short-circuited stub has been used at the input side to provide a return path for the dc current generated from the diode. It also prevents the DC leakage to RF side without using any additional dc blocks at RF input.

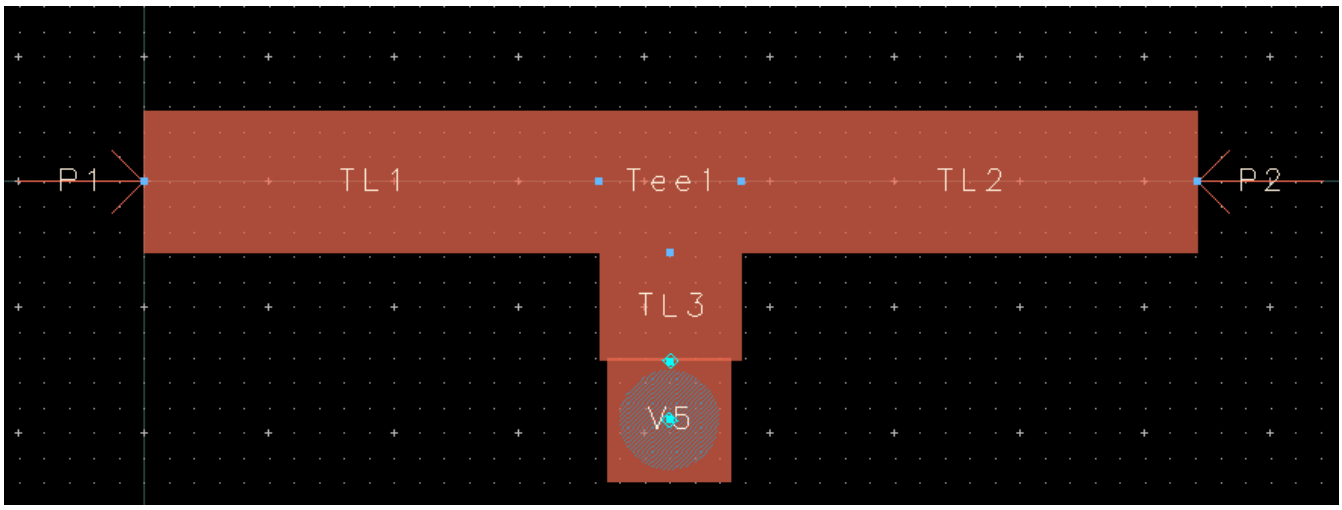

Fig. 7. Layout of Matching Network.

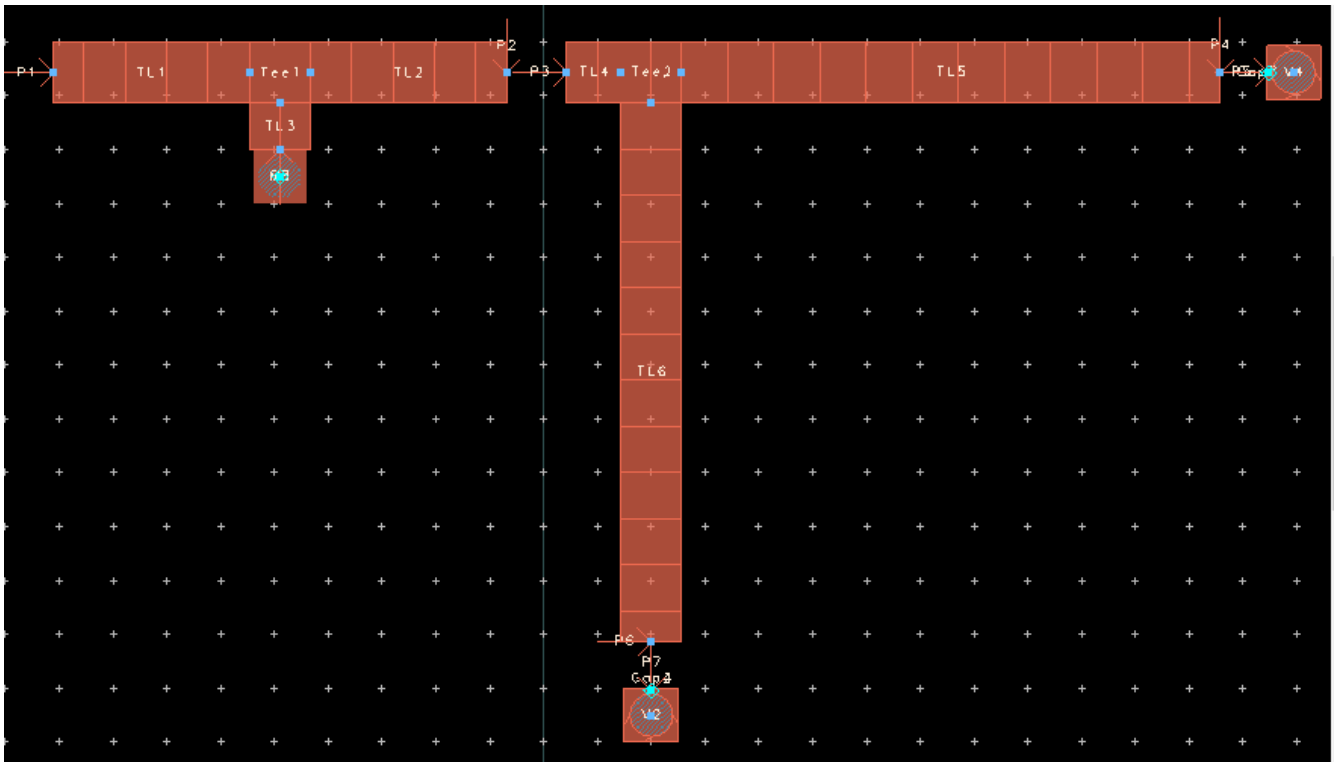

Fig. 8. Layout of the detector design along with matching network.

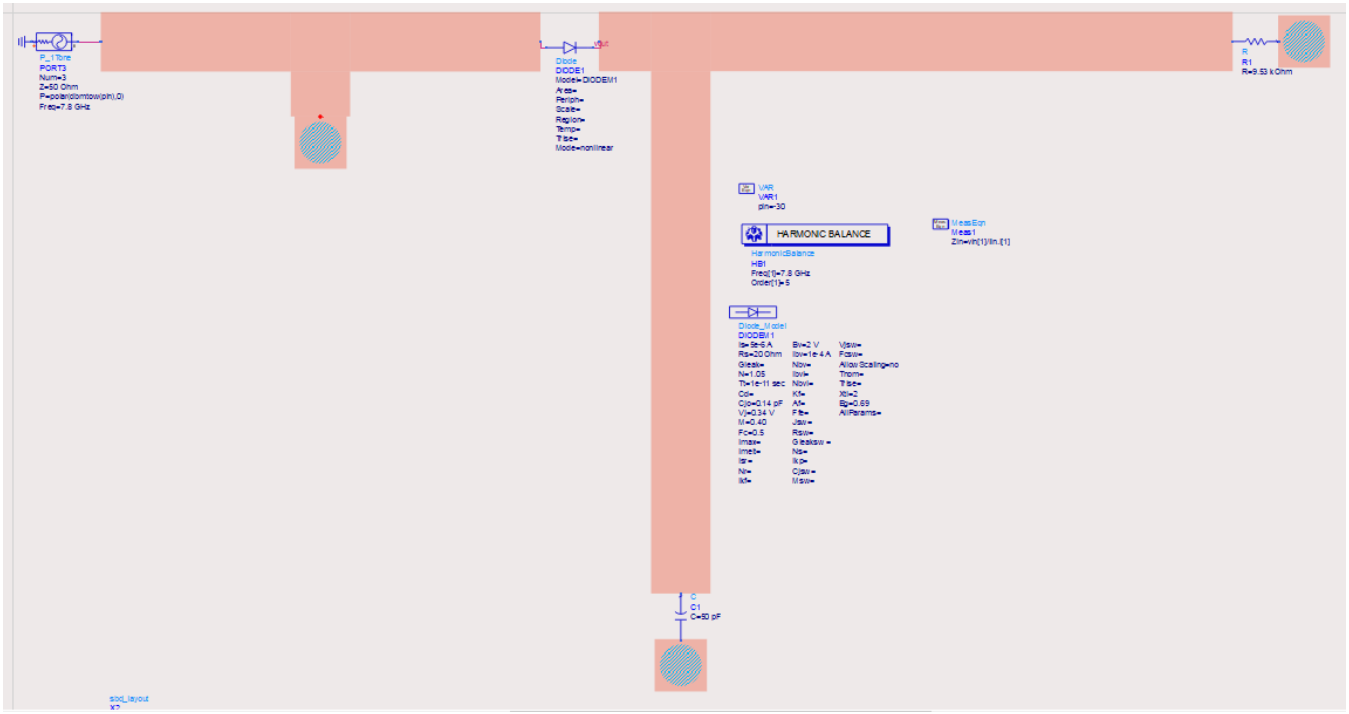

Fig. 8. Layout of the detector design along with matching network.

Fig. 8 shows the complete layout of the detector along with the matching network and Fig. 9 shows the final co-simulation of the EM model of detector. Here the diode, the capacitor and the resistor are connected to the EM model and S Parameter and Harmonic Balance simulation is carried out on it. The results obtained are discussed below.

➢ **Results:**

❖ **S11 parameter of the design**

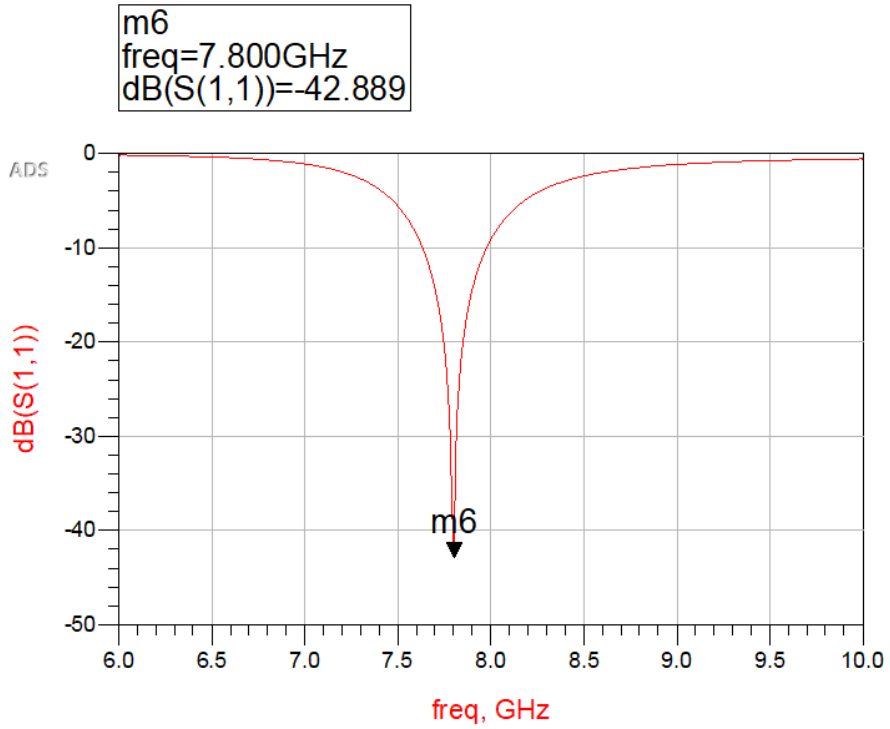

Fig.9. S_{11} of the final detector design

Fig. 9 shows the input reflection coefficient vs frequency plot. A good matching at 7.8 GHz is observed as -40 dB.

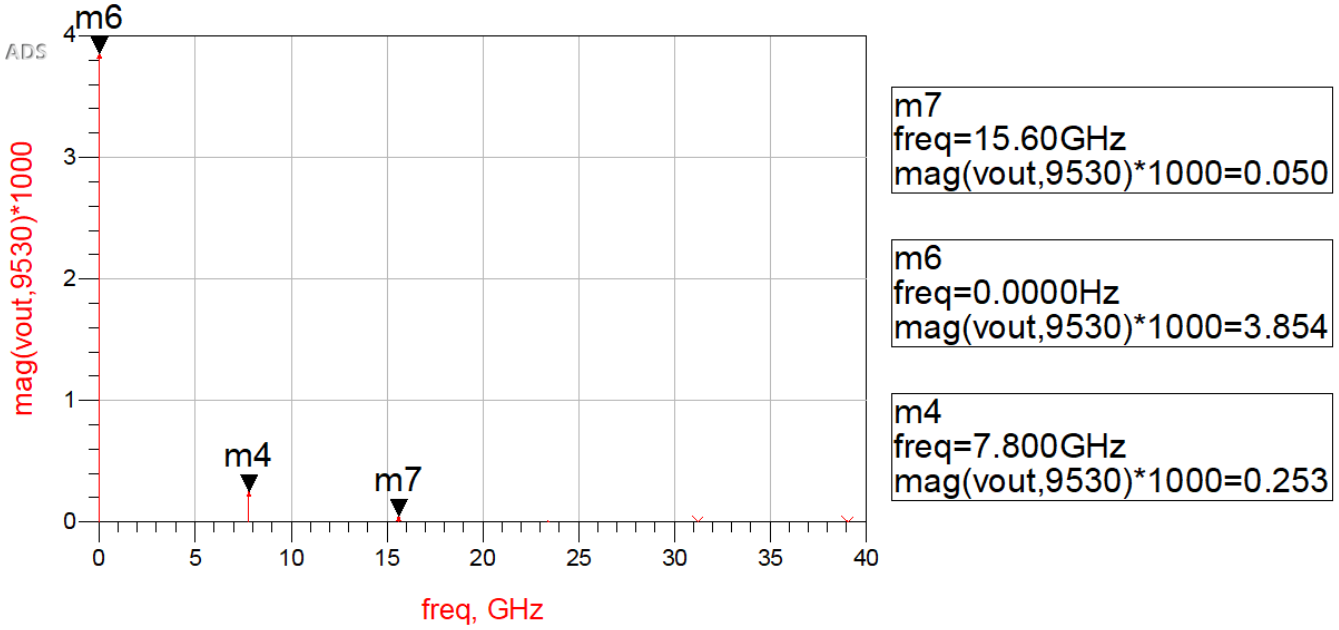

Fig.10. Magnitude of V_{out} in mV vs frequency plot for detector

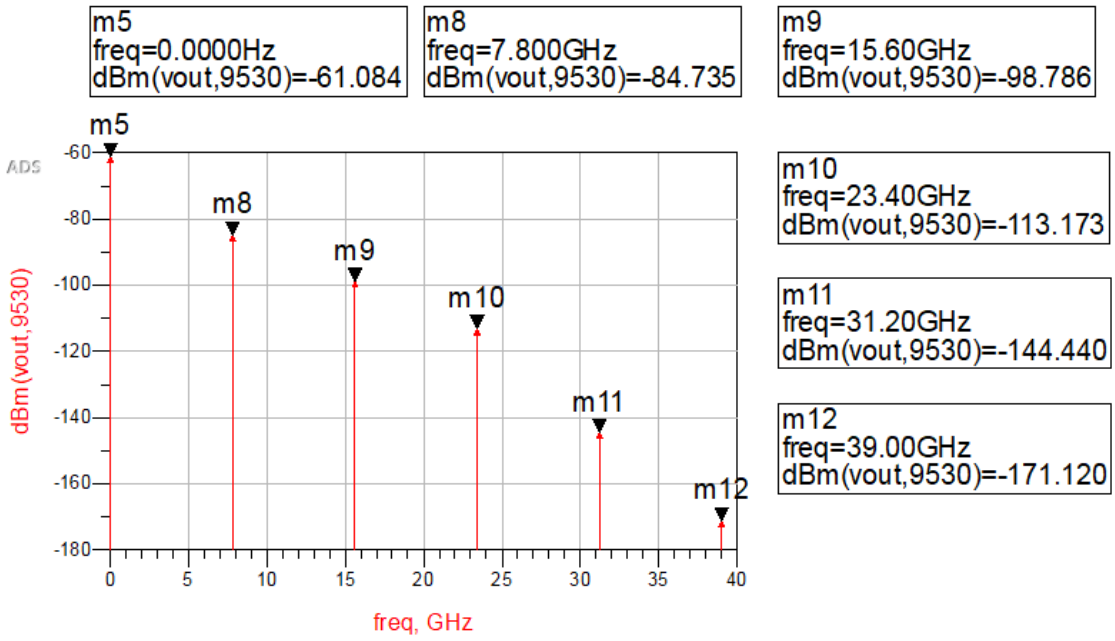

Fig.11. V_{out} in dBm vs frequency plot for detector

Fig.10 and Fig.11 show the variation of output voltage with frequency in different units of output

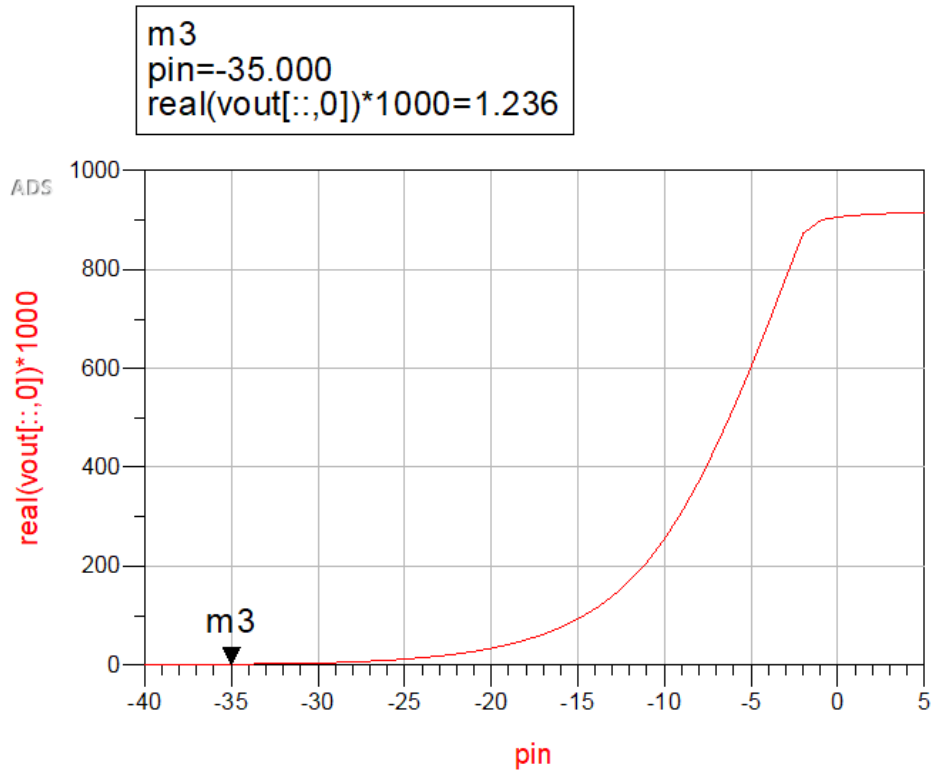

Fig.12. V_{out} (in absolute scale) vs input power plot for detector

voltage. The power fed to the detector is -40dBm via P_1 tone. From Fig. 11 it is clear that the DC output power is -61.084 dBm i.e. 21.084 dBm drop in power observed due to loss inside the structure. The 1st harmonic of V_{out} at 7.8 GHz is found to be -84.735 dBm and the successive harmonics are -98.786 dBm at 15.6 GHz, -113.173 dBm at 23.4 GHz, -144.440 dBm at 31.20 GHz and -171.12 dBm at 39 GHz respectively. Therefore, V_{out} follows a decreasing harmonic nature.

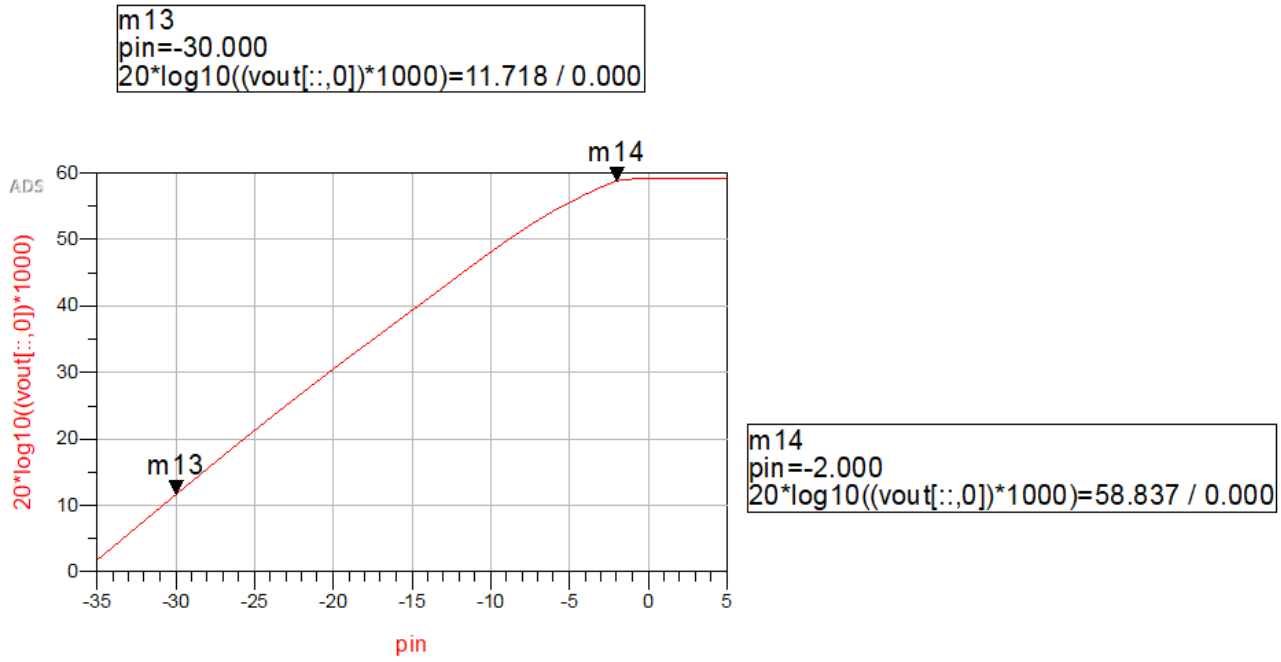

Fig.13. V_{out} (in log scale) vs input power plot for detector

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Fig.12 and Fig. 13 show the variation of output voltage with RF input power. It is clear from the figure that, the detector behaves as square law device. For input power of greater than -13 dBm to -2 dBm the diode is in linear region.

In the square law region, we have marked another point m_5 from which we can see the output voltage is 1.236 mV for an input power of -35 dBm. The target output power for the design of SBD Detector was 1 mV. Thus we can conclude that the Detector design satisfies the requirement and is a decent design for practical purpose.