DESIGN OF A MICROWAVE AMPLIFIER

- **Components:**
  - Metal: **Copper**
    - Conductivity: 58000000 Siemens/m
    - Relative Permittivity (εr): 1
  - Substrate: **Rogers RO4003C**
    - Relative Permittivity **(**εr): 3.55
    - Dielectric Loss Tangent ($tan\delta$): 0.0027
- **Design Specifications:**
  - Substrate Thickness = 0.508mm
  - Metal Thickness = 0.017mm
- **Design Criteria:**

  Operating Frequency: 7.8 GHz
- **Block Diagram**

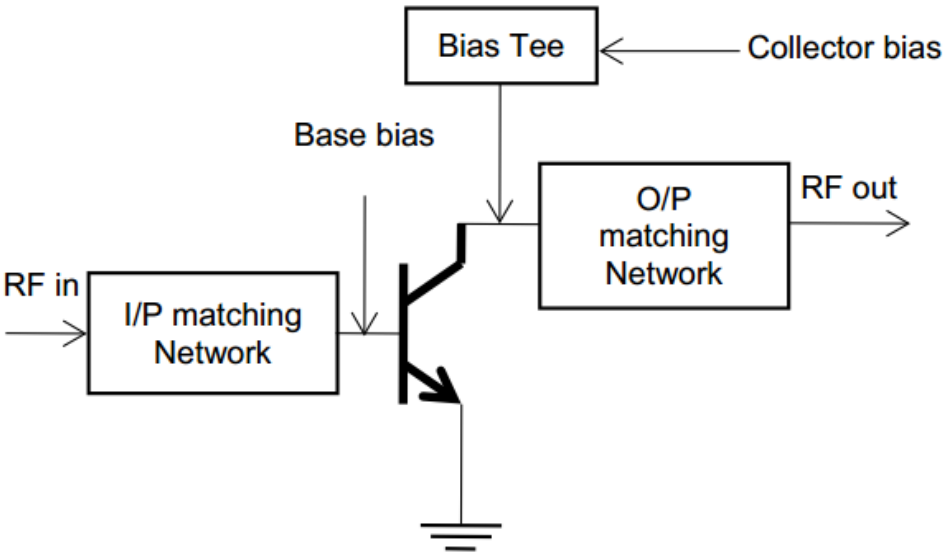


Fig. 1. Block diagram of the amplifier

Fig. 1 shows the complete block diagram of the amplifier. It consists of a BFU730F transistor, input and output matching network and bias tee network. Each individual component is designed and verified using ADS simulator and finally all components are connected to form the complete network.

➢ DC bias points of the amplifier:

If we assume that the amplifier is working as a linear amplifier in class A mode, then the first step of the design is to fix the dc Q point.

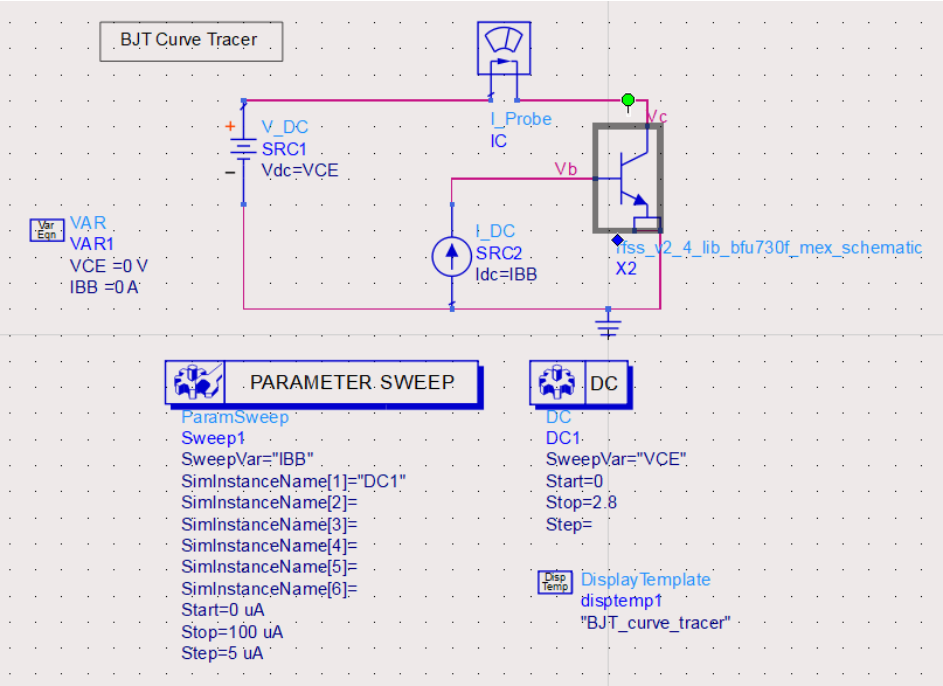


Fig. 2. DC bias circuit of the transistor amplifier

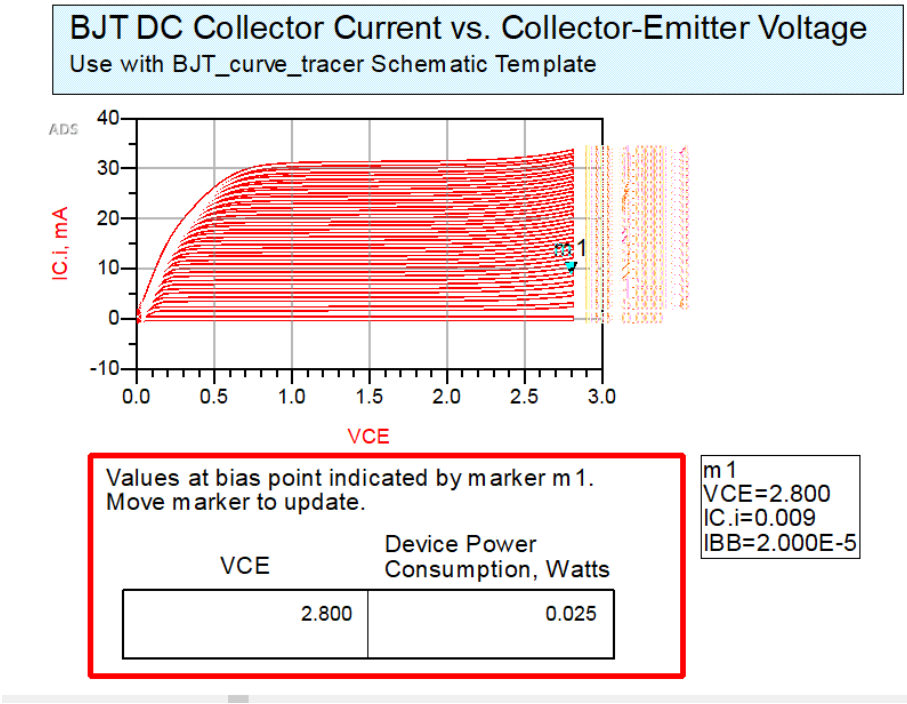


Fig. 3. Output characteristics of the transistor amplifier

Fig. 2 shows the circuit diagram of the DC bias of the transistor amplifier. Here NXP's BFU730F transistor has been used. This circuit is used to find the output characteristics and load line of the amplifier. The simulated results are shown in Fig. 3. For the given value of

collector current I_C (17 mA) the base current I_B and collector to emitter voltage V_{CE} are found to be 50.4 µA and 2 V respectively.

➢ **Design of bias network and verification of bias point values:**

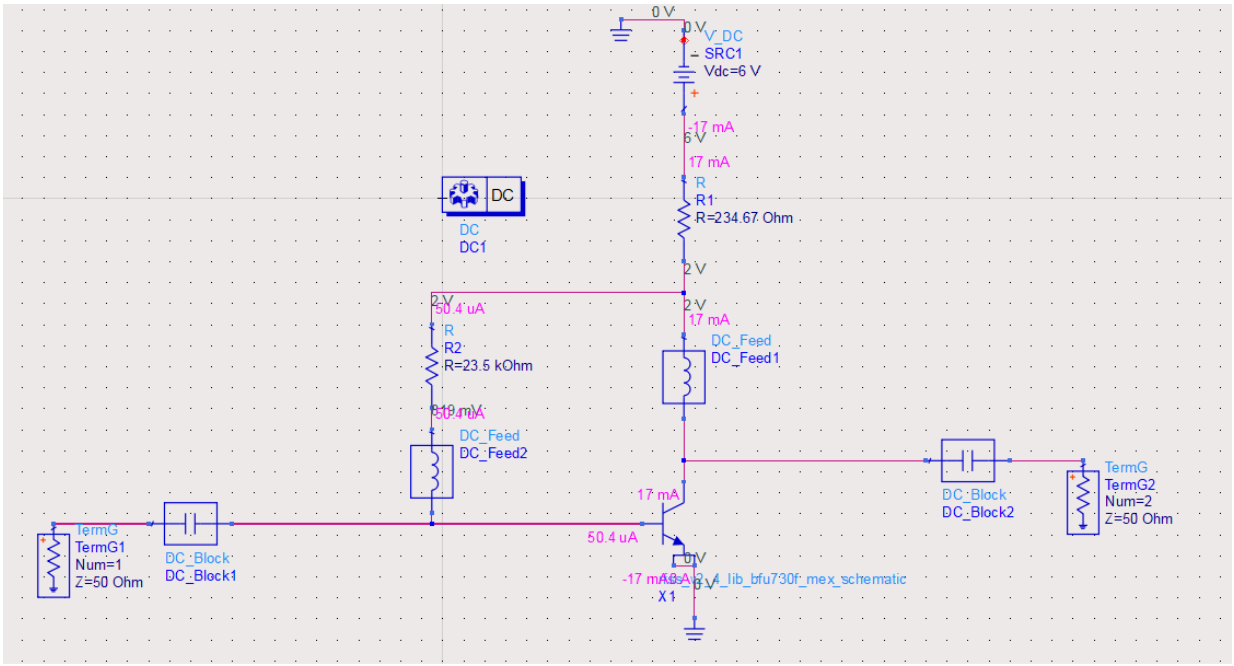


Fig. 4. Circuit to verify bias point values

Fig. 4 shows the circuit along with its bias point values. Here a bias tee is incorporated between collector of the transistor and DC source to isolates the DC source from RF input and output side. By changing the available values of R_C and R_B, the base current, collector current, and collector to emitter voltage have been optimized for the value that have been obtained as the DC bias point in the previous section. The closest possible value of I_B, I_C and V_{CE} are found to be 50.4 µA, 17mA, and 2V respectively for R_B = 23.5 kΩ and R_C = 234.67 Ω.

❑ **Stability analysis:**

In Fig. 5, along with the S-parameter setup, a load-stability and source stability circle and µ items are taken into the window from component palette to check the stability of the amplifier. The value of µ of the amplifier at 7.8 GHz is plotted in Fig. 6. For the amplifier to be unconditionally stable the value of µ should be greater than one. But here µ is found to be less than one. Therefore, the amplifier is not unconditionally stable. It is stable for a certain range of passive source and load impedances.

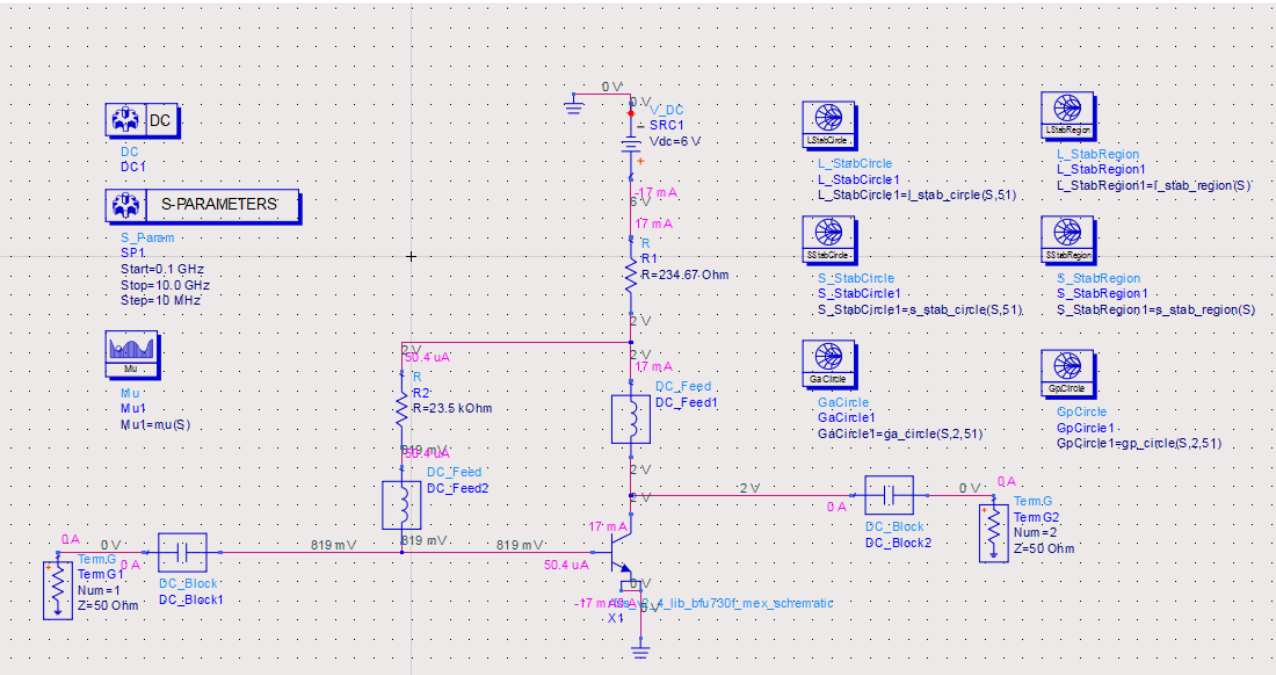


Fig. 5. Circuit to verify the stability of the amplifier

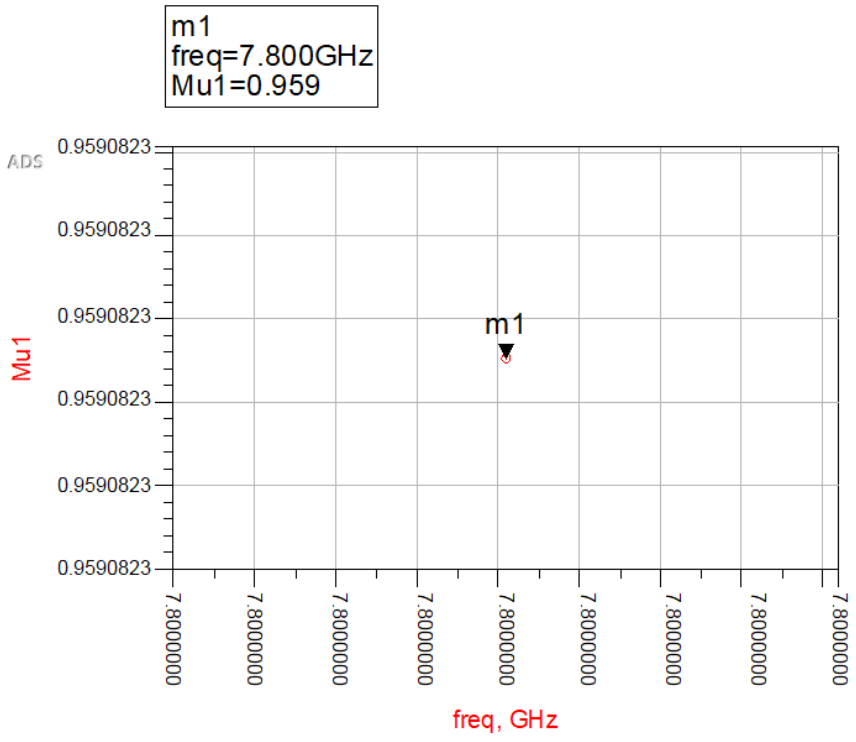


Fig. 6. Study of μ with frequency

The load and the source stability circle of the amplifier are shown in Fig. 7. It is clear from figure that the entire smith chart is not in stable region. Some portion of the smith chart is out of the stability region. Therefore, the amplifier is now conditionally stable. In order to make the amplifier unconditionally stable, stability network can be used:

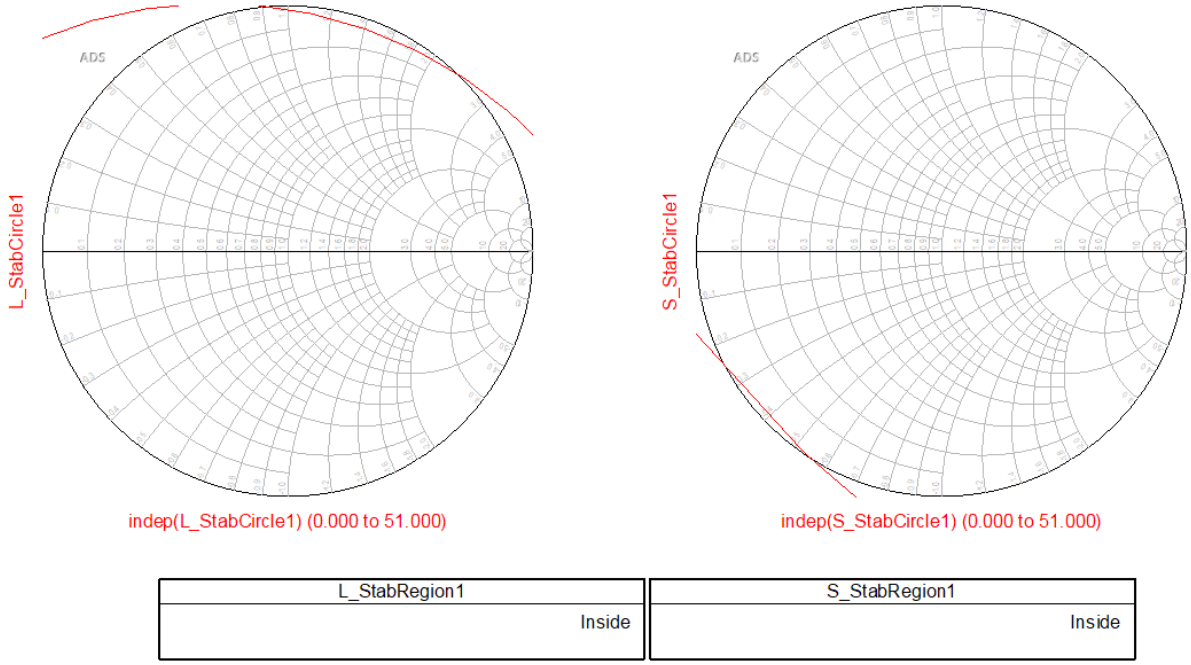


Fig. 7. Load and source stability circle of the amplifier

- **Design of Stability Network:**

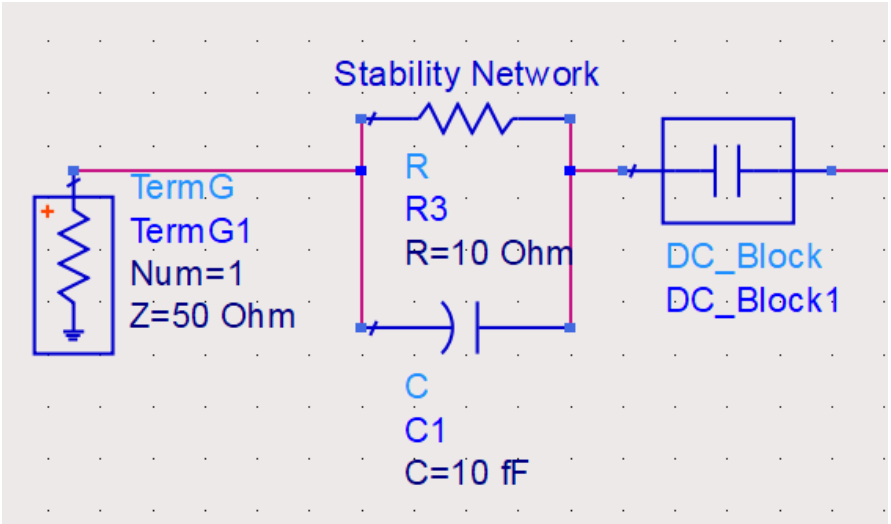


Fig. 8. Stability network of the amplifier

This can be achieved by using various combinations of series and shunt resistor and/or capacitor at the input or output side. An example is shown in Fig. 8, where a parallel *RC* combination is used in series with the source. In the circuit, *R* part damps the low frequency instability and the *C* part retains the gain in the high frequency stable region. The resistance of 10 Ω and the capacitor of 10fF are connected in parallel combination.

➢ **Schematic of circuit including the Stability Network:**

Fig. 9 shows the schematic diagram of the amplifier. The results obtained are discussed below.

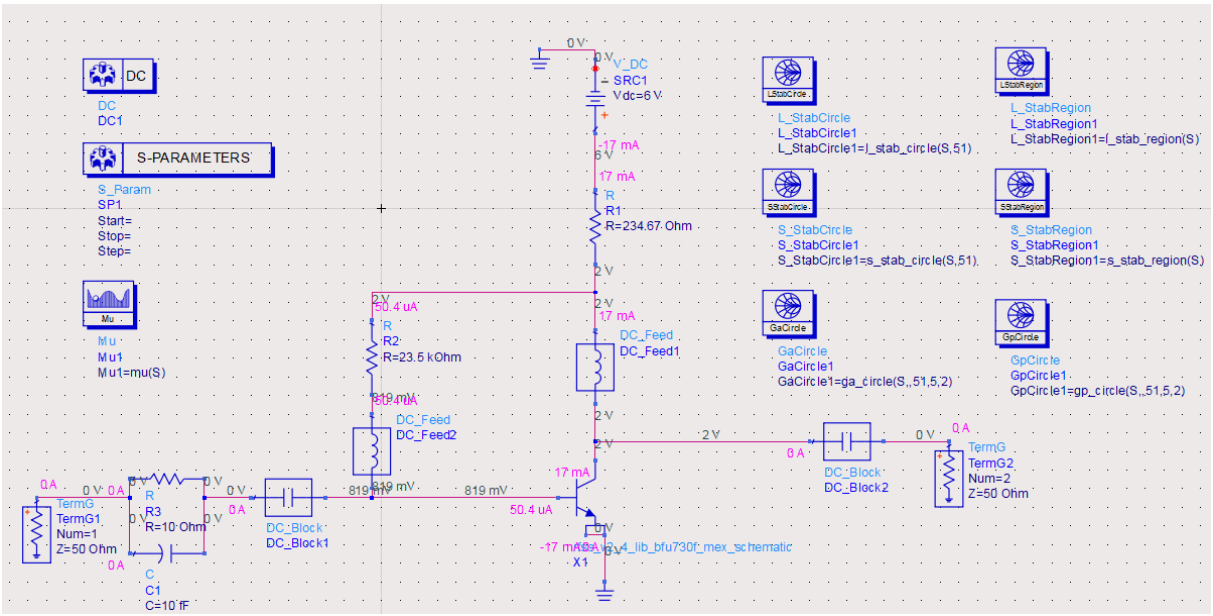


Fig. 9. Schematic diagram of the transistor with stability network of R3 and C1.

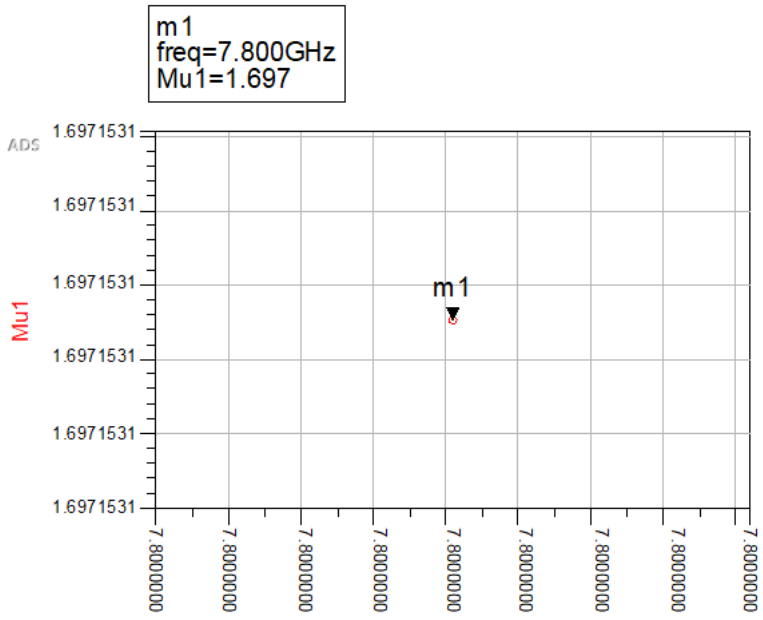


Fig. 10. μ vs frequency plot with stability network applied.

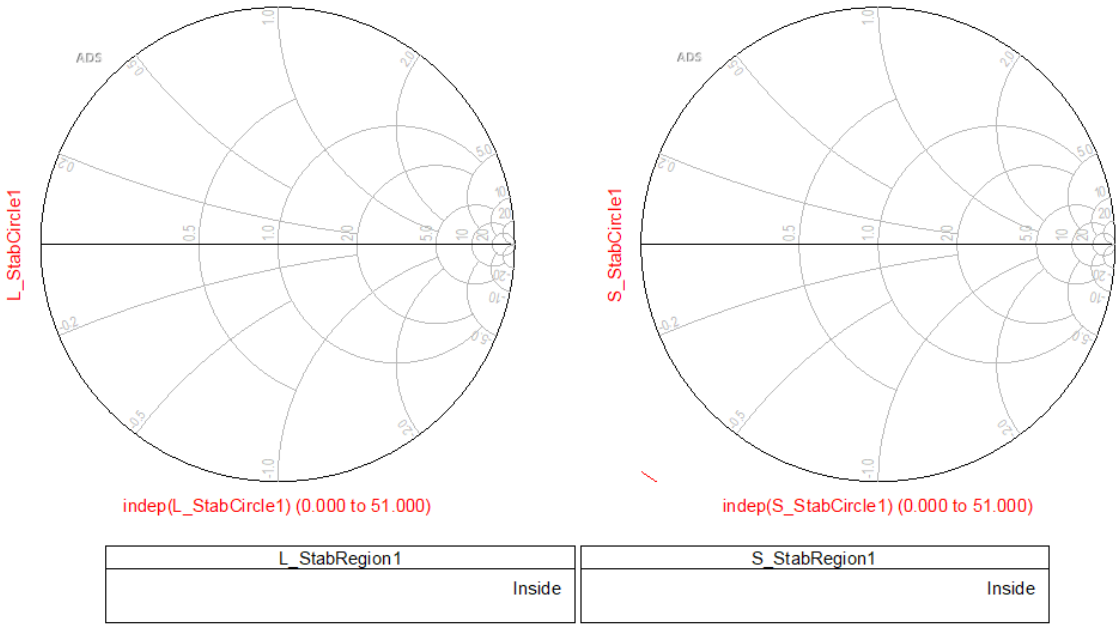


Fig. 11. Load and source stability circle of the amplifier

The value of μ and the stability circles are shown in Fig. 10 and Fig. 11 respectively. The value of μ is found to be 1.697 which indicates the amplifier is unconditionally stable. Looking at the load and the source stability circles in Fig. 11, we can see that the entire smith chart is in stable region.

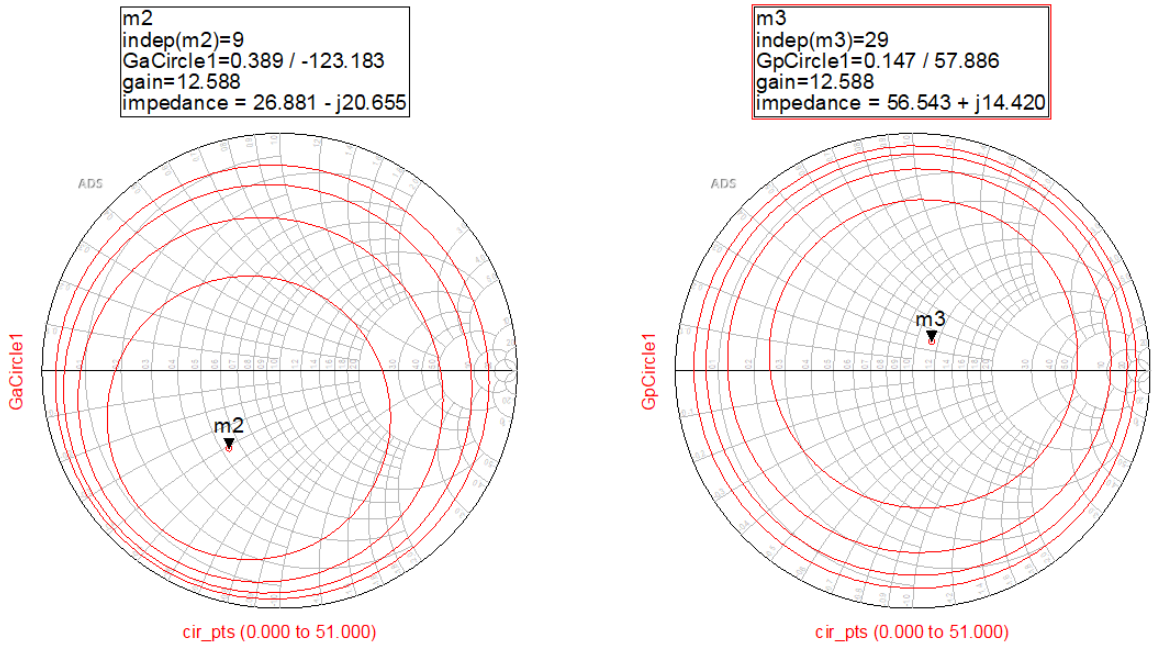


Fig. 12. Gain circles plot of the amplifier

The gain circles of the amplifier are plotted in Fig. 12. The maximum gain, as discussed earlier, is found to be 12.588. The load values for input and output matching network are found to be (26.881-j20.655) Ω and (56.543+j14.420) Ω respectively.

❑ Design of input and output matching networks:

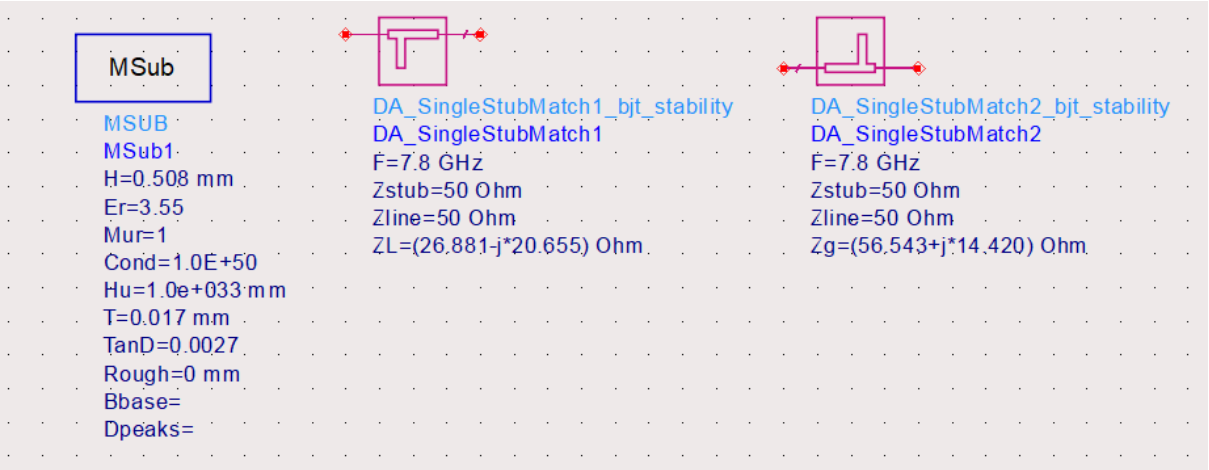
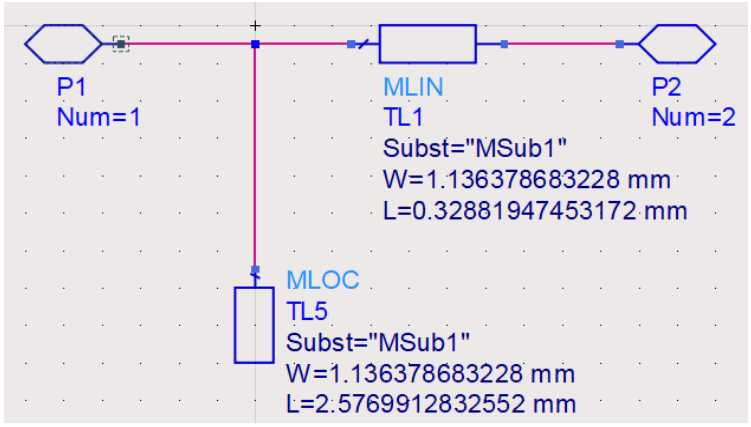
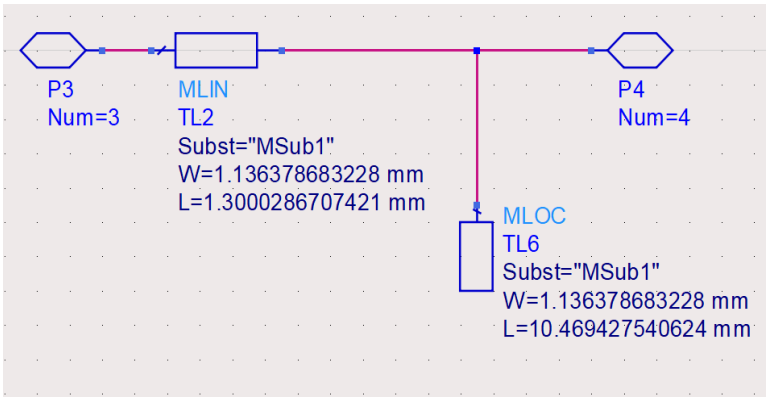


Fig. 13. Input and output matching networks in smart component form

The input and output matching networks are now designed for the load values obtained from the gain circles. Fig. 13 shows the input and the output matching networks in the smart



(a)



(b)

Fig. 14. Schematic of (a) input matching network (b) output matching network

component form. The schematic view of the input and output matching networks along with the dimensions are shown in Fig. 14.

❑ Design of complete amplifier circuit:

Fig. 15 shows the complete amplifier circuit with the matching circuits at the input and at the output sides. For the maximum gain of the a plifier, the matching networks are optimized further and the S-parameters, stability and gai of the final design are studied.

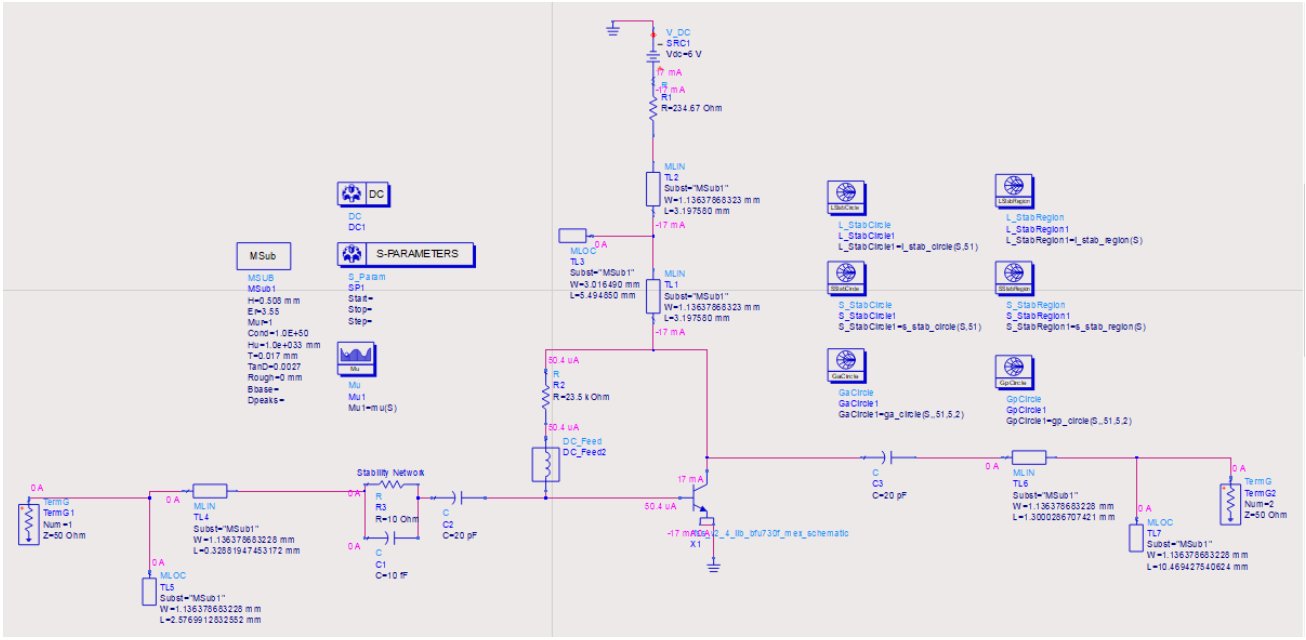


Fig. 15. Complete amplifier circuit

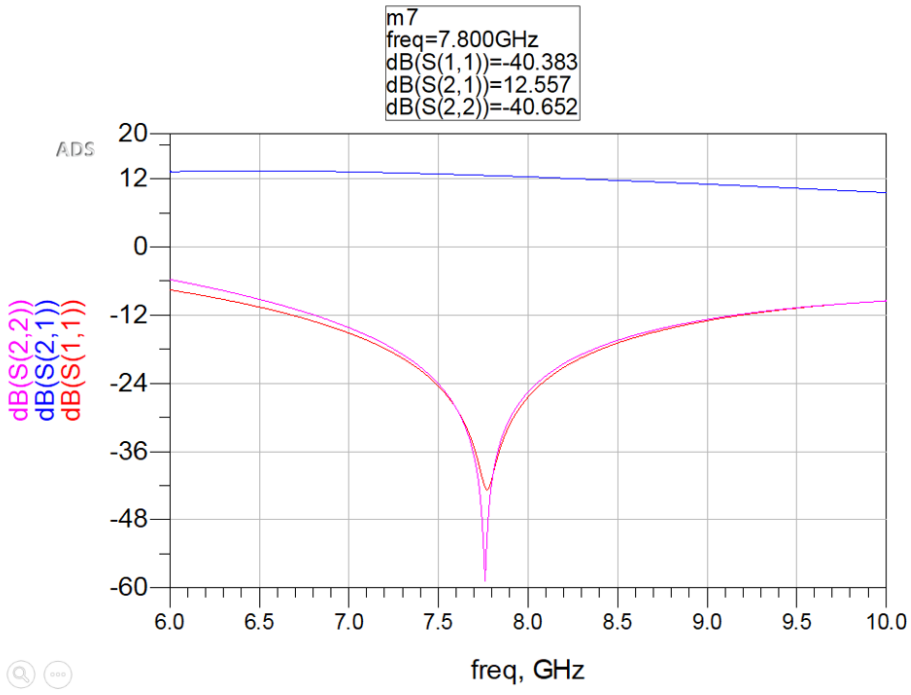


Fig. 16. S-parameters vs frequency plot of the amplifier

The S-parameters vs frequency plot of the final amplifier is shown in Fig. 16. A good impedance matching at 7.8 GHz along with 12.557 dB of S21 value is seen.

Fig. 17 studies the μ vs frequency plot. A value of μ approximately 1.08 at 4.1 GHz ensures the amplifier to be unconditionally stable.

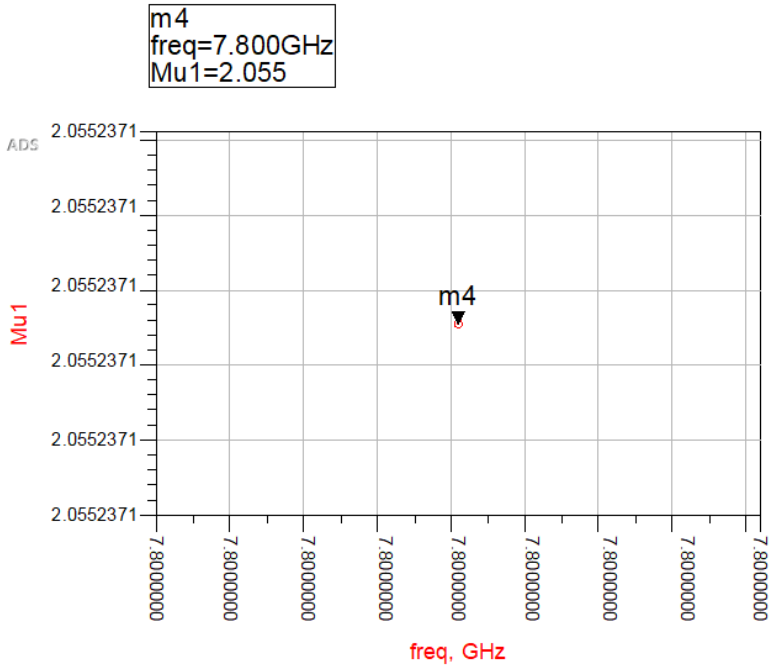


Fig. 17. μ vs frequency plot of the amplifier

The stability region of the amplifier is studied in Fig. 18. Both of the load and source stability circle encircles the entire smith chart and the stability is inside the circles. Therefore, the entire smith chart is in stable region.

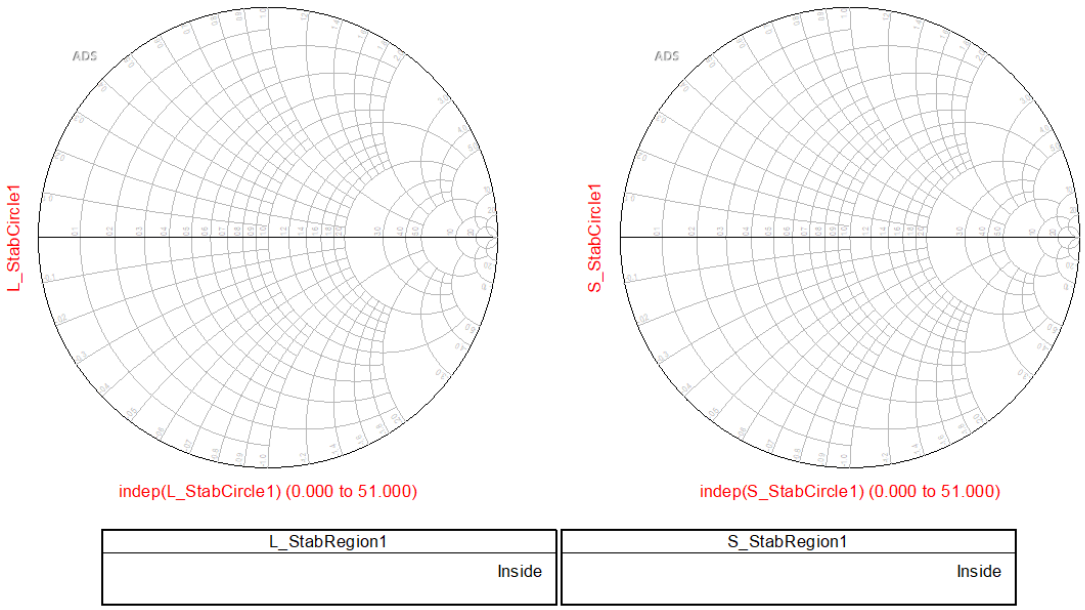


Fig. 18. Load and source stability circle of the amplifier

The final gain of the amplifier after the optimization for maximum gain is found to be 12.129 as shown in Fig. 19.

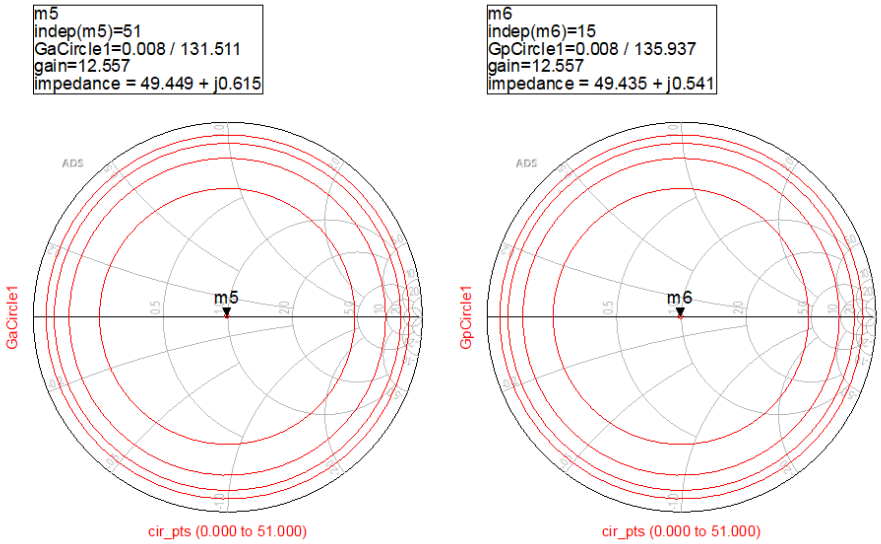


Fig. 19. Gain circles plot of the amplifier

❑ Layout Design:

In order to realize the practical view of the final amplifier, the schematic is transformed to layout. A systematic process containing various steps are followed which are mentioned below:

- The footprint of the transistor is generated
- A routing line is incorporated to connect the base resistor between base and collector of the transistor.
- The schematic of the bias tee is replaced with its layout.
- The schematic of the input and output matching networks are replaced by their respective layouts.

To minimize any error, the results are verified after each step. The final layout of the amplifier is shown in Fig. 20. The results obtained are discussed below.

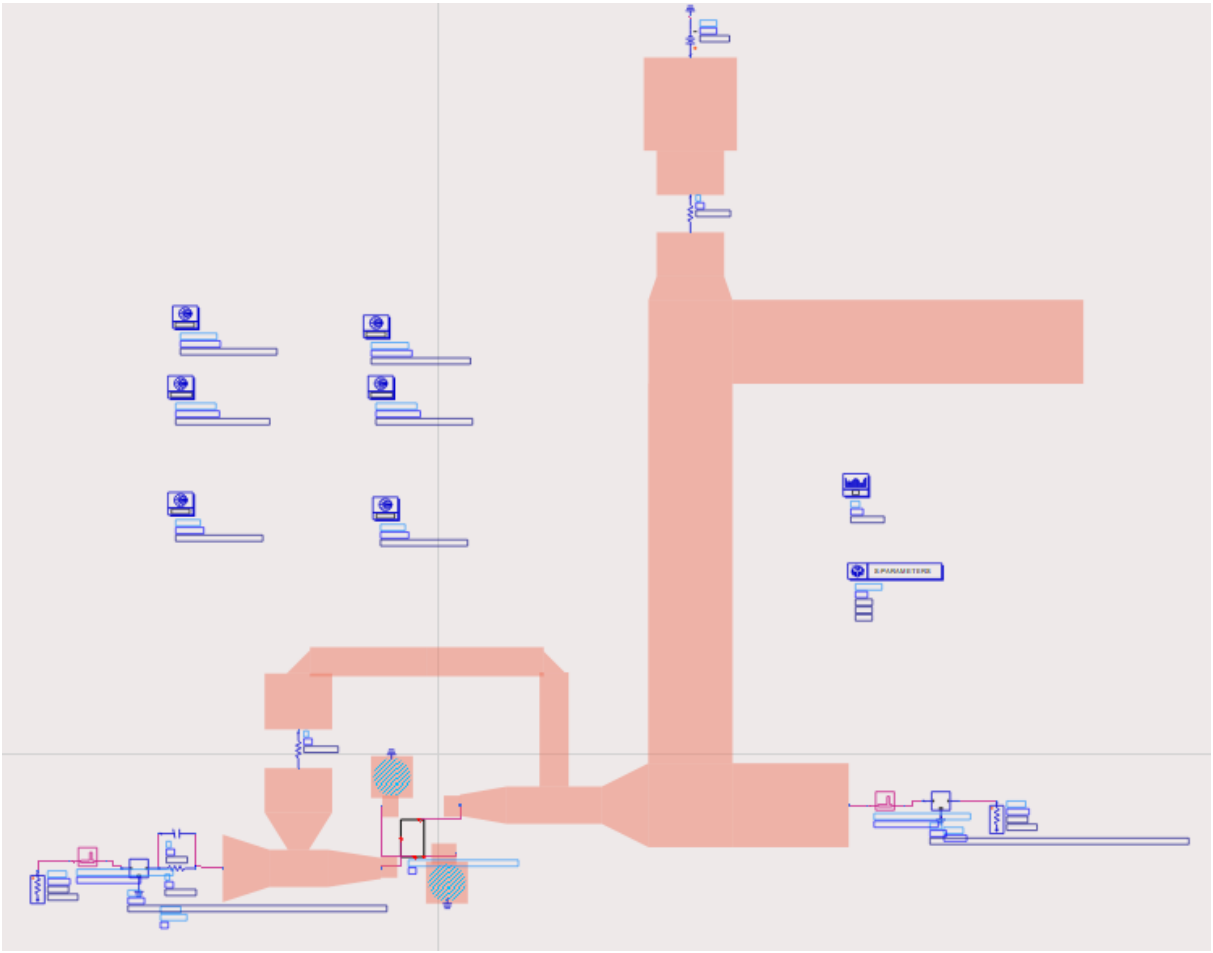


Fig. 20. Final layout of the amplifier

The S-parameters vs frequency plot of the amplifier is shown in Fig. 21. The input and output reflection coefficients are found to be below - 20 dB. The value of the transmission coefficient is found to be 10.382 dB which ensures good amplifier performance.

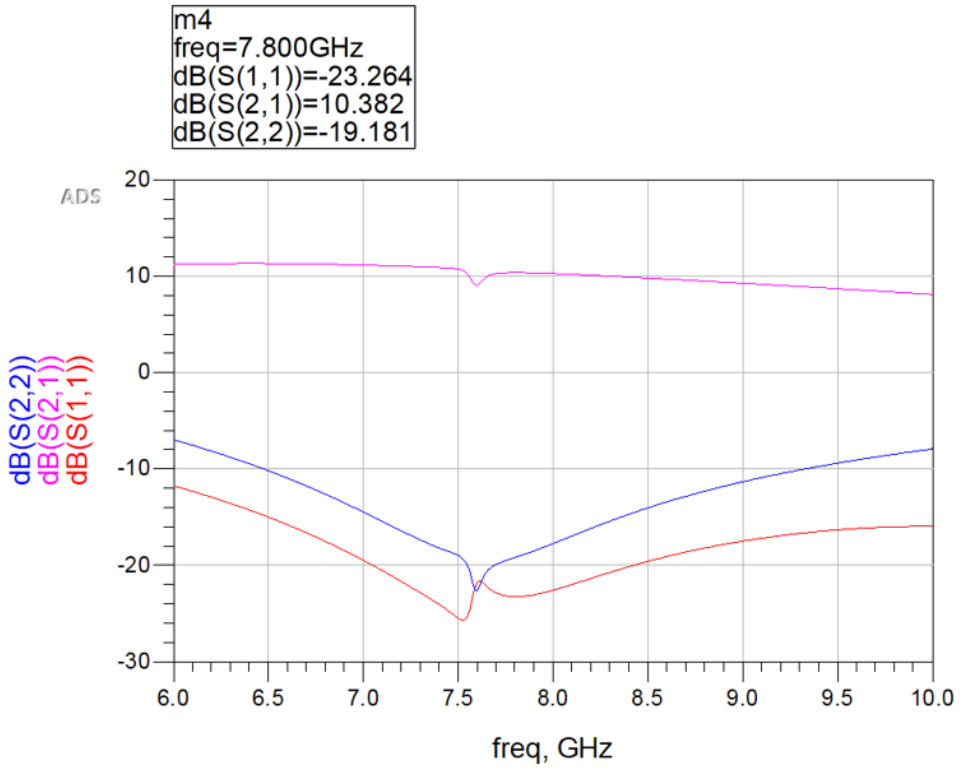


Fig. 21. S-parameters vs frequency plot of the amplifier layout

The stability of the amplifier is ensured by plotting μ at the operating frequency in Fig. 22. The value is found to be 1.349 indicating the amplifier to be unconditionally stable.

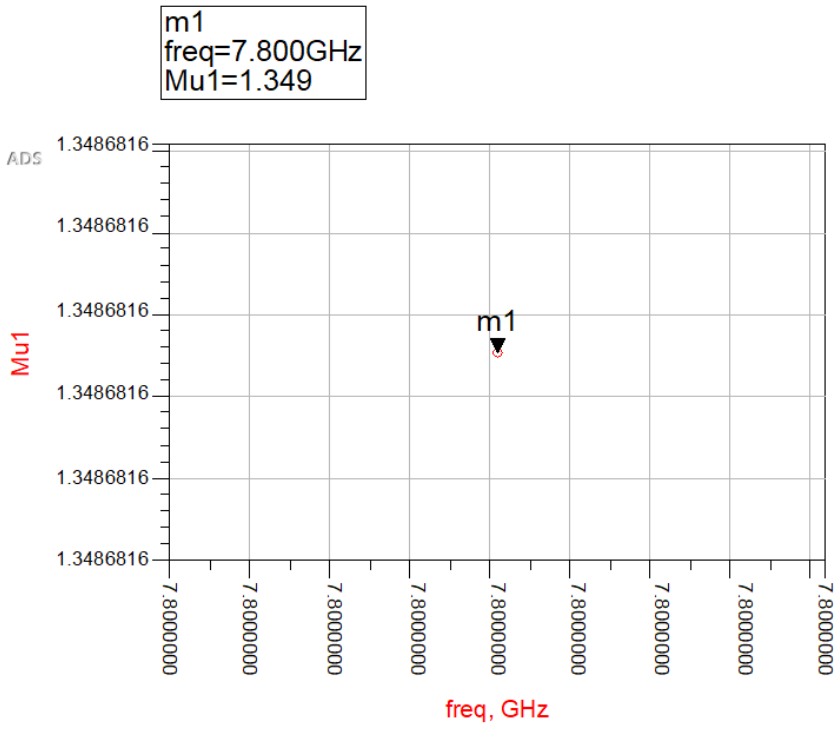


Fig. 22. μ vs frequency plot of the amplifier

The stability region of the amplifier is studied in Fig. 23. The figure is self-explanatory which indicates the entire smith chart is in stable region.

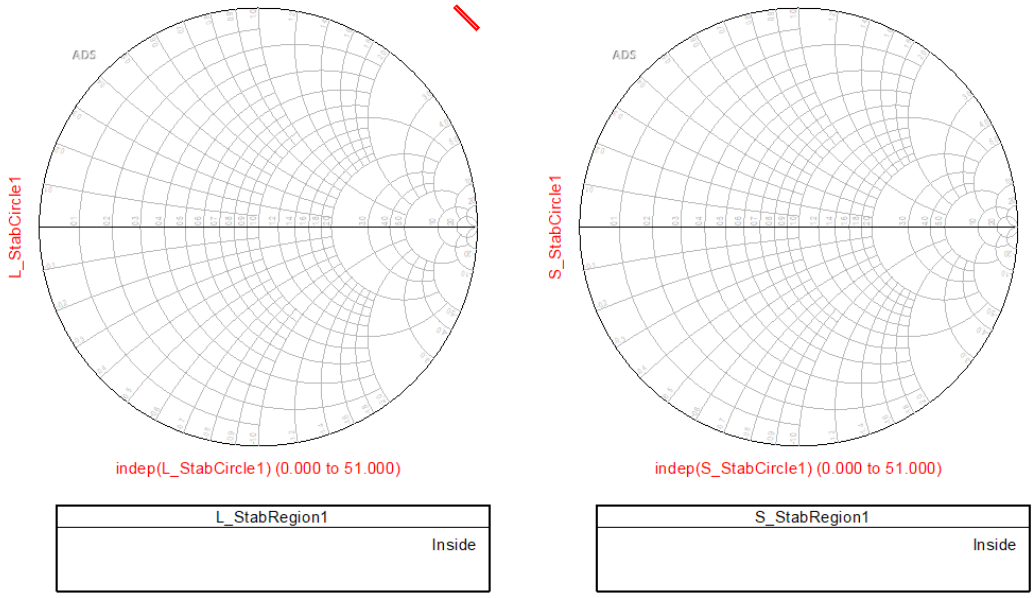


Fig. 23. Load and source stability circle of the amplifier

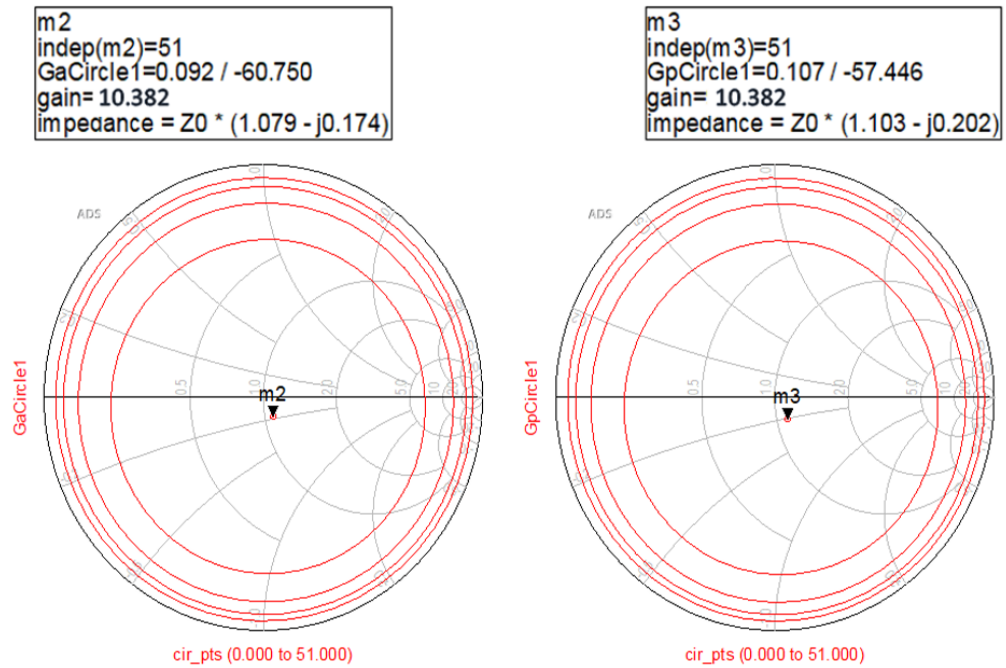


Fig. 24. Gain circles plot of the amplifier

The final gain of the amplifier layout is found to be 10.382 as shown in Fig. 24. The gain of the amplifier was 12.557 in the schematic design. The reduction in gain might be due to loss in the transmission lines and the interconnections of the layout and the coupling effects of the nearby strips.