DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY,
LONERE, RAIGAD-402103.
Mid-Term Test Examination-2017

Department: Computer Engineering **Sem:III**

Subject: Computer Organization and Architecture(CE303) **Marks:20**

Date: 04/10/17 **Time:2:30 to 3:30 (1 hour)**

Instructions:

All Questions are compulsory.

Each subquestion in Q:1) carries equal marks.

Q :1) Write the answers of the following: **(16 Marks)**

i) Do RISC instructions work on the CISC processor? Justify your answer.

ii) Give a short sequence of machine instructions for the task: " Add the contents of memory location A to those of location B, and place the answer in location C."
Instructions Load LOC, R_i and Store R_i, LOC are the only instructions available to transfer data between the memory and the general purpose register R_i.

iii) When data are received from or delivered to a device that is directly connected to the computer, What is the name of the process and device?

iv) Which factor is responsible for the great increase in processor speed? What does it do to increase the processor speed?

v) How does overflow rule differs with subtraction rule?

vi) In a typical 32-bits floating point format, What does the leftmost bit store? Give the neme of the representation?

vii) Suppose the instruction set architecture of the processor has only two registers. The only allowed compiler optimization is code motion, which moves statements from one place to another while preserving correctness. What is the minimum number of spills to memory in the compiled code?

viii) Consider a cache with a line size of 32 bytes and a main memory that requires 30 ns to transfer a 4 byte word. For any line that is written at least ones before being swapped out of the cache, what is the average number of times that the line must be written before being swapped out for a write-back cache to be more efficient that a write-through cache?

Q:2) a) Suppose that the processor has access to two levels of memory. Level 1 contains 1000 words and has an access time of 0.01 microseconds; level 2 contains 1,00,000 words and has an access time of 0.1 microseconds. Assume that if a word to be accessed in level 1, then the processor accesses it directly. If it is in level 2, then the word is first transferred to level 1 and then accessed by the processor. Suppose 95% of the memory accesses are found in the cache. Then, what should be the average time to access a word? **(2 marks)**

b) How is redundancy achieved in RAID system? **(2 marks)**