Design and Analysis of a Quadrature Downconverter

Anuj Kumar Tiwari, Nav Singhal, Ravi Kumar Sahu
International Institute of Information Technology, Hyderabad, India
{anuj.tiwari, nav.singhal, ravi.sahu}@students.iiit.ac.in

***Abstract*—Quadrature downconversion is a fundamental process in modern communication systems, enabling the separation of in-phase and quadrature-phase components, I and Q respectively, of a received RF signal. This paper presents the design, simulation, and performance analysis of a quadrature downconverter, focusing on designing the Quadrature Oscillator, the Frequency Mixer and the Low Pass Filter. We discuss the design process behind these components and their integration with each other.**

***Index Terms*—Quadrature downconversion, RF receiver, in-phase, quadrature-phase, noise performance, mixer, low pass filter**

I. Introduction

Quadrature downconversion is the process of translating a high-frequency RF signal to baseband by mixing the input with two orthogonal (sine and cosine) local-oscillator waveforms shifted by $90°$, yielding separate in-phase (I) and quadrature (Q) components for demodulation.

In this report, we present the design, simulation and analysis of a quadrature downconverter implemented in LTSpice.

We show the follow system designs and their integration to form a quadrature downconverter

- A low-phase-error quadrature oscillator that produces a 100 kHz Sine and Cosine wave ($90°$ phase shift)
- A passive-mixer topology using an NMOS device biased in the linear region, achieving minimal waveform distortion and low information loss.
- A second-order low-pass filter designed for a 2 kHz bandwidth, with component values chosen for standard manufacturing tolerances and processes.

Through Frequency Response Analysis (FRA) Plots, Transient Simulation Plots and Fast Fourier Transform (FFT) Plots.

The rest of this paper is outlined as follows. Section II reviews the theoretical background of quadrature mixing and signal representation. Section III details the system level design and LTSpice implementation of the quadrature oscillator, mixer, and filter. Finally, Section IV presents combined simulation results and performance metrics.

II. Theory and Background

A. Quadrature Downconversion Overview

Quadrature downconversion is a signal processing technique that is used to shift a high frequency radio signal (passband signal) to a lower complex baseband signal. This allows for easier post processing later on and mitigates effects such as aliasing when we pass the signal through an ADC (Analog to Digital Converter).

We achieve this by mixing (in a mathematical sense, multiplying) the RF signal and a LO (Local Oscillator) signal. This gives us 2 new frequency components which we call the in-phase component and the quadrature-phase component [1].

These signals are then filtered through an LPF to remove the high frequency terms and allow only the difference frequency terms ($f_{RF} - f_{LO}$) that carry the original wave and phase information at baseband.

Since the output signals are at a $90°$ phase difference, we can represent the complex analysis of the original RF signal in terms of these 2 newly obtained output signals. One wave would represent the real component of the original RF signal, and the other would represent the imaginary component.

III. System Design

A. Overall Block Diagram

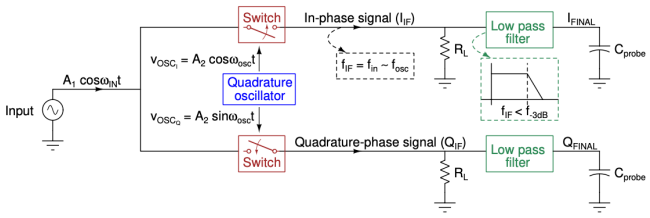

Fig. 1. Quadrature Downconverter Block Diagram

We use the block diagram in Fig. 1 to design and characterize our quadrature downconverter. Our quadrature oscillator provides 2 sinusoidal signals, with a phase difference of $90°$ between them. The switch is our NMOS, which acts as our mixer; the mixer multiplies the input signal and the LO wave, giving us 2 new waves as seen in the below equations.

$$v_{\text{IF}_I} = v_{\text{in}} \times v_{\text{OSC}_I}$$

$$= \frac{A_1 A_2}{2} \left[\cos(\omega_{\text{in}} t - \omega_{\text{OSC}} t) + \cos(\omega_{\text{in}} t + \omega_{\text{OSC}} t)\right]$$

$$v_{\text{IF}_Q} = v_{\text{in}} \times v_{\text{OSC}_Q}$$

$$= \frac{A_1 A_2}{2} \left[\sin(\omega_{\text{in}} t + \omega_{\text{OSC}} t) - \sin(\omega_{\text{in}} t - \omega_{\text{OSC}} t)\right]$$

We can see that we now have a higher contribution of 2 new frequencies in our frequency spectra, that is, $w_{in} + w_{OSC}$

and $w_{in} - w_{OSC}$. Since we only want the lower frequency component of our spectra, we use a LPF (Low Pass Filter) to allow only the $w_{in} - w_{OSC}$ frequency component to pass through. Hence we are able to reduce the MHz to GHz frequency of RF waves to a much lower kHz range while retaining waveform and phase information.

B. Quadrature Oscillator Design

1) Design Process: As per the datasheet [2], [3], the UA741 needs a 2V padding from both the rails. The UA741 also has a max slew rate of 0.5 Vμs^{-1}, for a frequency of 100 kHz and a 1 Vpp output, we can achieve a max peak voltage of,

$$2\pi f V p$$
$$= 2\pi \times 10^5 \times 0.5$$
$$= 0.314 \text{ V}\mu s^{-1}$$

As we can see, the required slew rate we need is below the max slew rate of the UA741, so we should not observe any distortion. We also bias the op-amp at mid rail since we want maximum voltage swing. If we consider the positive rails of +5V or 0V, then our op-amp can take values from 2-3 V; if we bias our op-amp at 2.5V, we can have a maximum signal output of 1 Vpp, which satisfies our output criteria [4], [5].

We also run into an issue with regards to the frequency, this is because the UA741 adds extra phase lag due to the finite open gain, the extra phase lag is given by $\Delta\phi = \arctan(\frac{f_\tau}{f_B})$ where f_τ is the oscillation frequency for which it is designed and f_B is the bandwidth, which is 1 MHz in the case of the UA741. [2]

There is something called the Barkhausen criteria [6] that necessitates the phase difference due to this lag to be 0. Since we pass this through 2 op amp integrators, we see a phase lag of $2\Delta\phi$; hence for the op-amp to maintain unity gain, it reduces the oscillation wave frequency. So we have to increase the cutoff frequency.

We initially choose the frequency values as per the gain equations given below, [3]

$$A\beta = \left(\frac{1}{R_1 C_1 s}\right)\left(\frac{R_3 C_3 s + 1}{R_3 C_3 s(R_2 C_2 s + 1)}\right)$$

When $R_1C_1 = R_2C_2 = R_3C_3$, this simplifies to,

$$A\beta = \frac{1}{(RCs)^2}$$

For oscillations to occur, the condition is that $s = j\omega$, and at the frequency where $\omega = \frac{1}{RC}$, the loop gain reaches 1 with a phase shift of $-180°$. *Note that β is the "feedback factor", but we will ignore its discussion as it exceeds the scope of this report*

So initially, for a frequency of 100 kHz we took a resistor with a value of 1.6 $k\Omega$ and a capacitor of value equal to 1 nF, however, on simulation we appear to get an oscillation frequency of 70 kHz. This is because of the reasons mentioned above. On manually increasing R and C, we get the theoretical cutoff frequency to be $\approx$ 270 kHz, which gives us a frequency of 100 kHz on simulating in LTSPICE.

Taking all of these into consideration, we come up with the circuit schematic as shown in Fig. 2.

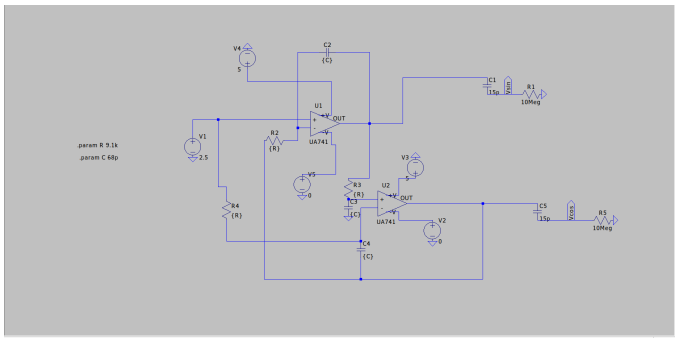

Fig. 2. Quadrature Oscillator Schematic

2) LTSpice Simulation of Quadrature Oscillator: In Fig. 3 we can see that the in-phase voltage is around 1 Vpp which is nearly the same as the quadrature-phase component voltage. A slight deviation can be expected due to higher order circuit parameters and their associated equations.

In Fig. 4 we can see the FFT Plot for our Quadrature Downconverter and observe that the peak is at 99.92 kHz. Once again we can attribute a slight decrease due to LTSpice simulating parasitic capacitance and other internal factors. This is however within our $\pm 5\%$ tolerance and hence is acceptable.

From, Fig. 5 we can see that the time delay between the 2 waves when they reach an amplitude of 0 is,

$$\Delta t = 2.511\mu s$$

We note that the time period of the wave is,

$$T = \frac{1}{f} \implies \frac{1}{100 \times 10^3} \implies 10\,\mu s$$

The phase difference is given by,

$$\Delta\phi = \frac{\Delta t}{T} \times 360°$$
$$= \frac{2.511\mu s}{10\mu s} \times 360°$$
$$\approx 90.396°$$

From these figures and their associated equations, we can infer that we do in fact get 2 waves, a Sine wave and a Cosine wave, with a maximum amplitude of 1 Vpp and a frequency of approximately 100 kHz.

C. Frequency Mixer Design

1) Design Process: What we want the mixer to do is essentially mix different voltage signals, that is, multiply them together so we can combine/encode one signal into the other. Note that multiplication in the time domain results in convolution in the frequency domain [7], [8].

So we need to find a device that is able to,

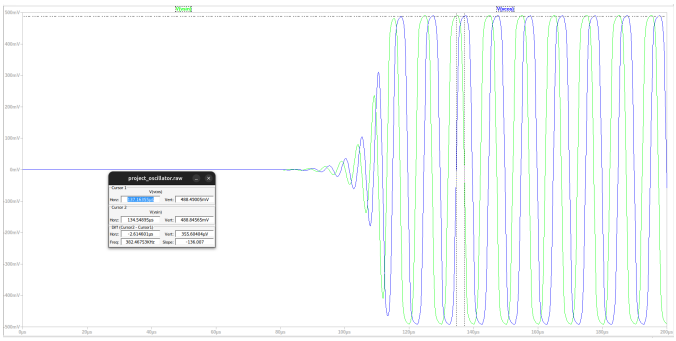

Fig. 3. Quadrature Oscillator Waveforms

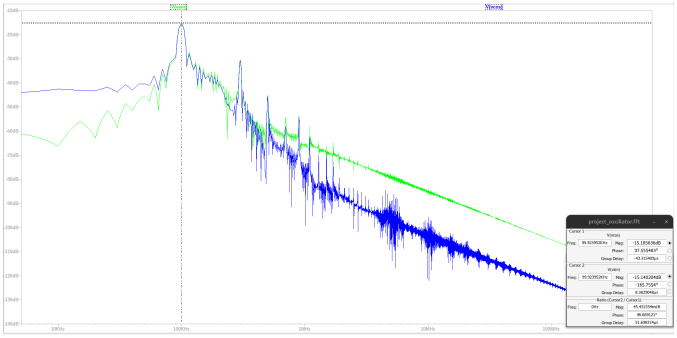

Fig. 4. Quadrature Oscillator Spectrum

- Produce a function that is a product of 2 different voltage sources
- Does not modify the signal waveform or phase information

Conveniently, the NMOS transistor biased in the linear region fits our needs perfectly. As we know, the drain current for an NMOS acting in the linear region is [5],

$$i_d = \mu_n C_{ox} \frac{W}{L} V_{DS}((V_{GS} - V_{th}) - \frac{V_{DS}}{2})$$

where, $\mu_n C_{ox}$ is a process defined parameter, $\frac{W}{L}$ is a circuit designer defined parameter, V_{DS} is the voltage across the Drain with respect to the Source, V_{GS} is the voltage across the Gate with respect to the Source, and V_{th} is the Threshold Voltage of the NMOS.

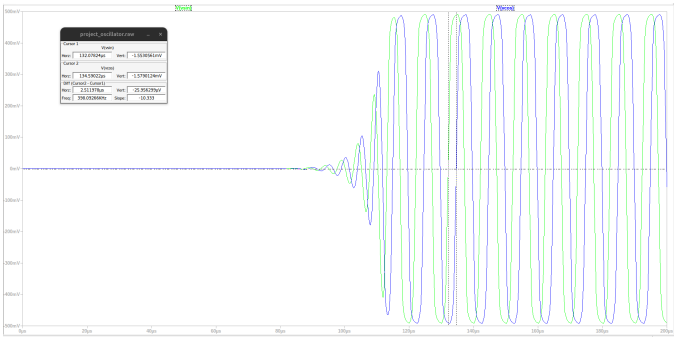

Fig. 5. Quadrature Oscillator Phase Shift

From this, we can see that we are able to get a function which has the product of 2 different voltage sources, which is one of our major requirements.

Another thing we see is that in the linear region, there is no amplification of any sort. The NMOS behaves as a voltage controlled resistor, so we see no change in the waveform as well as no alteration in the phase information. This satisfies our second major requirement.

We move onto building our mixer circuit, we need to provide 3 voltage sources,

- A bias voltage for biasing the NMOS in the linear region (V_{BIAS})
- We need a voltage source for representing the Local Oscillator Signal (V_{OSC})
- We need a voltage source for representing the RF Signal that we are inputting into the quadrature downconverter (V_{IN})

We also need a load resistor so that we can convert our current function into a voltage function, that is,

$$V_{out} = i_d \times R_L$$

We also would like to have a high pass filter present from the view of the V_{OSC} so as to only allow the high frequency elements of our local oscillator to pass through. This is done so we don't attenuate the signal later on through our low pass filters near the downconverter output [4], [5].

Similarly, we would like to have a low pass filter to be present so as to only allow the DC component to pass through. This is done to prevent the reduced voltage swing that would occur if there were a higher frequency component.

Taking all of these into consideration, we come up with the circuit design in Fig. 6

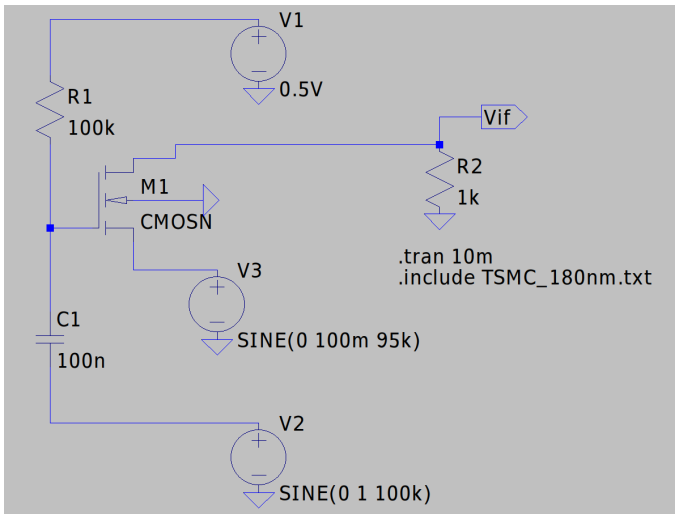

Fig. 6. Mixer Circuit Schematic

From the viewpoint of V_{OSC}, the capacitor is in series and the resistor appears to be in parallel with the load (NMOS), hence it acts as a high-pass filter.

From the viewpoint of V_{BIAS}, the resistor is in series and the capacitor appears to be in parallel with the load (NMOS), hence it acts as a low pass filter.

We keep the capacitor at 100 nF and the resistor at 100 $k\Omega$. This provides us with a time constant of 10 ms, which implies a settling time of around 50 ms. This is very good for our use case and the cutoff frequency is $\approx$ 157.07 Hz.

2) LTSpice Simulation of Mixer Stage: In Figs. 7 to 12, we see the transient responses for input frequencies 95 kHz, 98 kHz, 99 kHz, 101 kHz, 102 kHz, and 105 kHz. The corresponding frequency spectra obtained from the FFT analysis are shown in Figs. 13 to 18.

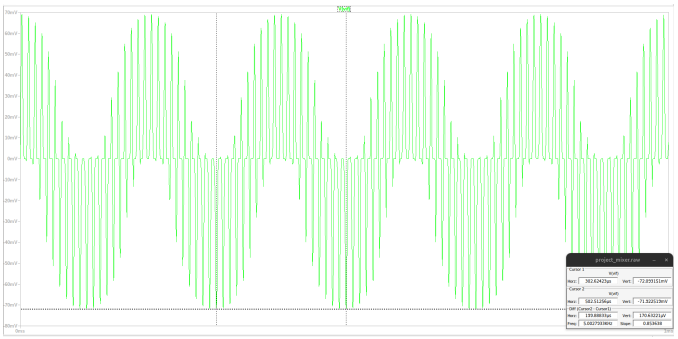

Fig. 7. Transient Response at 95 kHz

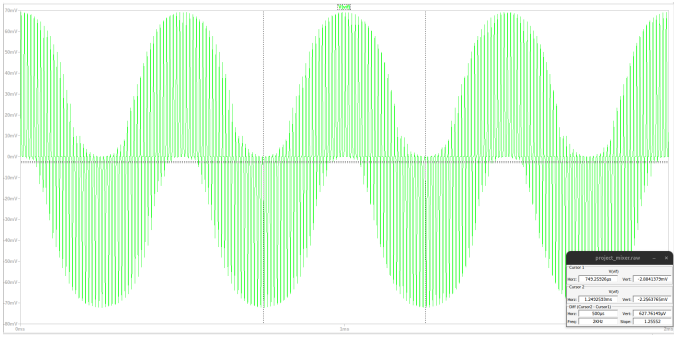

Fig. 8. Transient Response at 98 kHz

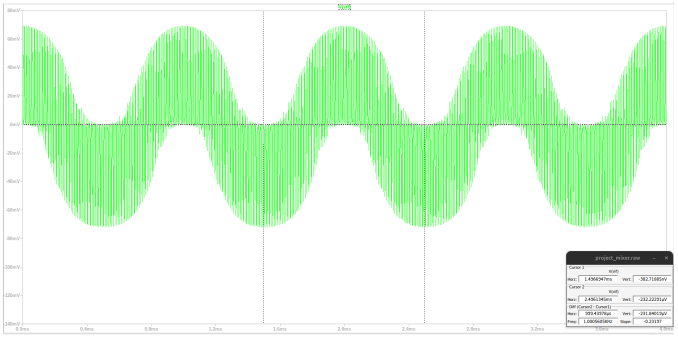

Fig. 9. Transient Response at 99 kHz

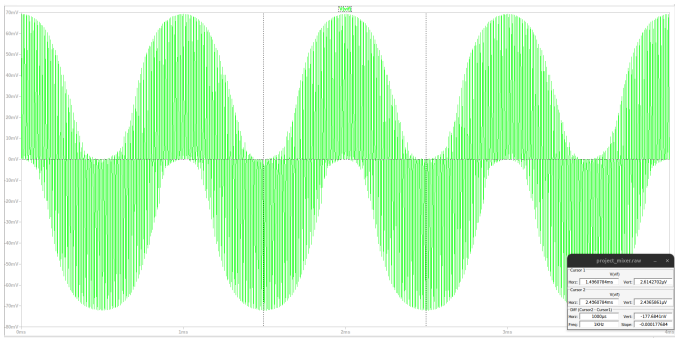

Fig. 10. Transient Response at 101 kHz

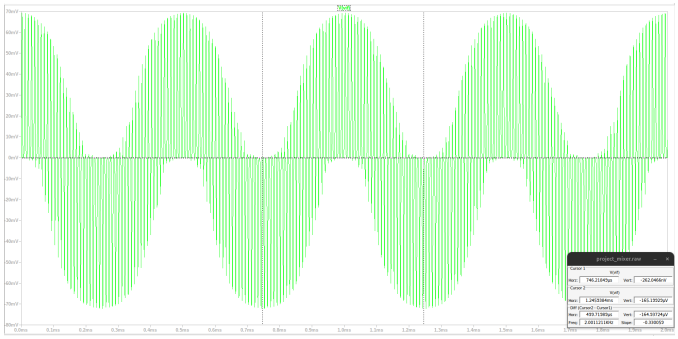

Fig. 11. Transient Response at 102 kHz

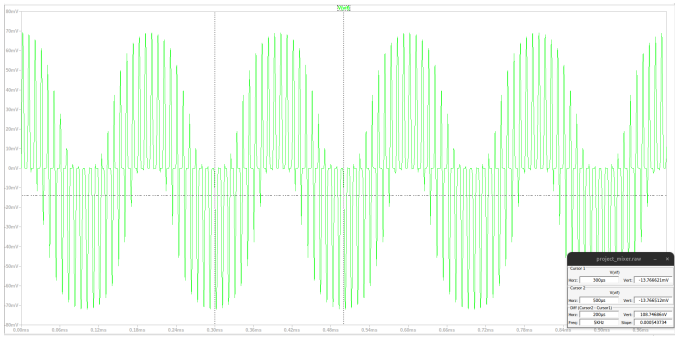

Fig. 12. Transient Response at 105 kHz

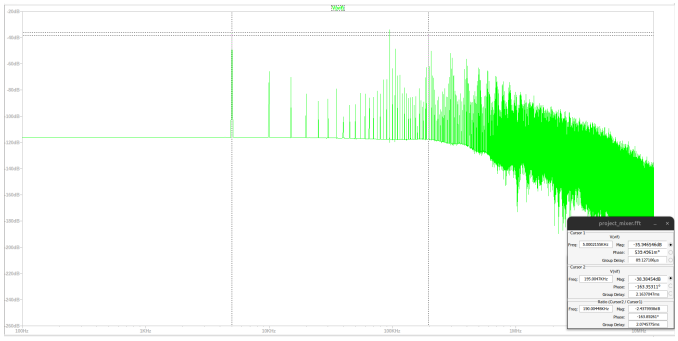

Fig. 13. FFT Spectrum at 95 kHz

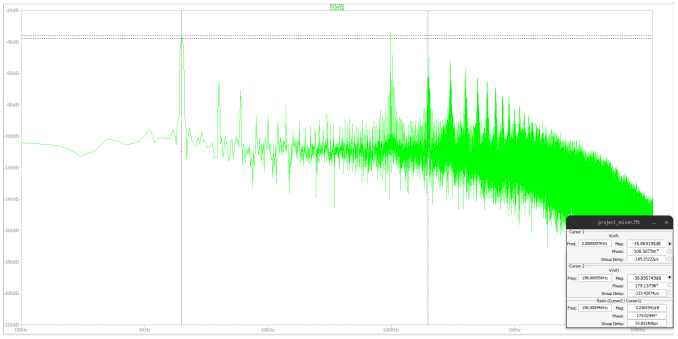

Fig. 14. FFT Spectrum at 98 kHz

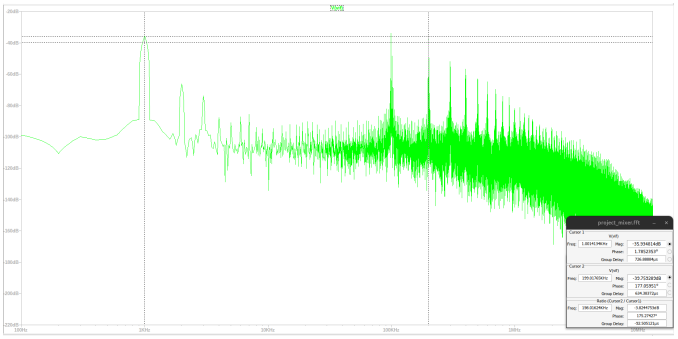

Fig. 15. FFT Spectrum at 99 kHz

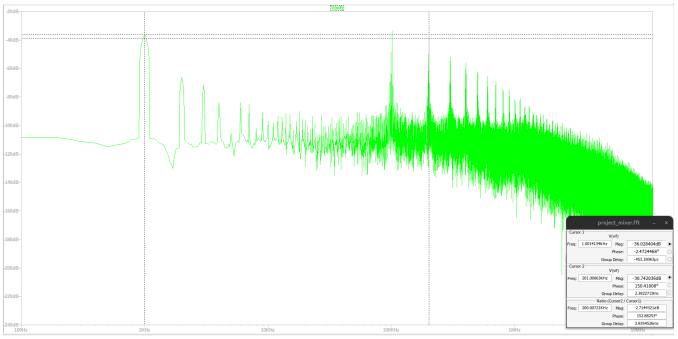

Fig. 16. FFT Spectrum at 101 kHz

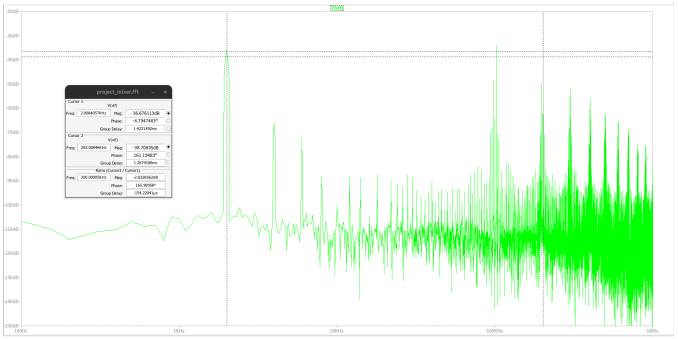

Fig. 17. FFT Spectrum at 102 kHz

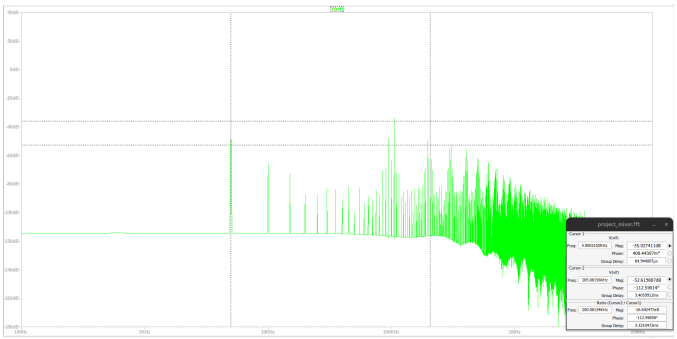

Fig. 18. FFT Spectrum at 105 kHz

D. Low Pass Filter Design

1) Design Process: We want to design a LPF (Low Pass Filter) with the -3 dB gain at 2 kHz; so we want the cutoff frequency to be 2 kHz. This means that all RF frequencies within a range of $f_{OSC} - 2\ kHz$ to $f_{OSC} + 2\ kHz$ would be passed through the quadrature downconverter. The rest would be attenuated, and we would not get a clean output waveform.

The cutoff frequency is given by,

$$f_c = \frac{1}{2\pi RC}$$

where R and C are the values of resistance and capacitance in the LPF.

Setting f_c to 2 kHz we get,

$$2 \times 10^3 = \frac{1}{2\pi RC}$$

$$\implies RC = 7.958 \times 10^{-6} s$$

$$\implies RC \approx 79.6\,\mu s$$

We see that the time constant is on the order of 10^{-4}, this results in a very low settling time, as discussed earlier while designing the HPF (High Pass Filter) and LPF for the mixer, which is one of our main requirements.

Now we need to choose C and R such that they fit commonly available values used in manufacturing processes. We take the capacitor to be 10 nF (which is the standard 103 ceramic capacitor).

From this we get the resistor to be $\approx$ 7958 Ω. We take the nearest value which is 8 kΩ. This gives us a 0.00525% error for the resistance, much below the $\pm 5\%$ tolerance.

Since we have taken the resistor as 8 $k\Omega$, we can expect a drop in the cutoff frequency, hence the final cutoff frequency that we end up with is,

$$f_c = \frac{1}{2\pi \times 8 \times 10^3 \times 10 \times 10^{-9}}$$

$$\implies f_c \approx 1989.44\ Hz$$

Hence our cutoff frequency is 1989.44 Hz, which is within the $\pm 5\%$ tolerance as well. From this we construct our circuit schematic as can be seen in Fig. 19.

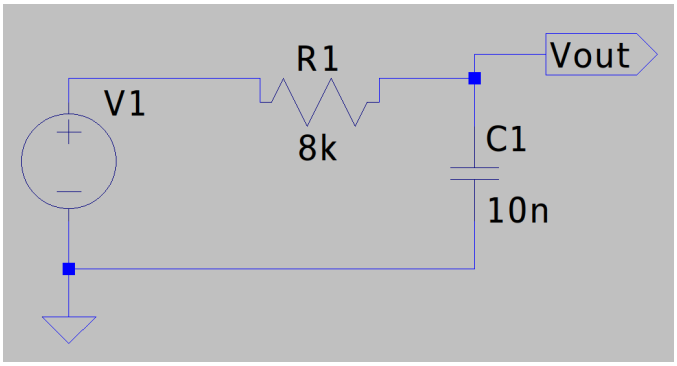

Fig. 19. Low Pass Filter Schematic

2) LTSpice Simulation of LPF: From the FRA (Frequency Response Analysis) plot in Fig. 20, we see that the -3 dB frequency is in fact $\approx$ 2 kHz

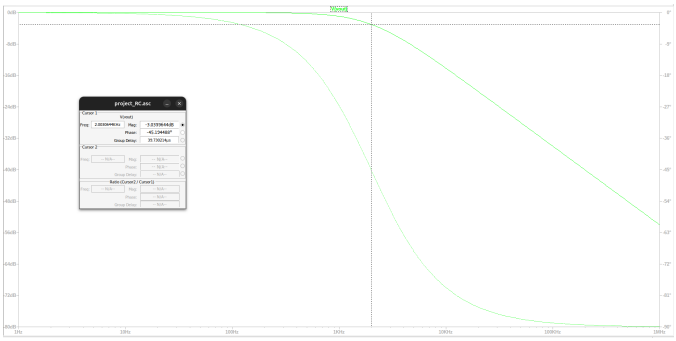

Fig. 20. -3 dB Frequency for LPF

We ran the simulation at 4 different frequencies: 1 kHz, 2 kHz, 5 kHz, and 10 kHz. The following results can be seen in Fig. 21

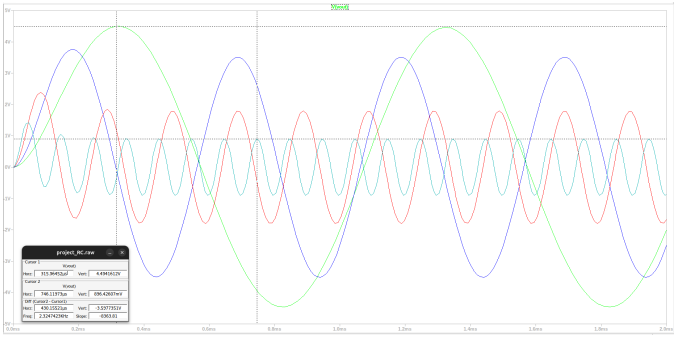

Fig. 21. LPF Transient Run for frequencies 1 kHz, 2 kHz, 5 kHz and 10 kHz

Note that the following colour scheme is followed in the above plot; Green:1 kHz, Blue:2 kHz, Red:5 kHz and Teal:10 kHz

IV. Simulation Results and Analysis

A. Combined Simulation of Downconverter

Considering all the 3 individual components we have designed and built, we move onto assembling them together to build the quadrature downconverter. Below in Fig. 22, the full circuit schematic can be seen . In the following Figs. 23 to 36 we can see the FFT and transient outputs for the oscillator and the complete circuit at input frequencies. of 95 kHz, 98 kHz, 99 kHz, 101 kHz, 102 kHz, 105 kHz.

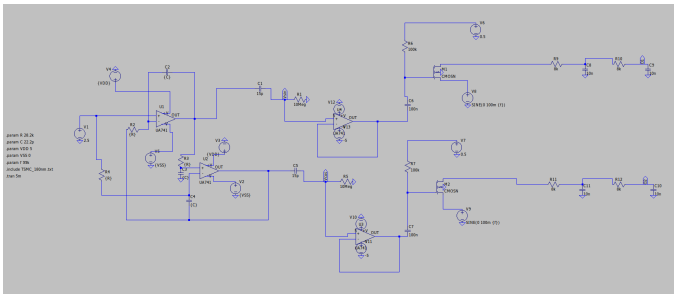

Fig. 22. Quadrature Downconverter Schematic

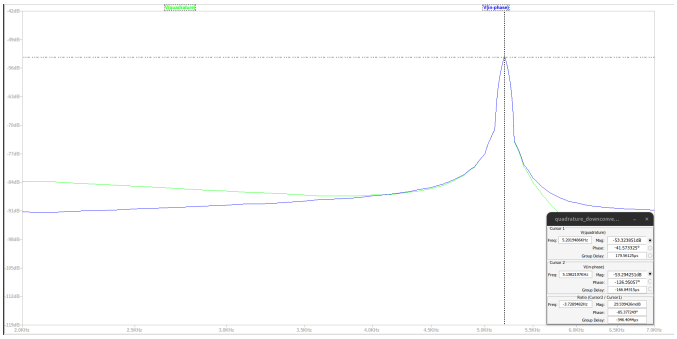

Fig. 23. Complete Circuit FFT Output at 95 kHz

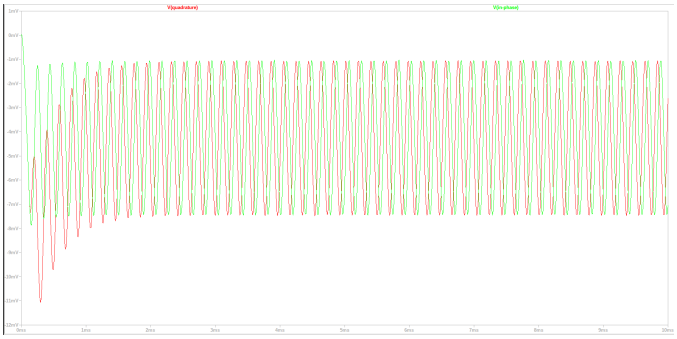

Fig. 24. Complete Circuit Transient Output at 95 kHz

B. Observations

We ran into quite a few issues during integration. One of the main issues was impedance loading between the oscillator and the mixer. Another issue we encountered was the inability of the first-order LPF to properly filter out the higher-frequency signals.

The mixer had low input impedance, which caused the oscillator frequency to decrease from 100 kHz to 98.5 kHz. To address this, we implemented a unity-gain buffer to offer high

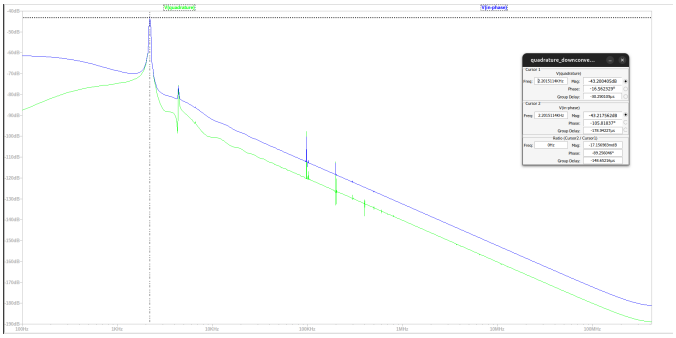

Fig. 25. Complete Circuit FFT Output at 98 kHz

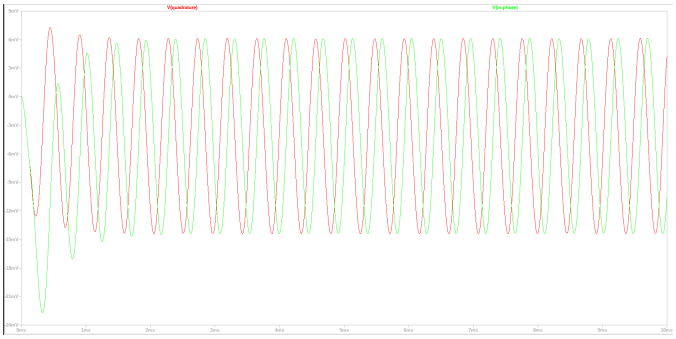

Fig. 26. Complete Circuit Transient Output at 98 kHz

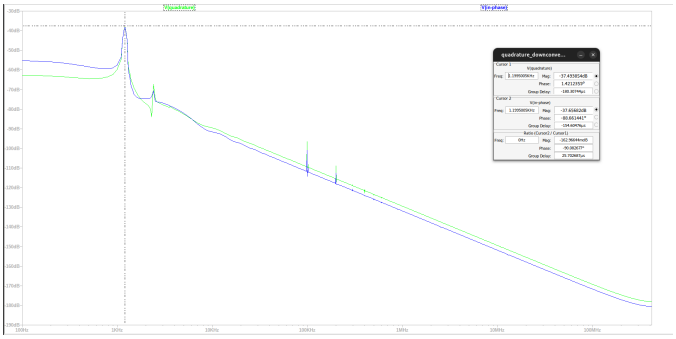

Fig. 27. Complete Circuit FFT Output at 99 kHz

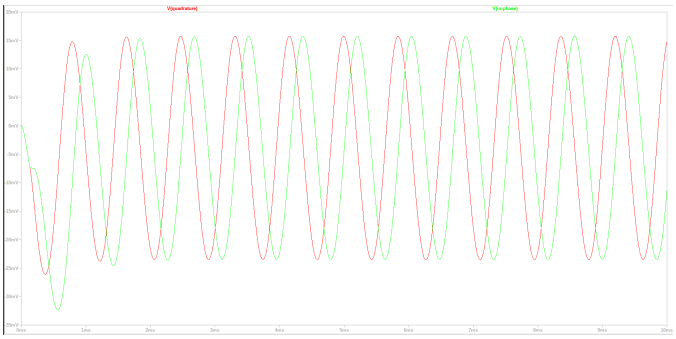

Fig. 28. Complete Circuit Transient Output at 99 kHz

Fig. 29. Complete Circuit FFT Output at 101 kHz

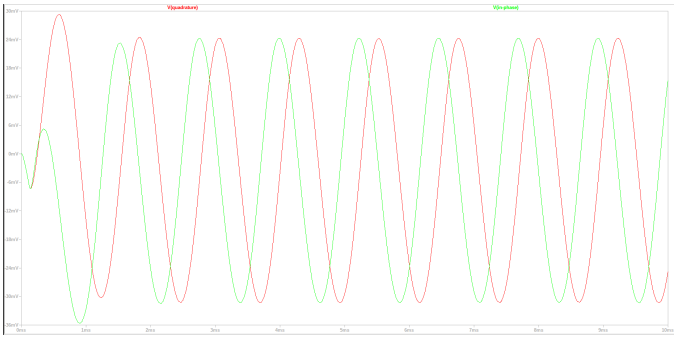

Fig. 30. Complete Circuit Transient Output at 101 kHz

Fig. 31. Complete Circuit FFT Output at 102 kHz

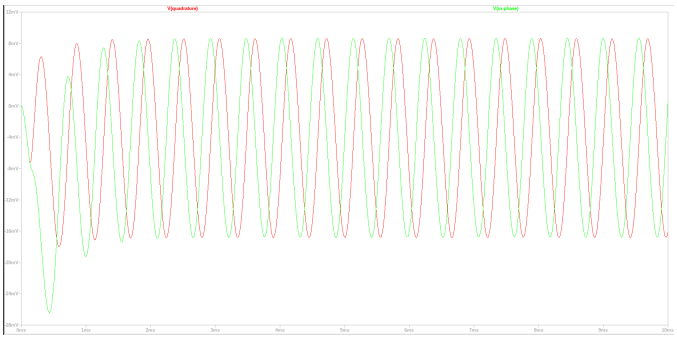

Fig. 32. Complete Circuit Transient Output at 102 kHz

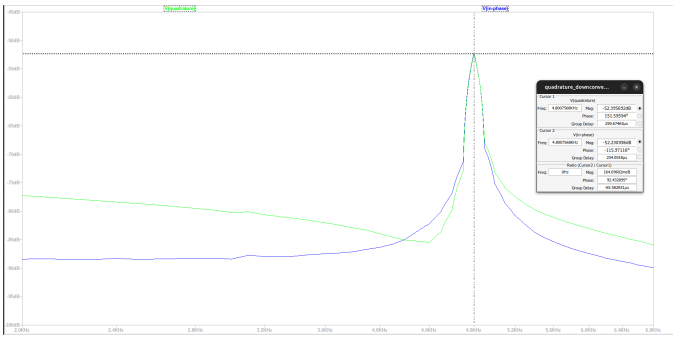

Fig. 33. Complete Circuit FFT Output at 105 kHz

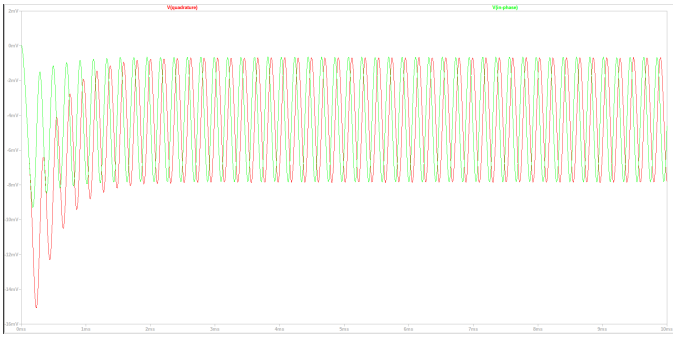

Fig. 34. Complete Circuit Transient Output at 105 kHz

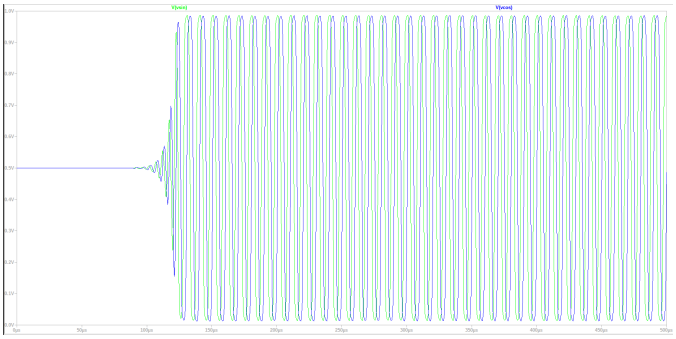

Fig. 35. Complete Circuit Transient Output of Oscillator

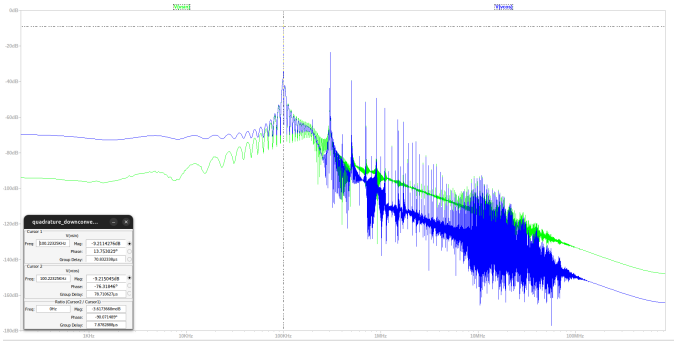

Fig. 36. Complete Circuit FFT Output of Oscillator

input impedance for the oscillator looking into the mixer. We also changed the resistor and capacitor values to compensate for the increased parasitic capacitance simulated by LTspice and to account for the fact that the UA741 is a very slow op-amp with a slew rate of only $0.5, V\mu s^{-1}$.

With the new changes, we now have the resistors and capacitors in the oscillator component set to 28.2 $k\Omega$ and 22.2 pF, respectively. Do note that 22.2 pF is not a standard capacitor value, but it can be replaced by a 22 pF capacitor, resulting in a new oscillation frequency of nearly 100.4 kHz instead of the previous 100 kHz.

The other issue was that a first-order LPF has only a -20 dB roll-off, which is insufficient to fully attenuate the higher-frequency signals. Hence, we had to add another LPF with the same cutoff frequency (2 kHz), giving us a -40 dB roll-off and a smoother output. The tradeoff in this case, however, is that our output signal is quite attenuated (a 200 mVpp RF input gives a 24 mVpp output), and we would need to amplify the output signal for any usable operation.

After solving these issues, the Quadrature Downconverter functioned as expected, providing us with a way to convert an RF signal to a lower-frequency wave while maintaining frequency and phase integrity up to a $\pm 5\%$ tolerance.

We also see a lot of distortion in the FFT plots because of how the FFT algorithm is implemented by LTSPICE and processes the data using a custom number of data points and how the window is defined along with the type of windowing algorithm. Hence, this is why we see random peaks at higher frequencies along with a bunch of random noise. [9]

V. Conclusion

In this report, we have shown how to design, simulate and analyze a quadrature downconverter consisting of an oscillator, passive NMOS mixer and second-order LPF. The oscillator, built using UA741 op-amps, generated sine and cosine waveforms near 100 kHz with a measured frequency of 99.92 kHz and with a very low phase error (around 0.036°), which falls well within the ±5% design margin. The passive mixer, based on an NMOS switching configuration, successfully multiplied the RF input with the LO signals while preserving signal shape and relative phase, as verified from the FFT simulations ranging from 95 kHz to 105 kHz.

The LPF, designed using standard 8 kΩ and 10 nF components, achieves a cutoff frequency of approximately 1.989 kHz, in close agreement with the design requirement of 2 kHz. This ensures that unwanted mixing products and higher-frequency components were attenuated while preserving the desired baseband signal. When combined, the overall system demonstrated effective downconversion maintaining amplitude and phase integrity.

While the simulations validate the theoretical design, small deviations are expected during practical hardware implementation due to component tolerances, parasitics, and non-idealities. However, these deviations should still remain within the acceptable ±5% tolerance defined for this design.

REFERENCES

[1] R. Holzel, "A simple wide-band sine wave quadrature oscillator," *IEEE Transactions on Instrumentation and Measurement*, vol. 42, no. 3, pp. 758–760, June 1993.

[2] Texas Instruments, *UA741 Operational Amplifier Datasheet*, https://www.ti.com/lit/ds/symlink/ua741.pdf, Texas Instruments, Dallas, TX, USA, 2015, document Number: SBOS094C. [Online]. Available: https://www.ti.com/lit/ds/symlink/ua741.pdf

[3] R. Mancini, "Design of op amp sine wave oscillators," *Texas Instruments Analog Applications Journal*, August 2000. [Online]. Available: https://www.ti.com/lit/an/sloa060/sloa060.pdf

[4] P. Horowitz and W. Hill, *The Art of Electronics*, 2nd ed. Cambridge University Press, 1989.

[5] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. Oxford University Press, 2014.

[6] Wikipedia contributors, "Barkhausen stability criterion," https://en.wikipedia.org/wiki/Barkhausen_stability_criterion, 2025, accessed: May 2, 2025.

[7] ——, "Mixer (electronics)," https://en.wikipedia.org/wiki/Mixer_(electronics), 2025, accessed: May 2, 2025.

[8] IIIT Hyderabad, EC2.103 Course Team, "Analog electronic circuits (ec2.103): Course project manual, spring 2025," Internal course document, IIIT Hyderabad, 2025, instructor: Prof. Zia Abbas. Credits: Abhishek Srivastava.

[9] A. aka, "What's the junk at the end of my fft in ltspice?" https://electronics.stackexchange.com/questions/370920/whats-the-junk-at-the-end-of-my-fft-in-ltspice, 2018, accessed: 2025-05-03. [Online]. Available: https://electronics.stackexchange.com/questions/370920/whats-the-junk-at-the-end-of-my-fft-in-ltspice