



## LM5109B High Voltage 1-A Peak Half-Bridge Gate Driver

### 1 Features

- Drives Both a High-Side and Low-Side N-Channel MOSFET
- 1-A Peak Output Current (1.0-A Sink and 1.0-A Source)
- Inputs Compatible With Independent TTL and CMOS
- Bootstrap Supply Voltage to 108-V DC
- Fast Propagation Times (30 ns Typical)
- Drives 1000-pF Load With 15-ns Rise and Fall Times
- Excellent Propagation Delay Matching (2 ns Typical)
- Supply Rail Undervoltage Lockout
- Low Power Consumption
- 8-Pin SOIC and Thermally-Enhanced 8-Pin WSON Package

### 2 Applications

- Current-Fed, Push-Pull Converters
- Half- and Full-Bridge Power Converters
- Solid-State Motor Drives
- Two-Switch Forward Power Converters

### 3 Description

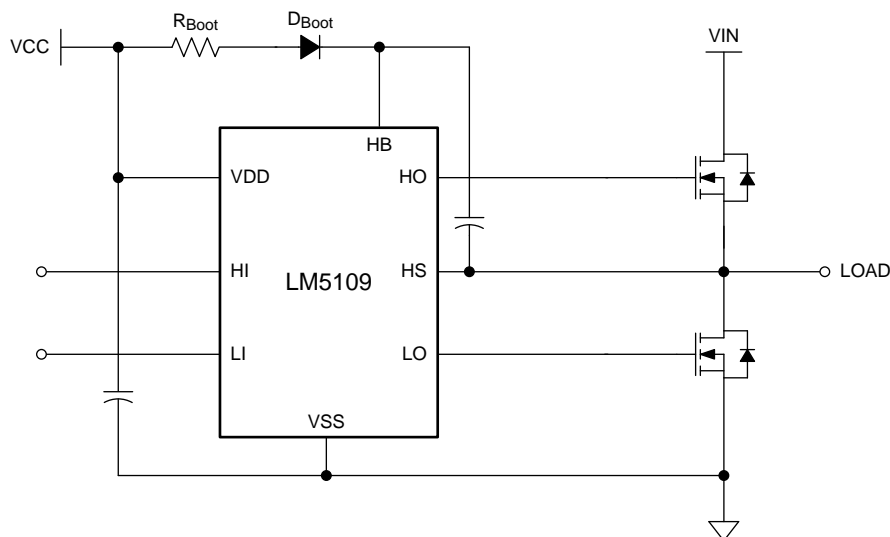
The LM5109B device is a cost-effective, high-voltage gate driver designed to drive both the high-side and the low-side N-channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of working with rail voltages up to 90 V. The outputs are independently controlled with cost-effective TTL and CMOS-compatible input thresholds. The robust level shift technology operates at high speed while consuming low power and providing clean level transitions from the control input logic to the high-side gate driver. Undervoltage lockout is provided on both the low-side and the high-side power rails. The device is available in the 8-pin SOIC and thermally-enhanced 8-pin WSON packages.

**Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5109B	SOIC (8)	4.90 mm × 3.91 mm
	WSON (8)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Application Diagram**



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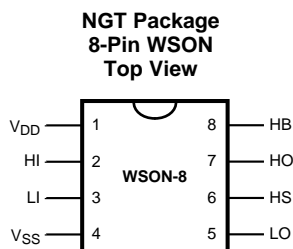
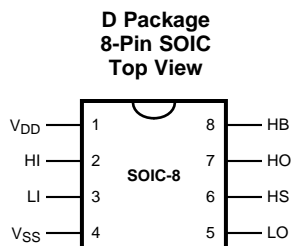
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C	Page
<ul style="list-style-type: none"> <li>Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul>	<b>1</b>

Changes from Revision A (March 2013) to Revision B	Page
<ul style="list-style-type: none"> <li>Changed layout of National Data Sheet to TI format .....</li> </ul>	<b>1</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN			DESCRIPTION
NO. <sup>(1)</sup>	NAME	TYPE <sup>(2)</sup>	
1	V <sub>DD</sub>	P	Positive gate drive supply – Locally decouple to V <sub>SS</sub> using low ESR and ESL capacitor located as close to IC as possible.
2	HI	I	High-side control input – The HI input is compatible with TTL and CMOS input thresholds. Unused HI input must be tied to ground and not left open.
3	LI	I	Low-side control input – The LI input is compatible with TTL and CMOS input thresholds. Unused LI input must be tied to ground and not left open.
4	V <sub>SS</sub>	G	Ground – All signals are referenced to this ground.
5	LO	O	Low-side gate driver output – Connect to the gate of the low-side N-MOS device.
6	HS	P	High-side source connection – Connect to the negative terminal of the bootstrap capacitor and to the source of the high-side N-MOS device.
7	HO	O	High-side gate driver output – Connect to the gate of the high-side N-MOS device.
8	HB	P	High-side gate driver positive supply rail – Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal of the bootstrap capacitor to HS. The bootstrap capacitor must be placed as close to IC as possible.

- (1) For 8-pin WSON package, TI recommends that the exposed pad on the bottom of the package be soldered to ground plane on the PCB and the ground plane must extend out from underneath the package to improve heat dissipation.
- (2) G = Ground, I = Input, O = Output, and P = Power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
$V_{DD}$ to $V_{SS}$	–0.3	18	V
HB to HS	–0.3	18	V
LI or HI to $V_{SS}$	–0.3	$V_{DD} + 0.3$	V
LO to $V_{SS}$	–0.3	$V_{DD} + 0.3$	V
HO to $V_{SS}$	$V_{HS} - 0.3$	$V_{HB} + 0.3$	V
HS to $V_{SS}$ <sup>(2)</sup>	–5	90	V
HB to $V_{SS}$		108	V
Junction temperature	–40	150	°C
Storage temperature, $T_{stg}$	–55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1 V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than  $V_{DD} - 15$  V. For example, if  $V_{DD} = 10$  V, the negative transients at HS must not exceed –5 V.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
$V_{DD}$	8	14	V
HS <sup>(1)</sup>	–1	90	V
HB	$V_{HS} + 8$	$V_{HS} + 14$	V
HS slew rate		50	V/ns
Junction temperature	–40	125	°C

- (1) In the application, the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed –1 V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than  $V_{DD} - 15$  V. For example, if  $V_{DD} = 10$  V, the negative transients at HS must not exceed –5 V.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM5109B		UNIT
		D (SOIC)	NGT (WSON)	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	117.6	42.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	64.9	34.0	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	58.1	19.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	17.4	0.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	57.6	19.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	–	8.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

T<sub>J</sub> = 25°C (unless otherwise specified), V<sub>DD</sub> = V<sub>HB</sub> = 12 V, V<sub>SS</sub> = V<sub>HS</sub> = 0 V, No Load on LO or HO

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENTS							
I <sub>DD</sub>	V <sub>DD</sub> quiescent current	LI = HI = 0 V	T <sub>J</sub> = 25°C	0.3		mA	
			T <sub>J</sub> = −40°C to 125°C	0.6			
I <sub>DDO</sub>	V <sub>DD</sub> operating current	f = 500 kHz	T <sub>J</sub> = 25°C	1.8		mA	
			T <sub>J</sub> = −40°C to 125°C	2.9			
I <sub>HB</sub>	Total HB quiescent current	LI = HI = 0 V	T <sub>J</sub> = 25°C	0.06		mA	
			T <sub>J</sub> = −40°C to 125°C	0.2			
I <sub>HBO</sub>	Total HB operating current	f = 500 kHz	T <sub>J</sub> = 25°C	1.4		mA	
			T <sub>J</sub> = −40°C to 125°C	2.8			
I <sub>HBS</sub>	HB to V <sub>SS</sub> current, quiescent	V <sub>HS</sub> = V <sub>HB</sub> = 90 V	T <sub>J</sub> = 25°C	0.1		μA	
			T <sub>J</sub> = −40°C to 125°C	10			
I <sub>HBSO</sub>	HB to V <sub>SS</sub> current, operating	f = 500 kHz	0.5		mA		
INPUT PINS LI AND HI							
V <sub>IL</sub>	Low level input voltage threshold	T <sub>J</sub> = 25°C		1.8		V	
		T <sub>J</sub> = −40°C to 125°C		0.8			
V <sub>IH</sub>	High level input voltage threshold	T <sub>J</sub> = 25°C		1.8		V	
		T <sub>J</sub> = −40°C to 125°C		2.2			
R <sub>I</sub>	Input pulldown resistance	T <sub>J</sub> = 25°C		200		kΩ	
		T <sub>J</sub> = −40°C to 125°C		100      500			
UNDERVOLTAGE PROTECTION							
V <sub>DDR</sub>	V <sub>DD</sub> rising threshold	V <sub>DDR</sub> = V <sub>DD</sub> − V <sub>SS</sub>	T <sub>J</sub> = 25°C	6.7		V	
			T <sub>J</sub> = −40°C to 125°C	6.0	7.4		
V <sub>DDH</sub>	V <sub>DD</sub> threshold hysteresis			0.5		V	
V <sub>HBR</sub>	HB rising threshold	V <sub>HBR</sub> = V <sub>HB</sub> − V <sub>HS</sub>	T <sub>J</sub> = 25°C	6.6		V	
			T <sub>J</sub> = −40°C to 125°C	5.7	7.1		
V <sub>HBH</sub>	HB threshold hysteresis			0.4		V	
LO GATE DRIVER							
V <sub>OLL</sub>	Low-level output voltage	I <sub>LO</sub> = 100 mA, V <sub>OHL</sub> = V <sub>LO</sub> − V <sub>SS</sub>	T <sub>J</sub> = 25°C	0.38		V	
			T <sub>J</sub> = −40°C to 125°C	0.65			
V <sub>OHL</sub>	High-level output voltage	I <sub>LO</sub> = −100 mA, V <sub>OHL</sub> = V <sub>DD</sub> − V <sub>LO</sub>	T <sub>J</sub> = 25°C	0.72		V	
			T <sub>J</sub> = −40°C to 125°C	1.2			
I <sub>OHL</sub>	Peak pullup current	V <sub>LO</sub> = 0 V		1		A	
I <sub>OLL</sub>	Peak pulldown current	V <sub>LO</sub> = 12 V		1		A	

## Electrical Characteristics (continued)

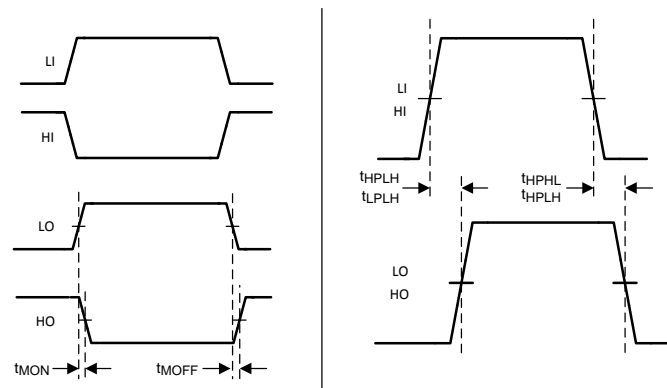
$T_J = 25^\circ\text{C}$  (unless otherwise specified),  $V_{DD} = V_{HB} = 12\text{ V}$ ,  $V_{SS} = V_{HS} = 0\text{ V}$ , No Load on LO or HO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>HO GATE DRIVER</b>						
$V_{OLH}$	Low-level output voltage	$I_{HO} = 100\text{ mA}$ , $V_{OLH} = V_{HO} - V_{HS}$	$T_J = 25^\circ\text{C}$		0.38	V
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$		0.65	
$V_{OHH}$	High-level output voltage	$I_{HO} = -100\text{ mA}$ , $V_{OHH} = V_{HB} - V_{HO}$	$T_J = 25^\circ\text{C}$		0.72	V
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$		1.2	
$I_{OHH}$	Peak pullup current	$V_{HO} = 0\text{ V}$		1		A
$I_{OLH}$	Peak pulldown current	$V_{HO} = 12\text{ V}$		1		A

## 6.6 Switching Characteristics

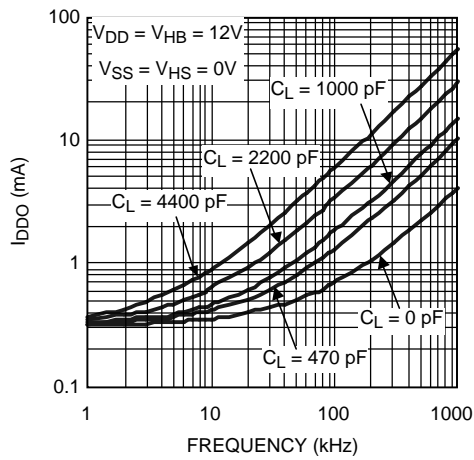
$T_J = 25^\circ\text{C}$  (unless otherwise specified),  $V_{DD} = V_{HB} = 12\text{ V}$ ,  $V_{SS} = V_{HS} = 0\text{ V}$ , No Load on LO or HO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LPHL}$	Lower turnoff propagation delay (LI falling to LO falling)	$T_J = 25^\circ\text{C}$		30		ns
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$			56	
$t_{HPLH}$	Upper turnoff propagation delay (HI falling to HO falling)	$T_J = 25^\circ\text{C}$		30		ns
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$			56	
$t_{LPLH}$	Lower turnon propagation delay (LI rising to LO rising)	$T_J = 25^\circ\text{C}$		32		ns
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$			56	
$t_{HPLH}$	Upper turnon propagation delay (HI rising to HO rising)	$T_J = 25^\circ\text{C}$		32		ns
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$			56	
$t_{MON}$	Delay matching: Lower turnon and upper turnoff	$T_J = 25^\circ\text{C}$		2		ns
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$			15	
$t_{MOFF}$	Delay matching: Lower turnoff and upper turnon	$T_J = 25^\circ\text{C}$		2		ns
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$			15	
$t_{RC}, t_{FC}$	Either output rise and fall time	$C_L = 1000\text{ pF}$		15		ns
$t_{PW}$	Minimum input pulse width that changes the output			50		ns

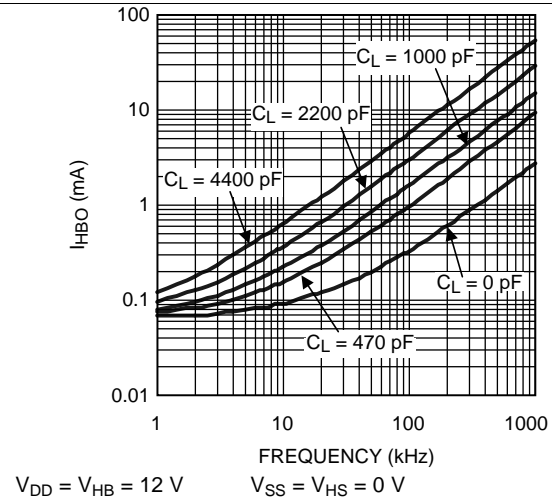


**Figure 1. Typical Test Timing Diagram**

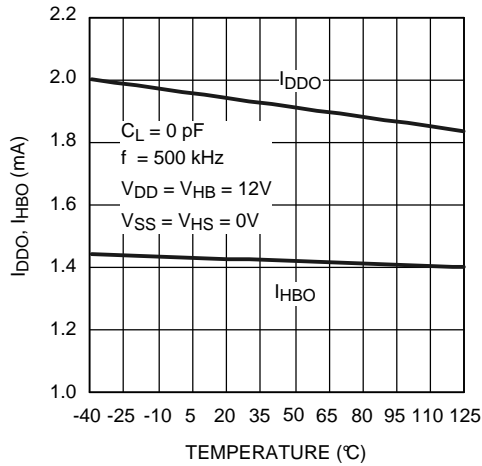
## 6.7 Typical Characteristics



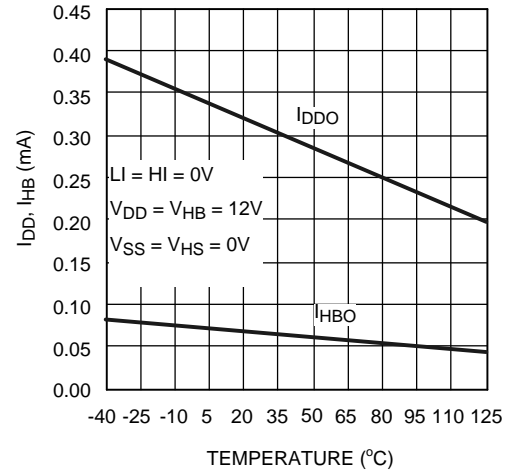
**Figure 2. V<sub>DD</sub> Operating Current vs Frequency**



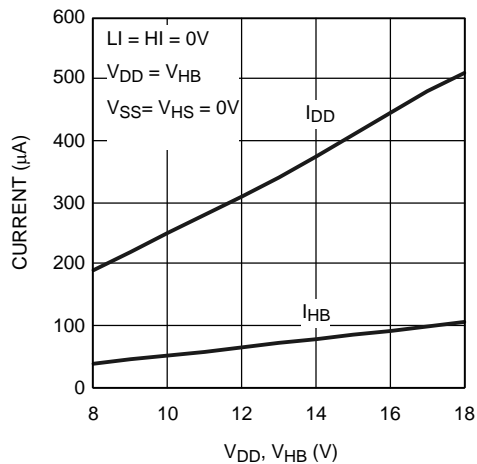
**Figure 3. HB Operating Current vs Frequency**



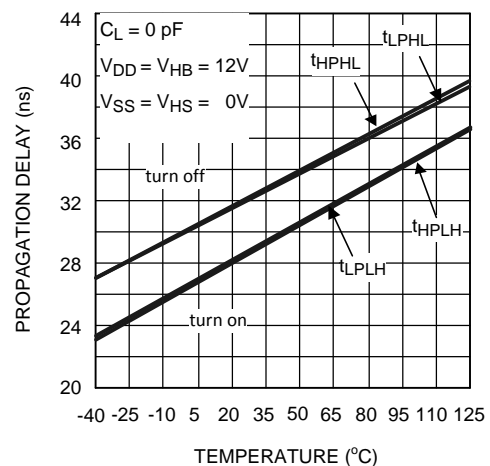
**Figure 4. Operating Current vs Temperature**



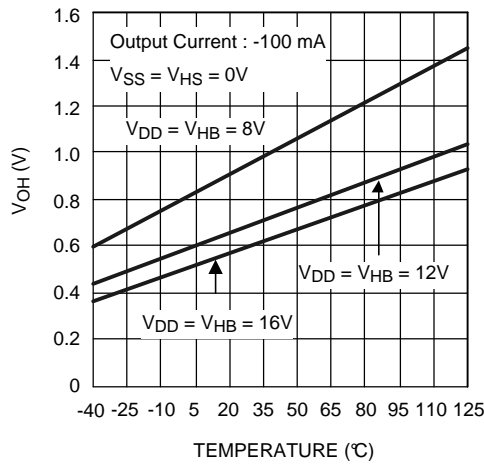
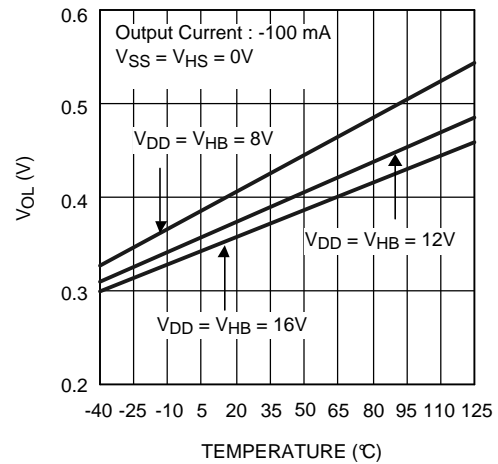
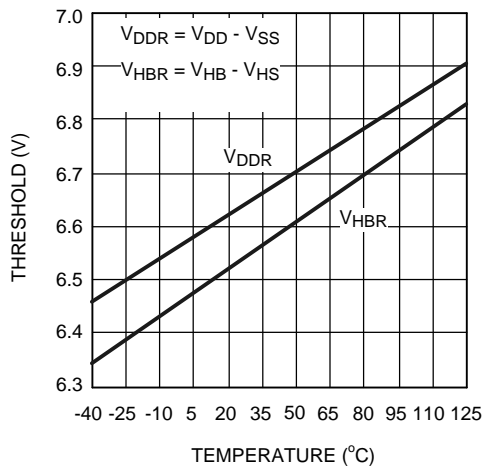
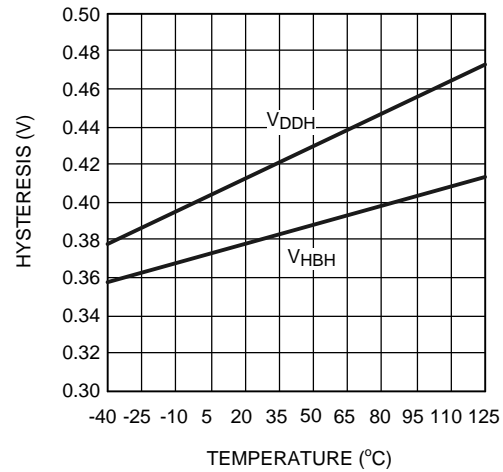
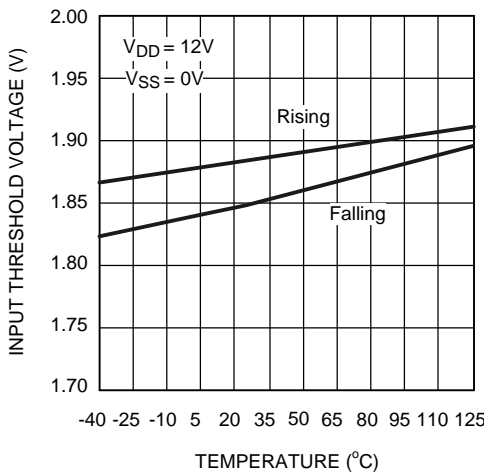
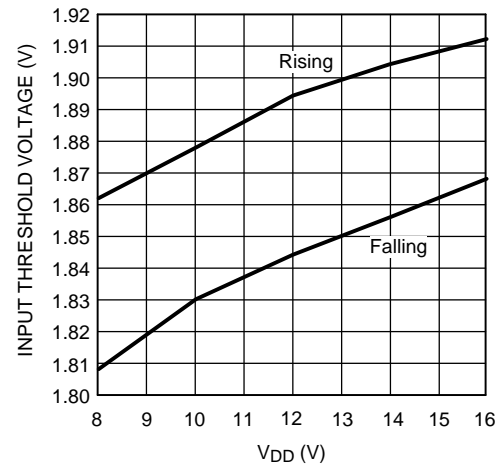
**Figure 5. Quiescent Current vs Temperature**



**Figure 6. Quiescent Current vs Voltage**



**Figure 7. Propagation Delay vs Temperature**

**Typical Characteristics (continued)**

**Figure 8. LO and HO High Level Output Voltage vs Temperature**

**Figure 9. LO and HO Low Level Output Voltage vs Temperature**

**Figure 10. Undervoltage Rising Thresholds vs Temperature**

**Figure 11. Undervoltage Hysteresis vs Temperature**

**Figure 12. Input Thresholds vs Temperature**

**Figure 13. Input Thresholds vs Supply Voltage**

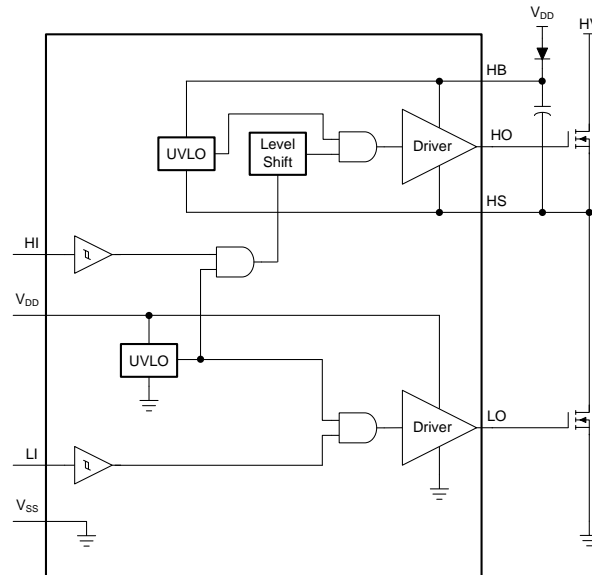


## 7 Detailed Description

### 7.1 Overview

The LM5109B is a cost-effective, high-voltage gate driver designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configuration. The outputs are independently controlled with TTL and CMOS-compatible input thresholds. The floating high-side driver is capable of working with HB voltage up to 108 V. An external high-voltage diode must be provided to charge high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout (UVLO) is provided on both the low-side and the high-side power rails.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Start-Up and UVLO

Both top and bottom drivers include UVLO protection circuitry which monitors the supply voltage ( $V_{DD}$ ) and bootstrap capacitor voltage ( $V_{HB-HS}$ ) independently. The UVLO circuit inhibits each output until sufficient supply voltage is available to turn on the external MOSFETs, and the built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the VDD pin of the LM5109B, the top and bottom gates are held low until  $V_{DD}$  exceeds the UVLO threshold, typically about 6.7 V. Any UVLO condition on the bootstrap capacitor ( $V_{HB-HS}$ ) will only disable the high-side output (HO).

**Table 1. VDD UVLO Feature Logic Operation**

CONDITION ( $V_{HB-HS} > V_{HBR}$ )	HI	LI	HO	LO
$V_{DD}-V_{SS} < V_{DDR}$ during device start-up	H	L	L	L
$V_{DD}-V_{SS} < V_{DDR}$ during device start-up	L	H	L	L
$V_{DD}-V_{SS} < V_{DDR}$ during device start-up	H	H	L	L
$V_{DD}-V_{SS} < V_{DDR}$ during device start-up	L	L	L	L
$V_{DD}-V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	H	L	L	L
$V_{DD}-V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	L	H	L	L
$V_{DD}-V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	H	H	L	L
$V_{DD}-V_{SS} < V_{DDR} - V_{DDH}$ after device start-up	L	L	L	L

**Table 2. VHB-HS UVLO Feature Logic Operation**

CONDITION ( $V_{DD} > V_{DDR}$ )	HI	LI	HO	LO
$V_{HB-HS} < V_{HBR}$ during device start-up	H	L	L	L
$V_{HB-HS} < V_{HBR}$ during device start-up	L	H	L	H
$V_{HB-HS} < V_{HBR}$ during device start-up	H	H	L	H
$V_{HB-HS} < V_{HBR}$ during device start-up	L	L	L	L
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	H	L	L	L
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	L	H	L	H
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	H	H	L	H
$V_{HB-HS} < V_{HBR} - V_{HBH}$ after device start-up	L	L	L	L

### 7.3.2 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output which is referenced to the HS pin and provides excellent delay matching with the low-side driver.

### 7.3.3 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance, and high-peak current capability of both outputs allow for efficient switching of the power MOSFETs. The low-side output stage is referenced to VSS and the high-side is referenced to HS.

## 7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See [Start-Up and UVLO](#) for more information on UVLO operation mode. In normal mode when the  $V_{DD}$  and  $V_{HB-HS}$  are above UVLO threshold, the output stage is dependent on the states of the HI and LI pins. The output HO and LO will be low if input state is floating.

**Table 3. INPUT and OUTPUT Logic Table**

HI	LI	HO <sup>(1)</sup>	LO <sup>(2)</sup>
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
Floating	Floating	L	L

(1) HO is measured with respect to the HS.

(2) LO is measured with respect to the VSS.

## 7.5 HS Transient Voltages Below Ground

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than  $-0.3$  V below HS can activate parasitic transistors resulting in excessive current flow from the HB supply, possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible to be effective.
2. HB to HS operating voltage must be 15 V or less. Hence, if the HS pin transient voltage is  $-5$  V, VDD must be ideally limited to 10 V to keep HB to HS below 15 V.
3. Low-ESR bypass capacitors from HB to HS and from VDD to VSS are essential for proper operation. The capacitor must be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.



## Typical Application (continued)

### 8.2.1 Design Requirements

Table 4 lists the design parameters of the LM5109B.

**Table 4. Design Example**

PARAMETER	VALUE
Gate Driver	LM5109B
MOSFET	CSD19534KCS
V <sub>DD</sub>	10 V
Q <sub>G</sub>	17 nC
f <sub>SW</sub>	500 kHz

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Select Bootstrap and VDD Capacitor

The bootstrap capacitor must maintain the V<sub>HB-HS</sub> voltage above the UVLO threshold for normal operation. Calculate the maximum allowable drop across the bootstrap capacitor with Equation 1.

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL} = 10 \text{ V} - 1 \text{ V} - 6.7 \text{ V} = 2.3 \text{ V}$$

where

- V<sub>DD</sub> = Supply voltage of the gate drive IC
- V<sub>DH</sub> = Bootstrap diode forward voltage drop
- V<sub>HBL</sub> = V<sub>HBRmax</sub> – V<sub>HBH</sub>, HB falling threshold

Then, the total charge needed per switching cycle is estimated by Equation 2.

$$Q_{\text{Total}} = Q_G + I_{HBS} \times \frac{D_{\text{Max}}}{f_{\text{SW}}} + \frac{I_{HB}}{f_{\text{SW}}} = 17 \text{ nC} + 10 \mu\text{A} \times \frac{0.95}{500 \text{ kHz}} + \frac{0.2 \text{ mA}}{500 \text{ kHz}} = 17.5 \text{ nC}$$

where

- Q<sub>G</sub> = Total MOSFET gate charge
- I<sub>HBS</sub> = HB to VSS Leakage current
- D<sub>Max</sub> = Converter maximum duty cycle
- I<sub>HB</sub> = HB Quiescent current

Therefore, the minimum C<sub>Boot</sub> must be:

$$C_{\text{Boot}} = \frac{Q_{\text{Total}}}{\Delta V_{HB}} = \frac{17.5 \text{ nC}}{2.3 \text{ V}} = 7.6 \text{ nF}$$

In practice, the value of the C<sub>Boot</sub> capacitor must be greater than calculated to allow for situations where the power stage may skip pulse due to load transients. TI recommends having enough margins and place the bootstrap capacitor as close to the HB and HS pins as possible.

$$C_{\text{Boot}} = 100 \text{ nF}$$

As a general rule the local V<sub>DD</sub> bypass capacitor must be 10 times greater than the value of C<sub>Boot</sub>, as shown in Equation 5.

$$C_{VDD} = 1 \mu\text{F}$$

The bootstrap and bias capacitors must be ceramic types with X7R dielectric. The voltage rating must be twice that of the maximum V<sub>DD</sub> considering capacitance tolerances once the devices have a DC bias voltage across them and to ensure long-term reliability.

### 8.2.2.2 Select External Bootstrap Diode and Its Series Resistor

The bootstrap capacitor is charged by the  $V_{DD}$  through the external bootstrap diode every cycle when low-side MOSFET turns on. The charging of the capacitor involves high peak currents, and therefore transient power dissipation in the bootstrap diode may be significant and the conduction loss also depends on its forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

For the selection of external bootstrap diodes, refer to *AN-1317 Selection of External Bootstrap Diode for LM510X Devices*, [SNVA083](#). Bootstrap resistor  $R_{BOOT}$  is selected to reduce the inrush current in  $D_{BOOT}$  and limit the ramp up slew rate of voltage of  $V_{HB-HS}$  during each switching cycle, especially when HS pin have excessive negative transient voltage.  $R_{BOOT}$  recommended value is between  $2\ \Omega$  and  $10\ \Omega$  depending on diode selection. A current limiting resistor of  $2.2\ \Omega$  is selected to limit inrush current of bootstrap diode, and the estimated peak current on the  $D_{Boot}$  is shown in [Equation 6](#).

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{DH}}{R_{Boot}} = \frac{10\text{ V} - 1\text{ V}}{2.2\ \Omega} \approx 4\text{ A}$$

where

- $V_{DH}$  is the bootstrap diode forward voltage drop (6)

### 8.2.2.3 Selecting External Gate Driver Resistor

The external gate driver resistor,  $R_{GATE}$ , is sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver.

Peak HO pullup current are calculated in [Equation 7](#).

$$I_{OHH} = \frac{V_{DD} - V_{DH}}{R_{HOH} + R_{Gate} + R_{GFET\_Int}} = \frac{10\text{ V} - 1\text{ V}}{1.2\text{ V} / 100\text{ mA} + 4.7\ \Omega + 2.2\ \Omega} = 0.48\text{ A}$$

where

- $I_{OHH}$  = Peak pullup current
- $V_{DH}$  = Bootstrap diode forward voltage drop
- $R_{HOH}$  = Gate driver internal HO pullup resistance, provide by driver data sheet directly or estimated from the testing conditions, that is  $R_{HOH} = V_{OHH} / I_{HO}$
- $R_{Gate}$  = External gate drive resistance
- $R_{GFET\_Int}$  = MOSFET internal gate resistance, provided by transistor data sheet (7)

Similarly, Peak HO pulldown current is shown in [Equation 8](#).

$$I_{OLH} = \frac{V_{DD} - V_{DH}}{R_{HOL} + R_{Gate} + R_{GFET\_Int}}$$

where

- $R_{HOL}$  is the HO pulldown resistance (8)

Peak LO pullup current is shown in [Equation 9](#).

$$I_{OHL} = \frac{V_{DD}}{R_{LOH} + R_{Gate} + R_{GFET\_Int}}$$

where

- $R_{LOH}$  is the LO pullup resistance (9)

Peak LO pulldown current is shown in [Equation 10](#).

$$I_{OLL} = \frac{V_{DD}}{R_{LOL} + R_{Gate} + R_{FET\_Int}}$$

where

- $R_{LOL}$  is the LO pulldown resistance (10)

For some scenarios, if the applications require fast turnoff, an anti-parallel diode on  $R_{Gate}$  could be used to bypass the external gate drive resistor and speed up turnoff transition.

### 8.2.2.4 Estimate the Driver Power Loss

The total driver IC power dissipation can be estimated through the following components.

1. Static power losses,  $P_{QC}$ , due to quiescent current –  $I_{DD}$  and  $I_{HB}$

$$P_{QC} = V_{DD} \times I_{DD} + (V_{DD} - V_{DH}) \times I_{HB} \quad (11)$$

2. Level-shifter losses,  $P_{IHBS}$ , due high-side leakage current –  $I_{HBS}$

$$P_{IHBS} = V_{HB} \times I_{HBS} \times D$$

where

- $D$  is the high-side switch duty cycle (12)

3. Dynamic losses,  $P_{QG1\&2}$ , due to the FETs gate charge –  $Q_G$

$$P_{QG1\&2} = 2 \times V_{DD} \times Q_G \times f_{SW} \times \frac{R_{GD\_R}}{R_{GD\_R} + R_{Gate} + R_{GFET\_Int}}$$

where

- $Q_G$  = Total FETs gate charge
- $f_{SW}$  = Switching frequency
- $R_{GD\_R}$  = Average value of pullup and pulldown resistor
- $R_{Gate}$  = External gate drive resistor
- $R_{GFET\_Int}$  = Internal FETs gate resistor (13)

4. Level-shifter dynamic losses,  $P_{LS}$ , during high-side switching due to required level-shifter charge on each switching cycle –  $Q_P$

$$P_{LS} = V_{HB} \times Q_P \times f_{SW} \quad (14)$$

In this example, the estimated gate driver loss in LM5109B is shown in [Equation 15](#).

$$P_{LM5109B} = 10\text{ V} \times 0.6\text{ mA} + 9\text{ V} \times 0.2\text{ mA} + 72\text{ V} \times 10\text{ }\mu\text{A} \times 0.95 + 2 \times 10 \times 17\text{ nC} \times 500\text{ kHz} \times \frac{12\text{ }\Omega}{12\text{ }\Omega + 4.7\text{ }\Omega + 2.2\text{ }\Omega} + 72\text{ V} \times 0.5\text{ nC} \times 500\text{ kHz} = 0.134\text{ W} \quad (15)$$

For a given ambient temperature, the maximum allowable power loss of the IC can be defined as shown in [Equation 16](#).

$$P_{LM5109B} = \frac{T_J - T_A}{R_{\theta JA}}$$

where

- $P_{LM5109B}$  = The total power dissipation of the driver
- $T_J$  = Junction temperature
- $T_A$  = Ambient temperature
- $R_{\theta JA}$  = Junction-to-ambient thermal resistance (16)

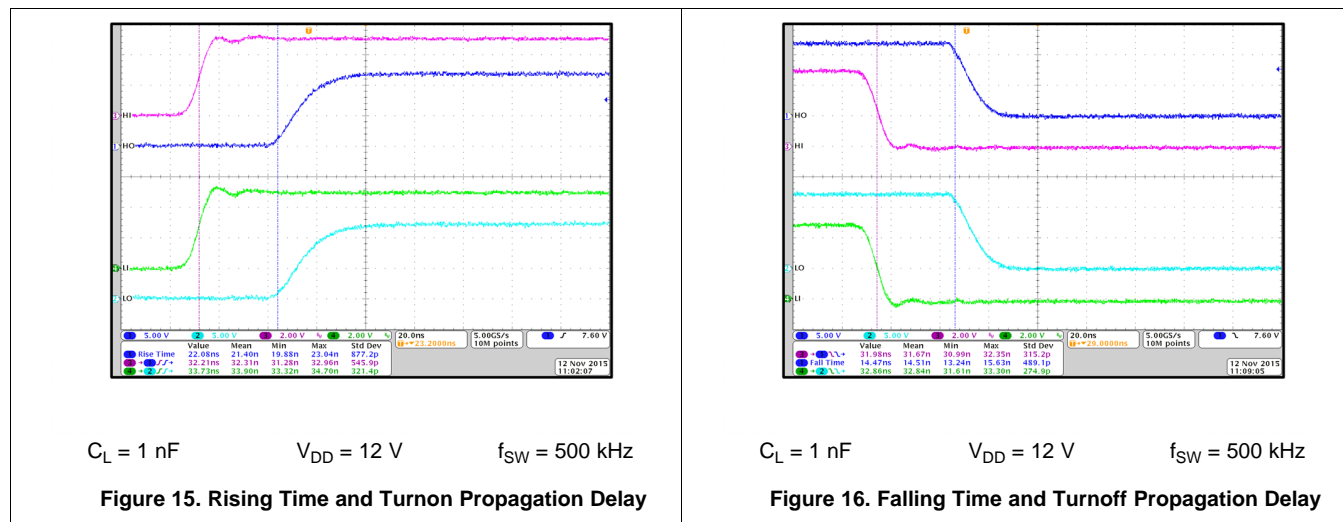
The thermal metrics for the driver package is summarized in the [Thermal Information](#) table of the data sheet. For detailed information regarding the thermal information table, please refer to the Texas Instruments application note entitled *Semiconductor and IC Package Thermal Metrics* ([SPRA953](#)).

### 8.2.3 Application Curves

Figure 15 and Figure 16 shows the rising and falling time as well as turnon and turnoff propagation delay testing waveform in room temperature, and waveform measurement data (see the bottom part of the waveform). Each channel (HI, LI, HO, and LO) is labeled and displayed on the left hand of the waveforms.

The testing condition: load capacitance is 1 nF,  $V_{DD} = 12$  V,  $f_{SW} = 500$  kHz.

HI and LI share one same input from function generator, therefore, besides the propagation delay and rising and falling time, the difference of the propagation delay between HO and LO gives the propagation delay matching data.



## 9 Power Supply Recommendations

The recommended bias supply voltage range for LM5109B is from 8 V to 14 V. The lower end of this range is governed by the internal undervoltage lockout (UVLO) protection feature of the  $V_{DD}$  supply circuit blocks. The upper end of this range is driven by the 18-V absolute maximum voltage rating of the  $V_{DD}$ . TI recommends keeping a 4-V margin to allow for transient voltage spikes.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the  $V_{DD}$  voltage drops, the device continues to operate in normal mode as long as the voltage drop does not exceed the hysteresis specification,  $V_{DDH}$ . If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 8-V range, the voltage ripple on the auxiliary power supply output must be smaller than the hysteresis specification of LM5109B to avoid triggering device-shutdown.

A local bypass capacitor must be placed between the VDD and GND pins. And this capacitor must be located as close to the device as possible. A low-ESR, ceramic surface mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100-nF, ceramic surface-mount capacitor for high-frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220-nF to 10- $\mu$ F, for IC bias requirements. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore a 22-nF to 220-nF local decoupling capacitor is recommended between the HB and HS pins.

## 10 Layout

### 10.1 Layout Guidelines

Optimum performance of high-side and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low-ESR and low-ESL capacitors must be connected close to the IC between VDD and VSS pins and between HB and HS pins to support high peak currents being drawn from VDD and HB during the turnon of the external MOSFETs.
2. To prevent large voltage transients at the drain of the top MOSFET, a low-ESR electrolytic capacitor and a good-quality ceramic capacitor must be connected between the MOSFET drain and ground (VSS).
3. To avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the source of the top MOSFET and the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
  - The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver must be placed as close as possible to the MOSFETs.
  - The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

### 10.2 Layout Example

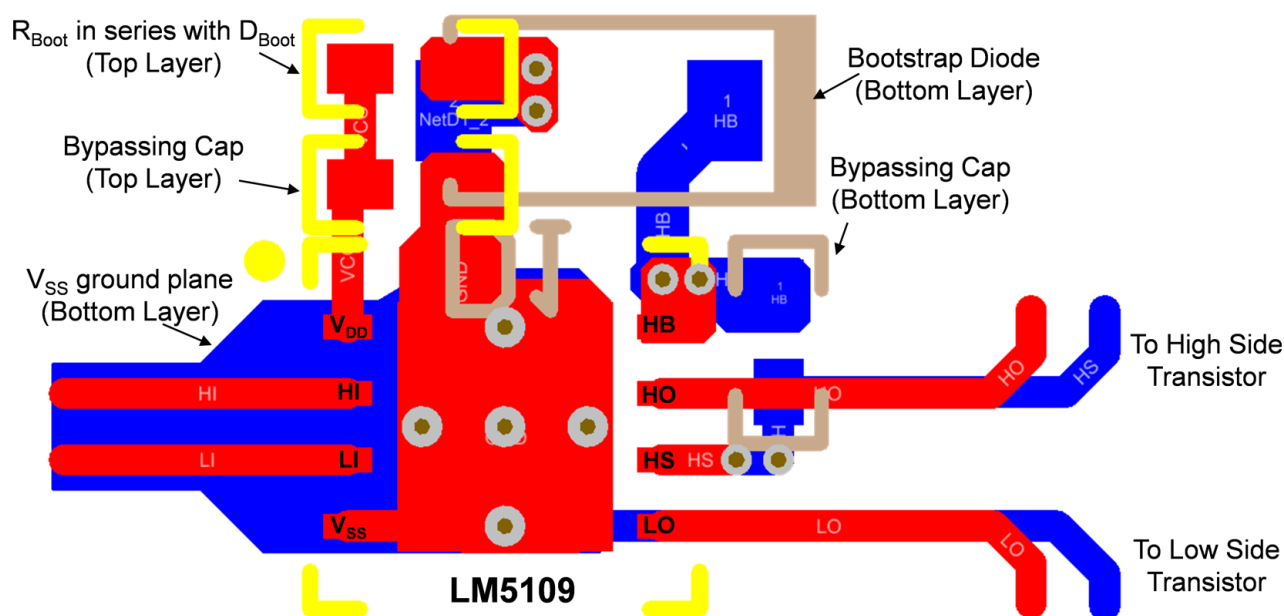


Figure 17. Layout Example



## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- *AN-1317 Selection of External Bootstrap Diode for LM510X Devices*, [SNVA083](#)
- *Semiconductor and IC Packaging Thermal Metrics*, [SPRA953](#)

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5109BMA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	L5109 BMA	
LM5109BMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5109 BMA	<a href="#">Samples</a>
LM5109BMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5109 BMA	<a href="#">Samples</a>
LM5109BSD/NOPB	ACTIVE	WSO	NGT	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	5109BSD	<a href="#">Samples</a>
LM5109BSDX/NOPB	ACTIVE	WSO	NGT	8	4500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	5109BSD	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5109BMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5109BSD/NOPB	WSO	NGT	8	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

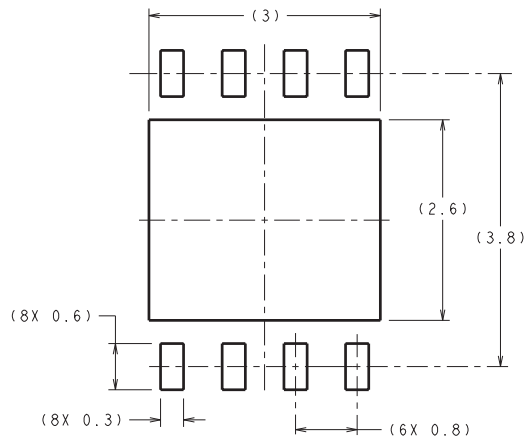
## TAPE AND REEL BOX DIMENSIONS



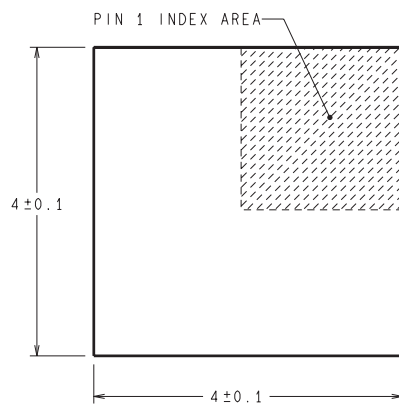
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5109BMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5109BSD/NOPB	WSON	NGT	8	1000	203.0	203.0	35.0

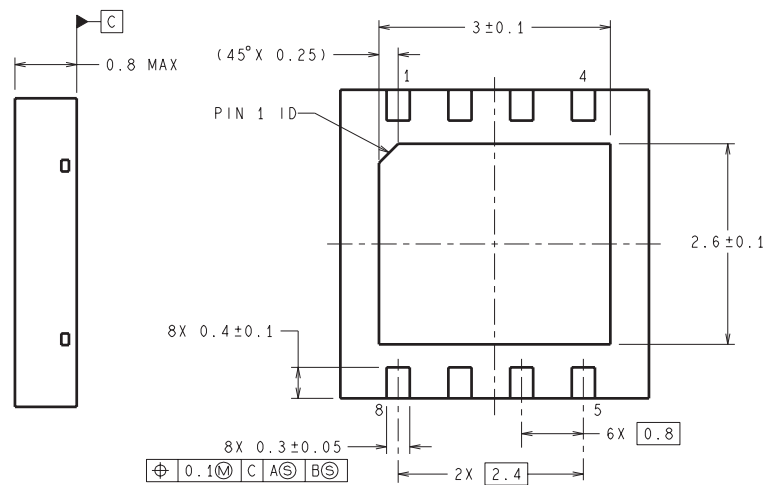
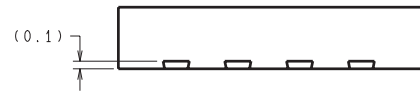
NGT0008A



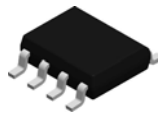
## RECOMMENDED LAND PATTERN



**DIMENSIONS ARE IN MILLIMETERS**  
DIMENSIONS IN ( ) FOR REFERENCE ONLY



SDC08A (Rev A)



**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

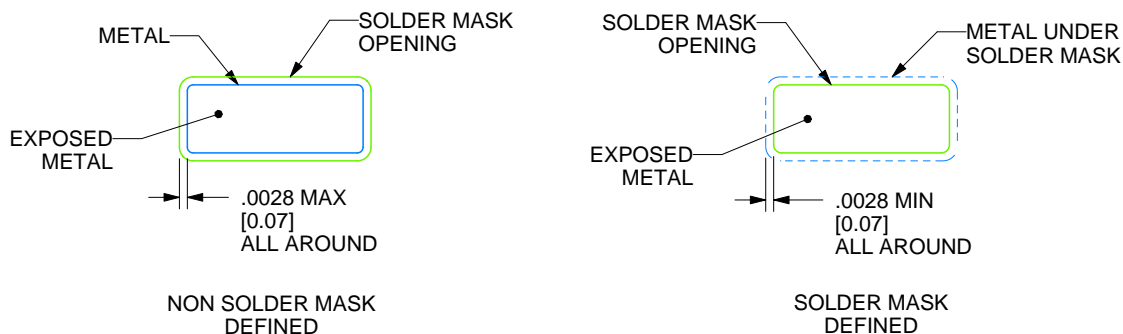
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

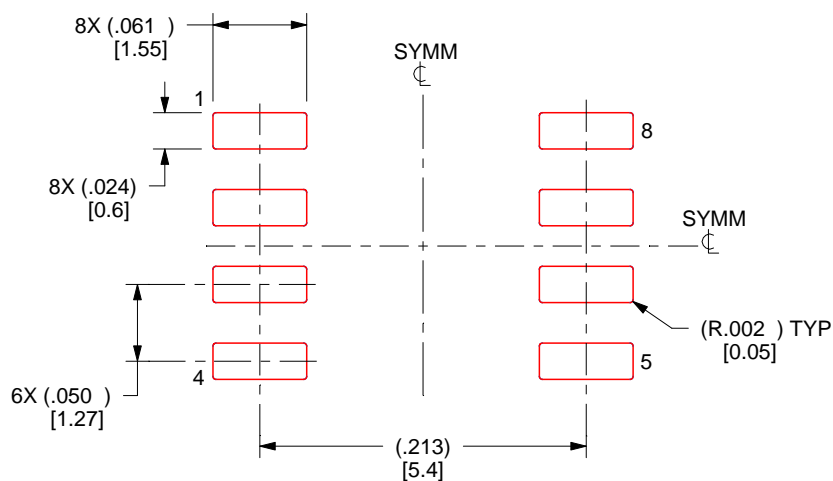
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



**D0008A**

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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