A Low Power and Low Signal 5-bit 25 MS/s Pipelined ADC for Monolithic Active Pixel Sensors

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Abstract—For CMOS monolithic active pixels sensor readout, we developed a 5 bit low power analog to digital converter using a pipelined architecture. A non-resetting sample and hold stage is included to amplify the signal by a factor of 4. Due to the very low level of the incoming signal, this first stage compensates both the amplifier offset effect and the input common mode voltage dispersion. The converter consists of three 1.5 bit sub-ADC and a 2 bit flash. We present the results of a prototype, made of eight ADC channels. The maximum sampling rate is 25 MS/s. The total DC power consumption is 1.7 mW/channel on a 3.3 V supply voltage recommended for the process. But at a reduced 2.5 V supply, it consumes only 1.3 mW. The size of each ADC channel layout is only 43 μm $*$ 1.43 mm. This corresponds to the pitch of two pixel columns each one would be 20 μm wide. The full analog part of the converter can be quickly switched to a standby idle mode in less than 1 μs; thus reducing the power dissipation to a ratio better than 1/1000. This fast shutdown is very important for the ILC vertex detector as the total DC power dissipation becomes directly proportional to the low beam duty cycle.

Index Terms—1.5 bits per stage, low power, MAPS tracker, pixel sensors, pipelined ADC, switched capacitor design.

I. INTRODUCTION

MONOLITHIC ACTIVE PIXEL SENSORS (MAPS) fabricated in CMOS technology offer several well known advantages for vertex detectors, high precision beam telescopes and imaging devices.

Granularity, flexibility, radiation tolerance, compactness, random access and fast read-out are among their most appealing characteristics. On the other hand, the associated readout electronics design is constrained in several aspects:

— the process used has to be chosen according to its particle detection performances (e.g. epitaxial layer thickness);
— the minimum readable signal may be very small (typically a couple of mV);
— the layout has to be adjusted to the (small) pixel pitch;
— the number of metal layers may be modest (4 or 5 only);
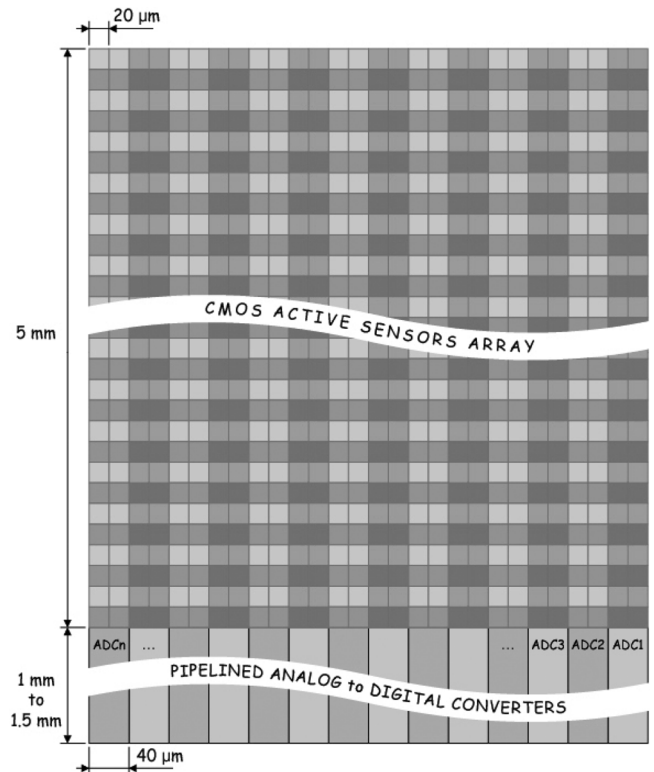— and, of course, the power budget is a critical issue.

Fig. 1. Sketch view of a MAPS array with a data conversion stage.

The design presented here follows the requirements of pixel arrays designed at IPHC-Strasbourg in collaboration with DAPNIA-Saclay, in perspective of the Linear Collider vertex detector [1]. The arrangement of the pixel array with its associated read-out and A/D conversion stages is illustrated in Fig. 1.

The IPHC develops fast sensors made of pixel columns read out in parallel, featuring an architecture allowing a frame read-out frequency in excess of 10 kHz. Each pixel includes a micro-circuit allowing the signal extraction by computing the difference between the reference level and the readout signal [2]. Each column is presently ended with a discriminator, which will be replaced in future by an ADC.

The pixel's columns width amounts to 25 μm at present, but it should become 20 microns in the next prototypes. The minimal signal delivered by each column is typically on the order of a mV, which translates into a first challenge for the read-out circuit design. Next comes the fast sampling rate ambitioned (10 MS/s). Finally, the power budget should remain as low as about 500 μW/column.

Due to the low value of the Least Significant Bit (LSB ~1 mV), the design of the first stage of this converter is critical ac-
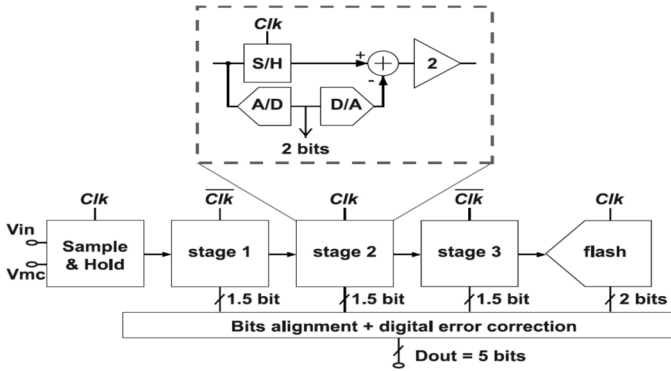
Fig. 2. General block diagram of a pipelined converter.

cording to the offset and the signal to noise ratio. With a sampling rate beyond 10 MHz, pipelined architecture is usually considered as a good compromise because it implies less power dissipation and area than a full flash. An overview block diagram is shown in Fig. 2 [3]–[5].

The first stage samples and holds the analog input signal. It is followed by a set of pipelined stages. Each one produces a digital estimate of an incoming held signal, then converts this estimate back to the analog, subtracts the result from the held input. This residue is then amplified before being transferred to the next stage. Eventually the last stage is a full flash that determines the least significant bits. The successive digital results from the pipelined stages are appropriately delayed throughout a bit alignment network. Then a digital correction stage helps to recover the errors due to the comparators offset. Therefore, low offset comparators are not necessary and the power consumption is reduced.

This paper describes hereafter each stage of this converter and we present some testing results.

II. THE SAMPLE AND HOLD AMPLIFIER (SHA)

Charge redistribution non-inverting architecture is used. Fig. 3 illustrates the sampling phase (phi2 is ON). "veeSH!" is the name for the virtual ground. The signal is stored onto the set of 4 sampling capacitors $(C37\ldots C40)$. Then during the HOLD (phi1), the charge is transferred to the feedback capacitor C23. This results to amplification by 4 of the differential signal between the reference (dark level) and the intensity level. Each capacitor unit in this scheme is 100 fF.

A. Offset Issues

The schematic used is not a full differential because the common mode feedback control that would be necessary is power or area consuming. Due to the low level of the signal, the pseudo differential scheme used is sensitive to the offset coming from different sources.

1) The Amplifier's Offset: During the sampling phase (phi2) the amplifier's offset is registered on the feedback capacitor C_{23} and kept at the amplifier's input. The signal $V_{in} - V_{offset}$ will then be sampled. The previous held signal $Vout_{(n-1)}$ was stored on C_{22}. The output of the amplifier is thus maintained at $Vout_{(n-1)} + V_{offset}$ and will not be reset: this architecture is
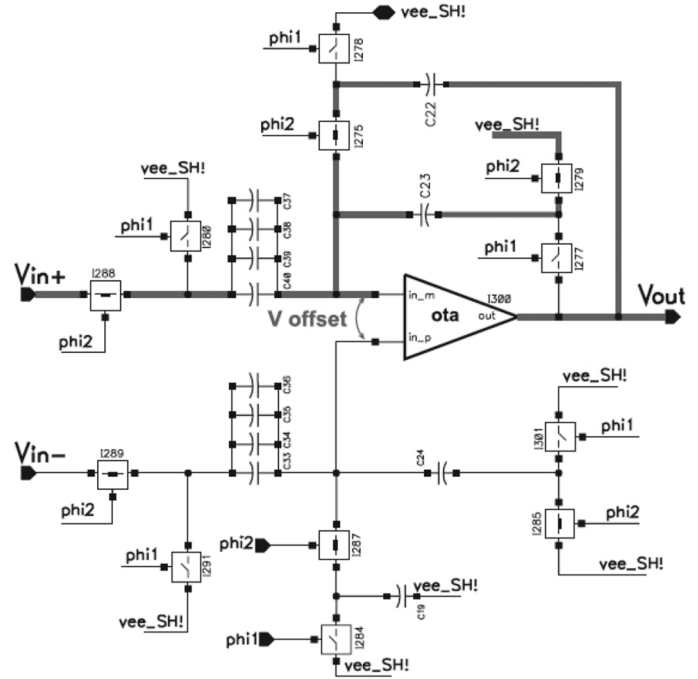
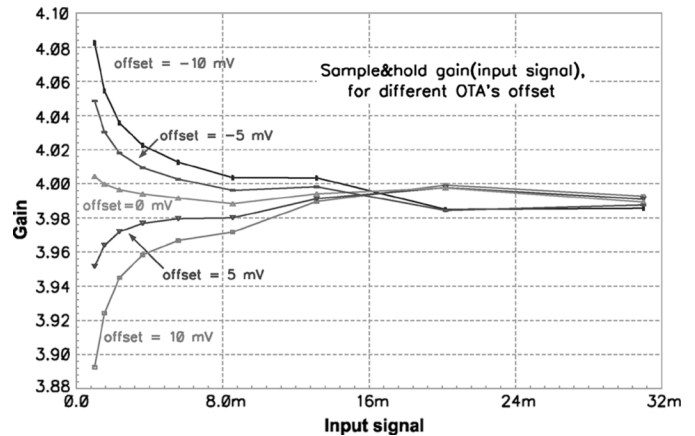

Fig. 3. Sample and Hold Amplifier (SHA) scheme.

Fig. 4. SHA gain according to the input signal, with the OTA's offset as a second parameter.

so called 'non resetting' SHA. During the HOLD phase (phi1), the charges are transferred from the sampling capacitors to the feedback capacitor C_{23} leading to an amplification in the ratio of the capacitors. Fig. 4 shows the gain variation according to the input signal. It stays close to the optimal value of 4, when the OTA's offset parameter varies from -10 mV up to 10 mV. One can notice a worse case error of 2.5% for the smallest signal. It comes from the OTA finite open loop gain as well as the parasitic capacitors effect. But this error is still acceptable for a 5 bit design.

2) The Charge Injections Offset: When the switches go to the "OFF" position, the charges coming from the transistors channel will create an offset that could be critical here since the capacitors are very small. This offset is controlled using "non overlapping 4 phase clocks" which are not detailed in the Fig. 3 scheme for ease of read.
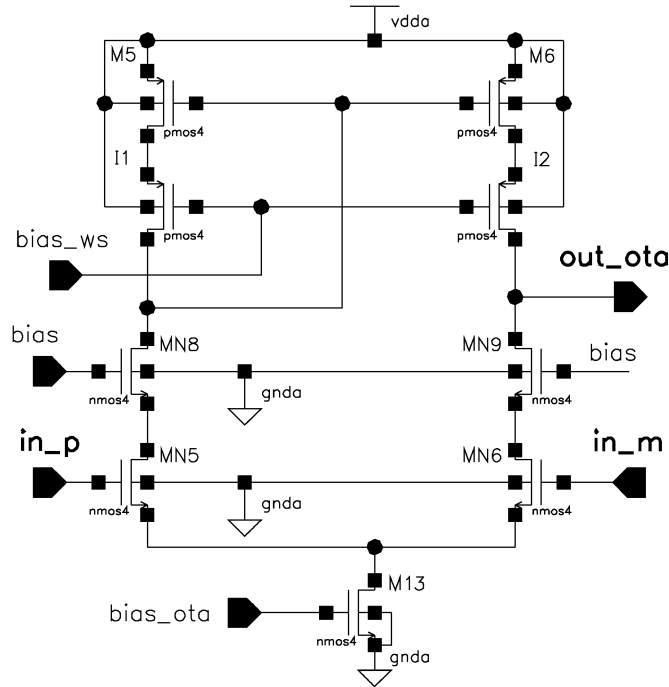
Fig. 5. A wide swing telescopic OTA.

Fig. 6. Bode diagram for the OTA on a 1 pF load.

Fig. 7. Bloc diagram of a 1.5 bit sub-converter stage.

3) The Pixels Common Mode Voltage Fluctuations: In Fig. 3 one can notice the symmetry between, the reference signal branch on one side going from node V_{in-} to the virtual ground "vee_SH!", and on the other side the intensity signal branch which is from node V_{in+} to the output node V_{out}. This symmetry reduces the fluctuations of the common mode level at the amplifier inputs even when the "dark level" from the pixel varies significantly.

4) The OTA's Input Parasitic Capacitor Effect: In the offset point of view, the finite value of the open loop gain makes this integrator very sensitive to the parasitic capacitors at the OTA's inputs. This offset could easily shift the output signal out of the converter's dynamic range. The random value of some parasitic capacitors will create also dispersion in the signal sent to the converter ADC. Hence during the layout design, great care has been taken with the OTA's input nodes.

B. Noise Issues

The KT/C noise is a critical parameter in this design because of the small value required for the capacitors to save area in the layout. The input sampling capacitor is only 400 fF which corresponds to a KT/C rms noise of 0.1 mV. Hence we have a safety margin of 1/10 between the rms noise and the minimum incoming signal. This ratio should be enough to maintain a quiet output code. Robustness against noise is maintained by taking care of additional thermal noise of the OTA.

C. The OTA Architecture

The amplifier designed for the SHA is used also for the converter multiplying stages. It is a telescopic cascode scheme as shown in Fig. 5 [6].

The current mirror load is a so called "wide swing cascode" [3]. It improves the dynamic range better than a basic cascode
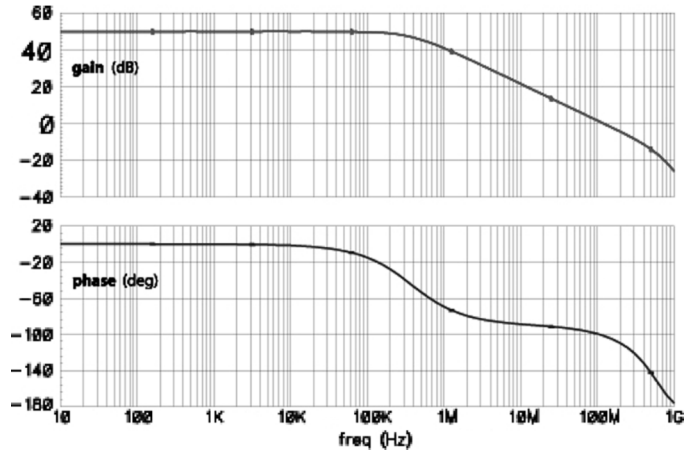
and makes the design robust for future low voltage version. The Bode diagram simulations results on a 1 pF load are shown in Fig. 6.

III. THE PIPELINED ADC

Fig. 7 illustrates the implementation of a 1.5 bit pipeline stage. The A/D block consists of two non critical comparators. The D/A conversion, subtraction, amplification, and S/H functions are performed by a switched capacitor circuit with a resolution of 1.5 bit per stage and an interstage gain of 2. Hence the transfer function of this stage is $Vs = 2 * Vin - \alpha Vref$ where α is set to 0 or 0.5 or 1, depending on the output code (b0, b1).

The transfer function for a 1.5 bit stage is shown in Fig. 8 by the continuous line. The dashed lines show possible variations of this transfer curve depending on the comparators offset spread. The expression "1.5 bit" is used to point out that only 3 combinations out of the 4 are acceptable for the output codes. The (1, 1) code is avoided, thereby the interstage amplifier should not saturate and this leaves room for the digital error correction.

This 1.5 bit configuration is particularly suitable to minimize the converter's total power dissipation because the amplifiers operate at a low closed-loop gain leading to a best settling time for minimum power consumption. Moreover this low gain per
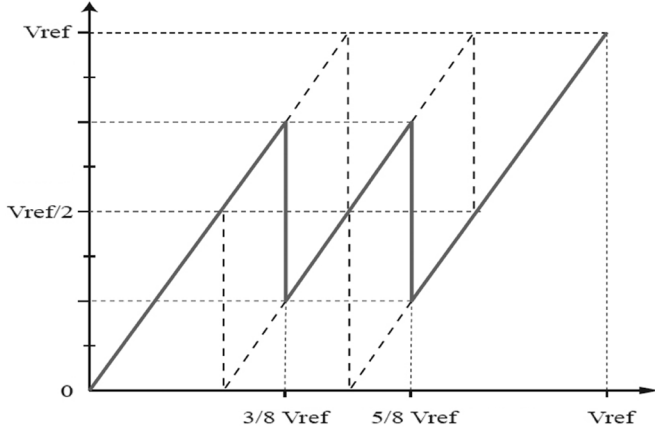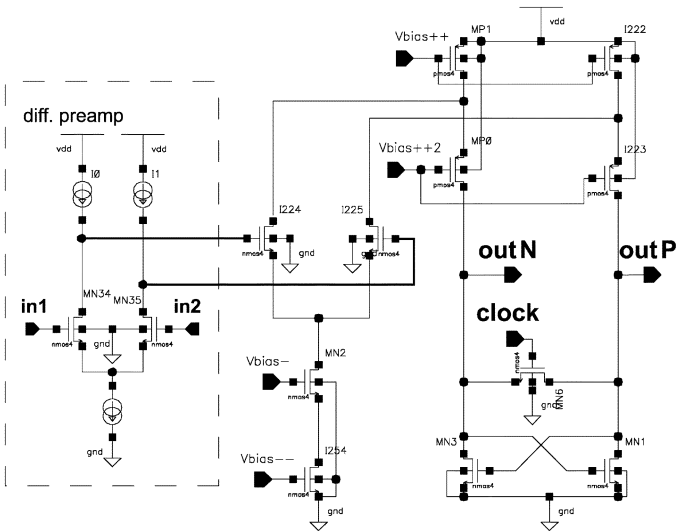
Fig. 8.   1.5 bits residue transfer curve.

Fig. 10.   The capacitive precise multiplier scheme.

Fig. 9.   The comparator scheme.

Fig. 11.   Layout of a prototype with 8 channel ADC.

TABLE I
POWER CONSUMPTION AND SAMPLING RATE TESTING RESULTS

	Sample & Hold	5 bits ADC	Full channel
Sampling rate	25 Mhz	25 Mhz	25 Mhz
Dimensions	43 μ * 250 μ	43 μ * 1250 μ	43 μ * 1500 μ
Power@3.3V	0.413 mW	1.287 mW	1.7 mW
Power@2.5V	0.313 mW	0.975 mW	1.288 mW

stage allows a maximum acceptable value for the comparators' offset, thus permitting low power latch architecture.

The maximum offset of these comparators is limited to Vref/8, where $\mathrm{Vref} = 4\,\mathrm{mV} * 2^5 = 128\,\mathrm{mV}$ is the full dynamic range. A simplified schematic of the comparator is given in Fig. 9. It consists of a low gain and low offset differential preamplifier followed by a latched folded cascode comparator [7].

A precise amplification by 2 is performed by two equal capacitors as shown in Fig. 10. The incoming signal is sampled during phase "phi1". It is amplified by charge redistribution during phase "phi2". During this amplification phase, the bottom plate of the sampling capacitor (C1) is connected to a reference voltage $\mathrm{Vref_i}$ which will be subtracted from the amplified signal. The residue resulting from this operation is transmitted to the next pipe line stage. The value for $\mathrm{Vref_i}$ is respectively 0 or $0.5 * \mathrm{Vref}$ or Vref depending on the comparators outputs (see Fig. 7). Vref is the dynamic range of the converter, with reference to the virtual ground.

A prototype has been designed in a CMOS 0.35 μ process from Austria Micro System. It includes 8 channels of this ADC. The 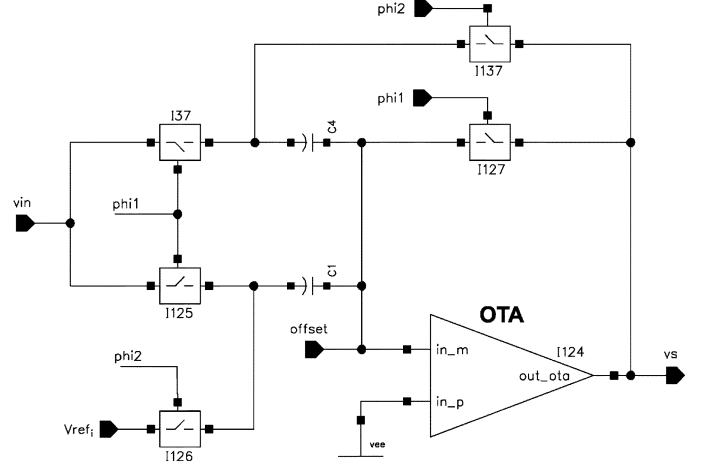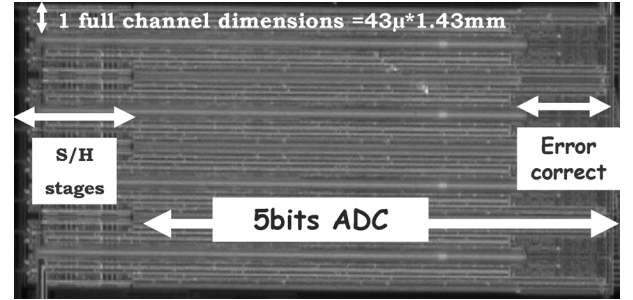layout is shown in Fig. 11. The dimensions of one full channel including the sample & hold stage is $43\,\mu\mathrm{m} * 1.43\,\mathrm{mm}$. One may notice also that the surface occupied by the digital error correction stage is about 1/5 of the full channel.

IV. TESTING RESULTS

The circuit has been tested successfully up to 25 MHz. This sampling rate and the power dissipation are summarized in Table I for two different power supply values (3.3 V and 2.5 V). The sample & hold consumption is specifically given to facilitate the comparison with other ADC designs.

The converter output differential and integral nonlinearity errors (*DNL, INL*) are shown in Fig. 12. For this test, the input signal was a sine wave with a peak-to-peak amplitude close to the ADC full-scale range. Then a statistical analysis method is applied to the output data. The DNL and INL were measured using a cumulative histogram method [8]. The DNL refers to the irregularity in the width of the quantization, while the INL quantifies the displacement of the transition levels from their nominal positions.
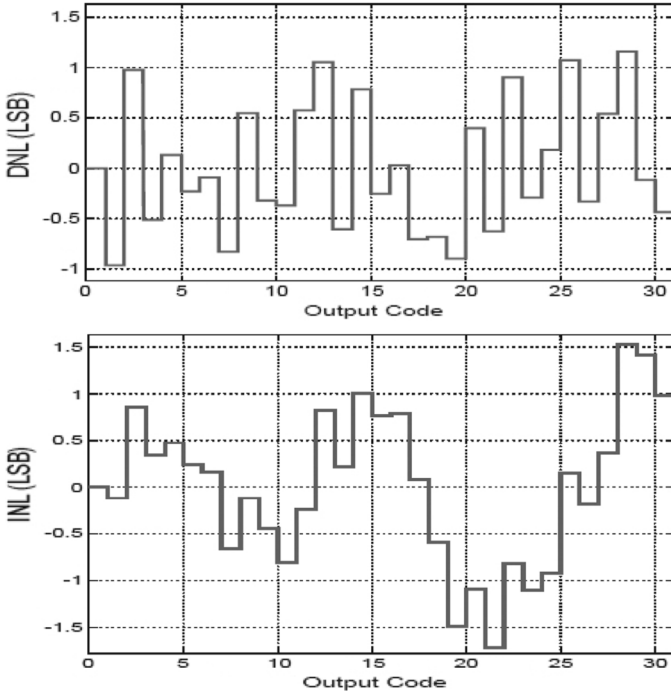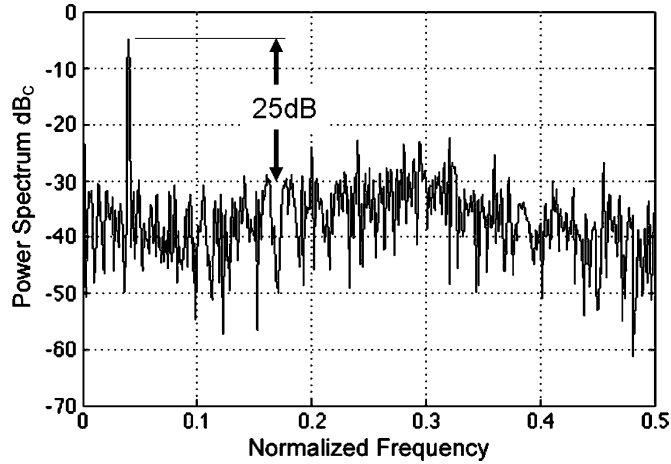
Fig. 12. Nonlinearity results: DNL and INL.

Fig. 13. FFT spectrum.

Fig. 14. Analog bias fast switching results.

Fig. 15. The full ADC wakening delay from the pulsing clock edge.

In Fig. 13 a fast Fourier transform spectrum for a 1 MHz sine wave input signal is shown. The frequency is presented normalized to the sampling rate (25 Mhz). The dynamic range is in the order of 25 dB. Some larger harmonics appear at medium frequencies and this point is still to be understood.

For the next ILC experiment, the beam duty cycle will be very low ($\sim$1%). It is therefore worthy to switch on the analog part of the circuit only when used, thus making the total power dissipation directly proportional to the beam duty cycle. This circuit includes such a fast and efficient "power ON" capability. The bias settling time result is given in Fig. 14.

From the falling edge of a pulsing clock, the bias current is settled after only 1 μs. In the standby idle mode (pulsing clock at high level), the full analog part of the converter is switched OFF and the analog power dissipation is reduced to a ratio better than 1/1000.
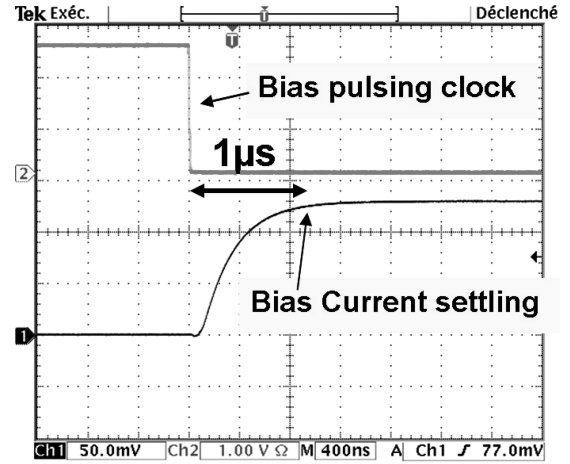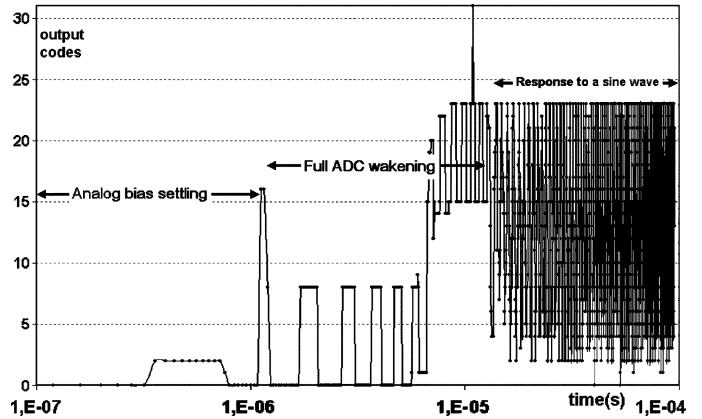
After the analog bias settling, there is an extra delay before the full converter can work properly. Fig. 15 shows how after a recovery time, the converter reacts to a sine wave input signal. One can notice the analog stages settling delay (1 μs); followed by a long recovery time (12 μs) for the full ADC, before then the correct output codes come out. A log time scale is used to emphasize the starting parasitic effect.

V. CONCLUSION

The design of a 5 bit 25 MS/s pipelined ADC has been presented, featuring the low level signal required for monolithic active pixel sensors. An output dynamic range of 25 dB is measured. The typical DC power dissipation is 1.7 mW. This converter is one of the possible candidates in perspective of the future International Linear Collider vertex detector. It includes an amplification sample and hold stage. A 1.5 bit/stage architecture is used for the converter in a non differential configuration. The layout deals with the pitch of the pixels array. The size of each channel layout is $43\,\mu$m$*1.43$ mm. We are still working to reduce the length of this converter's layout in our next version. A very efficient fast power pulsing is integrated with this circuit to reduce the total DC power dissipation according to the beam low duty cycle.

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