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Very Sensitive, Low Noise, Active Reset CMOS Image Sensor with In-Pixel ADC

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***Abstract*— Low light imaging is being researched intensively. The applications of increased sensitivity sensors expand to BioMed, security and communications providing low cost and effective alternatives to common imaging techniques based on microscopes, intensifiers etc. Lowering the inherent noise floor and achieving a higher sensitivity in CMOS sensor are found at the focus of the scientific society and new solutions emerge fast. Methods like output averaging, active reset (AR), and active column sensing (ACS) lower the noise floor but fail to provide the sensitivity boost, which requires a substantial signal amplification. The already proposed solutions, combining high gain and noise suppression still fall short of the sensitivity that would enable detecting a few electrons. This work proposes a very sensitive pixel, designed to capture an ultra-low illumination using three stage amplifiers' configuration, which allows for an effective reset operation and in-pixel analog to digital conversion (ADC). The provided measurement results prove the functionality of the proposed pixel architecture, indicating a remarkable sensitivity of 355V/lux*sec and detection limit of 3 electrons, achieved consuming only 6uW per pixel.**

***Index Terms*—Active Reset, Active Column Sensor, ADC, CMOS, Fixed Pattern Noise, image sensor, low noise, reset noise**

I. Introduction

BioMed, Bio-Mechanics, Biology are ones of the main beneficiaries of state of the art CMOS image sensors. Low power, low cost sensors embedded with sophisticated processing circuitry allow very sensitive and high speed optical signal detection [1]. Sensor sensitivity is crucial in a wide variety of Bio-Mechanical applications, where medical researches and professional sport teams are looking for monitoring biological activity within live tissues, muscles, the light emission of which is extremely low.

In the past, high sensitivity imaging was performed using bulky equipment scanning microscopes, intensifiers, Charge Coupled Devices (CCD) cameras. Development of CMOS Image Sensors (CIS) pushed the performance limits and allowed for light detection with no intensifiers added. The simplest method to increase the sensitivity is to design a pixel with a high conversion gain, which means to decrease the sensing node capacitance [2]. This solution is simple, but results in a sensitivity still below 10V/Lux*sec if preserving a decent frame rate.

Further sensitivity increase necessitates an active amplification. One of the most efficient solutions is to use a pixel comprising a Capacitive Trans-Impedance Amplifier (CTIA) [3]. Such a solution implies both active reset (AR) for the *KTC* noise suppression [4] and a sensitivity boost, proportional to the ratio between the photo-diode and the feedback capacitances. There are two adverse points: 1) the reset level is implied by the DC point of the single ended amplifier; 2) the capacitance ratio is bounded by the magnitude of the feedback capacitance. If this ratio is too small, it causes a substantial Fixed Pattern Noise (FPN), or makes the pixel susceptible to the parasitic charge injections.

There are a couple of methods to increase the signal boost. For instance, Single Photon Avalanche Diode (SPAD), a device capable of detecting a single photon [5] is one of the most common solutions for ultra-sensitive sensors. A single photon fallen onto SPAD can trigger a self-sustained avalanche event, which is transformed into a voltage spike, recorded by registers. The higher the light intensity, the higher the number of spikes latched into the memory. However, the exceptional SPAD sensitivity comes at expense of an increased power supply needed for generating the above breakdown electrical field. Though, recent advances of technology allowed for substantial power supply decrease, it is close to 5V, which is substantially higher than the typical power supply voltages. This complicates the sensor structure and increases the power budget for the SPAD based solutions. SPAD is also susceptible to dark current, which generates a finite undesired switching rate, reducing of which necessitates lowering an excess voltage over the detector, thus affecting negatively its detection probability.

Alternatively, an open loop amplifier can be accommodated inside a pixel [6]. This solution not only possesses an active reset, which lowers its noise floor, but not less important, the available signal boost is much more substantial than in pixels based upon the closed loop amplification. In the aforementioned work, the authors used a common source (CS) amplifier for self-reset and for signal boost. However, the achieved gain was comparable to CTIA and the FPN was relatively high. Thus, to achieve a low noise and high sensitive system, we propose: a) to perform the AR using a differential amplifier for the external control of the reset level; b) to use the same stage as a preamplifier for the further sensitivity boost, provided by the subsequent cascaded inverting amplifiers; c) to average the pixel output for the further noise reduction.

This work presents a modification of the AR technique, which in addition to low noise performance is aimed to reach a sensitivity of 300-400V/Lux*sec. the proposed pixel architecture is based upon three stage amplifiers' configuration: 1) differential amplifier for self-reset and signal boost; 2) & 3) single ended amplifiers for performing an analog to digital conversion (ADC). The presented design was implemented and measured experimentally. Herein, we characterize the prototype performance from a single pixel behavior to a final image capture.

In the experimental verification process, we came across some interesting tradeoffs, concerning the sensitivity, and signal to noise ratio (SNR). Therefore, we present a mathematical model, connecting these two parameters, with which the designers can obtain the optimal balance between the signal amplification and the picture quality. The subsequent paper chapters are: Schematic Design & Layout, where the overall sensor structure, reset configuration, pixel considerations and layout are discussed; Simulation Results, where we present the anticipated pixel performance; Experimental Results, where we present the measured figures of merit (FOMs), and Conclusions- is the section, which summarizes the study.

II. Schematic Design & Layout

A. Sensor Structure

The implemented sensor comprises *32 by 32 Low noise Digital Pixels' Array*, *Row Decoder* coupled with *Row Logic* blocks, and *Column Decoder* block for information readout (Fig. 1).

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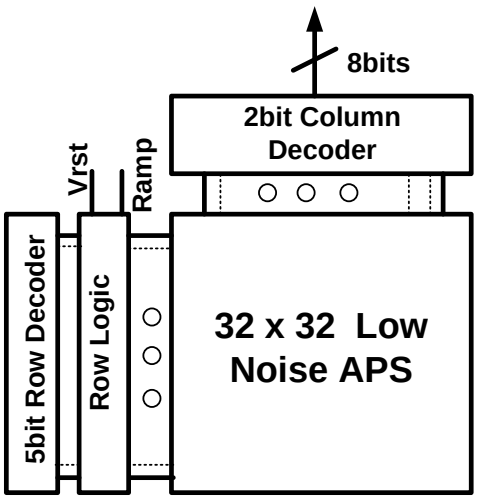

Fig. 1. Overall sensor architecture

The pixels' array operates in a rolling shutter mode, controlled by the *Row Logic* block, which asserts the corresponding command to the designated row by *AND*ing it with the *Row Decoder* select signal. Each row commences the photo-induced charge integration applying the active reset (AR). As a certain row finalizes the integration phase, it is selected for a single slope ADC, which is performed completely inside the pixel. At the same time, by means of the *Column Decoder*, groups, consisting of eight pixels, are selected and wired to the 8bit bus *Out* (Fig. 1), which is connected to the eight off-chip 8 bits counters. The in-pixel ADC generates a trigger once the reference meets the analog pixel level, thus creating a 8 bits digital word, which is further transferred to the screen. The analog voltages, such as reference and biases, required for pixel operation are generated off-chip and are fed externally to the chip core.

B. Pixel Structure

In previous work [1], one of the conclusions was that it would be beneficial to accommodate high gain amplifiers facilitating the Active Reset (AR) operation entirely inside the pixel. This way, the pixel will be substantially less susceptible to the coupling effects, rising from sharing analog busses within a single column. In addition, we found that switching of amplifiers' configuration negatively affects the signal integrity due to abrupt shifts in a DC operating point of the pixel readout circuitry. These findings were adopted as guidelines in our current design.

The pixel in Fig. 2 consists of photo-diode *(PD)*, AR switch, activated by *S_AR* signal, driven by the *Row Logic* block (Fig. 1); differential amplifier *(M1-M6)*; *Amp*- two cascaded common source amplifiers; an access switch to *Column Bus*, activated by *Row_S* signal. In addition to high and low power supplies *AVDD* and ground, we need three voltages, namely: *Bias_0*, *Cas_N*, and *Bias_1*. *Bias_0* controls the gate of *M4* that sinks the current from the differential pair *M1*, *M2*, whereas *Cas_N*, controls the cascode transistor *M3*, which increases the overall sink resistance at the point *S*, and levels up the common mode rejection ratio (CMRR). Transistors *M5* is the first stage output (*D1*), biased by the diode connected transistor *M6* (*D2*). The next two stages inside the *Amp* unit are biased by the *Bias_1* line. All the bias voltages are generated on the chip test-board.

Total transistor count is 14, which results to a relatively large pixel size of 30um x 30 um. However, in the future the designers plan using a pinned photodiode (PPD), which will enable to share effectively the amplification and ADC circuitry among 4 or more adjacent pixels [7]. Further optimization will involve pixel output adjustment to eliminate the complimentary phase in the access and active reset and switches.

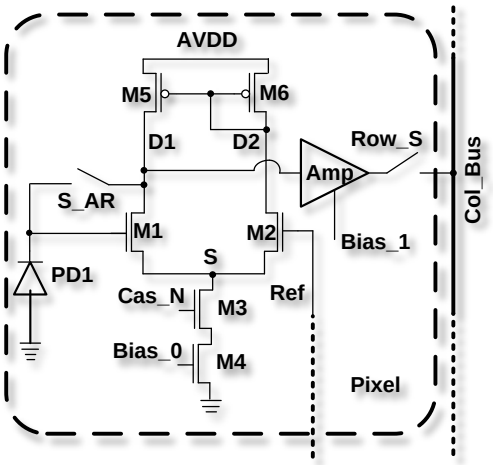

Fig. 2. Low noise, high sensitivity pixel schematic

C. Active Reset Using a Single Operational Amplifier

The pixel array operates in a rolling shutter method, when each row is reset, let to integrate and then digitized. To ensure smooth operation of the array, the pixel reference terminal *Ref* is driven through the *Row Logic* block. As long as the pixel is unselected, the logic block asserts a constant reset voltage V_{rst}. Once the pixel selected either for reset or for ADC, the node *Ref* is connected to a time varying signal *Ramp* (Fig. 1). This way, the gate potentials of *M2* (Fig. 2) inside the unselected rows are well-defined throughout the frame and the, undesired pixels' output switching are prevented.

During the reset phase of the i-th row, *the Ramp* signal becomes equal to the reset level V_{rst}. After the *Row Logic* block asserts this level to the node *Ref*, the signal *S_AR* is pulsed high, connecting the photo-diode *PD* to the *D1* node (Fig. 2). The formed unity gain connection of the differential stage, forces the node *PD* to become equal to the *Ref* level. Neglecting the parasitic feedback capacitances and the reset switch trans-conductance [4], the *KTC* noise maximal injections converge to:

$$\sigma_{kTC} = \sqrt{\frac{kT}{A_{diff} C_{PD}}} \quad (1)$$

, where k is the Boltzman Constant, T is the photo-diode ambient temperature, and C_{PD} is the photo-diode capacitance, and A_{diff} is the open loop gain of the differential stage. Resetting the photo-diode to a predetermined level, set by the analog bus *Ref*, provides an additional degree of freedom in tuning the pixel response, optimizing it for maximal gain dc operating point, contrarily to reset performed using a single input amplifier [3], [6], where the reset level is dictated by the current equilibrium throughout the stage. Moreover, using a single stage amplifier for the active reset operation yields a positive phase margin (PM), approaching 90^o eliminating a need for a frequency compensation network.

D. Charge Integration & In-Pixel ADC

The integration commences as *S_AR* signal goes low. The *PD* discharges with accordance to falling light intensity. Whilst the voltage of *PD* decreases, the terminal *Ref*, shared by the entire row remains constant till ADC phase starts. Therefore, the amplifier analog level and the *Amp* unit (Fig. 2) output are of no importance at this stage.

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ADC phase is performed in a row-by-row after the integration period elapsed. At this stage, differential and the *Amp* stages form high gain comparator, driving the *Column Bus*. Note that the comparator configuration is inherent and no switching is required to perform the ADC. We chose the simplest form of conversion- a single slope ADC, performed by a monotonously climbing signal *Ramp* (Fig. 1). Prior the conversion, the reference signal *Ramp* is reset initializing the comparator output to a "low" state. Then, the reference starts climbing, spanning the available *PD* range. The moment, the *Ramp*, crosses the *PD* level, the comparator flips its output to a "high" state. This change of state, through the *Column Decoder* is delivered to a corresponding register, stamping the generated so far digital count into registers located at the periphery (Fig. 1). The generated digital word is streamed to the screen to obtain the final image.

Important to note that ADC is performed 4 times, separately for each group, which might rise discrepancy between the pixels, exposed to the same light intensity, but residing within different groups of the scanned row. However, this issue can be resolved easily by minor adjustments in the counter values' range. The counter values' range will be rescaled by the ratio of the integration times of each of the four groups to the nominal integration time. Since there are four groups only and each ADC cycle is short, the adjustments are minor. If the sensor is exposed to extreme light conditions, then due to a certain dynamic range loss the proposed rescaling will cause some information loss, however, since we aim to capture mainly under low light intensities, this scenario becomes out of scope.

E. Layout

The pixel layout was performed in standard 4 metals 2 poly 0.35 um technology using area and coupling minimization techniques. The resulted pitch is 30um with 16.3% fill factor (FF).

The photo-diode is formed by an overlap of n-well region over p-substrate. Each photo-sensing area is encircled by a p-implant guard ring, biased at ground potential, for the crosstalk minimization. The area, surrounding the photo-diode, was covered with the top metal, shorted to the high power supply *AVDD* (Fig. 2), thus preventing an un-desired e/h pair optical generation and efficiently delivering the power to every pixel within the array.

The control lines and the pixel bias buses were laid to facilitate dense and minimized coupling layout. Digital control lines such as *RS* and *S_AR* with their complementary phases were separated from the analog buses i.e. placed in different pixel regions. Moreover, adjacent lines in both of the groups were implemented using Metal2 and Metal3, allowing for less coupling and for a closer placement. The output bus was implemented in Metal1, laid orthogonally to the rest of digital and analog lines, resulting a minimal coupling between them.

III. Simulation Results & Noise Analysis

During the design process, we performed numerous simulations both in time and frequency domains. Herein, we would like to concentrate on the AC simulations, since they determine the noise suppression, and the ADC precision.

Fig. 3 depicts the key AC characteristics of the proposed pixel. The utilized reset scheme is very promising, since it allows for both accurate reset and precise ADC employing the same constant amplifiers configuration. Since the reset is performed using one amplifier, we obtain a first order stable feedback system with remarkable phase margin (PM) of 75^0 (Fig. 3a). The gain of this stage is 35dB, which enables to suppress remarkably the *KTC* noise and to increase the sensitivity by almost two orders of magnitude (Fig. 3b). However, such a high gain imposed a gain restriction of the overall comparator for performing the ADC.

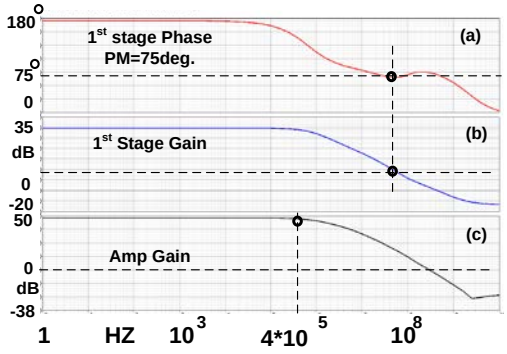

Fig. 3 a,b,c. AC pixel response: a) Phase of the 1st stage; b) Gain of the 1st stage; c) Amp gain.

The in-pixel comparator is formed by the differential amplifier and the unit *Amp* (Fig. 2). To attain 8 bit conversion resolution, the minimal gain of the unit *Amp* had to be 256, i.e. 48dB. We succeeded to achieve 50dB gain by cascading two common source stages, (Fig.3 c). Taking into account the gain of the 1st stage, we obtained a total amplification of 85dB. Such a boost limited the photodiode swing to 30mV, which decreased the intrinsic SNR, as will be discussed later on. The comparator bandwidth (BW) of 400 kHz, allowed for a clock cycle of 2.5us, making the overall conversion time 640us. However, we took advantage of two facts: 1) the comparator output flips only once during the whole conversion; 2) the comparator output changes mostly linearly between the "low" and the "high" state. Therefore, we could use much faster conversion clock and then to compensate for the anticipated comparator delay. The chosen clock cycle was reduced to 200ns, resulting 52us of a total conversion time.

A substantial decrease in the pixel swing compelled us to search for an appropriate noise reduction. The main noise sources are: the *KTC* or, so called "reset" noise, photo and dark generated shot noise, and the readout noise, having the following standard deviations σ_{kTC} (1), σ_{photo_shot}, σ_{dark_shot}, σ_{read}, respectively. Assuming a signal level V_{sig}, the overall signal to noise ratio for a single capture is given by:

$$SNR_0 = 20\log_{10}\frac{V_{sig}}{\sqrt{\sigma_{kTC}^2+\sigma_{dark\_shot}^2+\sigma_{photo\_shot}^2+\sigma_{read}^2}} \quad (2)$$

Relying on the process data and the noise simulations, we assessed the noise floor to be 4e-rms. It was not satisfactory, since we wanted to detect signals lower than that limit. Therefore, taking into account that all the noise sources are uncorrelated, we decided to sample the pixel multiple times [8] N_{av} to get the following SNR_{av}:

$$SNR_{av} = 20\log_{10}\frac{N_{av}V_{sig}}{\sqrt{N_{av}\left(\sigma_{kTC}^2+\sigma_{dark\_shot}^2+\sigma_{photo\_shot}^2+\sigma_{read}^2\right)}} = \quad (3)$$

$$= SNR_0 + 10\log_{10} N_{av}$$

Using the derived equation, it is apparent that the minimal number of samples to overcome the noise of 4 electrons is 16.

Averaging the noise improves not just the minimal SNR, but also the maximal limit. Usually, the shot noise variance, limited by the photon flux, is given by:

$$\sigma_{photo\_shot} = \sqrt{\frac{qV_{\max}}{C_{PD}}} \quad (4)$$

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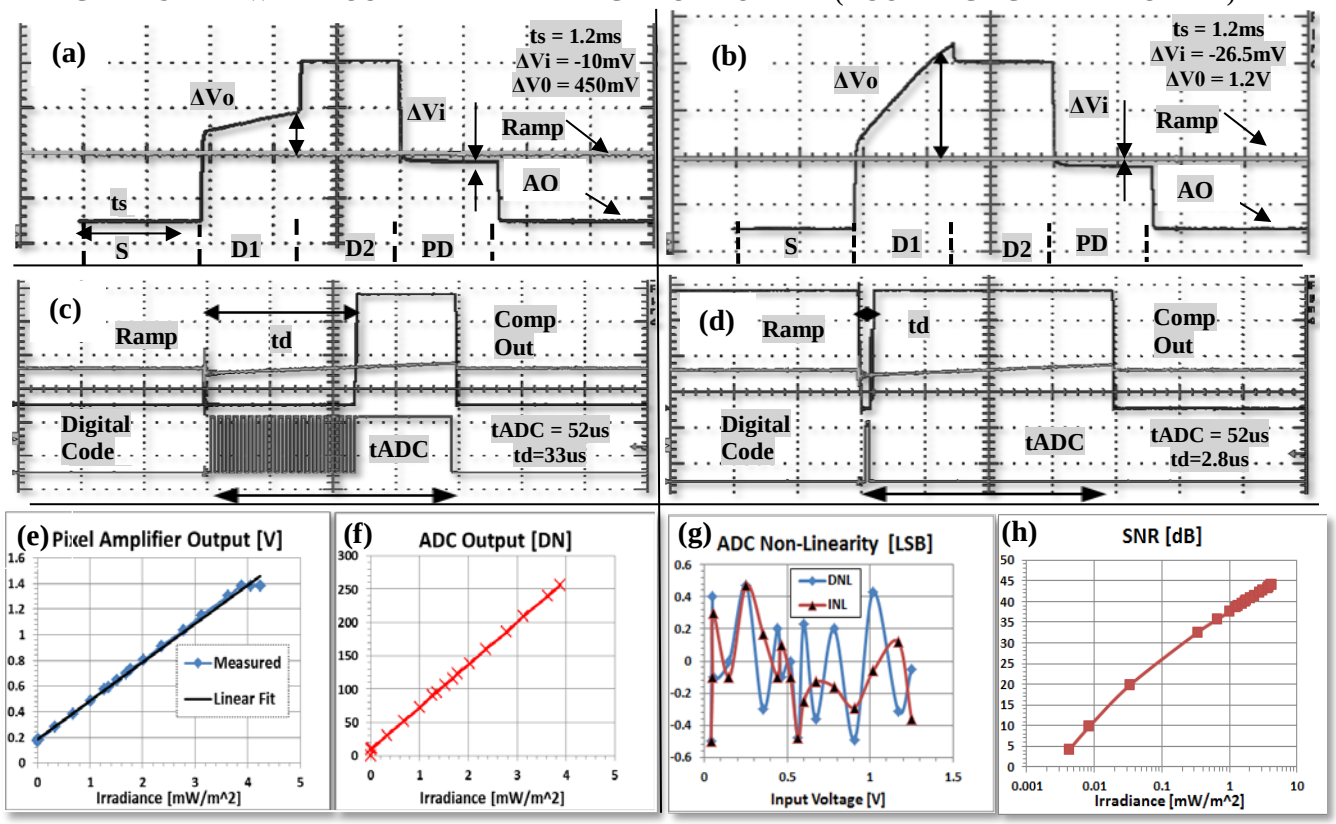

Fig. 4. **Pixel Response vs. Irradiance:** a) 1.4mW/m^2 ; b)3.8mW/m^2; **Pixel ADC**: **vs. Irradiance:** c) 1.4mW/m^2 ; d)3.8mW/m^2, e) Differential amplifier output @ Nav=16 , f) ADC Output @ Nav=16 , g) ADC Non Lin. Errors @ Nav=16. h) SNR @ Nav=16

,where q is the elementary electron charge and V_{max} is the maximal photodiode signal range, which is decreased if a signal boost is used. On the other hand, sampling the pixel multiple times increases its effective signal, thus compensating for the gain induced swing reduction. So, taking the amplification and the averaging effect into account, we obtain the following SNR_{max} limit:

$$SNR_{\max} = 20\log_{10}\sqrt{\frac{N_{av}C_{PD}V_{\max}}{qA_{diff}}} \quad (5)$$

Consequently, there is a tradeoff between the sensitivity boost and the final picture quality. The possible solution to attain a high sensitivity and feasible SNR is to increase the number of captures, but this step can compromise the sensor frame rate.

IV. Measurements Results

The fabricated pixel was tested for the conceptual functionality starting from the DC operating points of its components through the reset feasibility to ADC, leaving capturing of an image to a later research stage. After the DC points were established, we measured a sample pixel response to illumination. Using an on-chip unity gain opamp *AO* (Fig. 4 a, b), we scanned the pixel points of interest *S*, *D1*, *D2*, and *PD* (Fig. 2). For convenience of presentation, we provide a sample pixel response to three regions of illumination relative to saturation: low ~35%; and high ~95%, i.e. 1.4mW/m^2 and 3.8mW/m^2 respectively. The scan of each point started with an active reset and lasted for t_s. Points *S* and *D2*, representing constant bias points inside the pixel, as expected, were independent of the illumination level (Fig. 4 a, b). On the other hand, points *PD* and *D1* representing the input and output of the differential amplifier, changed according to the incoming illumination. Right after the reset, we can observe that *PD* converges to the reference level *Ramp* (0.93V). The chosen reset level is on the lower end of the input common range, which is over 2 Volts wide starting from 0.75V and going up to 2.9V (Table I). Then, as integration goes on, the photodiode *PD* discharges by *ΔVi*, while output *D1* charges by *ΔVo*, respectively. For example, under low illumination, a photodiode *PD* discharged by *ΔVi* of -10mV, while the output *D1* rose by 450mV, indicating a gain of 45, which is in a good agreement with the predicted value (Fig. 4 a, b). We can observe that right after the reset, *D1* deviates by 200 mV from the anticipated reset value. This happens due the amplified parasitic charge injections inflicted by the active reset feedthrough onto the *PD*. The injections' spatial variance on *D1* was assessed to be 6.7mV, which makes it the major offset FPN source (Table I). In the future, the offset component will be reduced employing the pinned photodiode (PPD) structure, which will enable for the correlated double sampling (CDS). The measured gain FPN component (Table I), indicates a spatial variance in an open loop of the in-pixel amplifier, which can be minimized by careful transistor sizing.

Feasibility of the in-pixel ADC was verified using an external voltage generator (Fig. 4 c, d). To prevent glitches on the ramp along its path from the generator to the in-pixel comparator, we decoupled carefully the relevant bus inside our prototype, minimized the switching activity on the test board, and picked the generator with an appropriate driving force. Each ADC phase starts as soon as both the signal *Ramp* and the comparator output *Comp Out* go low. Note, the lower and the upper bounds of the *Ramp* are set according to the *PD* swing. Following the reset, the reference climbs monotonously, spanning the *PD* signal. The higher the illumination, the lower is the *PD* level, thus we anticipate the *Ramp* to reach the input faster. Comparing Fig. 4 c and Fig.4 d, we conclude that the decision time t_d shortens from *33us* to *2.8us*, corresponding to the input illumination increase from 35% to 95% of the saturating intensity, respectively. It can be also observed that the *Digital Code* switching stop is perfectly aligned with the comparator decision. Each positive comparator pulse latches the corresponding *Digital Code* into off-board registers. For instance, under low conditions light the latched *Digital Code* is logic

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"1" (Fig. 4 c), whilst under the high illumination the resulted value is "0" (Fig. 4 d).

Table I
MEASURED CHIP CHARACTERISTICS

Pixel Figure of Merit	Value
Process	2P, 4M, 0.35 μm
Pixel area	30x30 [μm^2]
FF	16.3%
Input Common Range	0.75V-2.9V
Conv. Gain	26 μV/e-
Power Sup.	3.3V
Power per pixel	6μW
N. Floor @ no averaging	4 e- rms
Photodiode Swing	28mV
DR @ 16 Av. Cycl.	58dB
SNR @ 16 Av. Cycl.	43dB
Sensitivity [V/lx*s]	355
Offset, Gain FPN	0.65%, 0.75%
Det. Limit @ 16 Av. Cycl.	3e-
Max. ADC resolution	8 bit
Overall Gain	84dB
Row Exposure time	1.2ms

We also verified the overall ADC and SNR array performance. For the sake of uniformity, we present the ADC and SNR measurement with averaging for 16 cycles. We started by measuring the linearity of the differential amplifier, which was found to be linear by 98% (Fig 4e). The overall ADC response (Fig. 4f) was in close agreement with the response of the differential amplifier. Averaging of the samples improved substantially the ADC non linearity errors, reducing both the differential and integral non linearity (DNL, INL), respectively below 0.5LSB (Fig. 4g). The comparator decisions for every pixel had to be summarized and averaged for 16 times to improve the SNR, extending the detection limit to 3e- rms (Table I). Using the proposed reset structure the *KTC* noise was reduced, which extended the lowest detectable limit to 4.4uW/m^2 (Fig. 4h). The maximal value was observed near intensity of 3.9mW/ m^2, resulting dynamic range (DR) of 58dB (Table I).The measured noise distribution (Table II) indicates that the shot noise (*Shot*) contribution, consisting of photons (*ph*.) and the dark current (*d*.), is much more dominant than the *KTC*, the readout (*Read*) noise sources throughout 99% of DR.

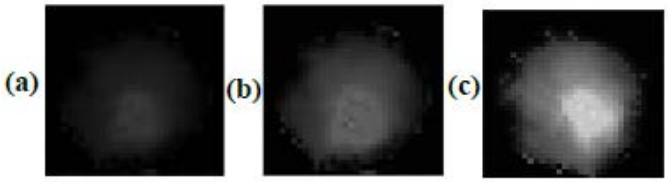

Fig. 5. Captures from two sensors**:** a) 3T pixel t_{int} =12ms; b) 3T pixel t_{int} =30ms; c) High sensitivity pixel t_{int} =1.2ms b) 3T pixel t_{int} =30ms; c) High sensitivity pixel t_{int} =1.2ms @ Nav16

To visualize the increased sensitivity effect, besides the discussed highly sensitive array (Fig.1), we accommodated an additional array consisting of basic 3T pixels [9]. We illuminated both of the arrays with the same 634nm laser. To mimic low illuminated environment, we positioned several attenuation filters in front of the laser source. The 3T based array was sampled after two integration periods 12ms and 30ms (Fig. 5 a, b), respectively; the increased sensitivity array was sampled using one integration time of 1.2ms (Fig. 5c). The results are in agreement with the expectations: 3T pixel, lacking the signal gain produces image slightly above 5 bits resolution (Fig. 5a). Extending the integration period, we increase the accumulated signal by 2.5 and thus add 1.3bits in average, making the total resolution 7 bits (Fig. 5b). Nevertheless, this image falls by 1 bit from the resulted 8 bits resolution of the highly sensitive array (Fig. 5c). The proposed sensor successfully captured the bright region of the laser beam and the dark ones, which generated a few electrons per capture.

Table III
NOISE DISTRIBUTION THROUGHOUT THE DYNAMIC RANGE [E-RMS]

	4.2uW/m^2	33uW/m^2	330uW/m^2	3.9mW/m^2
KTC	3.5	3.5	3.5	3.5
Shot (ph.& d)	2.5	5	12.5	36.5
Read	1	1	1	1
Total	4	6	13	37

V. CONCLUSIONS

We report a highly sensitive pixel with active reset using a cascaded amplifiers topology. The first amplification stage is used for the active reset and for a preliminary signal boost, which is equivalent to a similar sensitivity increase. The active reset, implemented with a single switch, and the reuse of a single amplifier for the reset and the sensitivity boost were proved to be feasible and functional. Subsequent two CS stages provide an additional gain to perform the ADC with a sufficient resolution. Reported measurements' results agree with the provided theoretical assessments. The primary advantage of the designed system is the ability to sense ultra-low optical signals due to an exceptional open loop gain of 84dB (Table I), which enabled to achieve a very high sensitivity and to span the amplified signal with a sufficient ADC resolution. The advantages over SPAD are: active reset minimizes the number of averaging cycles, causing the switching rate and thus the power to drop, while achieving remarkable sensitivity. Further work is to include a PPD based, scaled down pixel, featuring a selective power down, and utilizing a shared amplification and ADC structure. Using these improvements, and maintaining parallel data readout the pixel size and the power will be reduced, while the image resolution and sensor operating speed will be extended.

REFERENCES

[1] A. Spivak, O. Yadid-Pecht, "Design of a 128 x 128 CMOS APS with Extended Noise Suppression for High and Low Light Imaging Applications*", Int. Symp. on Circ. and Systems* (ISCAS), June 2014,pp.45-48.

[2] S. Min-Woong, *et al*., "A Low Dark Leakage Current High-Sensitivity CMOS Image Sensor With STI-Less Shared Pixel Design," *IEEE Trans. on Electron Devices*, vol.61, no.6, pp.2093-2097, June 2014.

[3] K. Murari, *et al*., "A CMOS In-Pixel CTIA High Sensitivity Fluorescence Imager," *IEEE Trans. on Biomed. Circuits and Systems*, vol. 5, no. 5, pp. 449–458, Oct. 2011.

[4] B. Pain, *et al*., "Reset noise suppression in 2-D CMOS photodiode pixels through column-based feedback-reset," in *Proc. Electron Dev. Meet. Dig. Int. Tech. Papers*, Dec. 2002, pp. 809–812.

[5] M. Perenzoni, *et al*., "A 160×120-pixel analog-counting single-photon imager with Sub-ns time-gating and self-referenced column-parallel A/D conversion for fluorescence lifetime imaging," in *IEEE Int. Solid- State Circuits Conference - (ISSCC)*, Feb. 2015, pp.1-3.

[6] C. Lotto; P. Seitz; T. Baechler, "A sub-electron readout noise CMOS image sensor with pixel-level open-loop voltage amplification," in *IEEE Solid-State Circuits Conference*, Feb. 2011, pp. 402 -404.

[7] D. Lee, *et al*., "Low-noise in-pixel comparing active pixel sensor using column-level single-slope ADC*," IEEE Trans. Electron Devices*, vol.55, no.12, pp.3383-3388, Dec.2008.

[8] A. Boukhayma, *et al*., "Temporal Readout Noise Analysis and Reduction Techniques for Low-Light CMOS Image Sensors," *IEEE Trans.on Electron Device*s, vol.63, no.1, pp.72-78, Jan. 2016.

[9] A. Spivak *et al*., "Wide-Dynamic-Range CMOS Image Sensors—Comparative Performance Analysis," *IEEE Transactions on Electron Devices*, Vol. 56, no. 11, pp.2446-2461, Nov.2009.

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