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Digital output for high performance MCT staring arrays

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ABSTRACT

The InfraRed staring arrays offered by SOFRADIR are more and more compact and offer system solutions in the different IR wavebands. The HgCdTe (Mercury Cadmium Telluride / MCT) material and process, as well as the hybridization technology, have been taken to an even more advanced level of sophistication to achieve these new staring arrays high performances. Latest developments have also been focused on the readout silicon circuit. A frame rate increase, new types of customized functions and digital converter are an important progress in this field. In order to match each system requirements, different flexible architectures of Analog To Digital Converter (ADC) have been developed. These developments implement specific requests in terms of frame rate, power consumption and resolution. Beyond the performance aspects, digital focal plan arrays can be considered as the first step towards a new low cost dewar family, since they allow for a more simple electrical interface on dewar designs. New results concerning these new readout circuit architectures are presented in this paper.

KEYWORDS

Infrared detectors, high performance, SOFRADIR, HgCdTe, IRFPA, small pitch, ADC

1 INTRODUCTION

The advantages of integrating Analog to Digital Converter (ADC) in cooled infrared (IR) focal plan arrays (FPA) are coming to light. This step in IR detector development will allow progresses in different ways. At first, this can be considered as a cost reduction at the system level, by cutting the necessity of implementing the ADC on the proximity electronic boards and by simplifying electrical interface including shielding. But cost reductions are applicable too at the integrated dewar detector level. Digital outputs can allow a simplification of the electrical interfaces, and by this way, a cost reduction of the price of some parts of the dewar. This is especially true in case of serial digital outputs. Integrated ADC is also a necessary step for integrating new functions in the read-out circuit, like automatic calibrations or data compression. At least, in a digital format, detector signal is less sensitive to the environmental perturbations.

The main limitation to ADC implementation in cooled sensor is ruled by the question: what is the price to pay in term of power consumption and size compared to the fully analog solution, for a comparable output signal quality, in term of SNR and linearity? The increased power consumption is both the direct power consumption needed to feed the converter but also, indirectly, the power needed to cool the increased size of the chip due to physical layout of the ADCs inside the readout circuit. To solve this problematic, Research and Development activities at Sofradir are oriented for proposing digital infrared detectors adapted to Sofradir's customers applications. Two kinds of ADC

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architectures are under validation. On the basis of these results, the choice of the architecture can be adapted to the system needs, addressing format from 320x256 to 1280x1024 pixels, pixel pitches from 15 to 30µm, and answering to frame rate frequency up to 120Hz for large format FPA.

2 ADC IMPLEMENTATION IN ARRAY SENSOR

2.1 Basic approaches

Analog to Digital conversion function have been integrated on image sensor chip since years in three main basic ways. The first one is output level ADC [1]: the pixel signals, after proper voltage conversion are multiplexed in column and then in line on one wire on which analog to digital conversion is performed. In this case, a unique ADC with sampling frequency operating at pixel rate needs to be designed.
The second one is column level ADC [2]: the pixels signals are multiplexed in column to the input of one ADC for each column. In this condition, the ADC sampling frequency is reduced to line rate. The line multiplexing is at digital signal level.
The third one is pixel level ADC [3][4]: the pixels signals are digitized directly by one ADC with sampling frequency at frame rate. In this case, data column and line multiplexing is digital.
Of course, lot of combinations can be generated from these basic architectures: one ADC for n pixels for pixel level ADC, or one ADC for n column for column ADC, or one ADC for n column and m lines for output level ADC. These combinations are equivalent to the basic solutions if we assume that one ADC operating at n*fs sampling frequency is equivalent to n ADC operating at fs sampling frequency with a n/fs delay between sampling time of two successive ADC. In both case the trade-off sampling frequency, power consumption is roughly the same. Only the ADC input signal bandwidth and sampling jitter constrain may produce major difference, but these limitations is not a major concern for most image sensor operating around 120Hz frame rate. For these reasons, in the following we will focus only on the three basic solutions.

2.2 ADC dedicated to cooled infrared detector

ADC power consumption issues will not help to choice the better solution because the three basic solutions are roughly equivalent for the same frame rate, SNR and linearity: one ADC operating at pixel rate will consume as much as n ADC operating at pixel rate divided by n and as much as n*m ADC operating at pixel rate divided by n*m.
So, the best ADC choice criteria for cooled sensor will be how much does the ADC architecture reduce the size and the power consumption of the fully analog circuit.

As far as output level ADC solution is concerned, the power consumption and area gain is not sensitive, because this solution consists in the addition of the analog circuit plus the ADC.
The area of the chip will be increased by the area of the ADC. Moreover, all the elements of the analog version of the detector are still there with the same specifications. The only change refers to the output driver sizing that could possibly be reduced, and thus its power consumption and size: on one hand, it just has to drive the ADC input sampling capacitor instead of the output capacitor induced by the signal path load and the external processing board . On the other hand, the ADC input sampling capacitor needs to be high enough to achieve good SNR and linearity, due to kT/C noise and component matching constraint. Thus the possibly gain in both power consumption and area will not be attractive. For this reason the output level ADC solution will not be interesting because it does not match the constraint of ADC integration in cooled sensor.
As far as column ADC solution is concerned, the line multiplexer and the output drivers that needs a large power consumption amount in the analog version are eliminated. However, the area gain is still not sufficient, even though the power consumption gain fixes the column ADC power consumption limit to an acceptable magnitude order.
The third solution seems the most suitable: the line multiplexer, the column readout amplifiers, the column multiplexer, as well as the output driver is suppressed. Moreover the analog chain between the pixel and the input of the ADC is reduced, which is favourable for electrical performances and signal processing.

Unfortunately, due to CMOS technology limitation, the pixel level ADC solution is physically difficult to design especially when the pixel step is small and when high ADC resolution is required. For this reason, the column level ADC solution will be preferred.
At column level, the sampling frequency of the ADC depends on the image sensor line frequency that is defined by the size of the array and the frame frequency.
Image sensor array in the array size, frame frequency range 320x256, 400Hz to 640x512, 120Hz would require ADC sampling frequency lower than 100KHz. At this sampling frequency, the ADC resolution need is more than 12 bits to perform both good SNR and linearity.
In this slow sampling speed, high resolution operating area, two families of Analog to Digital Converter are suitable: Integrating ADC and Sigma Delta ADC: sensor specifications as pixel pitch, column ADC area, and SNR, frequency, power consumption trade off will help to choice one or the other ADC class.

3 SIGMA DELTA ADC

3.1 Principle

Sigma Delta ADC is competitive solution for high resolution signal processing but with increased power consumption and size required by oversampling and digital filtering. In sensing application, the input signal is slowly varying with time and can be viewed as constant over conversion period. For this reason the special case of incremental sigma delta ADC where the integrator is reset prior to the signal conversion is of particular interest, especially for the design of optimal digital filtering [5]. In this condition, incremental sigma delta can have the same performance as conventional sigma delta at lower oversampling and hence lower power consumption. Moreover SNDR is better for bandlimited input signal due to idle tones reduction. The optimal filter is more complex than conventional sigma delta linear filter and thus its power consumption and size is increased but this extra power consumption is negligible compared to the saving in the analog front end.

3.2 Expected performances

The achievement of a stand alone incremental sigma delta test structure is under progress in collaboration with CEA LETI Grenoble [6]. In order to reach sufficient resolution, a second order incremental sigma delta ADC will be designed.

Based on a 0.35um CMOS technology, the column pitch will be 25um.
The goal of this test structure is to demonstrate that this ADC architecture is consistent with the constraints of cooled infrared detectors.
At 50KHz sampling frequency, the expected SNR is up to 86dB and THD is -90dB.
In the nominal condition, the power consumption including the digital filter will be less than 100uW per ADC.

Set-up adjustments and performances will be tested, in order to be able to anticipate results under different design. For future products, parameters like frame rate, resolution and power consumption can be foreseen in accordance with the pixels pitch in 0.35 silicon technology. As an example, this digital focal plan array can be developed: 128x128 format, 30µm pixel pitch, 300Hz frame rate, 20mW power consumption for the whole digital array.

4 INTEGRATING ADC

4.1 Principle

In parallel to the sigma delta validations, other ADC architecture has been developed. The starting point is a purely analog SOFRADIR readout circuit that is already in production [7]. The main characteristics of this circuit are: 640x512 pixels with 15um pixel step, operating at 120Hz with 35mW power consumption. The readout chip area is 1cm2 in technology CMOS 3.3V 0.35um. Due to a reduced pixel pitch and to CMOS technology limitations, the pixel

level ADC solution does not fit. So, the column level ADC solution was preferred. To be compliant with the SNR, linearity and frame rate of the touchstone analog circuit, our system study leads to an ADC resolution of 15 bits with a 62 kHz sampling frequency. Despite a possible degraded linearity risk, a single ramp dual slope ADC has been preferred to a single ramp single slope ADC. A single slope ADC would require a 1.9GHz counting frequency to match the ADC specification, which is out of the technology capability and out of the power consumption budget. The figure 1 shows the column ADC block diagram.

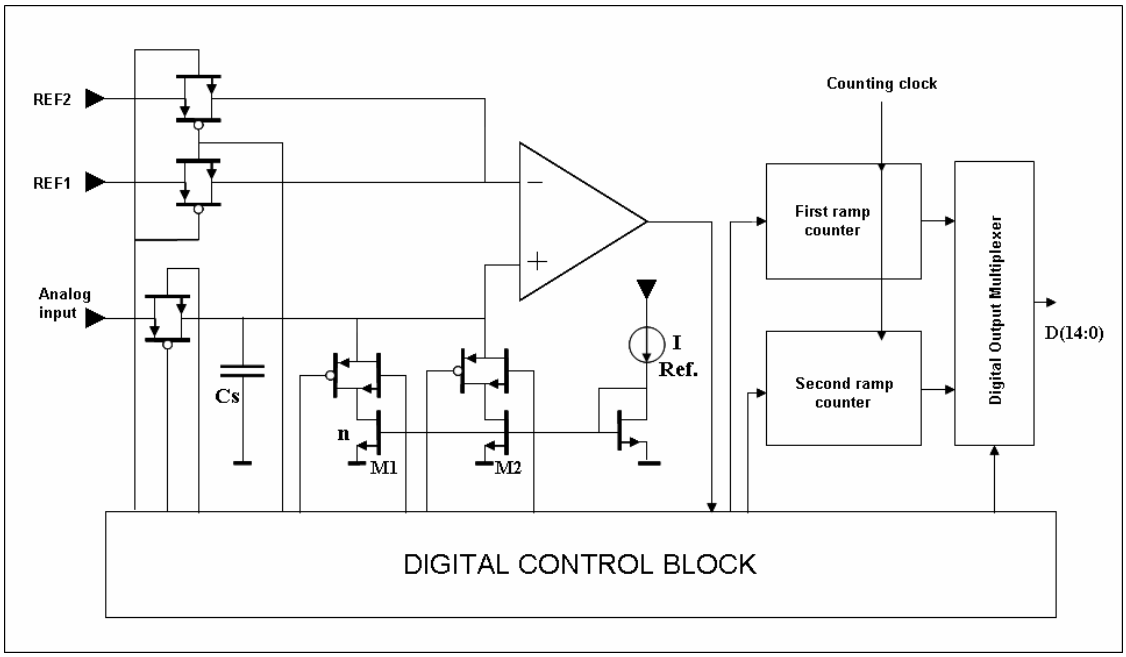

Figure 1: Integrating ADC

Figure 2 shows the voltage evolution at the positive input of the comparator.

In order to reduce power consumption and layout area, only one comparator is used: REF1 and REF2 voltage references are switched between the end of the first slope and the beginning of the second slope. Using only one comparator although correct the differential input offset error on voltage REF1–REF2 specifying the second slope voltage limitation. The absolute input error due to this comparator offset error on the first slope is corrected at system level as column offset during two points image calibration. To save power consumption, the two voltage slopes are simply generated by sampling input voltage in Cs capacitor and by applying two carefully matched current source M1 and M2 to this capacitor, one to generate the first slope, the other one to generate the second slope.At the conversion cycle end, the combination of the output of the two counter MSB and LSB gives the digital output value that would be driven out by the digital multiplexer at readout time.

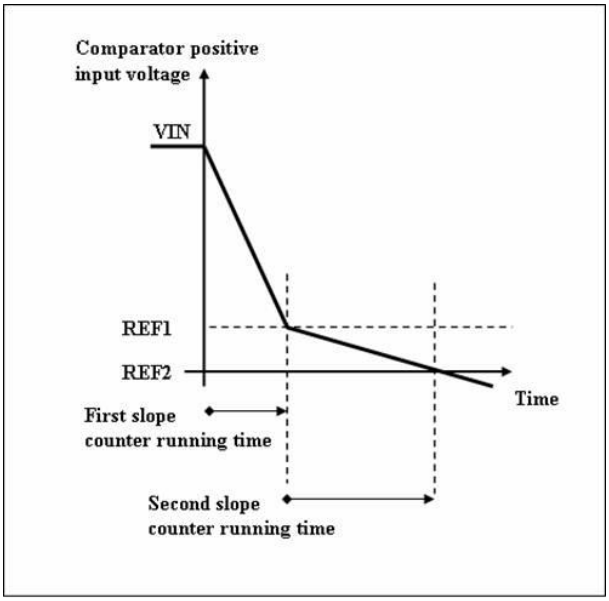

Figure 2: Voltage evolution, input of comparator

4.2 Results

This prototype read-out circuit was hybridized to MCT photo-voltaic array in mid-wave and full IRFPA tests have been performed.

Figure 3 shows photography of the original fully analog version on the right and the equivalent circuit integrating the 640 column converters on the left. The area of the chip is increased of 18%. Due to layout constrain, the column ADC pitch is not 15um but 30um. Even column ADC are at the right side of the pixel array and odd column ADC are at the left side.

At 120Hz nominal frame frequency, the power consumption is 65uW per ADC. This value is fully consistent with the use of cooled focal planes.

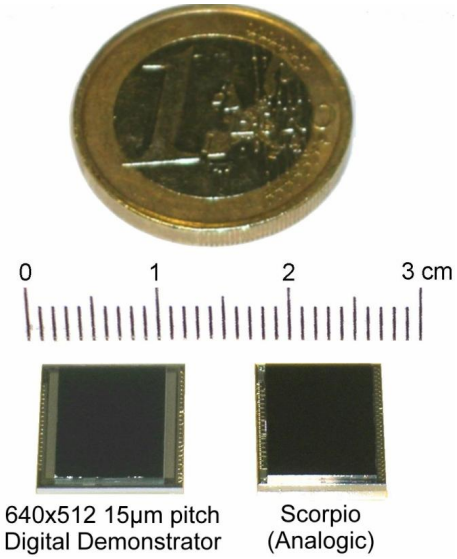

Figure 3: FPA pictures

Figure 4 presents the non-linearity variation of the read-out circuit versus the variation of the well fill obtained by integration time variation from 0.1 to 3.0 ms in front of 20°C scene temperature. This measurement demonstrates that the readout circuit non-linearity including the ADC non-linearity is better than ±0.5% over a large dynamic range.

Figure 5 shows the non-linearity variations of the detector in function of the well fill obtained by input flux variations. This non-linearity result, which is also under 0.5%, is representative of the whole detector performance, including photo-diodes characteristics. This measurement is performed at 1.2ms of integration time and with an input flux corresponding to a black-body temperature from 5°C to 45°C. The non-linearity observed upper than 70% of well fill is due to the field of view effect (pixels in the centre of the array begin to reach the saturation level).

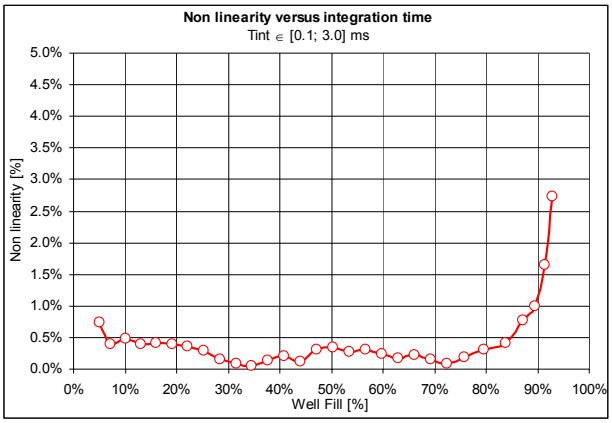

Figure 4: Non-linearity versus Integration time

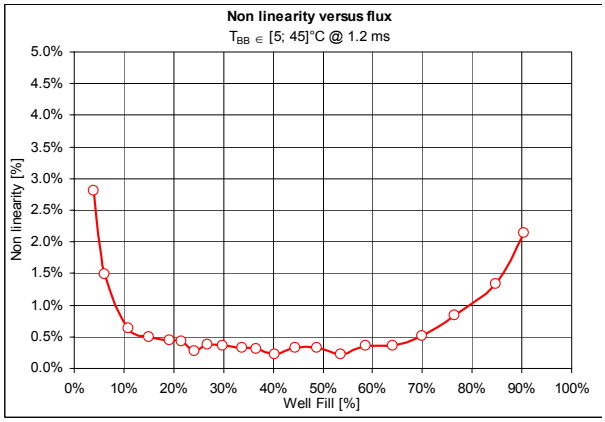

Figure 5: Non-linearity versus input flux

These results allow the validation of the choice of this design for such focal plane arrays.

On this first demonstrator, a problem of unexpected noise level was identified.
This was linked to a power supply noise due to power supply line sharing by the 640 converters. This power supply noise affects the comparator decision; especially while the second ramp, when low voltage amplitudes are processed.
Due to this fact, the measured SNR of the whole readout circuit was 72.7 dB. Taking into account the common part noise of the reference analog circuit, the ADC SNR estimation is 73.2dB. The reference circuit 80dB SNR outperform significantly this result.
Careful power line decoupling, combined with ADC digital activity optimisation will enable to reach the 80dB SNR target with a moderate chip area increase.

5 CONCLUSIONS

Sofradir developed a complete infrared staring array, 640x512 format at 15 µm pitch. The power consumption of this Read-Out circuit is not more than the current dissipated power of analog circuits, and is fully consistent with the cooled focal plane arrays.
In parallel, an other ADC architecture, a stand alone incremental sigma delta test structure, is under validation.
These two structures are complementary, and can answer to different specifications. For specific format or requirements, one of these architectures can be chosen. As a matter of fact, incremental sigma delta ADC is consistent with the choice of low formats and high speed, integrated ADC is well adapted to TV format at 15µm pitch like the SCORPIO detector. Based on these successful results, new Sofradir digital products will be offered in digital version beginning of year 2007.

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