14.3-bit extended counting ADC with built-in binning function for medical X-ray CMOS imagers

M.-S. Shin, J.-B. Kim and O.-K. Kwon

Proposed is a 14.3-bit extended counting analogue-to-digital converter (ADC) with built-in binning function for medical X-ray CMOS imagers. To reduce the area and improve the image resolution simultaneously, the proposed ADC internally performs the analogue binning operation without a charge amplifier. The ADC also uses an extended input range to realise true 14-bit dynamic range when applying the digital correlated double sampling technique. The proposed ADC was fabricated using a 0.35 μm CMOS process and the measured differential and integral nonlinearities of the 14.3-bit ADC are +0.97/−0.79 and +2.79/−1.70 LSB, respectively.

Introduction: Recently, the use of indirect-type X-ray CMOS imagers in digital radiography applications has increased because they have advantages of higher readout speed, lower noise, and a higher circuitry integration capability compared with X-ray imagers using amorphous silicon thin-film transistors [1]. Imagers for medical diagnostic applications using X-ray are required to have a full resolution mode for radiographic imaging and a binning mode for fluoroscopic imaging [2]. They also need high-resolution ADCs over 14-bit for high image quality. In the analogue binning method using a charge amplifier [2] for a binning operation it is difficult to acquire the image resolution over 14-bit because the charge amplifier requires high voltage gain and large sampling capacitors over 10 pF to reduce gain error and reset noise. Furthermore, a single-slope ADC used in [2] is not appropriate to obtain high-resolution images because the clock speed increases by a factor of 2 to raise 1-bit resolution. In this Letter, we propose the 14.3-bit extended counting ADC (EC-ADC) using a ΔΣ modulator instead of a charge amplifier for the 2 by 2 analogue binning operation.

Proposed pixel array configuration for analogue binning operation: Fig. 1 shows the block diagram of the pixel array and the readout circuitries for the analogue binning operation. Pixels on odd and even row lines are separately connected to two col lines as shown in Fig. 1. In the full-resolution mode, the readout operation of the pixel using three transistors is similar to the conventional one [3]. First, pixel1 and pixel2 are connected to ADC1 and ADC2 through col[1] and col[3], respectively. After A/D conversion, pixel3 and pixel4 are connected to ADC1 and ADC2 through col[2] and col[4]. In the binning mode, pixel1, pixel2, pixel3, and pixel4 are simultaneously connected to ADC1, and ADC2 is not used.

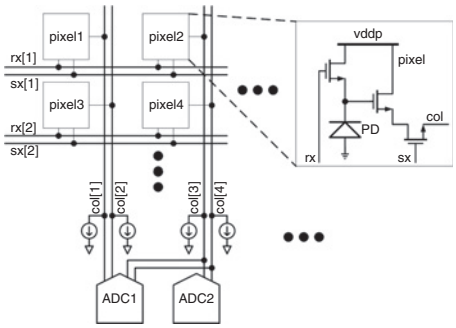

Fig. 1 *Block diagram of pixel array and readout circuitries for 2 by 2 analogue binning operation*

Proposed EC-ADC for analogue binning operation: The schematic and timing diagrams of the proposed EC-ADC, which indicates ADC1 in Fig. 1, are shown in Figs. 2*a* and *b*, respectively. The concepts of an EC-ADC were proposed to implement the high-resolution ADC and reduce its operating speed [4]. In our design, the first-order ΔΣ ADC converts the upper 3-bit and simultaneously performs the analogue binning operation. In the reset period, the charge of the integration capacitor (C_I) is fully discharged. The ADC performs different operations during the sample and hold (S&H) and ΔΣ modulation periods according to the operating modes, which are the full-resolution and binning modes. When the *bin_mod* is high, the ADC operates in the binning mode and vice versa. The ADC alternately receives the output voltage of a pixel through two column signal lines, col[1] and col[2], in the full-resolution mode. On the other hand, the ADC in the binning mode simultaneously receives four pixel output voltages through col[3] and col[4] of an adjacent column as well as col[1] and col[2]. To average four pixel output voltages, the capacitance of C_I in the binning mode should be four times larger than that in the full-resolution mode. The ADC repeats sampling and integration of the pixel output voltages eight times. The comparator output of the ΔΣ modulator is converted to 4-bit codes in the counter. In the last step of the ΔΣ modulation period, the ADC samples and integrates the common voltage (V_{CM}) to adjust the curve of the residue voltage (mod_aout) of the ΔΣ modulator as shown in Fig. 2*a*. The mod_aout is converted to 12-bit codes by a successive approximation ADC (SA-ADC) whose input range is between the positive and negative reference voltages (V_{REFP} and V_{REFN}). To correct the error from the offset of the ΔΣ modulator, C_I has double the capacitance of the sampling capacitor (C_S) and thereby the voltage range of the mod_aout is reduced to half of the input range of the SA-ADC. The error correction logic correcting the offset error uses an additional 1-bit conversion of the SA-ADC and finally outputs 15-bit codes. Because the voltage range of mod_aout is reduced, the input range (V_{IN}) of the EC-ADC is extended to 125% and is given by

$$V_{REFN} - \frac{3 \times (V_{REFP} - V_{REFN})}{16} < V_{IN} < V_{REFP} + \frac{V_{REFP} - V_{REFN}}{16} \quad (1)$$

Therefore, the output codes of the proposed EC-ADC ranges from 0 to 20479 (about 14.3-bit). The digital correlated double sampling technique (CDS) is used to reduce the column fixed pattern noise from the offset error of the ADC and pixel. However, the dynamic range of the column ADCs using the digital CDS is reduced because column ADCs use the input range of about 25% to cover the offset error of the ADC and pixel [5]. Therefore, the EC-ADC with the extended input range of 25% has true 14-bit dynamic range. The size of the capacitor array for the analogue binning operation is scaled down by a factor of the oversampling ratio due to the oversampling property, which makes it possible to layout the ADC in a small column pitch.

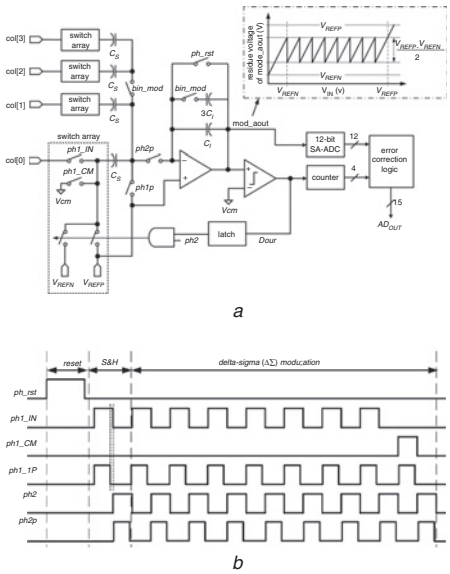

Fig. 2 *Proposed 14.3-bit extended counting ADC (EC-ADC)*

a Schematic diagram
b Timing diagram

Experimental results: For verifying the performance of the proposed EC-ADC, two column ADCs were implemented using a 0.35 μm CMOS process. Fig. 3 is the chip photograph of the column ADCs. For reading out 1.5 mega-pixels at 30 frames/s, the ADC has the conversion rate of 150 kHz. The area of the EC-ADC in a column is 100 × 1100 μm. The area of the ΔΣ modulator with the analogue binning operation is only 14% compared with a charge amplifier because the area of sampling capacitors is reduced to 1/8 by the oversampling. As shown in Figs. 4*a* and *b*, the measured differential and

integral nonlinearity of the 14.3-bit ADC are $+0.97/-0.79$ and $+2.79/-1.70$ LSB, respectively. The column ADCs can be applied to X-ray detectors with 14-bit dynamic range because the linearity of the ADC is not deteriorated in the extended input range as shown in Fig. 4. The power consumption of the ADC is 300 μW at 150 kS/s.

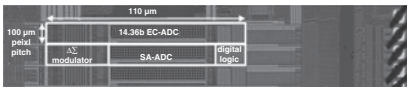

Fig. 3 *Chip photograph of proposed 14.3-bit EC-ADC*

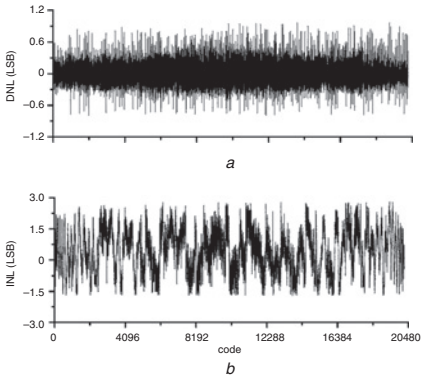

Fig. 4 *Measured nonlinearities of EC-ADC*

a Differential nonlinearity (DNL)
b Integral nonlinearity (INL)

Conclusion: A 14.3-bit EC-ADC is proposed for medical CMOS X-ray imagers. For the binning operation, the proposed EC-ADC uses the ΔΣ modulator instead of a charge amplifier. The area of the capacitor for the binning operation is reduced to 1/8 by the oversampling of the ΔΣ modulator and thereby the 14.3-bit EC-ADC is placed within a column pitch of 100 μm. Also, the 25% extended input range of the ADC realises true 14-bit dynamic range. Therefore, it is expected that the proposed EC-ADC is appropriate for high resolution CMOS X-ray imagers.

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