A 9-V/Lux-s 5000-Frames/s 512 × 512 CMOS Sensor

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***Abstract*—A high-responsivity 9-V/Lux-s high-speed 5000-frames/s (at full 512 × 512 resolution) CMOS active pixel sensor (APS) is presented in this paper. The sensor was designed for a 0.35-μm 2P3M CMOS sensor process and utilizes a five-transistor pixel to provide a true parallel shutter. Column-parallel analog-to-digital converter (ADC) architecture yields fast readout from pixels and digitization of the data simultaneously with acquiring a new frame. The chip has a two-row SRAM to store data from the ADC and read previous rows of data out of the chip. There are a total of 16 parallel ports operating up to 90 MHz delivering ∼1.3 Gpixel/s or 13 Gb/s of data at the maximum rate. In conclusion, a comparison between two high-speed digital CMOS sensor architectures, which are a column-parallel APS and a digital pixel sensor (DPS), is conducted.**

***Index Terms*—Active pixel sensor (APS), CMOS sensor, digital pixel sensor (DPS), high-speed imaging, shutter.**

I. Introduction

IMAGE sensors with the frame rate of more than 1000 frames/s are needed for variety of applications such as air-bag inspection, destruction testing, and ballistic tests. CMOS sensors have a number of architectural and performance advantages over CCDs that are crucial for such high-speed imaging. The pixel readout in the typical CMOS sensor is essentially column parallel, so the sensor, if designed properly, can easily support fast data readout through as many ports as needed for the given data rate. The digitization in a CMOS sensor is done on the chip. In combination with low-voltage operation, this results in considerable power savings on the camera level. Also, CMOS sensors show none of the high-speed CCD artifacts such as the panel-to-panel fixed pattern noise (FPN), blooming, and smear.

One of the first high-speed high-resolution CMOS sensors [1] was built using the 0.5-μm process, had a 10-μm three-transistor (3T) pixel, an 8-b column-parallel analog-to-digital converter (ADC), and operated at 500 frames/s with 1-Mpixel resolution. Yet, the sensor had a rolling shutter limiting its application and some visible column-to-column FPN because the ADC offset correction was only 5 b.

More advanced high-speed megapixel sensors with a true freeze-frame (or parallel) shutter were commercially available from Photobit, Fillfactory, and Fraunhofer Institute beginning in 2000; however, details of their implementation were not disclosed in the literature until now. Meanwhile, some shutter techniques, such as high-efficiency shuttering using pixel n-well [2] or performing 4T NMOS-only shuttering [3] were reported, but the performance of these reported sensors was not the best at the time. For instance, the pixel [2] had a very high dark current. The architecture [3] did not allow simultaneous exposure and pixel read. Also, the data rate [3] did not exceed 100 Mpixels/s.

Recently, an alternative high-speed digital pixel architecture was implemented [4]. The digital pixel sensor (DPS) CMOS image sensor with an in-pixel ramp ADC achieved a rate of 10 000 frames/s at 352 × 288 resolution. The paper claimed the scalability along with the mainstream digital CMOS process as an advantage of the DPS.

This paper reports a high-speed 512 × 512 CMOS APS sensor built using a traditional column-parallel ADC architecture. The sensor has a five-transistor (5T) shutter pixel. Since the operation was targeted for very high speed, achieving a high responsivity was the key requirement along with the sensor speed.

The paper is arranged as follows. Section II addresses the design features of the high-speed high-responsivity CMOS APS sensor. It includes an overall architecture, the implementation of a 5T shutter pixel, noise calculations, and the column circuit schematic. Section III presents the measured sensor performance. Section IV is a comparison between the high-speed APS and DPS implementations and between the two technologies. The paper is concluded with a summary, acknowledgment, and list of references.

II. Design for High Speed and High Responsivity

A. Architecture

The architecture of the sensor is very similar to the one referenced in [1]. The sensor has a pixel array, row decoder and driver, column readout circuits with ADC in each column, column-wise memory to store data from the ADC and read previous row of data out, sense amps for memory readout, output drivers, and several controllers—two (top/bottom) for pixel read, column sample-and-hold and ADCs, and two (top/bottom) for a memory operation (Fig. 1). One difference to the implementation [1] is the use of two column readouts for one column of pixels. This was done to boost the speed. Another difference is the use of an analog amplifier with fixed gains of 1, 2, 4, and 8 prior to the ADC. The ADC was designed as a 10-b. The sensor has a total of 16 output ports 10 b each.

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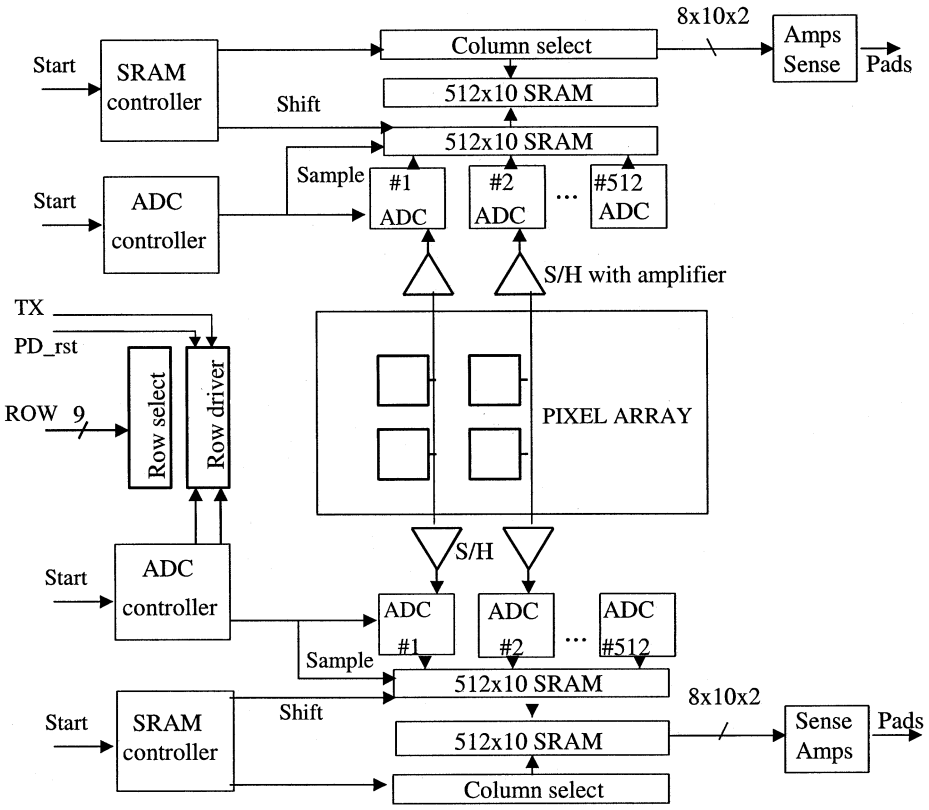


Fig. 1. Block schematic of the sensor.

B. High-Responsivity Shutter Pixel

The standard mixed-mode CMOS process leaves few possibilities for the realization of the parallel shutter in pixels. The pixel can be either a photogate (with noiseless charge transfer to a pixel analog memory) or a photodiode with either voltage sharing or charge transfer. The latter would require solving the lag issue [5], so it was not selected for the implementation due to additional risks. The photogate pixel test chip built in the target process did not show satisfactory quantum efficiency (QE), so it also was not selected. The one chosen for the implementation was a photodiode with voltage sharing. The pixel schematic is shown in the top of Fig. 2. The photodiode is reset through the rst_PD switch, which is a global operation for the entire pixel array. An accumulated photo-signal is transferred to the pixel memory FD by closing switch TX. The pixel memory is reset through the rst_mem switch right after reading the signal from the memory and/or globally just before the signal transfer, if needed for dark signal reduction. All switches operate in the triode regime to insure full reset or full transfer. Although triode operation doubles kTC noise compares to subthreshold reset, it insures no image lag, which is important for high-speed operation.

The switches in pixel can be PMOS only. This allows very good isolation of the memory built-in N-well [2]. However, the pixel N-well serves as an effective parasitic drain for photogenerated electrons and may substantially hinder the collection; hence, the QE. The application primarily required high responsivity and was not very critical to a minor leakage of photosignal

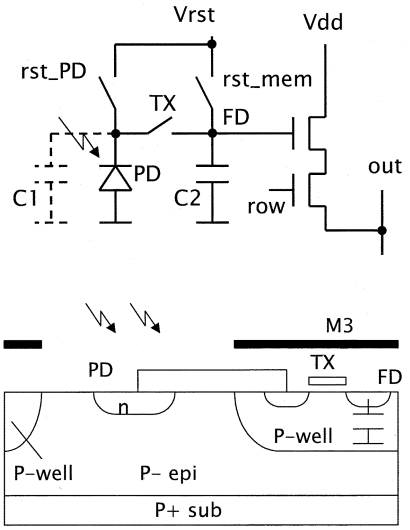


Fig. 2. Schematic of the shutter pixel and its physical implementation.

into the shutter storage, so we selected an all-NMOS switch implementation.

The process provided the option of leaving an original lightly doped p epi-layer in the area of the pixel array. In a regular twin-well process, it would have a P-well implant. The design rules also allowed an island of the original substrate in each pixel with a size of 12 μm and larger. We made use of this opportunity, implementing an N/P-photodiode in the island of the lightly doped substrate while placing the analog memory (which is simply a source–drain capacitance) in a P-well. This

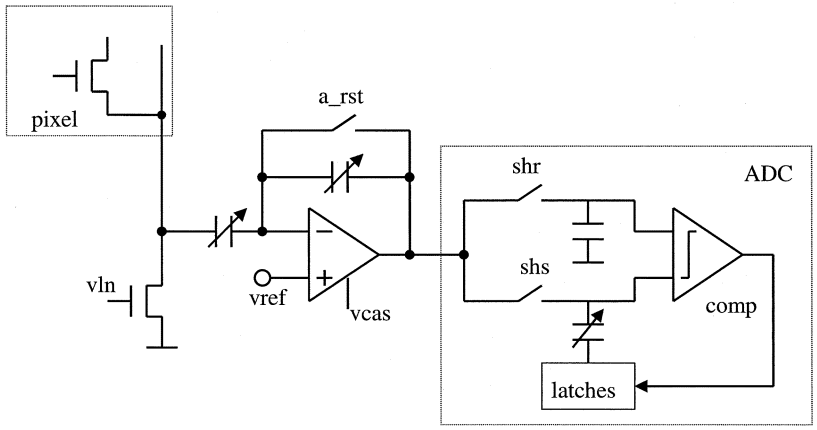


Fig. 3. Simplified schematic of the column front-end circuit.

would supposedly limit the diffusion of photoelectrons into the memory because of the difference in acceptor concentration in the two areas. (The simple theory based on the steady state between the two regions predicts a reduction in photoelectron concentration and hence diffusion current into the P-well region by approximately the ratio of the substrate doping concentrations.) In order to reduce the carrier diffusion to the neighboring pixel, a P-well guard ring was implemented, confining the carriers within the P-epi photodetector "pocket." A physical sketch of the pixel is drawn in the bottom of Fig. 2.

The simplest way to reach high responsivity is to use a bigger pixel. Responsivity is the total collected charge divided by the pixel capacitance. The number of photons is proportional to the photon flux, integration time, pixel area, and QE. If we fix the size of the photodiode and the floating diffusion (FD) and start increasing the overall pixel size, assuming that QE does not degrade, the responsivity, defined in volts per Lux-second, will grow as a square of the pixel pitch. Because high responsivity was an important requirement, we chosen a relatively large 16-μm pixel and relatively small photodiode and FD.

The capacitance of the photodiode and the pixel memory was optimized from noise and dynamic range considerations as described below.

C. Pixel Noise

The dominant noise source in the pixel is the kTC noise from several switches. The reset of the photodiode with capacitance C_1 leaves charge noise with a variance of kTC_1 added to the signal charge. Another noise charge with a variance of kTC_2 comes to the signal charge from the reset of the memory with capacitance C_2. At the closing of TX, these charges will be the sum, and result in noise voltage at the sensing node FD with a noise square $kT/(C_1 + C_2)$. Additional noise comes from a charge redistribution between C_1 and C_2 after opening of TX. This contributes to signal voltage variance by term $kTC_1/(C_2[C_1 + C_2])$. To understand this, consider a loop that includes C_1, C_2, and the TX switch, in which C_1 and C_2 are serially connected. Taking a reference voltage after resetting C_2 again will add another noise voltage with variance kT/C_2 to the signal. Summing squares of the noises together gives a simple expression for the total pixel noise voltage

$$V_n^2 = 2kT/C_2.$$

Although pixel noise does not depend on the photodiode capacitance, the signal voltage V_s after collecting of a photo-charge Q_s degrades with larger photodiode capacitance according to the formula

$$V_s = Q_s/(C_1 + C_2).$$

The optimal ratio between C_1 and C_2 is when they are approximately equal. If C_1 is smaller, it would limit the pixel charge-handling capacity and reduce the signal-to-noise ratio (SNR) unless multiple sampling of the photo-charge into the memory during the collection is used. This cannot be done during the time of reading the pixels, so for the purpose of maximizing the frame rate this mode was not given much attention, and the capacitance ratio was chosen to be approximately 1 to 1.

Pixel noises can be simply reduced by a factor of $\sqrt{2}$ if, instead of taking a true reset sample, we take the sample while reset switch is ON. This, however, adds an offset to the pixel signal and presents another difficulty to overcome.

The pixels are read row by row. Data from the first row goes to the bottom column circuit, the data from the second row goes to the top circuit, and so on.

D. Column Readout and ADC

Column readout is similar to [1]. The difference is an amplifier prior to ADC and 10-b ADC design. The schematic of the front-end column circuit is drawn in Fig. 3. It operates as follows. The first signal voltage from the pixel is the pixel signal voltage followed by the pixel reset voltage, which is of a higher level. While reading the pixel signal, the amplifier is reset and the amplifier reset level is sampled into one of the ADC capacitors. Before performing the pixel reset the amplifier feedback is released, and, after pixel reset is completed, the amplified difference between the pixel reset and the pixel signal referenced to the amplifier reset voltage is sampled into another ADC capacitor. Thus, using a differential ADC input, the amplifier offset varying from column to column is cancelled. In this implemen-

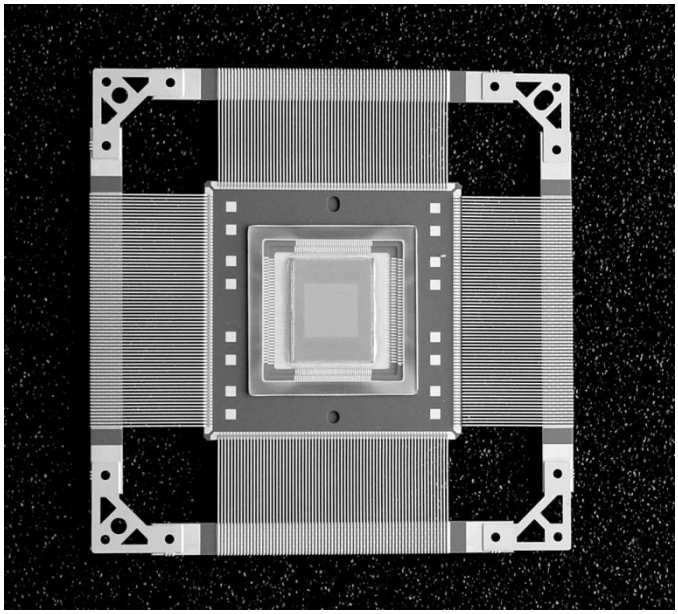


Fig. 4. Photograph of the packaged sensor.

tation, we used a simple cascoded differential amplifier with PMOS input transistors. Fixed gains were 1, 2, 4, and 8.

While performing analog-to-digital (A/D) conversion, data are written into the column SRAM with independent write–read operations (parallel column-wise in-serial out) [1].

III. Implementation and Characterization Results

The chip was designed and fabricated in 0.35-μm 2P3M United Microelectronics Corporation (UMC) CMOS sensor process. The chip size was 12.1 mm (H) × 16 mm (V). The chip was packaged into a custom 288CQFP package with decoupling capacitors for digital VDD, analog VDD, and ADC reference voltage (shown in Fig. 4).

The image sensor was fully characterized using custom PC board and image acquisition and characterization software. Initially, the board acquired the 8 top bits from the sensor, but was later upgraded to 9 b with the goal of better characterizing the ADCs. Most of the measurements presented here were performed with 8-b accuracy, but the most sensitive ones including noise and dark signal nonuniformity (DSNU) were repeated with the 9-b setup.

Measurements were done at room temperature with the sensor operating at 2500 frames/s. The ADC reference was 1 V with gain equal to 1. The ADC differential nonlinearity (DNL) is drawn in Fig. 5. The maximum error at several codes points to the 8-b accuracy. However, since we observed almost a twofold reduction in noise acquiring 9 b compared to 8 b, this rather witnessed about 9-b "statistical" resolution of the ADC. The clear message is that a "bad" 9-b ADC is better than the "ideal" 8-b ADC. The commonly accepted definition of the ADC accuracy somehow ignores this fact. We also observed an excessive ADC temporal noise possibly from the comparator, which masked the DNL. True DNL might be less than 1 b on a 9-b scale.

The slope of the noise square versus signal plot (in Fig. 6) allows us to determine the overall sensor conversion gain (in least significan bits (lsbs) per electron) under the assumption of the shot noise at large signals. Then, the pixel conversion gain was determined using the pixel-to-ADC voltage gain obtained from simulations.

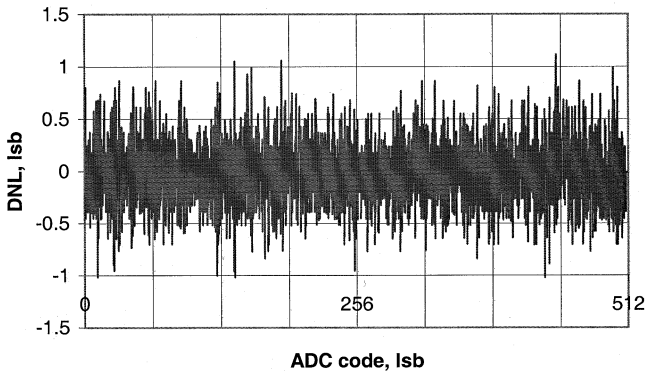


Fig. 5. ADC DNL. Here, lsb stands for the least significant bit. The measurements are done with a 9-b acquisition board.

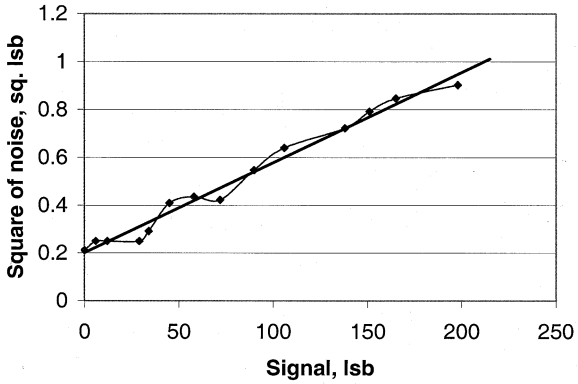


Fig. 6. Measurements of conversion gain (8-b data acquisition board).

TABLE I
Summary of the Sensor Characterization**

Resolution	512x512
Pixel pitch	16 um
ADC architecture	Successive-approximation 10b
ADC resolution	> 8 bit
Responsivity at 550 nm	9 V/ Lux.s
Noise	70e^-
Saturation	60,000 e^-
Conversion gain	16 uV/e^-
DSNU*	0.2% or 125e^- r.m.s. or 1.5% p-p
PRNU at ½ saturation	0.6% r.m.s. or 4% p-p
Dark signal	< 50 mV/s
Shutter efficiency	99%
Nonlinearity	< 1.5%
Power	500 mW

**All numbers are at 2500 frames/s. DSNU includes frozen temporal noise

The results of the measurements are summarized in Table I.

Table I shows that a high responsivity of 9 V/Lux·s for a reasonable dynamic range of 59 dB was achieved. Such a responsivity allows the sensor to capture images under room illumination at a rate up to 1000 frames/s using a commercial $F = 1/2.7$ lens, and at the gain of only 1. A 5000-frames/s imaging requires an outdoor sunlit operation or an additional projector (indoors).

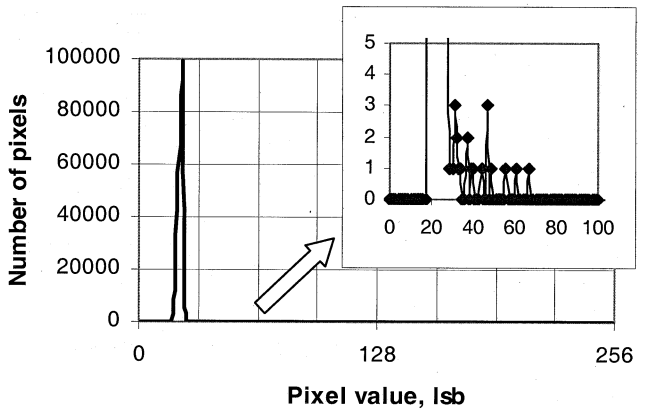


Fig. 7. Dark signal histogram taken at low speed (30 frames/s) and its tail (shown in the inset).

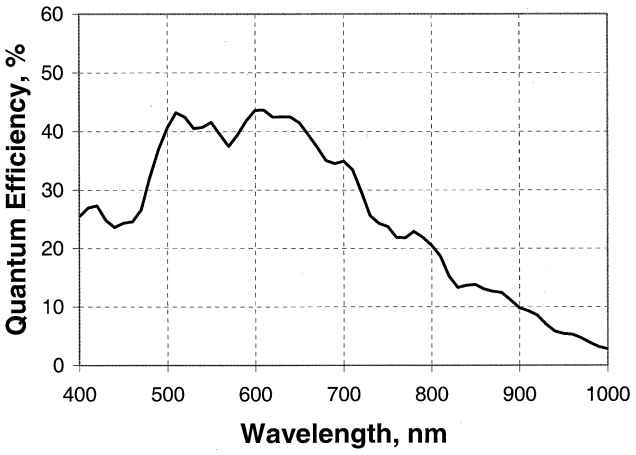


Fig. 8. The spectral response of the sensor.

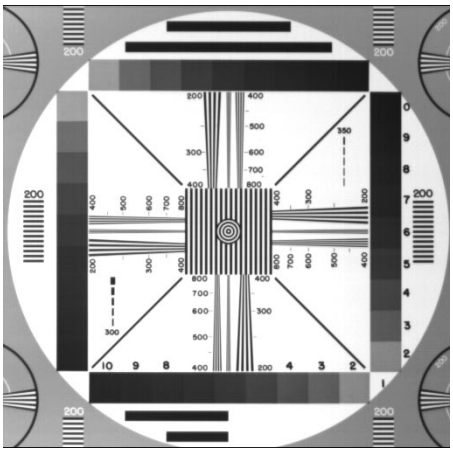


Fig. 9. Image obtained from the sensor at 5100 frames/s.

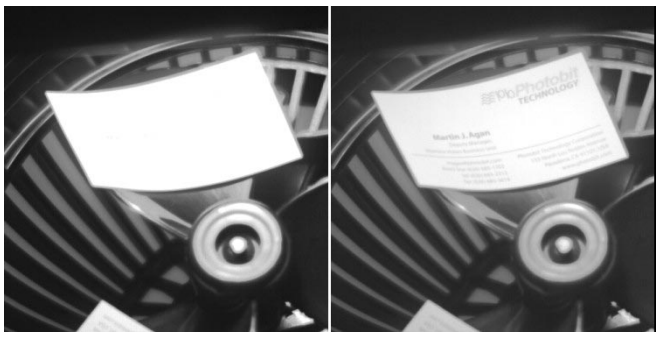


Fig. 10. When a regular image gets saturated (left), double sampling of the photosignal into the memory (right) extends the dynamic range.

Sensor gain settings can also be used, although this reduces the dynamic range. The sensor sensitivity that is the ability to see in dark is defined by both the responsivity and the noise. For the combined (spatial + temporal) noise of 125e$^-$, one needs a minimum of 11 Lux front-plate illumination to have the SNR of 10, when the 9-V/Lux·s sensor operates at 5000 frames/s with the full frame exposure time.

Noise reduction was verified to be approximately 20% when using the "clamped reset" for reset voltage sampling. The deviation from a theoretically expected $\sqrt{2}$ reduction was explained by the ADC quantization error. When the latter was subtracted, good correspondence to the prediction noise reduction was observed. In this pixel reset mode, DSNU was also reduced by 22%–25%. However, an asymmetric pixel reset resulted in an offset coming from the pixel, which saturated the amplifier at gains starting at 2. Further circuit improvements are needed to compensate for pixel offset in this mode.

In the 5T pixel with voltage sharing, the dominant contributor to the pixel FPN is the asymmetry between the rst_PD and rst_mem operations and the variance of the switch feedthrough across the pixel array. The DSNU results should be expected to somewhat worse than in the 3T pixels. Nonetheless, the subjective quality of the image was good, especially taking into account the high-speed aspect of operation. Also, DSNU can be improved at the camera level by subtracting a dark frame. The histogram of the dark frame taken at a temperature of 23 °C and a low speed of 30 frames/s is presented in Fig. 7. It peaks at 23 lsb. This value was mostly a dark offset. The chip did not have an automatic black level adjustment, but did allow dark offset change. Dark current contribution to the signal was relatively small, approximately 2 lsb on average, although several white spots started developing at the such a low frame rate. The inset in Fig. 7 points into a dozen pixels showing a higher dark current. This tail almost disappears at 60 frames/s and is invisible at 120 frames/s.

QE (that includes fill factor) of the pixel is shown in Fig. 8. The response can be characterized as red-greenish. A response of less blue can be attributed to a smaller active area of the detector and its deeper junction. The cut-off in the near infrared area is a combination of the fundamental silicon energy gap limit, as well as a limited collection depth when using a 7-μm epi-wafer on a heavily doped P+ substrate.

This section is concluded with two pictures. The image of a TV chart (Fig. 9) is taken by the sensor with unity gain running at 5130 frames/s using a 90-MHz board oscillator. At the higher oscillator rates the sensor SRAM readout started failing, showing several noisy columns.

Fig. 10 shows another picture, demonstrating a dual slope response extending the dynamic range at the high end. Here the sensor ran at 1250 frames/s and the signal was sampled twice into the memory, after 12 rows and after a full frame (512 rows). A similar idea for an image sensor with a rolling shutter was disclosed in [6]. In this paper, the fusion is done within the pixel.

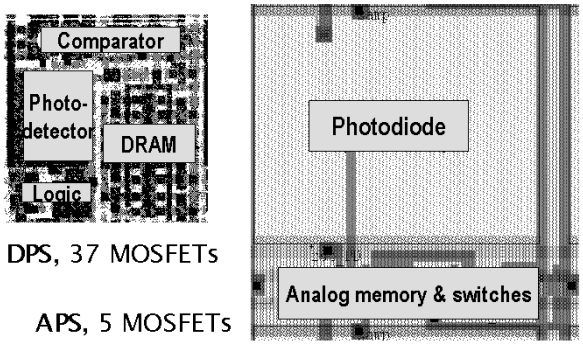


Fig. 11. Comparative drawing of the DPS and the APS pixels. The size ratio is approximately correct.

TABLE II
COMPARISON OF THE APS AND THE DPS

	APS	DPS
Process	0.35um	0.18um
Resolution	512x512	352x288
Frame rate	5,000 Frames/s, 10,000 @512x256	10,000 Frames/s
ADC	>8 bit	8 bit
Pixel	16um	9.4um
Periphery size	4mm	1mm
Responsivity	9 V/Lux-s	0.11 V/Lux-s
Total Noise	125e⁻ or 2 mV	115e⁻ or 1.5 mV

IV. COMPARISON BETWEEN HIGH-SPEED APS AND DPS

Since the speed, resolution, and data rate of a 1.3-Gpixel/s for the sensor were comparable to the parameters of the DPS sensor [4], it was interesting to compare these two sensors and the technologies.

Fig. 11 presents a drawing of the two pixels. Table II compares resolution, speed, pixel size, periphery size, ADC accuracy, responsivity, and the combined temporal and spatial noise of two sensors.

The APS pixel is bigger, but this alone does not explain a higher responsivity of nearly 100. If the DPS pixel grew from 9.4 to 16 μm, its responsivity might have grown seven times, assuming that the pixel fill factor is limited by X–Y wiring. Another order of difference in responsivity may be attributed to the usage of a nonadjusted digital CMOS process for DPS implementation, but primarily because of much worse area utilization by DPS. For instance, the DPS must accommodate 37 MOS's in the pixel whereas the APS uses only five. Some additional loss of the QE in DPS is the diffusion of photoelectrons into the pixel N-well.

The total noise in Table II includes both the spatial and the temporal components. Noise for the DPS was converted from lsbs to volts assuming a 1-V ADC reference, and into electrons using conversion gain of 13.1 μV [4]. The total noise in electrons was a 10% higher in APS. DPS noise was dominated by the temporal noise. Its spatial noise was canceled by the digital CDS to the estimated level of about 20e⁻. In the APS, FPN exceeded the temporal noise by 60%. As we discussed earlier, this FPN came from pixel switches and can be subtracted by using a dark frame memory, the one the DPS uses to perform digital CDS. Then the APS noise is expected to drop to 70e⁻.

If we put together the numbers for responsivity and the noise (in volts), the conclusion would be that the APS was 60 times more sensitive than the DPS.

One advantage of the DPS is that it occupies less periphery chip area. In the APS, substantial space ~4 mm/side went on a column readout. However, the DPS needs to use an external memory of the frame size to perform digital CDS. This reduces the area advantage of DPS.

The speed of the two sensors was essentially the same, 1.3 Gpixel/s.

In general, the DPS with pixel-parallel ADC should exhibit a higher speed because it needs only one conversion per frame, whereas a column-parallel ADC performs as many conversions as the number of rows in the frame. However, the ramp ADC currently used in the DPS is a very slow type of ADC, so it is not obvious that the DPS with the pixel ramp ADC completes the conversion faster than the APS with algorithmic ADC. Let us compare APS and DPS sensors in terms of the number of clock cycles needed to complete the pixel and ADC operations.

The DPS pixel requires two A/D conversions: one for the signal and the other for reset. Pixels perform conversion in parallel, but data are read out line by line. Two A/D conversions will require $2*2^{Nbit} = 2^{Nbit+1}$ clocks, where Nbit is the ADC resolution. The readout of two words will most likely require four clocks per one row. The total number of clocks per A/D and the pixel readout is $2^{Nbit+1} + 4N_{\rm rows}$.

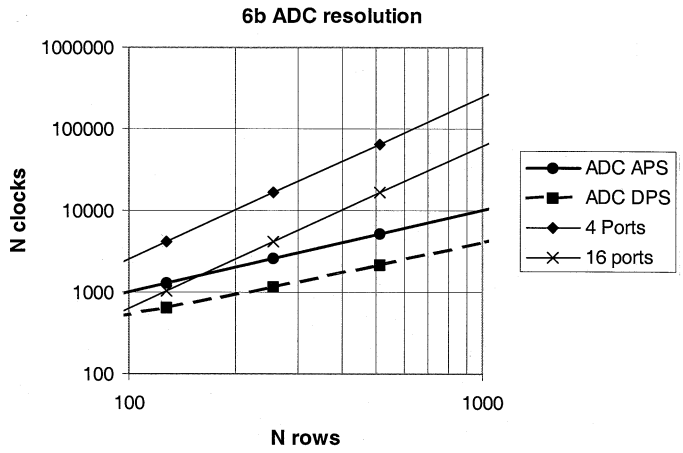
An APS with algorithmic column ADC and pipelining of the pixel readout and the A/D conversion requires approximately $(Nbit + 4) * Nrows$ clocks to perform pixel readout and ADC for entire pixel array.

The plot of the number of clock cycles versus number of rows for a 6-b ADC accuracy and a 12-b ADC accuracy are presented in Fig. 12. The conclusion is that the DPS performs A/D conversion faster at a low ADC resolution and in the case of the 12-b ADC for sensor format larger than VGA (640 × 480). The APS has an advantage in the case of high A/D conversion accuracy and sub-VGA format.

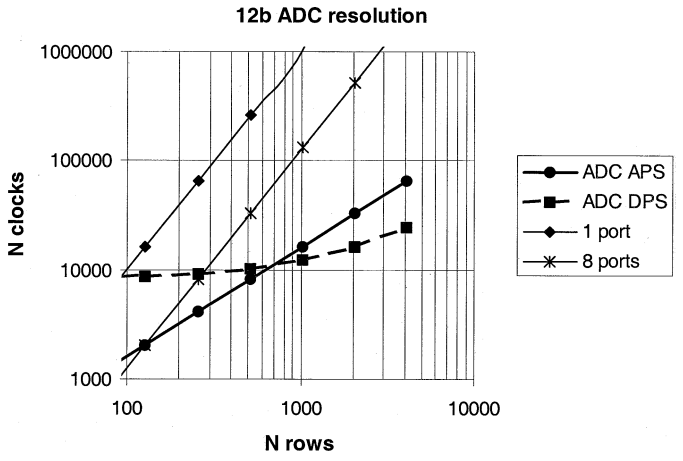
ADC speed is an important factor, but it is not the only one that limits sensor speed. Output interface presents another limitation. In general, if we have N ports M bits each, the number of clocks needed to read out the sensor array of the dimension $N_{\rm rows}$ by $N_{\rm rows}$ will be equal to $N_{\rm rows}^2/(NM)$.The number of clocks needed to read out the frame of $N_{\rm rows}^2$ pixels through 1, 8, or 4, 16 ports is also plotted in Fig. 12. For the most practical resolutions (the number of rows is several hundred and more), it is the output that limits the image sensor throughput for both high-speed APSs and DPSs.

In addition, note the following considerations about the two technologies.

1) If DPS uses the mainstream digital process which is not well suited for imaging [7], QE and dark current are not expected to be good. However, once the dedicated DPS pixel process is developed, the APS can also benefit from



(a)



(b)

Fig. 12. Number of clock cycles required by the APS and DPS to perform ADC operations for (a) 6-b ADC accuracy and (b) 12-b accuracy. Also shown is output port data throughput limitation.

it. As an example, we have drawn a column ADC using 0.18-μm rules, which is in only one quarter height of the ADC in the 0.35-μm process.

2) In order to route a wide data bus in a minimum pixel space, the DPS should use more than three layers of metal. A thick "sandwich" is probably not the best starting point to optimize optical performance of the sensor and reduce a pixel-to pixel optical crosstalk.
3) The APS can easily boost an analog pre-ADC gain to get higher responsivity. To some extent this can also be done in the DPS pixel by lowering ramp voltage swing. However, a noticeable offset from pixel to pixel will not allow us to use this technique efficiently.
4) In an APS, only one row of pixels is selected at a time and consumes power, so routing of the pixel power supply is not an issue. In a DPS, ADCs operate simultaneously. The bigger the dimensions of the DPS, the more critical is the power routing. A noticeable voltage drop in power lines may give rise to image shading (gradient in the image which is supposed to be uniform) and image shadowing (crosstalk between bright and dark image areas). Solving this issue may force the designer to seek subthreshold comparator operation. Then, however, temporal noise of active MOSFETs in a pixel may become an issue. Also, since the reset and the pixel signal are spread in time, there is a possibility of catching additional $1/f$ noise from the analog MOSFETs in the pixel.

In conclusion, the high-speed APS has shown an apparent advantage over the high-speed DPS in responsivity. This is due to the use of a simpler pixel and thus higher fill factor and because of a specialized CMOS sensor process. The comparative analysis shows that the DPS should be seeking opportunities in applications, which require low ADC resolution, smaller imager dimension, and which can tolerate smaller responsivity. Then the DPS's periphery size advantage may transform into a lower cost. The comparison also showed an opportunity for a high-spatial-resolution high-speed DPS. However, in our opinion, such a design presents a serious challenge and requires solving many engineering issues such as power routing, crosstalk, and noise arising from simultaneous operation of an array of the ADCs. Although this paper is about high-speed imaging, it is worth mentioning that the megapixel digital still camera market is still driven by CCDs pushing the pixel size to a pitch of less than 3 μm, so, as for a CMOS being competitive with CCDs in the consumer market, there is little choice but to use only simple pixels, which means an APS.

When discussin the high-speed APS, the primary design issues for the future are reduction of the periphery size and the pixel temporal and spatial noises. In this regard, the transition to smaller design rules and to a buried type of photodiode would be beneficial.

V. Conclusion

A high-responsivity 9-V/Lux·s, high-speed 5000-frames/s 512×512 CMOS APS sensor with column-parallel ADCs was designed, manufactured, and characterized.

The comparison of high-speed digital sensors shows the superiority of the state-of-the-art APS technology regarding responsivity to light and sensitivity. The two major contributing factors are the relative simplicity of the APS pixel and the design for high responsivity in a specialized CMOS sensor process.

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