# A High-Speed CMOS Image Sensor With Column-Parallel Two-Step Single-Slope ADCs

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***Abstract*—This paper proposes a column-parallel two-step single-slope (SS) ADC for high-speed CMOS image sensors. Error correction scheme to improve the linearity is proposed as well. A prototype sensor of 320 × 240 pixels has been fabricated with a 0.35-$\mu$m CMOS process. Measurement results demonstrate that the proposed ADC can achieve the conversion time of 4 $\mu$s, which is ten times faster than the conventional SS ADC. The proposed error correction effectively removes the dead band problem and yields DNL of +0.53/ −0.78 LSB and INL of +1.42/ −1.61 LSB. The power consumption is 36 mW from a supply voltage of 2.8 V.**

***Index Terms*—Column-parallel ADC, single-slope (SS) ADC, two-step ADC.**

## I. Introduction

DUE TO THE benefit of low power consumption and easy system integration with on-chip circuits, recent advances in CMOS image sensors have made them viable alternatives to charge-coupled devices, particularly in high-speed videography. There exist three architectures for ADC integration in CMOS image sensors: a single-channel ADC, a pixel-level ADC, and a column-parallel ADC. The single-channel ADC uses a single ADC for an entire pixel array. Hence, extremely high-speed ADC should be required to achieve a high frame rate. The pixel-level ADC implements an ADC in every pixel, providing extremely high frame rate at the price of silicon area and power consumption. The column-parallel ADC which has an ADC in each column can achieve a good tradeoff among frame rate, fill factor, silicon area, and power consumption. Therefore, the column-parallel architecture is the most widely used architecture for both low-speed mobile imager and high-speed high-performance imager.

The column-parallel ADC architecture can be grouped by its ADC into a successive approximation (SA) ADC [1]–[3], a cyclic ADC [4], and a single-slope (SS) ADC [5], [6]. SA ADCs have been utilized in various high-speed image sensors up to 1000 frames/s at 512 × 512 pixels or UDTV sensors. Since the SA ADC should include a DAC that occupies a large silicon area, it is not applicable for consumer products. Cyclic ADCs occupy less silicon area while keeping the comparable speed to SA ADCs. Ultrahigh-speed sensor that provides a pixel rate of 900 Mpixel/s has been reported in [4]. However, it consumes high power due to high-speed op-amp in each column. SS ADCs have been widely applied in a CMOS imager because they provide relatively high resolution with minimal area and low power consumption for a low-speed imager. Although high-speed CMOS imagers based on an SS ADC have been recently reported in [7] and [8], they use very high clock frequency which requires high power consumption.

Meanwhile, two-step SS ADCs based on multiple ramp signals have been recently reported in [9]–[11]. However, these two-step SS ADCs require several ramp generators corresponding to the number of coarse ADC steps. This architecture has increased area and power consumption due to the multiple ramp generators and multiple ramp signal lines. Therefore, coarse ADC resolution is limited to only 2 or 3 b with little speed improvement.

This paper proposes a new two-step SS ADC using a single ramp generator for high-speed image sensors [12]. Section II describes the operation principle and the limit of a conventional two-step SS ADC. Section III proposes a new two-step SS ADC architecture and the error correction. Section IV presents the experimental results, and Section V provides the conclusion.

## II. Conventional Two-Step SS ADC

In a CMOS image sensor with column-parallel SS ADCs, each column consists of a comparator and latches, whereas a ramp generator and a counter are shared by all ADCs, as shown in Fig. 1. Each comparator in a column compares a ramp signal with an input signal from the pixel array, and then, the output of the comparator is changed when the ramp signal exceeds the input signal. The change of the comparator output causes the latch to store the counter value that corresponds to the time elapse until the ramp signal reaches to the input signal level. Therefore, an SS ADC requires $2^P$ clock steps for a $P$-bit A/D conversion.

Among general ADCs, a two-step ADC divides the A/D conversion process into $M$-bit coarse and $N$-bit fine ADCs where $P = M + N$ in an ideal case [13]. First, the coarse ADC performs A/D conversion with a large step size, and then, the result of the coarse ADC is converted to an analog signal using a DAC. The difference between the input signal and the DAC output is called *residue*, and it is digitized by the fine ADC. The outputs of the coarse ADC and the fine ADC represent the upper bit and the lower bit of the final ADC, respectively.

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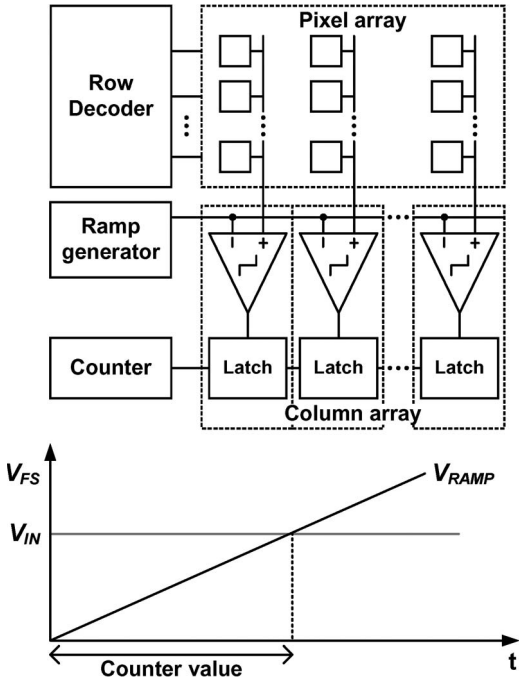


Fig. 1. Block diagram and timing diagram of a column-parallel SS ADC.

This two-step ADC scheme is applicable to an SS ADC. Fig. 2(a) shows the principle of the two-step SS ADC. The first ramp signal spans the full scale, $V_{\rm FS}$ with the step of $\Delta_C$ which is $V_{\rm FS}/2^M$. The comparator finds the section in which the input belongs to among $2^M$ sections. Then, the second ramp signal spans the range of the section that was found during the coarse ADC with the step of $\Delta_F$ which is $\Delta_C/2^N$. The comparator finds the subsection in which the input belongs to among $2^N$ subsections. The conversion time of the two-step SS ADC is reduced to $2^M + 2^N$ clock steps.

Fig. 2(b) shows the block diagram of the conventional two-step SS ADC based on multiple ramp signals [9]. During the coarse ADC phase, all comparators uses the ramp signal $V_{rc}$, which spans full scale, to find the upper bits of the overall ADC. Then, each column selects one of the multiple ramps depending on the coarse ADC outputs. During the fine ADC phase, all $2^M$ ramps operate concurrently, and each ramp spans $\Delta_C$, as shown in Fig. 2(a). Then, the output of the fine ADC corresponds to the lower bits of the overall ADC. This two-step SS ADC with multiple slopes requires $2^M$ ramp generators which consume high power and $2^M$ ramp signal lines which occupy large area. The mismatch of the ramp slopes and offsets cause serious performance degradation. Therefore, the choice of coarse ADC resolution $M$ is generally limited to only two or three, and thus, the speed improvement is not significant.

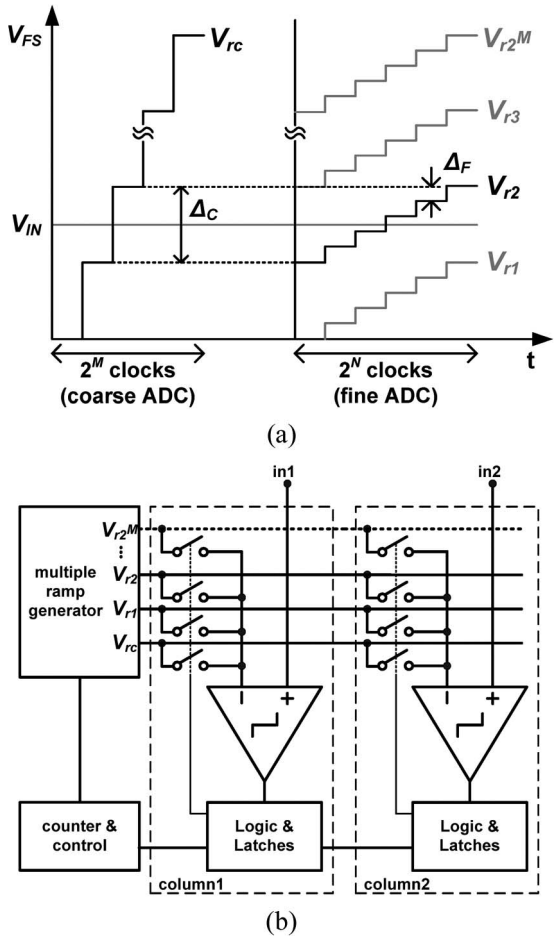


Fig. 2. Conventional two-step SS ADC with multiple ramp. (a) Timing diagram. (b) Block diagram.

## III. Proposed Two-Step SS ADC

### A. Operation Principle of Proposed ADC

The basic concept of the proposed circuit is to store the ramp value at the moment of latching during the coarse ADC and then using the stored value as an offset voltage of the ramp signal during the fine ADC. The stored ramp value corresponds to the result of DAC to obtain the residue after the coarse ADC in two-step ADC.

Fig. 3(a) shows the schematic diagram of the proposed two-step SS ADC. The column ADC consists of a comparator, a capacitor, three switches, a logic gate, and latches. A DAC-based ramp generator and a counter are shared by all column ADCs. $C_1$ and $\phi_1$ are used for CDS operation [14] which cancels the first comparator offset and the pixel offset. $C_2$ and $\phi_2$ are used to cancel the offset of the second comparator which compensates the limited gain of the first comparator. Fig. 3(b) and (c) shows the ramp signal waveform and the timing diagram for two-step SS ADC. When the coarse ADC starts, switches $S_C$ and $S_H$ are on, respectively. This switch arrangement makes the capacitor voltage $V_H$ follow the ramp signal $V_R$. If the input signal $V_{IN}$ is $m\Delta_C < V_{IN} < (m+1)\Delta_C$, the comparator output $V_O$ is changed to logic high when $V_R$ becomes $(m+1)\Delta_C$. Then, the upper $M$-bit latch stores the counter value as a coarse ADC result $m$. $S_H$ is turned off at this moment, and the ramp signal is stored in the capacitor $C_H$. Therefore, $V_H$ is given by

$$V_H = (m+1)\cdot\Delta_C. \tag{1}$$

The counter is reset and the fine ADC phase starts. $C_H$ is connected in series with the ramp signal by turning on the

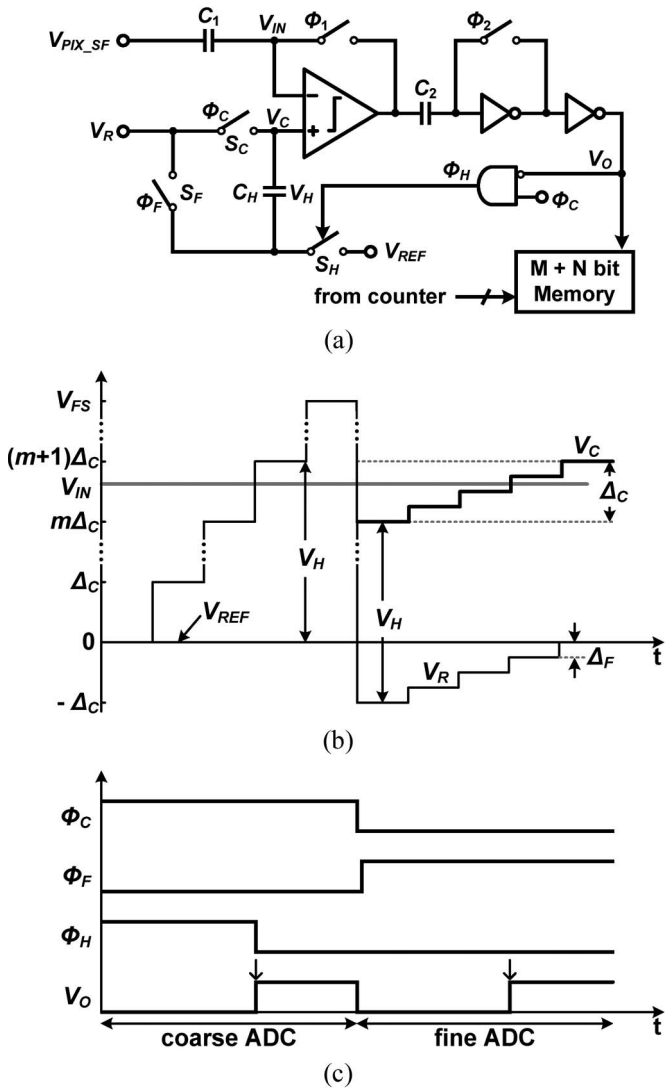


Fig. 3. Proposed two-step SS ADC with single ramp. (a) Simplified schematic diagram. (b) Ramp signal waveform. (c) Timing diagram: Arrows represent the moment of latching.

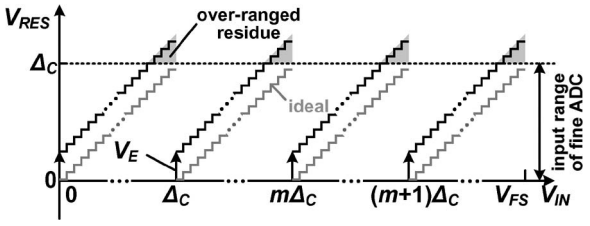


Fig. 4. Residue plots of proposed ADC with nonidealities.

switch $S_F$ while $S_C$ and $S_H$ are off. Then, the comparator reference voltage $V_C$ becomes the sum of the ramp signal and $V_H$ obtained from the coarse ADC as follows:

$$V_C = V_R + V_H = V_R + (m+1) \cdot \Delta_C. \tag{2}$$

where the ramp signal spans from $-\Delta_C$ to $V_{REF}$, as shown in Fig. 3(b). Then, $V_C$ spans from $m\Delta_C$ to $(m+1)\Delta_C$. When $V_C$ exceeds the input signal, the comparator changes its output to logic high again and the counter output is stored in the lower $N$ bits of the latch as a fine ADC result $n$.

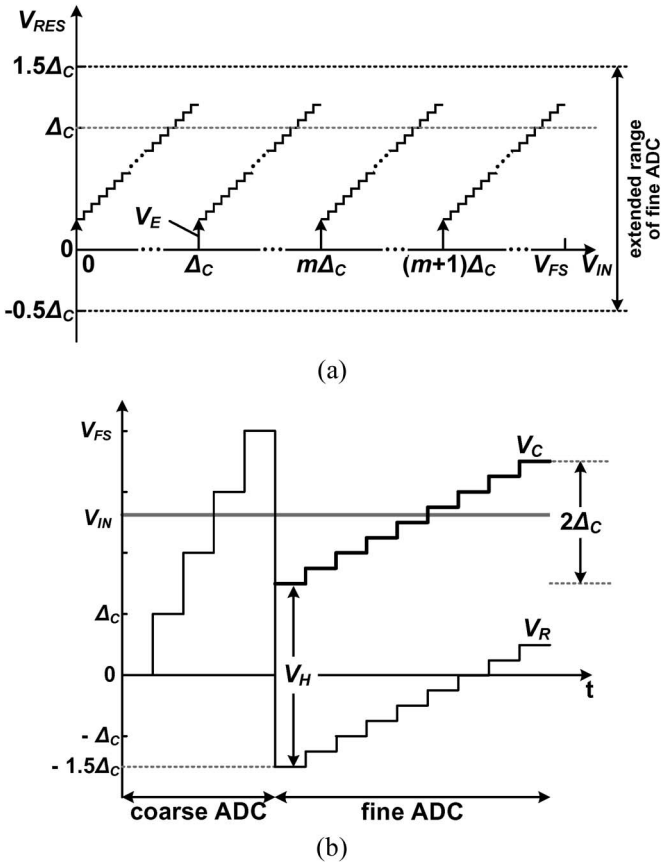


Fig. 5. (a) Residue plot of the proposed ADC with error correction. (b) Proposed ramp signal for error correction.

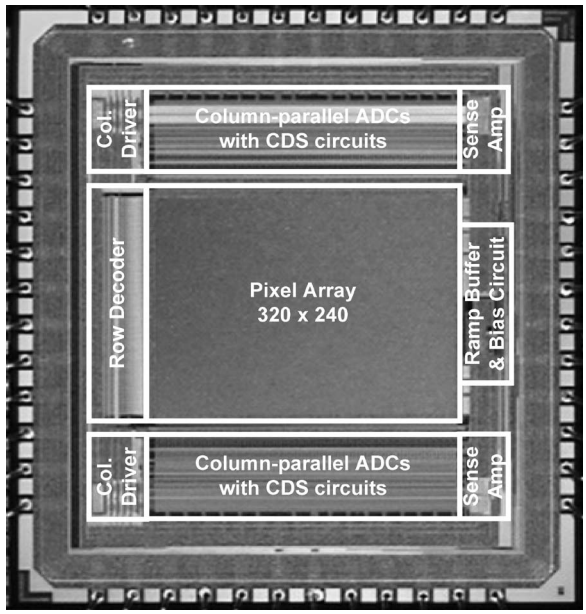


Fig. 6. Chip micrograph of the prototype sensor.

Combining these two results, the final digital output, $p$ can be obtained as follows:

$$p = 2^N \cdot m + n. \tag{3}$$

Unlike the conventional two-step SS ADC with multiple ramp generators, the proposed structure with single ramp

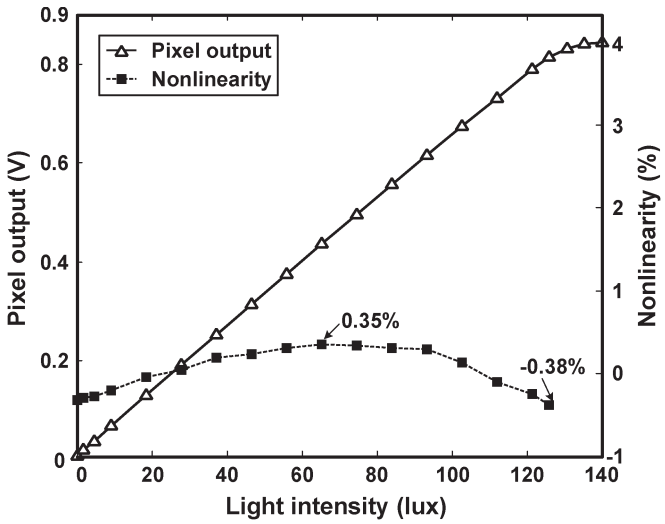


Fig. 7. Photoelectric conversion characteristics at 80 frames/s.

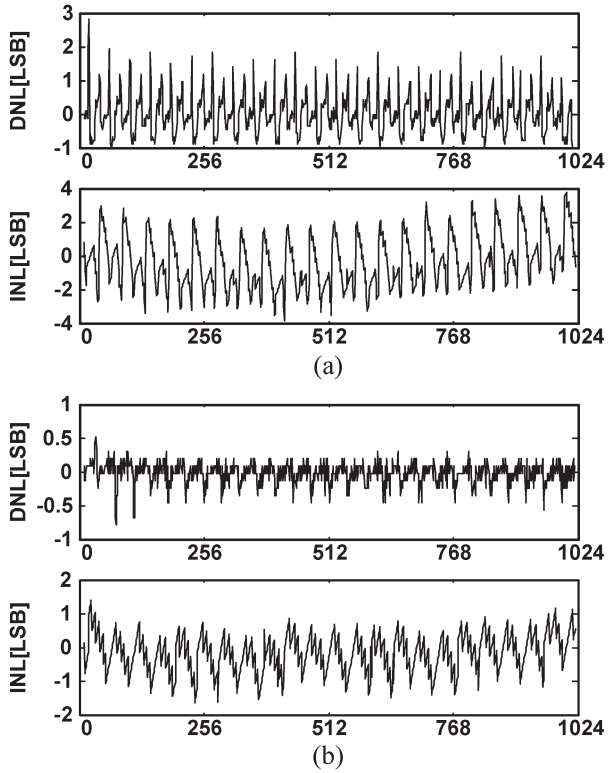


Fig. 8. Measured DNL and INL. (a) Without error correction. (b) With error correction.

generator enables to divide the resolution for coarse and fine ADCs arbitrarily. In particular, the total number of clocks is minimum when $M = N$.

### B. Error Correction

Nonidealities such as comparator offset and clock feedthrough of sampling switches may make the proposed structure malfunctioned. Unlike the common two-step ADCs, the same comparator is used for both of the coarse and fine ADC phases. Therefore, the comparator offset causes the offset of the overall ADC curve without causing the dead band. Although, this

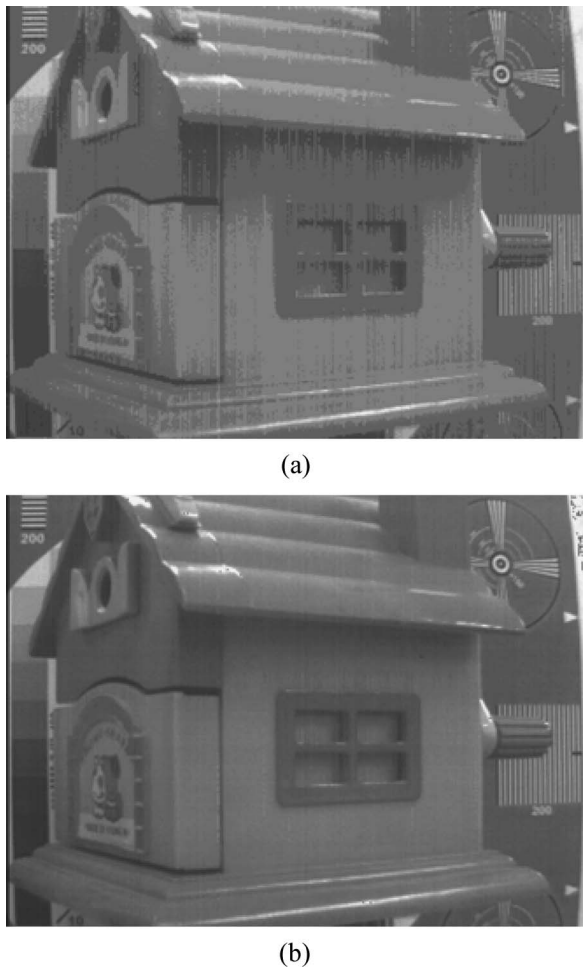


Fig. 9. Lower 8b images from the prototype sensor. (a) Without error correction. (b) With error correction.

offset is canceled out at the input using CDS. The signal-dependent charge injection can be minimized by turning off $S_H$ prior to $S_C$.

The major source of error in the proposed two-step SS ADC is signal-independent charge injection and clock feedthrough when $S_H$ is turned off. The influence of this error can be analyzed with the residue plot where the residue is defined as follows:

$$V_{RES} = V_{IN} - (V_H - \Delta_C). \tag{4}$$

Taking into account the signal-independent error, $V_E$ caused by feedthrough of $S_H$, (1) should be rewritten as follows:

$$V_H = (m+1) \cdot \Delta_C - V_E. \tag{5}$$

The residue plot is obtained from (4) and (5), as shown in Fig. 4. $V_E$ causes vertical shift of the residue plot exceeding the input range of the fine ADC. This overranged residue is converted to a saturated value (all 1s) in the fine ADC phase and, hence, results in dead bands in the final digital output.

To solve this problem, the input range of the fine ADC is extended covering the overranged residue, as shown in Fig. 5(a). This extension is achieved by expanding the range of fine ramp signal by $\pm 0.5\ \Delta_C$, as shown in Fig. 5(b). This

TABLE I
PERFORMANCE SUMMARY

| | [9] | Conventional SS ADC | This work |
|---|---|---|---|
| Technology | 0.25-$\mu$m CMOS | 0.35-$\mu$m CMOS | |
| Array format | 400 (H) × 330 (V) | 320 (H) × 240 (V) | |
| Pixel size | 7.4 $\mu$m × 7.4 $\mu$m | 5.6 $\mu$m × 5.6 $\mu$m | |
| Sensitivity* | N/A | 0.52 V/lux·s | |
| Conversion gain* | N/A | 46 $\mu$V/e- | |
| Full well capacity* | N/A | 18,500e- | |
| Random noise at dark* | N/A | 490 $\mu V_{rms}$ | |
| Dynamic range* | N/A | 64.8 dB | |
| ADC resolution | 3b-coarse / 8b-fine | 10 bit | 5b-coarse / 6b-fine |
| ADC DNL | N/A | +0.64/-0.7 LSB | +0.53/-0.78 LSB |
| ADC INL | +1.4/-1.0 LSB | +1.44/-1.58 LSB | +1.42/-1.61 LSB |
| A/D Conversion time | 16 $\mu$s | 41 $\mu$s | 4 $\mu$s |
| Column FPN at dark | 0.13% | 0.12% | 0.1% |
| Maximum frame rate | 144 frames/s | 92 frames/s | 700 frames/s |
| Power supply | 2.5 V | 2.8 V | 2.8 V |
| Power consumption | 52 mW | 30 mW | 36 mW |

* Pixel data at 12.5-ms integration time.

extension corresponds to the introduction of one bit redundancy in classical two-step ADC. Subsequently, the digital outputs of coarse and fine ADCs are combined as in (3). Although the dead band is corrected by the proposed error correction scheme, the $V_E$ still causes the offset in the final output. The column-to-column deviation of $V_E$ may cause columnwise fixed pattern noise (FPN) the same as in conventional SS ADC.

## IV. MEASUREMENT RESULTS

The prototype sensor is fabricated in a 0.35-$\mu$m double-poly triple-metal CMOS process. The chip micrograph is shown in Fig. 6. A 320 × 240 array of 5.6-$\mu$m pitch 4T-APS pixel and the proposed two-step SS ADCs are implemented on 3.6 mm × 3.2 mm die. The ADC clock frequency is 25 MHz. The resolution of the ADC is divided into 5-b coarse and 6-b fine ADCs to achieve a 10-b resolution. An identical image sensor with the conventional SS ADC was fabricated as well for the fair performance comparison.

Fig. 7 shows the measured photoelectric conversion characteristic of the pixel. The measured sensitivity is 0.52 $\mathrm{V/lx \cdot s}$. The nonlinearity of the pixel output is within $+0.35\%/-0.38\%$. The pixel random noise is 490 $\mu\mathrm{V_{rms}}$ at dark level. Fig. 8 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC. The measured DNL and INL without error correction are $+2.9/-1.0$ LSB and $+3.75/-3.85$ LSB while they are significantly reduced down to $+0.53/-0.78$ LSB and $+1.42/-1.61$ LSB with the proposed error correction. DNL without error correction causes obtrusive discontinuity in the captured image, particularly in low illumination, as shown in Fig. 9(a). This degradation is removed by the proposed error correction scheme, as shown in Fig. 9(b). The maximum frame rate is 700 frames/s. The A/D conversion time of the proposed ADC is improved by a factor of ten compared to the conventional SS ADC and a factor of four to the conventional two-step SS ADC with multiple ramps [9]. The measured column FPN is under 0.1% at dark condition, which is close to the conventional SS ADC. The power consumption of the prototype sensor is 36 mW. The performance of the prototype imager is summarized with recently reported result [9] and the conventional SS ADC from the same fabrication process in Table I.

## V. CONCLUSION

A two-step SS ADC with error correction for high-speed CMOS imagers is proposed. As the proposed ADC uses a single ramp generator for the coarse and fine ADCs, it is free from ramp slope mismatch and high power consumption that were the bottlenecks of the conventional two-step SS ADC with multiple ramp generators. The measurement result demonstrated that the proposed ADC has ten times higher conversion speed without any significant increase of power consumption when compared to the conventional SS ADC. The measurement result also showed that the proposed error correction effectively removed the dead band. The proposed two-step SS-ADC can be used for high-resolution and high-speed image sensors in consumer electronics.

## REFERENCES

[1] A. Krymski and K. Tajima, "CMOS image sensor with integrated 4 Gb/s camera link transmitter," in *Proc. IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 2006, pp. 504–505.
[2] A. Krymski, N. E. Bock, N. Tu, D. Van Blerkom, and E. R. Fossum, "A high-speed, 240-frame/s, 4.1-MPixel CMOS sensor," *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 130–135, Jan. 2003.
[3] I. Takayanagi, M. Shirakawa, K. Mitani, M. Sugawara, S. Iversen, J. Moholt, J. Nakamura, and E. R. Fossum, "A 1.25-inch 60-frames/s 8.3-Mpixel digital-output CMOS image sensor," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2305–2314, Nov. 2005.
[4] M. Furuta, Y. Nishikawa, T. Inoue, and S. Kawahito, "A high-speed, high-sensitivity digital CMOS image sensor with a global shutter and

12-bit column-parallel cyclic A/D converters," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 766–774, Apr. 2007.
[5] Y. Kim, Y. T. Kim, S. H. Choi, H. K. Kong, S. I. Hwang, J. H. Ko, B. S. Kim, T. Asaba, S. H. Lim, J. S. Hahn, J. H. Im, T. S. Oh, D. M. Yi, J. M. Lee, W. P. Yang, J. C. Ahn, E. S. Jung, and Y. H. Lee, "A 1/2-inch 7.2 MPixel CMOS image sensor with 2.25 $\mu$m pixels using 4-shared pixel structure for pixel-level summation," in *Proc. IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 2006, pp. 1994–2003.
[6] S. Ham, W. Jung, D. Lee, Y. Lee, and G. Han, "Ramp slope built-in-self-calibration scheme for single-slope column analog-to-digital converter complementary metal–oxide–semiconductor image sensor," *Jpn. J. Appl. Phys.*, vol. 45, no. 7, pp. L201–L203, Feb. 2006.
[7] Y. Nitta, Y. Muramatsu, K. Amano, T. Toyama, J. Yamamoto, K. Mishina, A. Suzuki, T. Taura, A. Kato, M. Kikuchi, Y. Yasui, H. Nomura, and N. Fukushima, "High-speed digital double sampling with analog CDS on column parallel ADC architecture for low-noise active pixel sensor," in *Proc. IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 2006, pp. 2024–2031.
[8] S. Yoshihara, Y. Nitta, M. Kikuchi, K. Koseki, Y. Ito, Y. Inada, S. Kuramochi, H. Wakabayashi, M. Okano, H. Kuriyama, J. Inutsuka, A. Tajima, T. Nakajima, Y. Kudoh, F. Koga, Y. Kasagi, S. Watanabe, and T. Nomoto, "A 1/1.8-inch 6.4 Mpixel 60 frame/s CMOS image sensor with seamless mode change," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2998–3006, Dec. 2006.
[9] M. F. Snoeij, P. Donegan, A. J. P. Theuwissen, K. A. A. Makinwa, and J. H. Huijsing, "Multiple-ramp column-parallel ADC architectures for CMOS image sensors," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2968–2976, Dec. 2007.
[10] L. Lindgren, "A new simultaneous multislope ADC architecture for array implementations," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 9, pp. 921–925, Sep. 2006.
[11] "Double-ramp ADC for CMOS sensors," U.S. Patent 6 670 904, Dec. 30, 2003.
[12] J. Lee, S. Lim, and G. Han, "A 10 b column-wise two-stage single-slope ADC for high-speed CMOS image sensor," in *Proc. IEEE Int. Image Sensor Workshop*, Ogunquit, ME, Jun. 2007, pp. 196–199.
[13] B. Razavi, *Principles of Data Conversion System Design*. New York: IEEE Press, 1995.
[14] S. Lim, J. Cheon, S. Ham, and G. Han, "A new correlated double sampling and single slope ADC circuit for CMOS image sensors," in *Proc. Int. SoC Des. Conf.*, Seoul, Korea, Oct. 2004, pp. 129–131.

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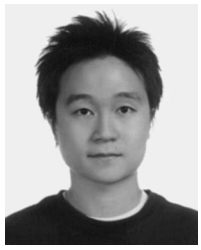

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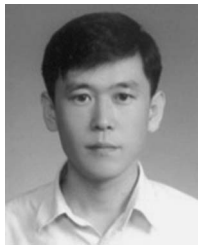

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