# A 3.9-$\mu$m Pixel Pitch VGA Format 10-b Digital Output CMOS Image Sensor With 1.5 Transistor/Pixel

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***Abstract*—A 3.9-$\mu$m pixel pitch VGA format 10-b digital output CMOS image sensor with 1.5 transistor/pixel has been developed for mobile applications. The newly developed CMOS pixel architecture realizes the minimum number of the transistors in one pixel. Small pixel size and sufficient fill factor are achieved by using the shared pixel architecture and floating diffusion driving. High conversion gain, low random noise, and low dark current are achieved by buried photodiode with complete charge transfer capability and correlated double sampling (CDS) circuit. The image sensor is fabricated in a thin planarized 0.35-$\mu$m single poly-Si double-metal customized CMOS process in order to provide good image performance. The image sensor achieves low noise floor of 330 $\mu$V and low dark current of 50 pA/cm$^2$ at 45 °C. This image sensor also realized various functions by on-chip digital and analog circuits.**

***Index Terms*—CMOS image sensors, modulation floating diffusion, sharing floating diffusion amplifier, small pixels.**

## I. Introduction

CMOS active pixel sensors are generally characterized by their low power consumption and capability for on-chip system integration [1]. By using these advantages, an APS-C size CMOS image sensor [2], an area auto-focus CMOS sensor [3], and camera-on-a-chip [4] have been realized. Recent digital still cameras and mobile phone cameras require high signal-to-noise ratio (SNR) in spite of small pixel size. However, CMOS image sensors currently are not widely used in such small pixel applications because of their low SNR than required, which leads to insufficient image quality.

Table I compares the features of CCD image sensors with those of CMOS image sensors. CCD image sensors are characterized by high SNR and small pixel size, but other characteristics (low power consumption, single power supply and on-chip system integration) are weak. In contrast, basic 3-transistor/pixel CMOS image sensors [5] in standard technology provide low power consumption and on-chip system integration, but suffer from $kTC$ noise and dark current problems. Four-transistor/pixel CMOS image sensors [2], [6] can realize ideal properties of low dark current, no $kTC$ noise, and high conversion gain by a buried photodiode with complete charge transfer capability as has been expected from the analogy with the buried photodiode on IL CCDs, but do not satisfy properties required for small pixel size.

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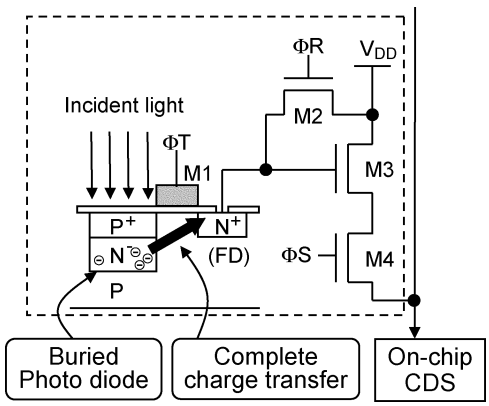


Fig. 1. Conventional 4-transistor/pixel CMOS image sensor configuration.

Fig. 1 shows a pixel schematic of the 4-transistor/pixel CMOS image sensor. Each pixel contains a buried photodiode, a transfer transistor, a reset transistor, an amplifying transistor, a select transistor and a floating diffusion (FD). Conventional use of the buried photodiode to improve the image quality requires the transfer transistor. Therefore, the fill factor is reduced by the extra transistor and its interconnecting wire. Thus, the minimum pixel size with the conventional design is limited by the large number of transistors and wires used in one pixel.

Pixel size reduction of the CMOS image sensors is presently performed by process shrinking [7], the conventional process shrinking done two-dimensionally and not three-dimensionally. On the other hand, the number of poly-Si and metal layers has been increasing and the thickness of insulation layers on photodiode has been becoming higher. Fig. 2 shows the problems of conventional pixel structure with on-chip microlenses. The first problem is degradation in the light gathering power of the on-chip microlenses. Reducing pixel size without proportionally decreasing the thickness of layers on photodiode degrades the light gathering capability of on-chip microlens, and nonflat passivation layer causes poor sensitivity. The passivation layer on the small photodiode becomes concave because of step coverage of the light shielding metal edge. Thus, incident light is refracted to the outside of the photodiode.

Another problem is a metal contamination by silicide process. The silicide process causes large dark current and white pixels [8] by metal contamination from silicide metal to the photodiode.

We have developed new pixel architecture and customized CMOS process to overcome these problems. This new pixel architecture employs two technologies, that is, sharing of a floating diffusion among four pixels to reduce the number

TABLE I
COMPARISON OF FEATURES BETWEEN CCD AND CONVENTIONAL CMOS IMAGE SENSORS

| | CCD | 3-transistor CMOS | 4-transistor CMOS |
|---|---|---|---|
| Pixel size | Small | Medium | Large |
| Sensitivity | Good | Bad | Good |
| KTC noise | None | Exists | None |
| Dark current | Small | Large | Small |
| ML~PD thickness | Thin | Thick | Thick |
| Power consumption | High | Low | Low |
| Single power supply | Difficult | Easy | Easy |
| System integration | Difficult | Easy | Easy |

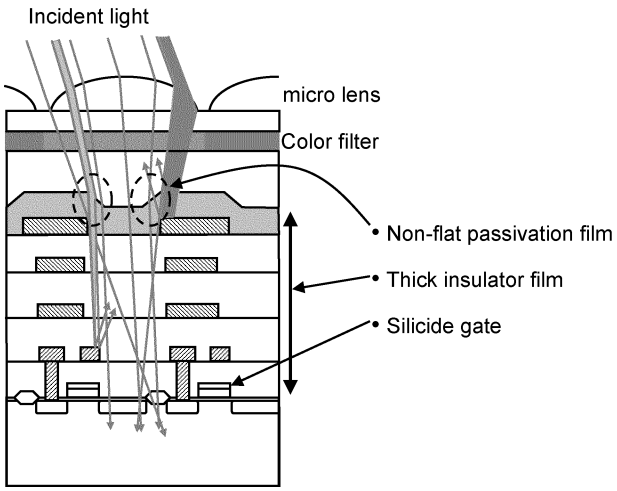


Fig. 2. Cross-sectional view of conventional CMOS image sensor.

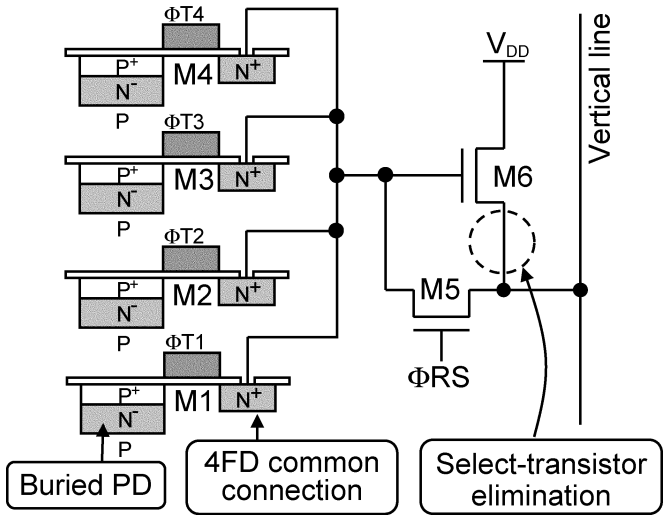


Fig. 3. 1.5-transistor/pixel CMOS image sensor configuration.

of transistors per pixel and floating diffusion modulation to eliminate the select transistor from the pixel. The customized CMOS process enables a flat passivation layer with thin metal layers and insulating layers on the photodiode.

By the new architecture and the customized process, we have developed a digital CMOS image sensor that realizes pixel size reduction with a high SNR and good light gathering power. In future, 0.25-$\mu$m or 0.18-$\mu$m CMOS process will provide less than 3-$\mu$m pixel pitch. This shared pixel architecture is promising technology for fabricating smaller pixels.

## II. 1.5-TRANSISTOR/PIXEL ARCHITECTURE

### A. Pixel Schematic

In order to realize small pixel CMOS image sensor with high image performance, reduction of the number of transistors in one pixel, the buried photodiode with complete charge transfer capability and CDS operation are indispensable. In this section, we describe new pixel architecture for small pixel CMOS image sensor with high sensitivity and low noise.

Fig. 3 shows the schematic of the 1.5-transistor/pixel. The pixel consists of transfer transistors (M1, M2, M3, and M4), reset transistor (M5), amplifying transistor (M6), floating diffusion (FD), and four buried photodiodes. By using M5 as a row select transistor, a conventional row select transistor becomes unnecessary.

Pixel selection is excused by modulating FD potential through the reset transistor and vertical line. Whereas the FDs of unselected pixels keep GND level, that of the selected pixel is set active level. The winner-take-all characteristic of the source-follower leads the selected pixel's signal to the vertical line.

In this architecture, the reset transistor (M5) and the amplifying transistor (M6) are shared by four photodiodes (PD1, PD2, PD3, and PD4). Thus, with six transistors per four pixels, only 1.5 transistors per pixel are used in this new configuration. As a result, a minimum number of transistors per pixel are realized.

### B. Operation

Fig. 4 shows a timing diagram of the pixel operation. M1, M2, M3, and M4 are controlled by the vertical shift register (VSR) and transfer signal charges from the photodiode to FD. Progressive scanning becomes possible by turning on M1, M2, M3, and M4 every 1H period independently. The exposure begins after signal charges are completely transferred from a photodiode to FD. In this photodiode reset, thermal reset noise is not generated because it is a full depletion reset. During the

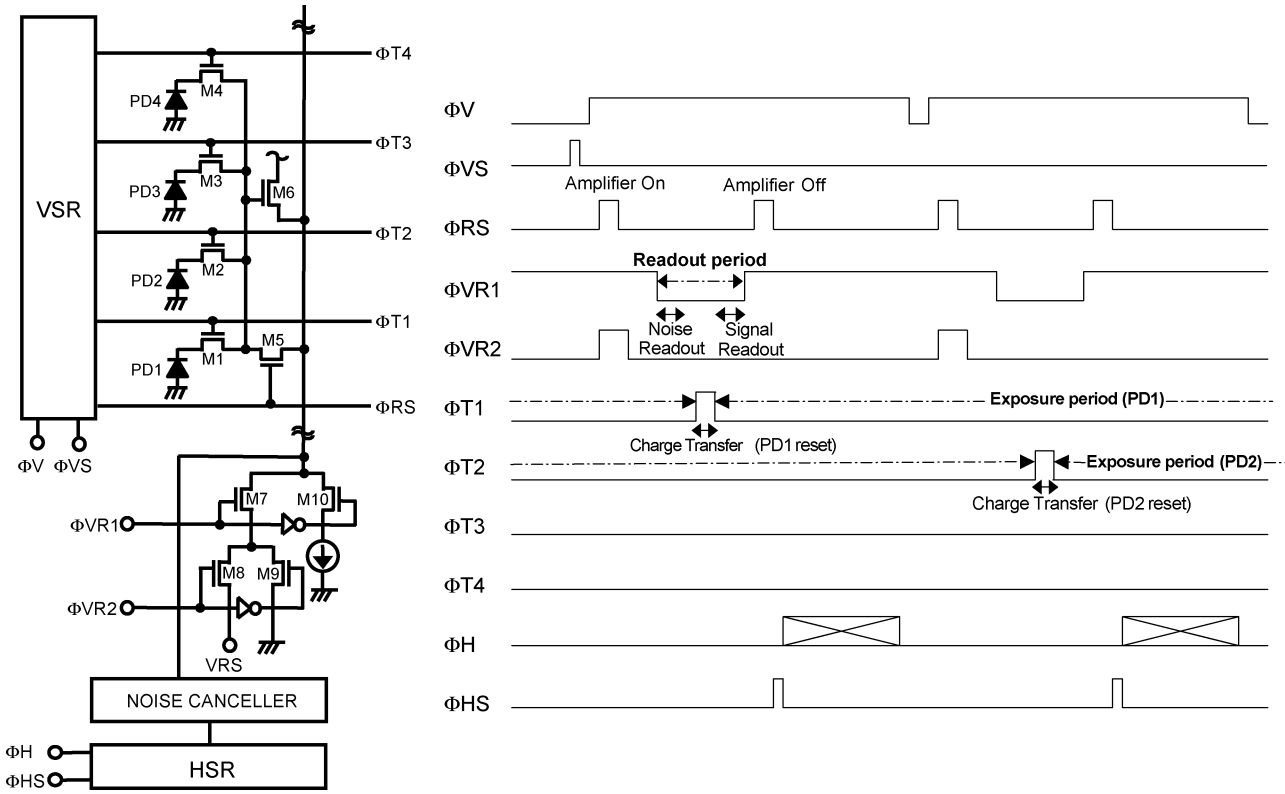


Fig. 4. Pixel schematic and timing diagram.

exposure period, photo current is accumulated in the depletion layer of the photodiode.

*1) Initializing:* In this period, the vertical line is used as reset voltage input line. At the beginning of readout period, the FD1 potential of a selected pixel is raised from GND to VRS by turning on both M7 and M8, and activating the amplifier. VRS is set so as to activate NMOS transistor. Other amplifiers stay in the off-state because the FDs of unselected pixels are in GND condition [Fig. 5(a)]. Each FD's node potential ($V_{\mathrm{FD1}}$, $V_{\mathrm{FD2}}$) is as follows:

$$V_{\mathrm{FD1}} = \mathrm{VRS}$$
$$V_{\mathrm{FD2}} = \mathrm{GND}$$

*2) Dark Signal Readout:* In this period, the vertical line is used as signal output line. At first, reset transistor is turned off, and $kTC$ reset noise is generated on FD node. $V_{\mathrm{FD1}}$ is given by

$$V_{\mathrm{FD1}} = \mathrm{VRS} + \sqrt{\frac{kT}{C_{\mathrm{FD1}}}}$$

where $k$ is Boltzmann's constant, $T$ is absolute temperature and $C_{\mathrm{FD1}}$ is the capacitance of the floating diffusion.

Then, the constant current source is connected to the amplifier by turning on M10, making possible source-follower readout. The dark signal output to CDS circuit is performed [Fig. 5(b)]. The dark signal $N_{\mathrm{OUT}}$ is given by

$$N_{\mathrm{OUT}} = G_{\mathrm{SF}} \times V_{\mathrm{FD1}} + \mathrm{FPN}_1$$

where $G_{\mathrm{SF}}$ is the gain of the pixel source-follower and $\mathrm{FPN}_1$ is the fixed pattern noise of the pixel source-follower.

*3) Charge Transfer:* When M1 turns on, the signal charges are completely transferred from the photodiode (PD1) to FD [Fig. 5(c)]. The photo-conversion voltage depends on the photo charge $(Q_{\mathrm{P}})$ and the capacitance of the floating diffusion $(C_{\mathrm{FD}})$. Thereby, the FD1 potential $V'_{\mathrm{FD1}}$ is given by

$$V'_{\mathrm{FD1}} = V_{\mathrm{FD1}} - \frac{Q_{\mathrm{P}}}{C_{\mathrm{FD1}}}$$

During the charge transfer period, the signal charges of the other photodiodes are not transferred because the transfer transistors connected to other photodiodes (PD2, PD3, and PD4) are off.

*4) Photo Signal Readout:* The photo signal is read out after charges are transferred and M1 is turned off [Fig. 5(d)]. The photo signal is given by

$$S_{\mathrm{OUT}} = G_{\mathrm{SF}} \times V'_{\mathrm{FD1}} + \mathrm{FPN}_1$$

The column-parallel CDS circuit subtracts the dark signal from the photo signal, reducing FPN and the thermal reset noise at FD. Output signal from the CDS circuit $V_{\mathrm{sig}}$ is given by

$$V_{\mathrm{sig}} = N_{\mathrm{OUT}} - S_{\mathrm{OUT}} = G_{\mathrm{SF}} \times \frac{Q_{\mathrm{P}}}{C_{\mathrm{FD1}}}$$

*5) Amplifier Off:* After the signal readout, the FD potential is fixed to GND by turning on both M7 and M9. The amplifier is cut off and readout from the pixel is disabled [Fig. 5(e)].

## III. Image Sensor Configuration

Fig. 6 shows the block diagram of the digital CMOS image sensor. This chip is fabricated using a 0.35-$\mu$m single-poly

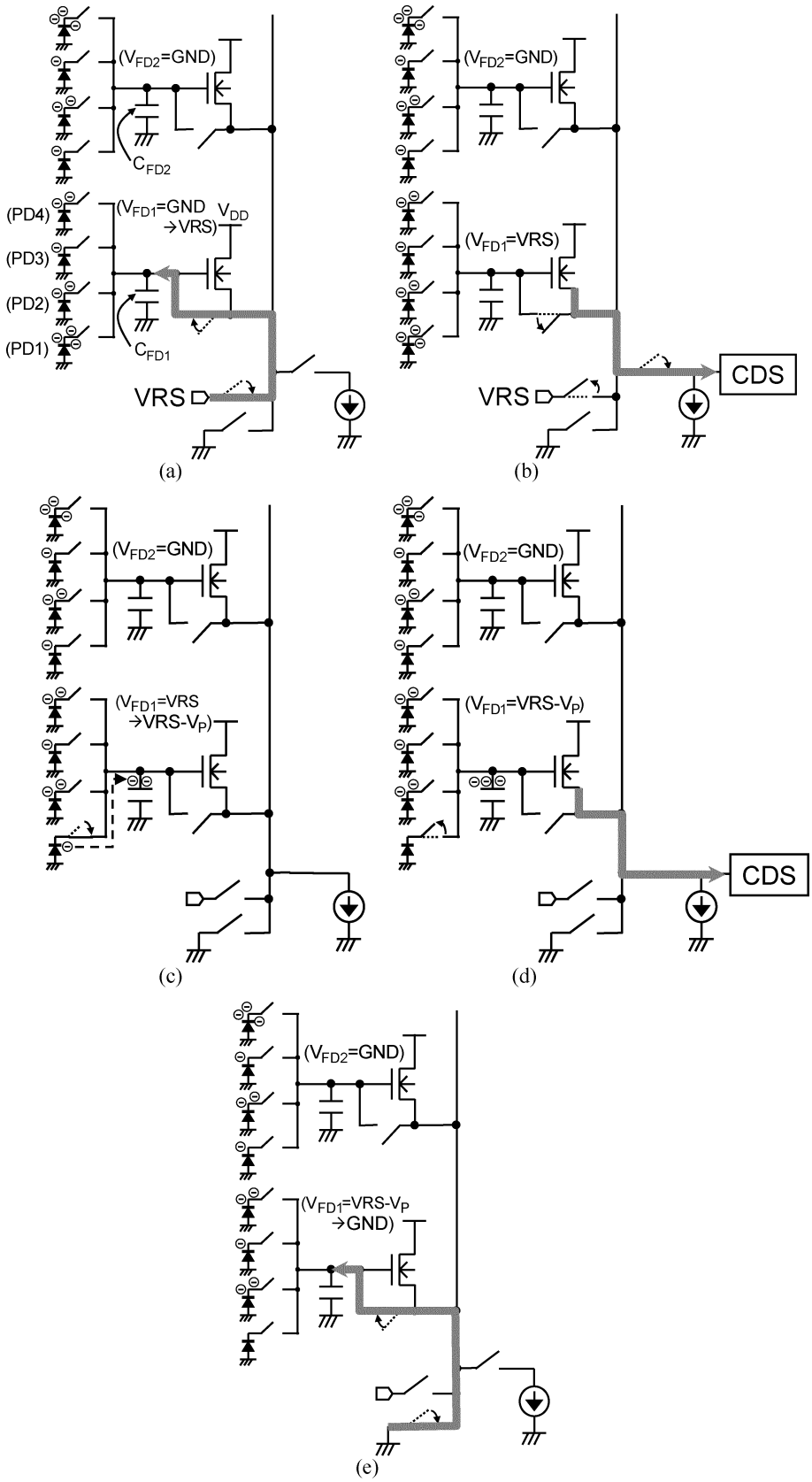


Fig. 5. Pixel operation method. (a) Initializing. (b) Dark signal readout. (c) Charge transfer. (d) Photo signal readout. (e) Amplifier off.

double-metal CMOS process. The CMOS image sensor consists of 703 $\times$ 499 effective pixels with a column noise canceller and scanning circuits, and outputs analog signals and auto-gained 10-b parallel digital signals. The image sensor further includes a voltage regulator, a timing generator (TG), an auto gain control (AGC), a 10-b digital-to-analog converter (DAC), and

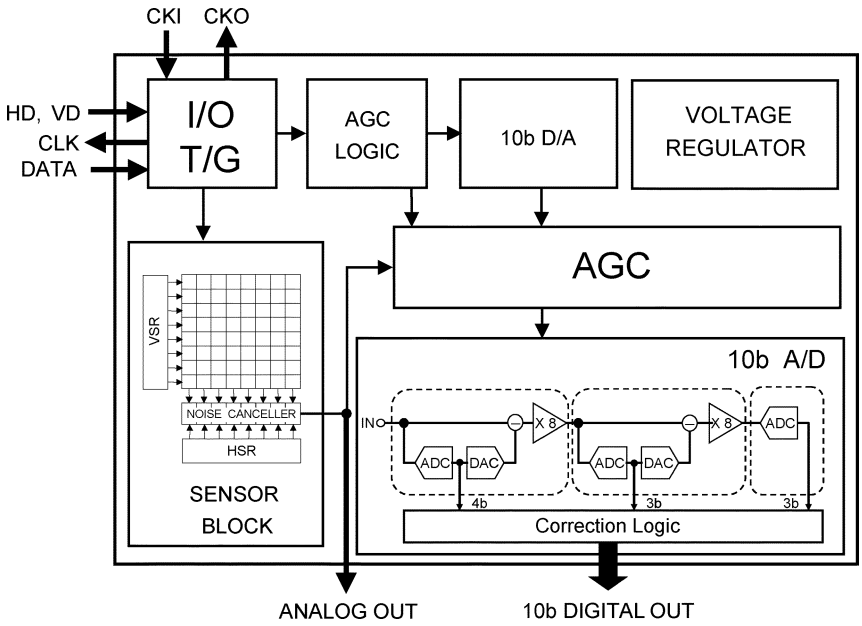


Fig. 6. Digital CMOS image sensor configuration.

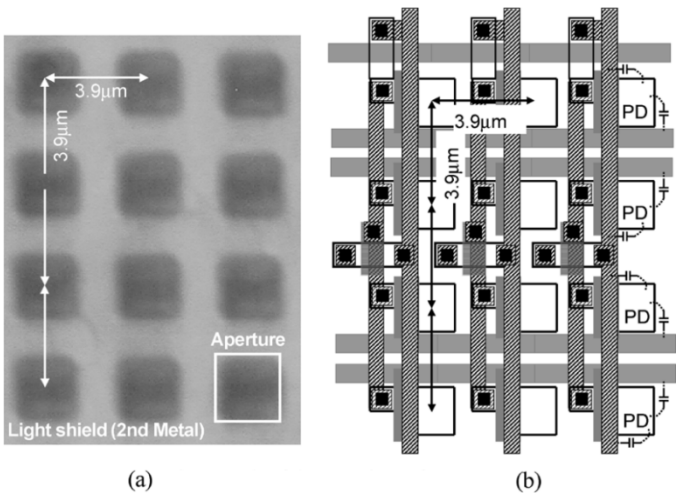


Fig. 7. Pixel pattern layout. (a) Microphotograph of the top view of the image area. (b) Pixel layout without light shield.

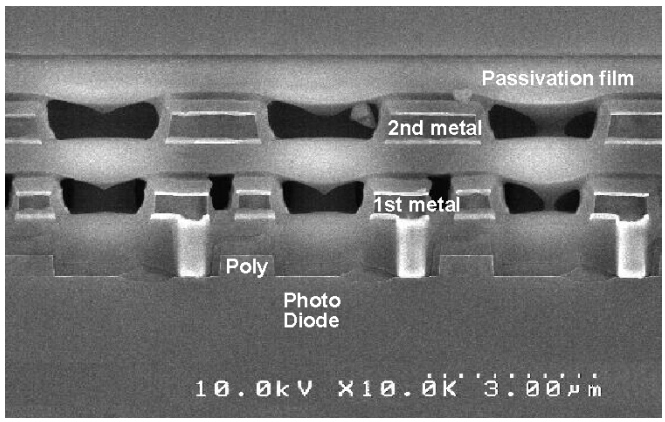


Fig. 8. SEM photograph (cross-sectional view) of the pixel.

a 10-b pipelined analog-to-digital converter (ADC). The single ADC architecture is more suitable for a small pixel pitch image sensor than a column ADC architecture, because it is difficult to realize high resolution (>12 b) and small column pitch with the column ADC. The timing generator block is controlled by clock pulses and serial communication and generates pulses for the chip operation. The voltage regulator generates various voltages for operation of each block. The bandgap circuit is also on chip in order to generate constant voltages.

The image sensor operates with a single master clock and runs at frequencies up to 12.27 MHz. Programmable features include variable frame rate operation using a constant frequency master clock, electronic exposure control, dark level control, and progressive/monitoring mode selection. The programmable gain is 0–18 dB (0.375-dB step) and the fixed gain is either 0 or 12 dB, therefore, total programmable gain of 30 dB is available.

## IV. Low Optical Stack and Low Noise Pixel

### A. Single-Poly-Si Double-Metal Layout

Fig. 7 shows a microphotograph of the top view of pixels [Fig. 7(a)] and pixel pattern layout [Fig. 7(b)]. The photodiode is formed with identical aperture shape and 3.9-$\mu$m pitch. Not only a light shielding metal but also the first metal and the poly-Si of the photodiode perimeter are arranged so that the parasitic capacitances are almost equal and apertures defined by metal line layouts are equal among the pixels. If the symmetry of the PDs is lost, photo-response nonuniformity (PRNU) increases. Therefore, symmetric photodiode layout is indispensable for high image quality. Clock lines of the transfer transistor and the reset transistor are formed by a poly-Si layer. In order to minimize clock delay caused by high resistance of poly-Si, the VSR is arranged at both sides of the image area as shown in Fig. 10. A line connecting FD and a vertical signal line are formed by the first metal layer. The light-shielding layer is formed by the second metal layer and is also used as a power supply line. Thus,

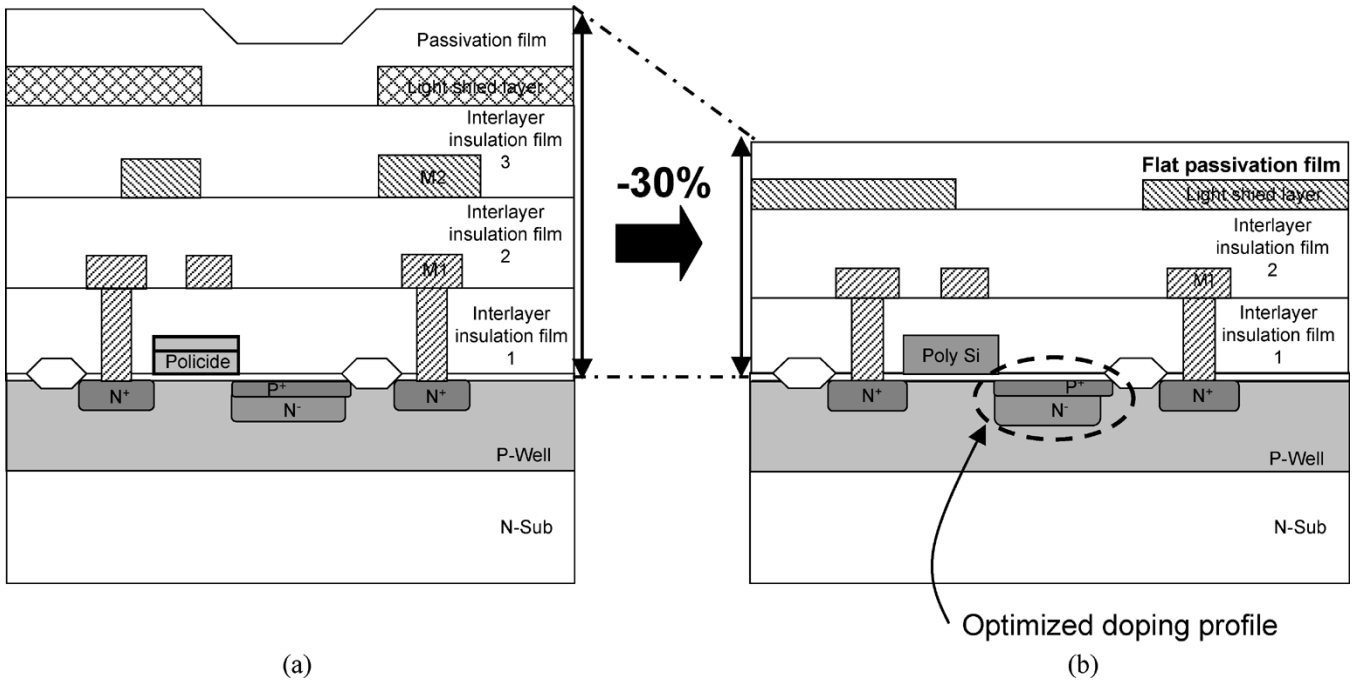


Fig. 9. Pixel structure compared with that of a conventional 1P 3M CMOS process. (a) Conventional structure. (b) New structure.

TABLE II
COMPARISON OF FEATURES BETWEEN NEW CMOS IMAGE SENOR AND CONVENTIONAL CMOS IMAGE SENSORS

| | 1.5-transistor CMOS | 3-transistor CMOS | 4-transistor CMOS |
|---|---|---|---|
| Transistors/pixel | 1.5 | 3 | 4 |
| Wires/pixel | 1.5 | 4 | 5 |
| Pixel size | Small | Medium | Large |
| Sensitivity | Good | Bad | Good |
| Dark current | Small | Large | Small |
| KTC noise | None | Exists | None |

with six wires per four pixels, only 1.5 wires per pixel are realized in this new configuration. By this pixel architecture, a sufficient fill factor of 17% is realized with a 0.35-$\mu$m design rule.

### *B. Thin Planarized Pixel Structure*

Fig. 8 shows a scanning electron microscope (SEM) photograph (cross-sectional view) of the pixel. The image sensor is fabricated in a single poly-Si double-metal customized CMOS process, and a top passivation layer is planarized. The planarized passivation layer is important to prevent lowering of sensitivity. Furthermore, the on-chip microlenses are fabricated without using a conventional thick planarization layer due to the flat passivation layer. The planarization is more effective for light at large incident angle.

Fig. 9 shows the comparison of a conventional CMOS structure and new pixel structure. The thicknesses of metal layers and insulation layers are reduced approximately 30% compared with the conventional single-poly-Si triple-metal (1P 3M) CMOS process. A surface region of the photodiode has shallow junction depth and high concentration diffusion layer. Low dark current is achieved by adopting an optimized buried photodiode with low stress LOCOS isolation and low damage nonsilicide process. The nonsilicide process is adopted to prevent impurity contamination. The doping profile in the photodiode is optimized in order to realize low dark current and large saturation charges. As a result, very low dark current and enough saturation charges are achieved.

Table II compares features of the conventional CMOS image sensors with that of the new image sensor. The number of the transistors and the wires are reduced dramatically; therefore, small pixel size with high SNR becomes possible.

## V. SPECIFICATIONS AND PERFORMANCE

Fig. 10 shows a chip microphotograph of the CMOS image sensor. It includes 703(H) $\times$ 499(V) effective pixels compatible with the VGA standard. The chip size is 4.74 $\times$ 6.34 mm$^2$.

Fig. 11 shows photo-conversion characteristics of the image sensor. The conversion linearity has been obtained in the range of the output voltage from about 1 to 230 mV. The image sensor specifications and performance are listed in Table III. The CMOS image sensor has a low dark current of 50 pA/cm$^2$ at 45 °C and low random noise (RN) of 0.33 mV$_{\rm rms}$ without image lag. No image lag and good photo-conversion linearity

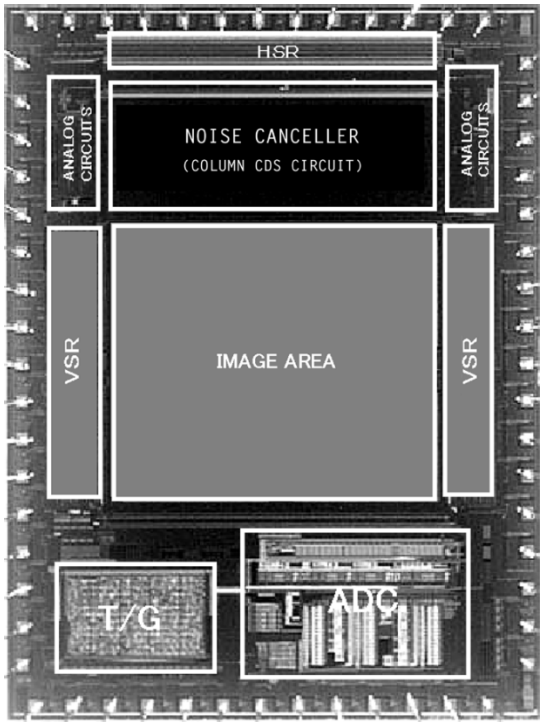


Fig. 10. Chip microphotograph.

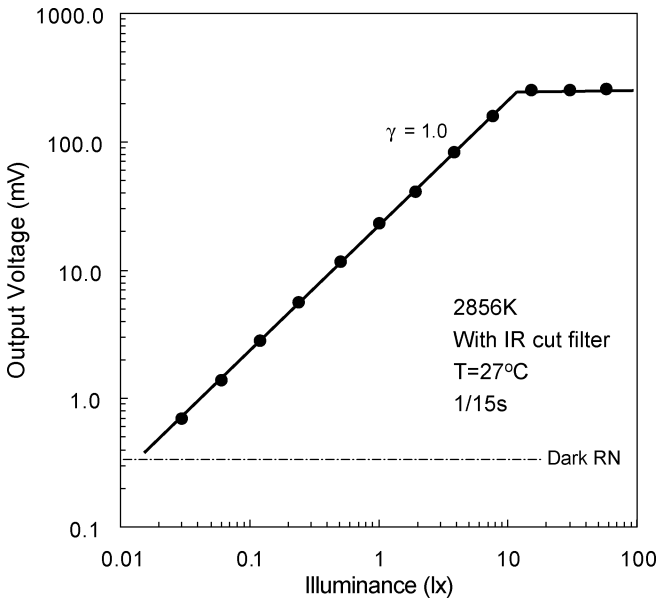


Fig. 11. Photoelectric conversion characteristics.

suggest that complete charge transfer is performed. FD capacitance generally increases because of the common connection of FD, but FD capacitance is reduced by an advanced design rule resulting in a high conversion gain of 23 $\mu$V/e$^-$ in this work. ADC differential nonlinearity (DNL) of 0.5 LSB and integral nonlinearity (INL) of 1 LSB are obtained, and maximum conversion speed is 10 MS/s. The PRNU of 1.2% peak-to-peak is somewhat larger than the conventional ones. Future work will concentrate on decreasing the PRNU of this new pixel architecture. Fig. 12 is a sample image taken by the digital CMOS image sensor.

TABLE III
CHARACTERISTICS OF THE IMAGE SENSOR

| | |
|---|---|
| Technology: | 0.35μm CMOS (1P, 2M) |
| Voltage supply: | 5.0V |
| Chip size: | 4.74(H) x 6.34(V)mm$^2$ |
| Array size: | 703(H) x 499(V) |
| Pixel size: | 3.9 x 3.9μm$^2$ |
| Pixel fill factor: | 17% |
| Transistors per pixel: | 1.5Transistors |
| Frame rate: | 15fps |
| ADC resolution: | 10b |
| ADC conversion time: | 10MS/s |
| ADC DNL/INL: | 0.5LSB/1LSB |
| Conversion gain: | 23μV/e$^-$ |
| Saturation : | 10000e$^-$ |
| Image lag: | below measurement accuracy |
| PRNU: | 1.2%pp |
| RN: | 0.33mV$_{rms}$ (Gain=1) |
| FPN: | 0.20mV$_{rms}$ (Gain=1) |
| Dark current: | 50pA/cm$^2$ (@45°C) |
| Dark output voltage: | 0.19mV (@45°C,1fps) |

Fig. 12. Sample image.

## VI. CONCLUSION

We have developed a shared 1.5-transistor/pixel architecture using a buried photodiode with complete charge transfer capability for realizing high SNR and small pixel CMOS image sensor. By using the newly developed pixel architecture and a thin planarized CMOS process, the CMOS image sensor achieves 3.9-$\mu$m pixel pitch, enough saturation charge, and high SNR. A low optical stack photodiode achieves high light gathering capability.

The 1.5-transistor/pixel architecture has great advantages for fabricating high SNR small pixel image sensors. This shared pixel architecture will help to produce mobile phones and digital cameras for low-cost and high-performance applications.

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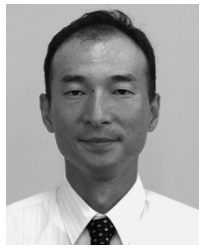

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