An 84 pW/Frame Per Pixel Current-Mode CMOS Image Sensor With Energy Harvesting Capability

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***Abstract*—In this paper, we present an ultra-low-power current-mode image sensor with energy harvesting capability. By biasing the in-pixel transconductance amplifier in triode region and using a pipelined 9-bit current-mode analog-to-digital converter (ADC), a power consumption as low as 84 pW/frame per pixel is achieved. Besides the ultra-low-power feature, the proposed 6T pixel can also be used as a solar cell by reconfiguring the in-pixel P+/Nwell photodiode, which can generate several micro watt power at *Klux* illumination levels. As a result, this energy harvesting imager is very suitable for wireless image sensor network applications. The test chip with a 128 $\times$ 96 pixel array resolution is fabricated using a 0.35 μm CMOS technology. The random noise and the fixed pattern noise (FPN) in dark are 0.4% and 1%, respectively. In the energy harvesting mode, 4.85 μW power can be harvested using the reconfigurable pixel array.**

***Index Terms*—Active pixel sensor (APS), CMOS image sensor, current-mode, energy harvest, low-power.**

I. Introduction

STATE-OF-THE-ART wireless image sensor networks require ultra-low-power operation in order to avoid replacing battery and keep a longer lifetime. It is expected that the next generation of CMOS mega-pixel image sensor will consume less than 1 mW of power to support the continuously increased demand for wireless devices [1]. Power per frame per pixel is one of the most important Figure of Merit (FOM) for such imagers enabling to normalize the power consumption with respect to the frame rate as well as the pixel array resolution. Normally, the ADC and the peripheral circuitries jointly contribute most of the power consumption of the CMOS imager system [2]. Recently reported arts present 460 pW/frame per pixel dynamic Pulse Width Modulation imager reported in [2] and a 270 pW/frame per pixel contrast-based asynchronous scheme reported in [3]. Besides the ultra-low-power feature, energy harvesting is becoming an important scheme to extend the lifetime of the appliance. Several potential energy harvesting schemes can be chosen, such as vibration energy harvesting using MEMS devices and RF energy harvesting [4]. For a CMOS image sensor, the in-pixel photodiode can be used not only as a photodetector, but also as a light energy harvesting element (solar cell). As a result, it is interesting to utilize the light energy for an image sensor in order to harvest energy [5], [6].

In this paper, we report an ultra-low-power imager achieving a FOM of about 84 pW/frame per pixel, which is one of the lowest power designs ever demonstrated. A 6T current-mode pixel structure is proposed. The in-pixel transconductance amplifier is biased in triode region in order to minimize the output current. A 9-bit ADC is designed in the current-mode using pipelined scheme, achieving a sampling rate of about 1 M samples/s. By reconfiguring the in-pixel switch transistors, the P+/Nwell diode can be used as the photodiode in the imaging mode and as the energy harvesting element in the energy harvesting mode, respectively. A test chip is fabricated with a 128 $\times$ 96 pixel array using a standard 0.35 μm CMOS process.

This paper is organized as follows. Section II describes the imager architecture and its VLSI design. Section III demonstrates the simulation and measurement results as well as discussions. Section IV delivers the conclusion.

II. Imager Architecture and VLSI Design

A. 6T Reconfigurable Pixel

As shown in Fig. 1, the proposed CMOS image sensor architecture is composed of the pixel array, the current-mode ADC, the clock generator, and the peripheral digital circuit. The proposed pixel is implemented with 6 Transistors (6T) and one P+/Nwell photodiode. The transistors are composed of four NMOS switches, one PMOS reset transistor, and one NMOS transistor used as a transconductance amplifier. The pixel can operate in both energy harvesting mode and imaging mode. During the energy harvesting mode, the negative pole (Nwell) of the diode is connected to *Gnd*, while the positive pole (P+) is connected to the global power bus, by setting the control signal *Mode* to "1." As a result, the voltage at the power bus $V_{\rm bus}$ can be charged up until the photocurrent $I_{\rm ph}$ is equal to the forward biased current of the photodiode, as shown in (1). V_T is the thermal voltage (26 mW at 300 K), and I_S is the reverse saturation current of the diode

$$V_{\rm bus} = V_T \ln\left(\frac{I_{\rm ph}}{I_S} + 1\right). \tag{1}$$

During the imaging mode, the *Mode* signal is set to "0" and thus, the pixel is reconfigured as a normal 3-T current mode active pixel sensor (APS), as shown in Fig. 2. Since the supply voltage is 1.35 V for low-power consideration, the reset switch is implemented with a PMOS transistor. As a result, the voltage

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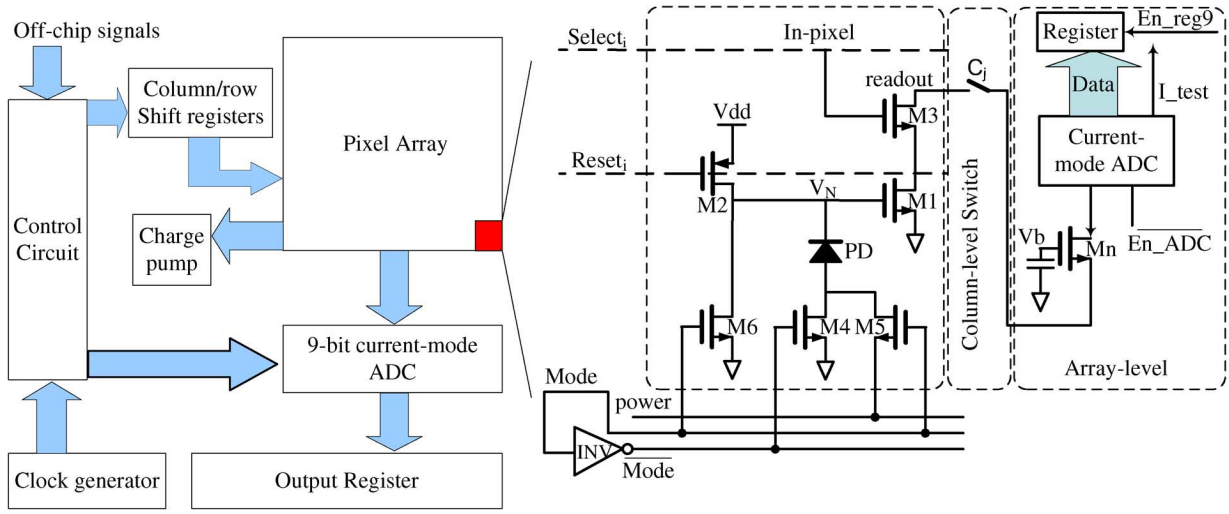

Fig. 1. The proposed imager's architecture.

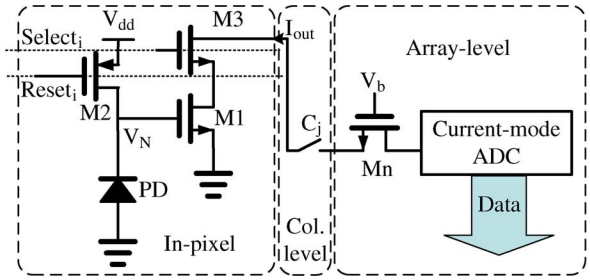

Fig. 2. The equivalent configuration of the proposed current-mode pixel during the imaging mode.

swing at the sensing node V_n can be from V_{th} to V_{dd}. In order to minimize the output current, the transconductance amplifier $M1$ is biased in the triode region instead of the saturation region. This biasing scheme is achieved by using an array-level NMOS transistor as a current limiter Mn and setting its biasing gate voltage V_b properly. With the second order Spice transistor model, the output current of the pixel can be described as

$$\begin{cases} I_{\text{out}} = k_{Mn}(V_{gsMn} - V_{thMn})^2 \\ I_{\text{out}} = k_{M1}\left[(V_{gs1} - V_{th1})V_{ds1} - V_{ds1}^2/2\right] \end{cases} \quad \forall\, V_{gs1} = V_n,\ V_{ds1} = V_b - V_{gsMn} \tag{2}$$

where k_{Mn} and k_{M1} are the device gain factors for transistor Mn and $M1$, respectively. Thus, the output current I_{out} as a function of the sensing voltage V_n can be depicted as (assuming $V_{th1} = V_{thMn} = V_{th}$ and $k_n = nk_1$)

$$\begin{cases} I_{\text{out}} = nk_1\left[\frac{(V_n - V_b)\left(2V_n - A - 2\sqrt{V_n^2 + BV_n + C}\right)}{(1+2n)^2} + D\right] \\ A = 2V_{th} + 4n(V_{th} - V_b) \\ B = 4n(V_b - V_{th}) - 2V_{th} \\ C = (2n+1)V_{th}^2 - 2nV_b^2 \\ D = (V_b - V_{th})^2/(1+2n) \end{cases} \tag{3}$$

Since the parasitic capacitance C_p at the source of Mn is proportional to the array size, the output time constant is dominated by the product of C_p and r_{bus}, where r_{bus} is the impedance at the source of Mn, as shown in (4)

$$\begin{aligned} r_{\text{bus}} &= r_{ds1}//(1/g_{mMp}) \approx 1/g_{mMp} \\ &= 1/\sqrt{(W/L)_{Mn}\mu_n C_{\text{ox}} I_{\text{out}}}. \end{aligned} \tag{4}$$

In order to minimize the impedance r_{bus} without increasing the output current, the transistor channel width of Mn should be large (large value of n). Ideally, if $n \gg 1$, (4) can be simplified as (5), leading to a quasi-linear function of Vn

$$I_{\text{out}} \approx k_1\left[V_n(V_b - V_{th}) + \frac{V_{th}^2 - V_b^2}{2}\right]. \tag{5}$$

In our simulation using a CMOS 0.35 μm technology, the bias voltage V_b of Mn is set to about 450 mV and the transistor size of Mn is set to 300 μm/0.35 μm ($n \approx 1700$), leading to a 2 μA maximum output current when $V_{dd} = 1.35$ V. The settling time is less than 100 ns considering a 500 fF bus capacitance, when the pixel's output reaches to 99.9% of its steady state.

The process variation of the V-I gain parameter $k1$ will introduce variations in terms of output current. Assuming the other parameters are fixed except $k1$, the absolute output signal variation and the percentage of the output signal variation for the saturated current-mode and the linear current-mode APS are given by (6) and (7), respectively

$$\begin{cases} \left.\frac{\partial I_{ds}}{\partial k_1}\right|_{sat} = (V_{gs} - V_{th})^2 \\ \left.\frac{\partial I_{ds}}{\partial k_1}\right|_{lin} = (V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2} \end{cases} \tag{6}$$

$$\begin{cases} \left.\frac{\partial I_{ds}}{I_{ds}\partial k_1}\right|_{sat} = \frac{(V_{gs} - V_{th})^2}{I_{ds}} = \frac{1}{k_1} \\ \left.\frac{\partial I_{ds}}{I_{ds}\partial k_1}\right|_{lin} = \frac{(V_{gs} - V_{th})V_{ds} - V_{ds}^2/2}{I_{ds}} = \frac{1}{k_1} \end{cases}. \tag{7}$$

Assuming $V_{th} = 0.6$ V, $V_{gs} = 1$ V, and $V_{ds} = 0.1$ V, $(\partial I_{ds}/\partial k_1)|_{sat}$ is 4.5 times larger than $(\partial I_{ds}/\partial k_1)|_{lin}$. However, the output current of the saturated current-mode is also larger than the linear mode, as a result, the percentage of the output current variation for both the saturated and linear current-mode APS will be similar.

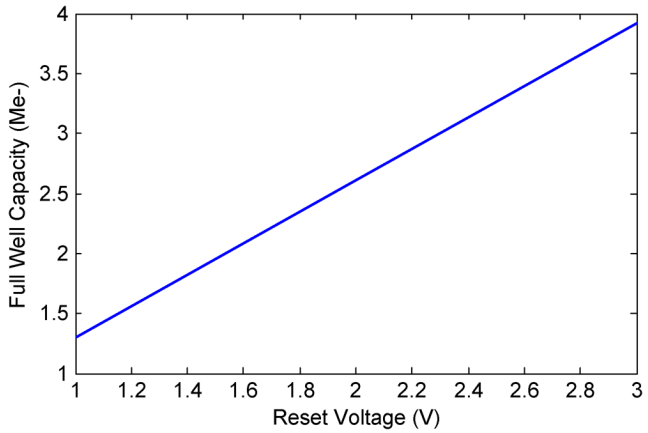

Fig. 3. The FWC as a function of the reset voltage.

The full well capacity (FWC) of the pixel is defined as follows:

$$\mathrm{FWC} = Cpd \times Vrst/e \tag{8}$$

where Cpd is the parasitic capacitance of the photodiode, $Vrst$ is the reset voltage of the photodiode and e is the electron charge (-1.6×10^{-19} C). Cpd is estimated from AMIS 0.35 μm HSPICE model and found to be around 209 fF. The FWC as a function of the reset voltage is illustrated in Fig. 3. The value of FWC in this work is much larger than the value of the conventional APS (normally in the range from 10 ke- to 100 ke-) due to a much larger photodiode area ($15\ \mu\mathrm{m} \times 10\ \mu\mathrm{m}$). It should be noted that, (6) assumes the reset voltage does not affect the parasitic capacitance Cpd. When taking this bias effect into account, the FWC will be increased.

B. Current-Mode ADC

The pipelined scheme is chosen to implement the 9-bit current-mode ADC, as shown in Fig. 4. This choice is made taking into consideration the power/sampling rate and the circuitry complexity. The output current of the pixel is sampled and held at the first bit cell using an NMOS-based capacitor C_{SH}, whose gate leakage current can be ignored using a 0.35 μm process. In this work, the ADC's reference current I_{ref} is 1 μA, which should be twice as large as the maximum output current of the pixel I_{out}. Since 1-bit/stage converting scheme is used, the output residue current is doubled by a current mirror before it enters into the current comparator of the next stage. The current comparator is composed of an NMOS current mirror Mn, a PMOS current mirror Mp and an inverter-based buffer Buf. The channel length of Mn and Mp is set to 2 μm, while the channel width are 2 μm and 4 μm for Mn and Mp, respectively. The transistor size of the buffer is set to the minimum feature. In order to minimize the averaged power consumption, an effective control scheme is implemented to turn on the ADC only during the read-out phase. When En_ADC is "1," the residue current of each stage is only the leakage current and as a result, the total power consumption of this ADC will be lower than 1% of its active state. For instance, at 10 frames/s, the enabled 9-bit ADC consumes a power of about $40\ \mu\mathrm{A} \times 1.35\ \mathrm{V} = 54\ \mu\mathrm{W}$ and the static power is only 300 nW when the ADC and the pixel are disabled. If the sampling rate of the ADC is larger than 1 MS/s, the overall averaged power consumption P_{avg} of the ADC can be estimated as follows:

$$P_{\mathrm{avg}} = 40\ \mu\mathrm{A} \times 1.35\ \mathrm{V} \times 12.3\ \mathrm{ms}/100\ \mathrm{ms} = 6.64\ \mu\mathrm{W}. \tag{9}$$

The ADC's output code as a function of the input current is not ideally continuous, especially when the most significant bit (MSB) changes its value. This discontinuity phenomenon is wildly reported in current mode ADC schemes, as addressed in [8]. This discontinuity can introduce larger random noise, which will be discussed in Section III. However, it should be noted that, the nonlinearity of the whole system is dominated by the pixel's transconductance amplifier $M1$.

C. Control Circuitry

The clock generator is implemented with a three-stage ring oscillator, as shown in Fig. 5. When the clock generator is active ($En_{\mathrm{osc}} = 1$"), the gate voltage of the NMOS tuning transistor M_T in each delay cell is set to a reference value V_{osc} and the ring oscillator can generate a clock signal for the imager system with a certain frequency. The system clock frequency is determined by the sampling rate of the ADC. If $En_{\mathrm{osc}} = 0$", the gate voltage of M_T is equal to zero and thus, the feedback loop is cut off and the imager enters into the energy harvesting mode. The select and reset signals are fed into the pixel array using row and column shift register chains. The pixel is reset row by row and it takes 128 clock cycles to perform the reset of a single row. Assuming the output clock frequency of the oscillator is 1 MHz, the reset operation for each frame takes about 12.288 mS as the same as the read-out time. If the maximum frame rate of this imager is 10 frames/s, the maximum integration time variation between different pixels is only 0.128%, which can be further corrected by external digital signal processing. A programmable 4-bit word $S[3:0]$ is implemented on chip to tune this imager's frame rate. During the integration phase, the shift register chain operates as a counter and the last register output is fed into a 16-stage D flip-flop, which constitutes a 16-stage frequency divider. Different values of S correspond to the D flip-flop's output and as a result, the integration time T_{int} can be determined as

$$T_{\mathrm{int}} = 2^S \times 12.288\ \mathrm{ms}, \quad \forall\, 0 \le S \le 15. \tag{10}$$

Since the harvested voltage at the global power bus V_{bus} is small (normally less than 0.5 mV), it is difficult to use such voltage to charge a battery. In order to increase the output voltage, an on-chip charge pump is implemented, as shown in Fig. 6, with a two-stage NMOS/PMOS cross-coupled structure [9]. By using PMOS transistor, this charge pump can significantly reduce the body effect on the second stage. The output voltage V_{out} of the charge pump could reach up to $V_{\mathrm{out}} = V_{in} + V_{thn} + V_{thp}$, which can be utilized to charge an external battery.

III. Experimental Results

The pixel layout is illustrated in Fig. 7. It occupies a pixel area of $21 \times 21\ \mu\mathrm{m}^2$ and achieves a fill-factor of 39% in

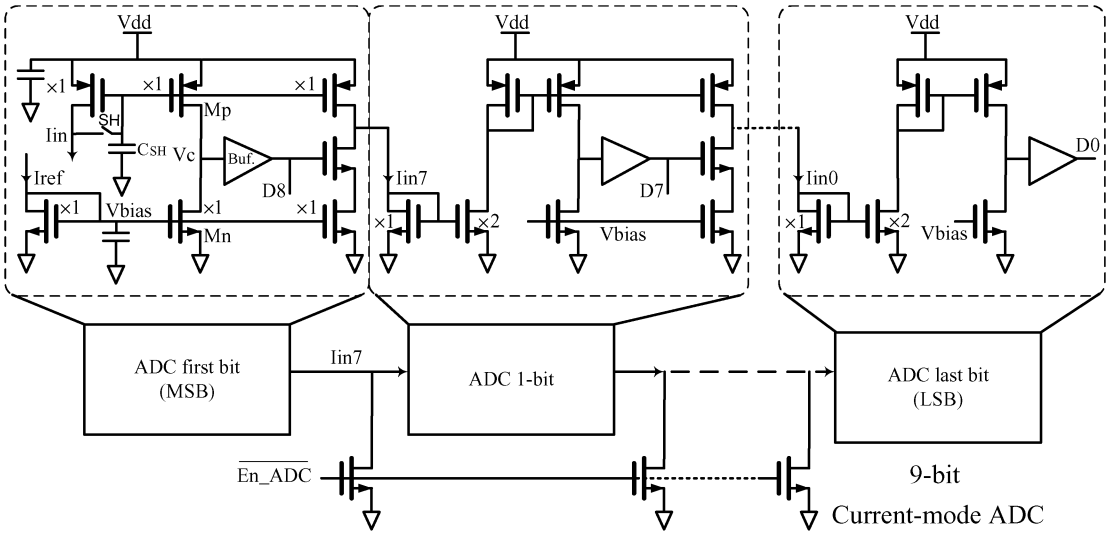

Fig. 4. The implemented 9-bit current-mode pipelined ADC schematic.

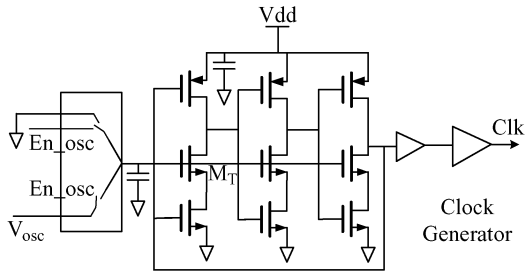

Fig. 5. The implemented clock generator schematic.

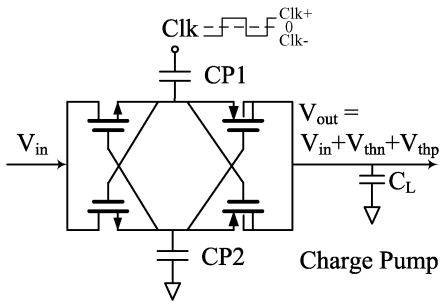

Fig. 6. The implemented charge pump schematic.

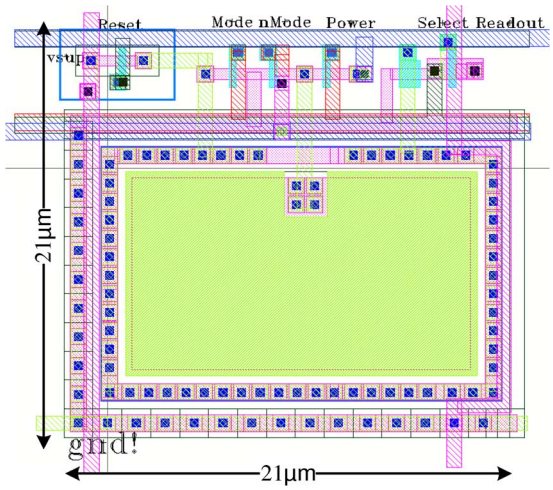

Fig. 7. The pixel layout including a P+/N-well energy harvesting photodetector, a Psub/N-well signal photodetector and six transistors. It occupies an area of $21 \times 21\ \mu\mathrm{m}^2$ in 0.35 μm CMOS technology.

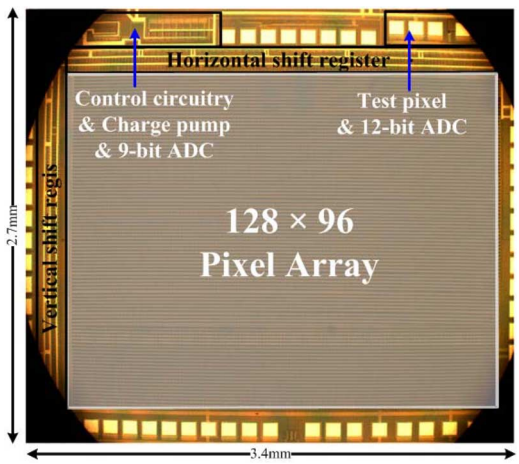

Fig. 8. The chip microphotograph. The chip is designed in 0.35 μm CMOS technology and occupies a total area of 8 mm^2.

0.35 μm CMOS technology. Fig. 8 illustrates the microphotograph of the prototype chip occupying a total area of 8 mm^2. Over 90% of the area is occupied by the 128 × 96 pixel array. Fig. 9 shows the DC output code of the current-mode ADC as a function of the voltage at the sensing node Vn. The measured response is shifted right compared with the simulation result, mainly due to the process variation of the CMOS technology. In Fig. 10, the measured random noise of the read-out circuit is plotted as a function of V_n, which is obtained by a 12-bit current-mode ADC using the same bit cell. For each measured point, 15 000 sampled data are recorded and the random noise is calculated by computing the standard deviation. It should be noted that, the measured data is not a monotonic function of the sensing voltage. One possible explanation is related to timing mismatch where at some points in the conversion (for example, "100000000" or "110000000"), where the most significant bits are "1" and the less significant bits are "0," a sudden input

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED DESIGN AND COMPARISONS WITH RELATED ART

Specifications	This work	Cho [11]	Gottardi [3]	Jun Ohta [2]	K. B. Cho [12]
CMOS technology	0.35μm	0.13μm	0.35μm	0.35μm	0.35μm
Pixel resolution	128 × 96	128 × 128	128 × 64	128 × 96	176 × 144
Supply voltage	1.35V	0.75V/1.25V	3.3V	1.35V	1.5V
Pixel pitch	21um	3.4um	26um	10um	5um
Pixel structure	6-T PMOS/NMOS	3-T NMOS	45-T PMOS/NMOS	3-T NMOS	3-T NMOS
Fill-factor	39%	38%	20%	18.5%	30%
ADC	9-bit Current-mode	10-bit	Contrast-based asynchronous	9-bit	8-bit
Frame rate	9.6 fps	15 fps	<4k fps	9.6 fps	30 fps
Power (sensor array)	3.2pW/frame.pixel	7.7pW/frame.pixel	N/A	3.6pW/frame.pixel	N/A
Power (ADC)	6.64uW@10fps	N/A	N/A	25uW@9.6fps	N/A
Power (total)	10uW@10fps 84pW/frame.pixel	N/A	22uW@10fps 269pW/frame.pixel	55uW@9.6fps 460pW/frame.pixel	550uW@30fps 723pW/frame.pixel
Random noise (dark)	>0.4% or 2LSB (raw)	0.73mVrms	N/A	0.95LSB	0.85LSB
Pixel FPN (dark)	>1% raw FPN (raw)	0.66%	N/A	0.12%	N/A
Well capacity	1.25 Me-	21 ke-	N/A	N/A	26 ke-
Dynamic Range	60dB	54dB	100dB	51.3dB	49dB
Energy Harvesting	80nA @ 350lux 9.7μA @ 3500lux	N/A	N/A	N/A	N/A

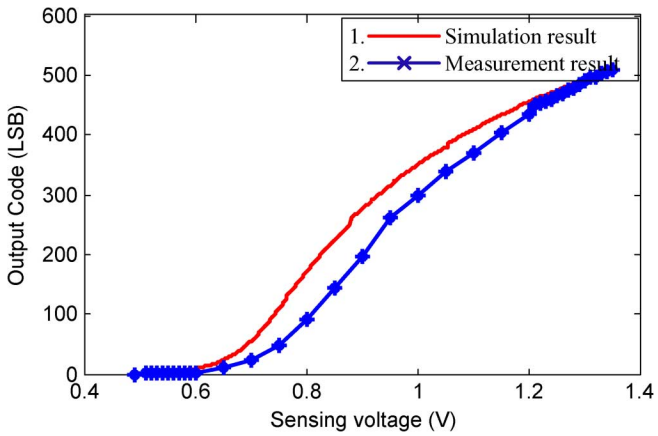

Fig. 9. The simulated and measured output code of the ADC as a function of the input signal.

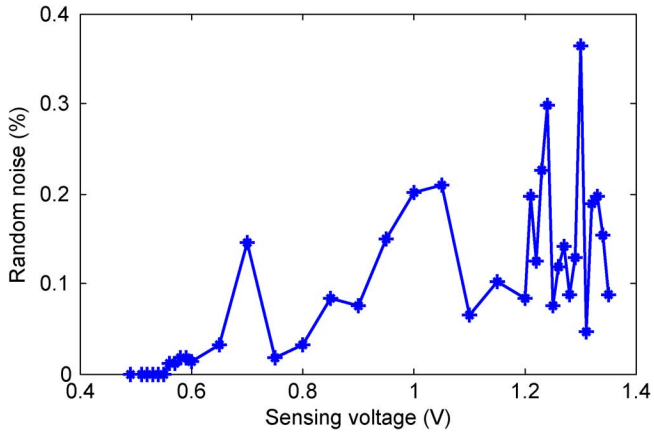

Fig. 10. The measured output random noise.

noise current can change the most significant bit value. If the less significant bits cannot generate the proper result before the output code is latched into the 9-bit registers, a large random noise can be introduced. Inserting a sample-and-hold circuit between each stage can significantly reduce such random noise. Increasing the supply voltage and the reference current can increase the signal-to-noise ratio (SNR). Nevertheless, the maximum random noise of the read-out circuit is still less than 0.4%, which determines SNR in dark, since the overall temporal noise of the imager in dark is dominated by the read-out noise [10]. Fig. 11 shows the captured image in dark illumination level when the random noise is removed from the raw image by the multisampling technique. As a result, the noise shown in Fig. 11 represents the fixed pattern noise

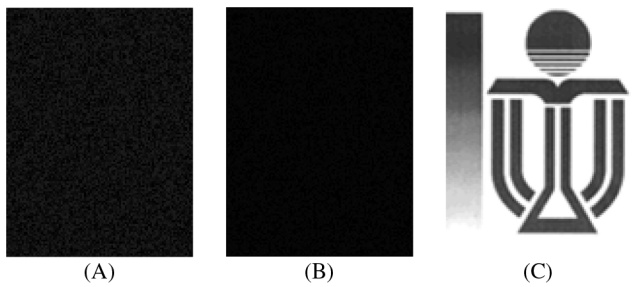

Fig. 11. (a) The captured raw image in dark (1% raw FPN with ten times amplification), (b) the corrected image by external digital CDS process (0.4% FPN with ten times amplification), and (c) a sample image captured at 10 f/s.

(FPN) in dark. Fig. 11(a) illustrates the raw FPN amplitude and allocation, while Fig. 11(b) shows the captured FPN image

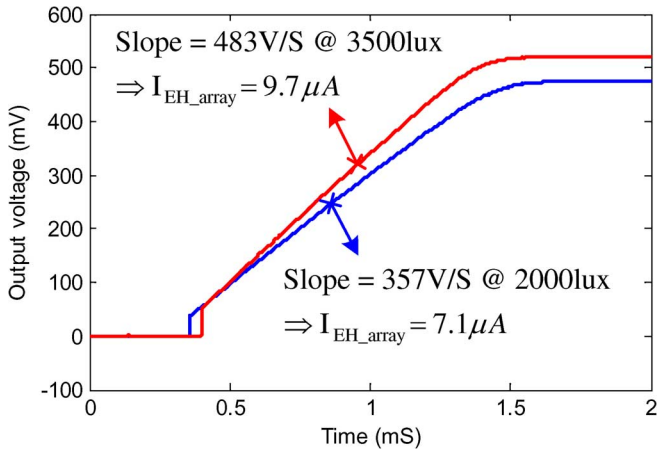

Fig. 12. The measured transient response of the harvested output voltage with a 20 nF load capacitor at 2000 and 3500 lux.

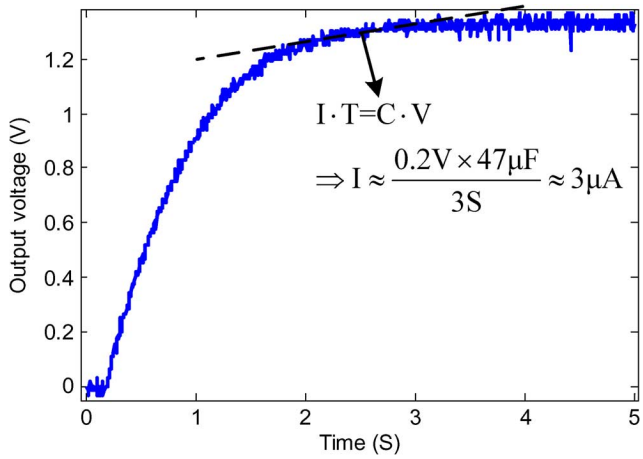

Fig. 14. Measured output transient voltage response of the charge pump at 600 lux illumination level with 47 μF load capacitance.

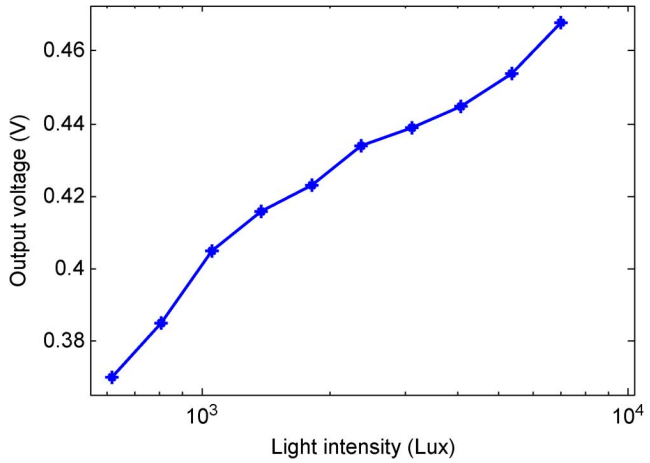

Fig. 13. Measured harvested output voltage (before the charge pump) as a function of the light illumination level.

after digital correlated double sampling correction (CDS) [13] and Fig. 11(c) shows a sample image captured at 10 f/s. About 1% raw FPN is measured at 10 frames/s in dark, while the corrected FPN is about 0.4%. The corrected FPN by the digital CDS is worse than the voltage mode APS scheme [14] mainly due to the strong nonlinearity of the in-pixel voltage-to-current transconductance amplifier. The operation speed of the ADC is also measured by feeding a sinusoid voltage signal into the sensing node V_n and the measurement result shows that up to 1.8 MS/s sampling rate can be achieved without obvious output distortion, which is consistent with the simulation result. The large well capacity can be achieved from a large pixel size which leads to a large photodiode area.

Fig. 12 illustrates the output transient measurement response in the energy harvesting mode. An 80 nA and a 9.7 μA current generated by the pixel array are measured at 350 lux and 3500 lux, respectively. At 3500 lux, a harvested power figure of $9.7\,\mu\text{A} \times 0.5\,\text{V} = 4.85\,\mu\text{W}$ is obtained. Since each frame in the imaging mode consumes about $10\,\mu\text{W} \times 0.1\,\text{s} = 1\,\mu\text{J}$, ideally operating in the energy harvesting mode for 200 mS can provide enough energy for one frame image capturing. Fig. 13 shows the relationship between the harvested output voltage and the environmental light intensity. Measurement results illustrate that the output voltage is approximately proportional to the log scale of the light intensity. The functionality of the charge pump is also measured in this work. Fig. 14 illustrates the measured transient response of the charge pump's output voltage. During this measurement, the capacitance of $CP1$ and $CP2$, as shown in Fig. 6, is 10 nF and the load capacitance C_L is 47 μF. The clock frequency is 1 KHz and the voltage swing of the clock signal is $\pm$1.35 V. The slope of this transient response represents the harvested current which can be used to charge the external battery. According to the measurement result in Fig. 14, the instantaneous current is about 3 μA, when the voltage at the loading capacitor is 1.3 V at 600 lux illumination level. Table I summarizes the performance of the proposed design and compares it with state-of-the-art related imagers. The table highlights the main features of the proposed design namely a state-of-the-art low-power consumption with the possibility of reconfiguring the design into energy harvesting mode.

IV. Conclusion

In this paper, an ultra-low-power 128×96 image sensor array with energy harvesting capability is fabricated and successfully measured using a 0.35 μm CMOS technology. The pixel operates in the current-mode under the triode region, with a single transistor biasing scheme. The output current signal is directly digitized using a 9-bit current-mode pipelined ADC. This imager features an 84 pW/frame per pixel power consumption, which is to the best of our knowledge the lowest power ever reported for CMOS image sensors. Additionally, the proposed pixel can be reconfigured into the energy harvesting mode, using the existing in-pixel photodetectors. Measurement results show that 9.7 μA current can be utilized at 3500 lux light intensity. By implementing an on-chip charge pump, the harvested voltage can be further enhanced up to about 1.7 V, which can be used for external battery charging. The total chip area is about 8 mm^2 and the pixel pitch is about 21 μm with a 39% pixel fill-factor. This low-power consumption and energy harvesting capabilities make the proposed CMOS image sensor very suitable for extended lifetime wireless sensor network applications.

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