2.6 A 3.6pW/frame·pixel 1.35V PWM CMOS Imager with Dynamic Pixel Readout and no Static Bias Current

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Low-power operation of CMOS imagers using a low voltage (around 1V or less) compatible with deep submicron logic circuits enables new imager applications, such as disposable medical cameras and autonomous wireless security cameras on a chip. Pulse width modulation (PWM) [1-2] is promising for this purpose. A PWM pixel can convert light intensity to a digital pulse width by using an in-pixel comparator with a low power-supply voltage without any degradation of signal-to-noise ratio (SNR). The benefit comes from a small jitter noise in pulse coding, which is suppressed by using a voltage gain larger than unity for the in-pixel comparator. In contrast, the source-follower used in a CMOS active pixel sensor (APS) suffers from degraded SNR due to its gain being less than unity.

One of the critical issues in PWM imagers is pixel size [2-3]. To shrink the pixel size, we have demonstrated a 3T/pixel configuration with an in-pixel common-gate amplifier (CGA) [4]. The CGA PWM scheme simplifies the sensor structure by eliminating the large capacitors required for correlated double sampling (CDS). These large capacitors are not required because the feedback reset of the photodiode (PD) used in the CGA PWM scheme suppresses the pixel fixed-pattern-noise (FPN) and the remaining FPN is further suppressed with digital CDS.

In this paper, we propose and demonstrate a low-power dynamic pixel readout (DPR) scheme with CGA PWM pixels based on dynamic operation of in-pixel comparators. DPR requires no static bias current even in the pixel readout. The power dissipation of the pixel array is dramatically reduced by 1 to 2 orders of magnitude compared with using normal static pixel readout (SPR).

Ordinary source-follower-based APSs biased by constant currents cannot use dynamic power reduction techniques for digital circuits (e.g., see Chapter 14 in [5]). To implement DPR in this work, current load activation and precharge switches were added to each vertical signal line. Static bias current is required only during pixel reset, which minimizes power dissipation because the reset period is very short. A 128×96-pixel CGA PWM imager with column-parallel 9b ADCs was prototyped in a standard 0.35μm CMOS technology. When the imager was operated with a single 1.35V power supply, the figure-of-merit (FOM) of the power dissipation, which is defined by normalizing the power dissipation at the pixel array by the product of the frame rate and the number of pixels, in SPR was reduced from 128pW/frame pixel to 3.6pW/frame pixel with DPR. The experimental results suggest that the proposed scheme should enable the realization of a 100μW, 30fps, 1Mpixel imager or a 144μW, 8fps, 5Mpixel imager. Use of low-threshold transistors with a V_{TH} less than 0.25V will enable a sub-1-V imager using this scheme, although V_{TH} was around 0.6V in the prototype.

Figure 2.6.1 shows a simplified schematic of the CGA PWM imager including its pixel circuit. Note that index $<i,j>$ indicates the horizontal (column) and vertical (row) positions in the array. To completely turn on the switches, bootstrapping was used in the ramp-selector, row-select, and row-reset transistors.

Figures 2.6.2 and 2.6.3 depict the pixel operating principle and a timing chart for one horizontal period (1H). 1H is composed of precharge, readout (discharge), and reset periods. The key point of the scheme is that the pixel readout needs no static bias current due to the dynamic operation of the in-pixel comparator. For comparison, part iv of Fig. 2.6.2 shows static pixel readout. In that case, the in-pixel comparator is always biased by a constant current. Before the pixel readout, $V_{SIG}<i>$ is precharged to V_{DD} by asserting the signal NPRECH with all row select transistors and column current loads off. During pixel readout, the vertical signal line acts as a dynamic memory, and its parasitic capacitance holds the precharged level. After the latch memory storing the temporary ADC result is initialized by activating the signal INITMEM, a decremental ramp waveform from the ramp generator is applied to $V_{RAMP}<j>$ through the ramp selector. The in-pixel CGA (M_{AMP}) compares $V_{RAMP}<j>$ with the PD voltage, $V_{PD}<i,j>$. The start and end voltages of the ramp are denoted by $V_{RAMP,ST}$ and $V_{RAMP,END}$, respectively. When $V_{PD}<i,j> - V_{RAMP}<j>$ reaches $V_{TH,AMP}$, M_{AMP} turns on to quickly discharge $V_{SIG}<i>$ down to $V_{RAMP}<j>$ from V_{DD}. Note that $V_{TH,AMP}$ is the V_{TH} of M_{AMP}. The pulse width is defined by the period from the start of the ramp to the time when $V_{SIG}<i>$ becomes equal to the threshold voltage of the column comparator, $V_{TH,CMP}$. The pulse width depends on the voltage drop of the PD during accumulation, $\Delta V_{PD}<i,j>$, from the reset level including pixel FPN, $V_{PD,RST}<i,j>$. Note that $V_{PD}<i,j> = V_{PD,RST}<i,j> - \Delta V_{PD}<i,j>$. The method for converting the pulse width to a digital value is the same as a single-slope ADC [6]. M_{AMP} requires a bias current only during the reset period. In this period, $V_{RAMP}<j>$ is set to $V_{RAMP,RST}$. The comparator works as a common-source amplifier, and $V_{PD}<i,j>$ is reset to $V_{PD,RST}<i,j> = V_{RAMP,RST} + V_{TH,AMP}<i,j>$. It is known that such a feedback resetting configuration reduces the pixel-level FPN included in $V_{TH,AMP}<i,j>$. In the accumulation period, $V_{RAMP}<j>$ becomes $V_{RAMP,HLD}$ (= V_{DD}) to turn M_{AMP} completely off to suppress sub-threshold leakage.

In the circuit design, the resistance of the horizontal ramp signal line must be small enough to suppress its input-image-dependent voltage fluctuation. The maximum fluctuation is approximately proportional to the square of the number of horizontal pixels, the resistance, and the peak current of the in-pixel comparator per pixel, which should be less than 1/2 the LSB of an ADC. Pixel layout is also important to avoid unexpected discharge of the vertical signal lines by the photo-generated carriers.

Figure 2.6.4 shows a micrograph of the CGA PWM imager. A timing generator and a bias circuit are provided off-chip. Figure 2.6.5 shows a captured image with DPR after digital CDS. For each row, readout of the signal level was followed by that of the reset level and external digital CDS (subtraction of the reset level from the signal level) was performed off-chip.

The table in Fig. 2.6.6 compares characteristics of DPR with those of SPR; the sensor chip was the same, but the applied signals were different. The in-pixel comparator gain was defined by the slew rate of the discharging period of the pixel output divided by that of the incident ramp signal. The power dissipation levels with DPR in the pixel array and the whole chip were reduced to 2.8% and 74% of those with SPR, respectively. Random noise was reduced possibly because there was no noise contribution from the current source in DPR. The FOMs for DPR and SPR of the prototype, and for the imager in [7] with a 1.5V power supply were 3.6, 128, and 8.7pW/frame pixel, respectively. The scheme presented here has the lowest power dissipation.

Acknowledgments:
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References:

[1] M. Nagata, M. Homma, N. Takeda et al., "A Smart CMOS Imager with Pixel Level PWM Signal Processing," *Symposium on VLSI Circuits Dig. Tech. Papers*, pp. 141-144, June 1999.
[2] D.X.D. Yang, A. El Gamal, B. Fowler et al., "A 640×512 CMOS Image Sensor with Ultrawide Dynamic Range Floating-Point Pixel-Level ADC," *IEEE J. Solid-State Circuits*, pp. 1821-1834, Dec. 1999.
[3] M. Shouho, K. Hashiguchi, K. Kagawa et al., "A Low-Voltage Pulse-Width-Modulation Image Sensor," 2005 *IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, pp. 226-229, June 2005.
[4] K. Kagawa, S. Sanshiro, T. Sasaki et al., "A Low-Voltage PWM CMOS Imager with Small Pixel Size Using an In-Pixel Gate-Common Comparator," *IEICE Electronics Express*, pp. 271-276, Apr. 2007.
[5] R. Baker, H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, Wiley-InterScience, New York, 1997.
[6] T. Sugiki, S. Ohsawa, H. Miura *et al.*, "A 60mW 10b CMOS Image Sensor with Column-to-Column FPN Reduction," *ISSCC Dig. Tech. Papers*, pp. 108-109, Feb. 2000.
[7] K. Cho, A.I. Krymski and E.R. Fossum, "A 1.5-V 550- W 176×144 Autonomous CMOS Active Pixel Image Sensor," *IEEE T. Elec. Dev.*, pp. 96-105, Jan. 2003.

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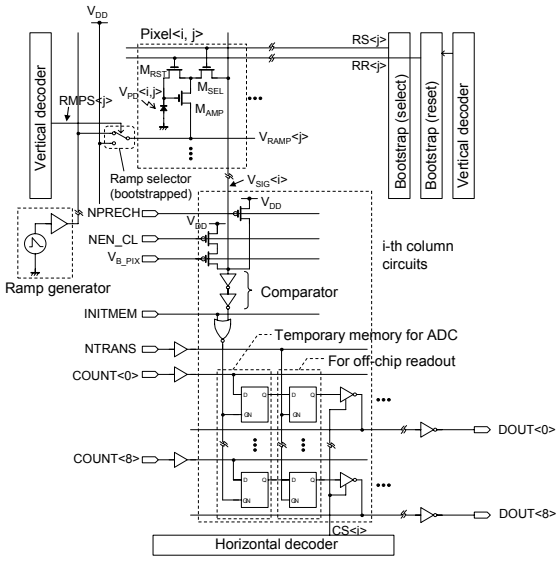

Figure 2.6.1: Schematic of GCA PWM CMOS imager.

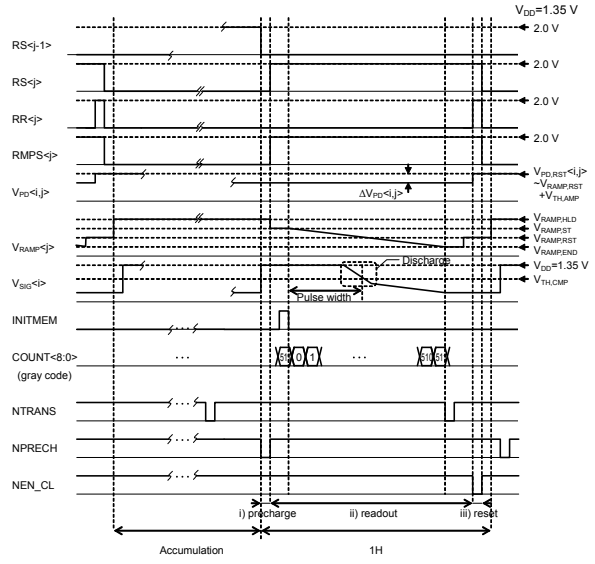

Figure 2.6.3: A timing chart of pixel operation.

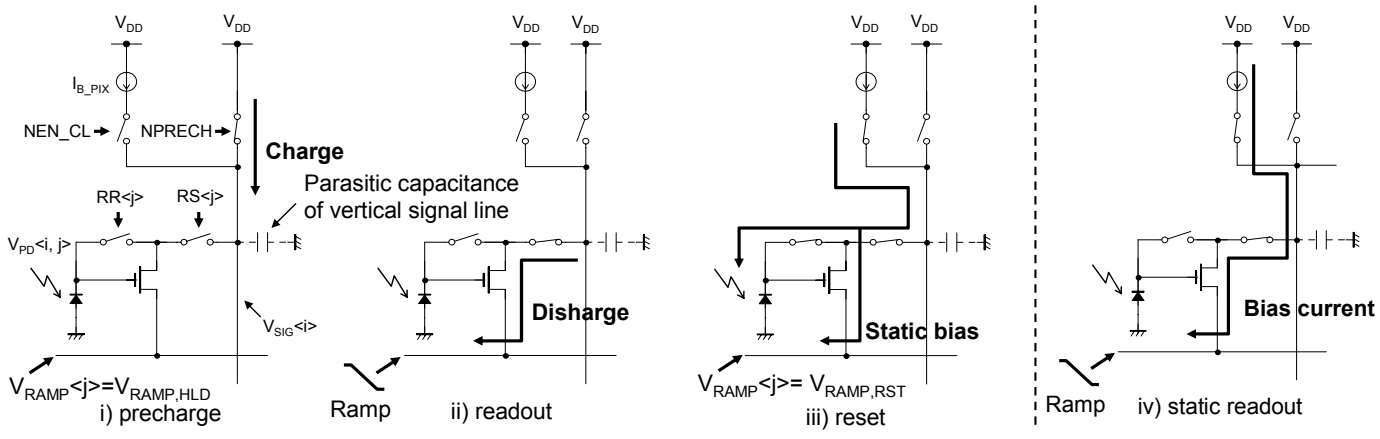

Figure 2.6.2: Pixel operations.

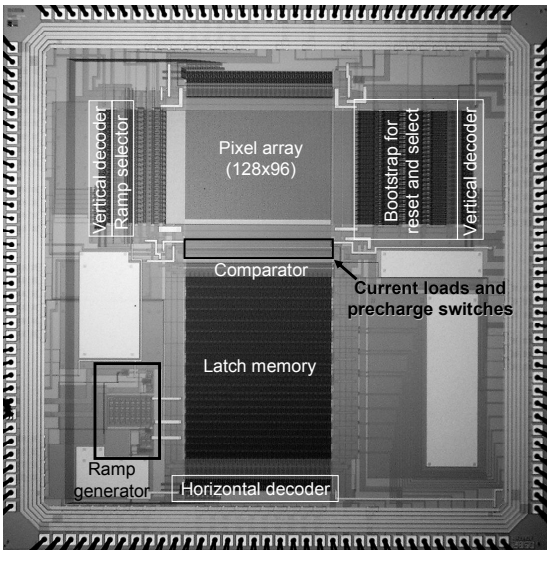

Figure 2.6.4: Micrograph of the fabricated CMOS imager.

V_{DD}=1.35V, $V_{RAMP,ST}$=380mV, $V_{RAMP,END}$=180mV, $V_{RAMP,RST}$=296mV

Figure 2.6.5: An example of the captured image after digital CDS operation.

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Technology	0.35-μm CMOS (2P3M, no photodiode option)	
Pixel size	10μm sq.	
Pixel count	128x96	
Power supply voltage	1.35V	
Fill factor	18.5%	
Frame rate	9.6fps	
	Static pixel readout (SPR)	Dynamic pixel readout (DPR)
Random noise (dark)	1.25LSBrms	0.95LSBrms
Pixel FPN (dark)	0.55%rms	0.12%rms
Column FPN (dark)	0.07%rms	0.03%rms
Sensitivity	784LSB/lx·s	792LSB/lx·s
Gamma	0.96	0.90
Dynamic range	51.3dB	53.7dB
In-pixel comparator gain	15.3	10.6
Power consumption (dark)	15.1μW (pixel array), 74.1μW (whole chip)	0.42μW (pixel array), 55.2μW (whole chip)
FOM (pixel array)	128pW/frame·pixel	3.6pW/frame·pixel

Figure 2.6.6: Specifications and characteristics of the PWM CMOS imager.

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