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Design and Implemention of ADC Implanted in 10 000 Frame/s High-Speed CMOS Sensor

Eri Prasetyo Wibowo, Hamzah Affandi, Boesono Soerowirdjo, B. Heruseto, Purnawarman Musa, and Michel Paindavoine

***Abstract*—This paper describes the design of pipeline ADC embedded in a high speed CMOS sensor that has been designed and fabricated by Paindavoine. The idea of ADC to be embedded in the high speed cmos sensor in order to reduce power, integrated so that the output of the CMOS sensor is already in digital form. An ADC is designed using Pipeline topology with considerations is simple in the design because it just makes a stage and the next stage is duplicated, relatively high speed and have good resolution. Pipeline ADC designed using 0.35 µm CMOS technology. Pipeline ADC successfully implemented in a electronics circuit and layout. It has been fabricated. The results of simulations show that the design of pipeline ADC is working properly and can be used to handle a high speed CMOS sensor that has speed of 10 000 frames/s.**

***Index Terms*—ADC, CMOS, high speed, pipeline. frame**

I. Introduction

Recently, improvements in the field of digital imaging world have been growing with two main image sensor technologies, namely, charge-coupled devices (CCD) and CMOS sensors. The continuous advances in CMOS technology for processors and DRAMs have made CMOS sensor arrays became alternative to the popular CCD sensors. New technologies provide the potential for integrating a significant amount of VLSI into a single chip, thereby, greatly reducing the cost, power consumption and size of the camera [1]-[4].

CMOS has major advantages in its management that can be incorporated with the sensor and converter level design. This indicates that CMOS has potential opportunities in the ease of design on a single chip, which is frequently termed as System on Chip (SoC).

As integrated circuits (IC) keep scaling down following Moore's Law, recent trends show a significant number of papers discussing the design of digital pixels [5]–[8] This trend is mainly motivated by the advantages of pixel-level analog-to-digital (A/D) converter such as high SNR, lower power consumption, and very low conversion speeds. Nevertheless, the resulting implementations of in-pixel analog-to-digital converter (ADC) are rather area consuming, strongly restricting the image processing capability of CMOS sensors.

A preliminary experiment for testing the CMOS sensor has been conducted by Michel Paindavoine et.al [9], [10]. In the experiment, an external ADC was used as data converter to input the FPGA. The test system is illustrated in Fig. 1.

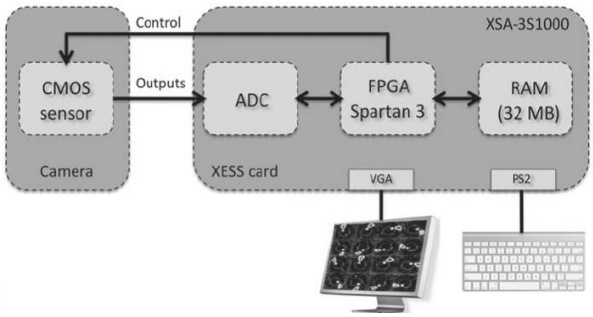

Fig. 1. Test of high speed camera experiment [9]

In the figure, the ADC was separated from CMOS sensor. In the next experiment CMOS sensor and ADC are designed and fabricated in the same single chip but independent of one another to facilitate the testing. The concept of this embedded ADC design is given in Fig. 2. The chip to be designed is illustrated at the most left of the figure.

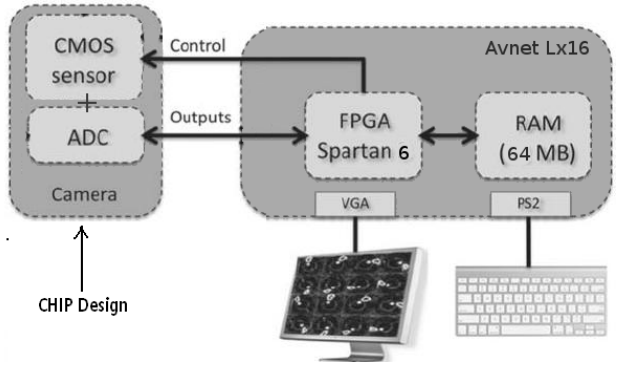

Fig. 2. Embedded ADC with CMOS sensor

This paper focuses on the design of ADC. It describes the acquisition system in parallel columns of pixels so that the speed of the acquisition up to 1.5625 µs per row (100 µs/64) or, approximately, 10,000 frames/second could be achieved. Further design and fabrication of the ADC is aimed to fulfill the above specification, i.e., to support high-speed sensor

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with conversion rate at 10,000 frames/second and minimum resolution of 8 bits. Pipeline type of the ADC has been carefully justified, and simulated using CAD software in the 0.35 μm CMOS technology.

II. Global Design

Before discussing the design of electronics circuit pipeline ADC, we will describe global design layout photograph, as is shown in Fig. 3. In the photograph, there are two separate designs. The first design is a high speed CMOS sensor containing a series of a 64x64 image sensor. The design also includes Linear and Non-linear analog processing unit in focal-plane. This design is carried out by a team of Universite de Bourgogne. On the other hand, the second part of the design is an 8 bits pipeline ADC, which is done by a team of Gunadarma University. The layout size of the sensor design is 8.99 mm2. While the size of 8 bits pipeline ADC would occupy 1mm x 0.800μm (1000μm x 800μm) and consisting of 734 transistors 49 poly-silicon capacitors.

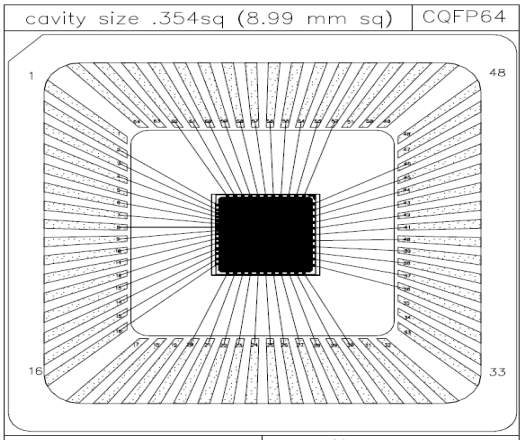

Fig. 3. Layout design of CHIP

The chip was designed and implemented using a 64 pins with CQFP64 models. Fig. 4 shows PINs designation of both designs.

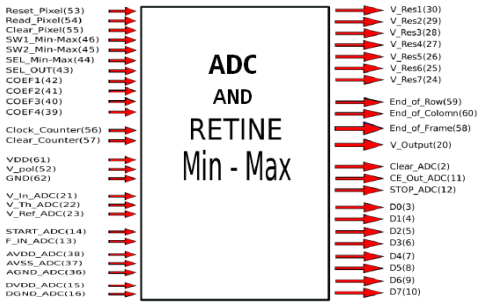

Fig. 4. The pin block global of Circuit

III. Circuit of Pipeline ADC Design

Block design of pipeline ADC is shown Fig. 5, composed of 8 stages with 1-bit/stage topology. Topology of 1-bit per stage requires some supporting components, namely, Op-Amp, Comparator, DAC (reference) and switch capacitor (SC). The principle of pipeline is a step process. Therefore, 8 bit ADC requires 8 stages synchronous digital outputs by employing 8 units delay circuit (D-FF). Clock is also needed to generate the ADC and the pulse delay unit (D-FF).

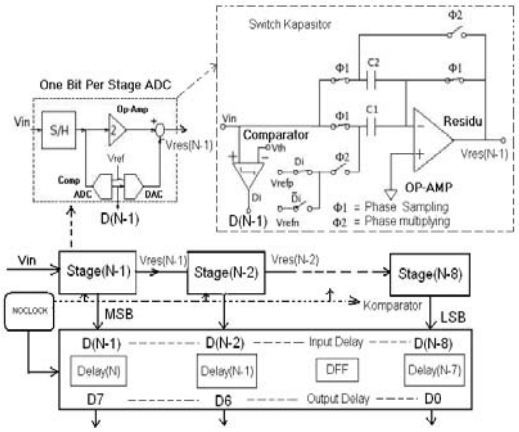

Fig. 5. Diagram block of 8 bits pipeline ADC 80 MSPS

The operation of the circuit is given in the following. If a DC input voltage *Vin* and frequency fin enters stage (N-1) in Fig. 5, the voltage is then sampled and held (S / H) at a sampling frequency (fs > 2fin). For fs = 80MHz, (equivalent to 12.5 ns), the sampling period would be 6.25ns and the hold time is 6.25ns. During the hold time of 6.25 ns, input signal is sampled and stored in the capacitor.

During the 2nd period of the sampling, the capacitor will charge and its voltage rises to the sampled voltage value *Vin* (Φ1). At the same time, the sampling voltage *Vin* is compared to a threshold voltage *Vth*. If *Vin* is higher than *Vth*, the output of the ADC will be at high level (=1). On the other hand, if *Vin* is lower than *Vth*, the ADC output will be low (=0). The completion of the sampling process will then be followed by multiplying process (Φ2) to obtain a residual voltage (*Vres*), which is required as input to the next stage.

If the digital value (Di) = 1, then the value of residue is

$$Vres(i) = 2xVin(i) - DiVrefp \quad (1)$$

If digital value (Di) =0, residual voltage is

$$Vres(i) = 2xVin(i) - Di.Vrefn \quad (2)$$

where value of *Vrefp*=2Vth and *Vrefn*=0V.

Fig. 6 is the elaboration of Fig. 5. The figure shows the design of 8-bits 80 MSPS pipeline ADC with 1 bit / stage topology.

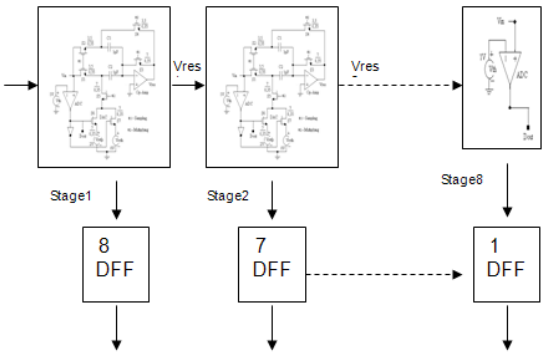

Fig. 6. Diagram block of 8-bits, 80 MSPS pipeline ADC circuit.

An 8-bits ADC requires 7 complete stages and 1 stage

comparator. Serial connection of the stages requires time delay circuit at each stage in order to produce output (Dout) in a parallel manner. By giving *Vin* from 0V to 2V with *Vth* = 1V, *Vrefp* = 2V and *Vrefn* = 0V, in which a given clock 256 the sampling time and multiplying. So that the length of time the conversion from 0V to 2V is 12.5 ns x 256 = 3.2 uS. With 1 step = 2V/256 = 7.8125 mV and DNL = ½ LSB = 3.9 mV.

A number of 36 pieces of positive edge-trigger D-FF are used for the delay-time circuit. If one D-FF consumes 200µW, it needs a total power consumption of only 7.2 mW.

IV. Layout of Pipeline ADC Design

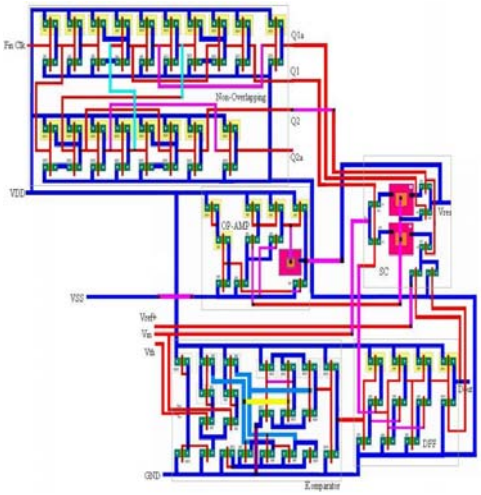

Fig. 7. Lay-out design of 1 bit /stage Pipeline ADC

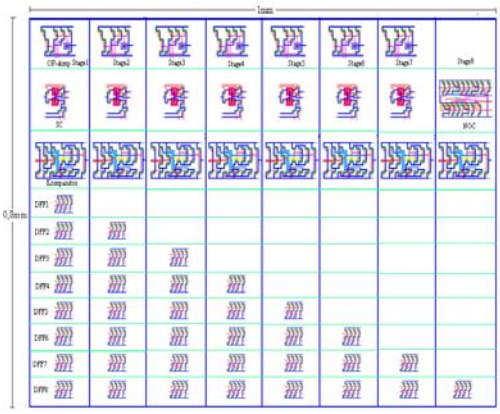

Fig. 8. Lay-out design of 8-bit pipeline ADC

Design of the layout of the ADC is implemented using the library from 0.35 µm AMS technology which exploits 4 metals for components interconnection. Figure 7 is a draft of 1-bit/stage ADC layout which, totally, occupies 280µm x 500µm area. As shown in the figure, the layout consists of 3 different parts as of the followings. The top part, which is the non-overlapping clock generator, occupies an area of 280µm x 125µm. A clock circuit is designed to drive the 7 stages and 1 stage SHA. The middle part of the layout consists of a series of op-amp and switch capacitors having 280µm x 250µm area. This part occupies the largest area due to 3 poly capacitors sitting in it. The bottom part comprises of a unit that contains the comparator ADC and latches to create digital output Dout, with an area of 280µm ×125µm.

The complete layout of the 8 bits pipeline ADC is seen in Fig. 8. It consists of 734 transistors and 49 poly capacitors. The area occupied for the ADC is 1000µm x 800µm.

V. Simulation Results

A series of simulations is carried out on both the electronic circuits design as well as on the layout design. For the electronic circuit, simulation is experimented to the one-bit ADC as well as to the 8 bit ADC. Simulation to one-bit ADC is important and intended to check the accuracy of the resulting residual values, which will be inputted to the next state.

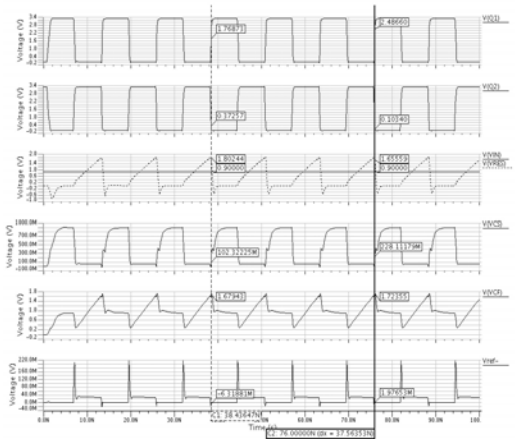

Fig. 9. Simulation results of 1 bit ADC with VIN=0.9V

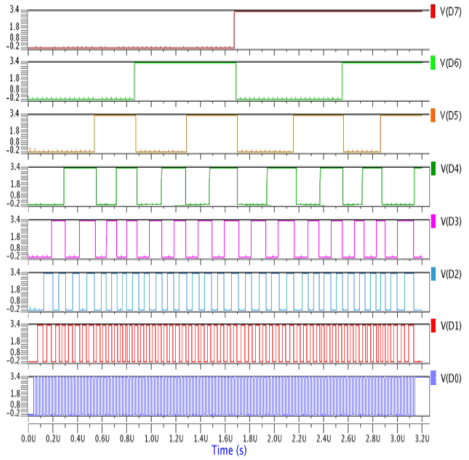

Fig. 10. Simulation of digital pipeline 8-bits ADC.

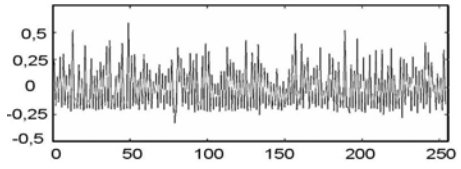

Fig. 11. DNL with ±0,6LSB

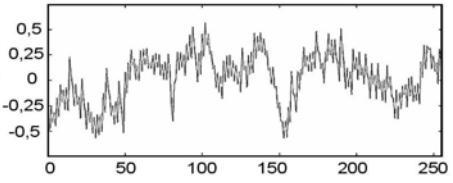

Fig. 12. INL with ±0,6LSB

Fig. 9 shows the result of one-bit ADC simulation. With Vin = 0,9V, the resulted value Vres at the ADC output is 1,80244V. Calculated residual value Vres for the same Vin would be 2.44mV. The difference between Vin value resulted from simulation and from calculation indicates an error of 0.24%. The next simulation is to examine the digital output of 8-bits ADC. The simulation is done by varying Vin from 0V to 2V where result of simulation can be seen at figure 10. These simulation to see the length of time the conversion and the error of each bit digital output that occurs. Analog input is given from 0V until 2V and a clock time it takes the length of 12.5 ns so conversion time is 3.2 uS (12.5 ns x 256). Suppose the input signal of 1.2 V and the resulting digital signal (10,011,001) error occurs 153 x 7.8125 mV = 1.195 V difference with 1.2 V input signal there is 5mV (± 0.6 LSB). To convert the analog signal 1.2 V takes time (12.5 ns x 8stage / 2 phase = 50ns), this ADC pipeline are eligible when each a pixel sensor has time of 100ns (Fs = 2Fin). With speed cameras 10,000 frames / s, each a frame comes is required 100 us, the method of reading the required time 100 µs /64-row = 1.5625 µs /row, so an ADC is given conversion time of 1.5625 µs. 8-bit pipeline ADC takes 50 nS/1-input analog conversion. Simulation results are shown in figure 10, a pipeline ADC has long conversion 3.2 uS (analog pixel signals of 0V to 2V) and this is enough to accommodate input from a camera with speed of 10 000 frames / s (100 µs/64).

From Simulation results of 8 bits ADC as shown in figure 10, can be calculated error value (error) of DNL and INL , the magnitude are ± 0.6 LSB. DNL and INL values shown in Fig. 11 and 12.

VI. Conclusions

8 bits pipeline ADC successfully designed over speed of 80 MSPS, so it is able to convert the output of high speed CMOS sensor has a speed of 10 000 frames / s.

The simulation results shown that the pipeline ADC worked very good, it was expressed with a small residual error and the digital error are 0.6 INL and 0.6 DNL.

Pipeline ADC is designed in a layout and has been sent to the fabrication process.

8 bits Pipeline ADC is designed using 734 transistors and 49 poly capacitors. While the size of the layout is 1mm x 0.8 mm.

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