Sigma-delta column-wise A/D conversion for cooled ROIC

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ABSTRACT

Designing a digital IR focal plane array (IRFPA) requires fulfilling very stringent requirements in terms of power consumption, silicon area and speed. Among the various ADC architectures like successive approximation, ramp or over-sampled converters, the best choice strongly depends on the application. We believe that sigma-delta converters, in spite of their quite high power consumption, are a promising solution for high-performance and medium size FPA, e.g. 320x240.
This paper presents the design of a second-order incremental sigma-delta ADC dedicated to cooled (77K) IRFPA applications. System-level simulations used to define the modulator parameters and specify its analog building blocks are presented. Circuit design of the switched-capacitor modulator and the digital decimation filter is described. The column ADC including the filter has been implemented in a standard 0.35µm CMOS process on the basis of a 25µm pitch and lead to a total length of 3200µm.
Test chips including a single ADC have been manufactured end of 2006. The first measurement results, at 77K, are presented along with perspectives and future developments. They demonstrate the following performance: 81dB Signal-to-Noise Ratio (SNR), 13 bits Effective Number Of Bits (ENOB) and 270µW power consumption at 17kSamples/s rate.

Keywords: Analog-to-digital converter, sigma-delta, ROIC, CMT, cooled IR detector, IRFPA

1. INTRODUCTION

The advantages of integrating A/D conversion in the readout integrated circuit (ROIC) are now established. It helps reducing the signal sensitivity to perturbations on the circuit and at the detector interface as well as decreasing system complexity and cost. It also enables further on-chip digital processing like image correction.
Cooled IRFPA applications require high resolution, low power consumption and small pixel pitch. The realization of a converter compliant with these constraints is quite challenging and demands an in-depth analysis from system to circuit level.
In this paper, we discuss architectural choices related to the integration of A/D conversion in a ROIC for cooled IRFPA. The system level dimensioning of a column-wise incremental sigma-delta ADC is presented. The design of a second-order switched-capacitor sigma-delta modulator and the subsequent digital decimation filter is described. Finally, the first measurement results of the realized ADC demonstrator are given.

2. CHOICE OF AN ADC ARCHITECTURE FOR COOLED IRFPA

2.1. ADC's position within a focal plane array

Integrating an ADC into the focal plane immediately raises the choice of its position within the array architecture: at pixel, column or output level. The implementation of the converter in the pixel is the most attractive. In this case the constraints linked to analog circuitry are significantly reduced since the analog buffers, multiplexers and output buffers are replaced by digital circuits. It lowers the signal sensitivity to on-chip degradation (e.g. noise and coupling) and may

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decrease the power dissipation. At the other end, a converter placed at the circuit's output, while removing analog output buffers, offers little benefit when considering the analog constraints and the power dissipation.
Actually, the density of CMOS process commonly used in IRFPA, the small pixel pitch and the resolution needed for high performance cooled IR products make the physical design of a suitable pixel level ADC extremely difficult.
Taking these elements into consideration we oriented our development toward a column level ADC.

2.2. ADC's architecture

The most popular ADC structures for column level A/D conversion are successive approximation, single-ramp and sigma-delta. Successive approximation converters have been used in visible CMOS sensors [1] [2] but offer limited resolution (about 10 bits). Single-ramp single-slope would not provide a good resolution within available conversion time. Single-ramp dual-slope overcomes this drawback but places important constraints on the design of analog blocks in order to assure a good linearity.
This work has been carried out in the common laboratory DEFIR between SOFRADIR and CEA-LETI. While SOFRADIR worked on the integration of a single-ramp dual-slope column level ADC in an IRFPA [3], CEA-LETI opted for a complementary development and focused on the design of an incremental sigma-delta ADC demonstrator.
Sigma-delta converters are appropriate for column-wise implementation [4] and offer a high potential in terms of resolution. The performance rather relies on the modulator structure which set over-sampling and noise shaping characteristics than on critical analog circuits. This makes them quite robust and flexible. The main difficulties for their use in IRFPA are the implementation of the modulator along with the decimation filter in a limited area and the tight power consumption budget.

2.3. Design goals

This ADC is targeting cooled (77K) medium size IRFPA (640*480 or 320*240) with 25µm pixel pitch for 50Hz or 100Hz frame rate. From these application-related parameters, we can derive other key specifications for a column ADC. The frame rate and detector dimension fix the column ADC minimum sampling frequency. If we consider a 320*240 array at 100Hz, this gives an ADC rate greater than 24kS/s. In this case, we assume a power consumption budget of 70mW for the 320 converters, thus about 220µW per ADC. The required resolution for these high-performance detectors is about 13 effective bits. This corresponds to a conversion error below $250\mu V_{p\text{-}p}$.

3. DESIGN OF A COLUMN-WISE INCREMENTAL SIGMA-DELTA ADC

3.1. System dimensioning

The theory of incremental sigma-delta converters [5] establishes the relationship between the modulator order, the number of cycles per sample (Nc) and the residual error in the estimation of input voltage. This error is lower than a value proportional to $1/Nc^{m}$ where m is the modulator order.
Choosing a high order modulator would help minimizing the converter error even for a moderate number of cycles. This would lead to an overall power reduction since the critical analog amplifiers would have reduced bandwidth constraints and the digital filter would work at a lower frequency. Here, the implementation in a 25µm pitch comes into account when considering the possible modulator order. Based on a 0.35µm standard CMOS process, the first rough area estimation gives about 400µm length per integrator in the modulator and 700µm length per filter order in the digital filter. Consequently, we opted for a second-order modulator which offers acceptable ADC dimensions.

In order to find out the relevant modulator parameters with respects to our design goals, we relied on a system analysis performed within the MATLAB SIMULINK environment. We modeled a second-order switched-capacitor incremental sigma-delta modulator as well as the digital $sinc^3$ decimation filter. Previous work reported in [6] details the modeling of switched-capacitor sigma-delta modulator's non-ideal effects like noise, gain and bandwidth limitations of analog amplifiers.
The system simulations allow us to determine the required number of cycles and to define modulator's building blocks specifications. The results obtained for various parameters are presented in Fig. 2. We can notice that reducing the number of cycles globally increases the conversion error and that a gain-bandwidth limitation of the amplifiers causes an important degradation at high input signal amplitude.

These results show that in 576 cycles with an amplifier having a DC gain of 60dB and a gain-bandwidth product of four times the over-sampled frequency (Fe), we can reach an error below $100\mu V_{p-p}$ after gain and offset correction. We will use these parameters as target specifications for the circuit design.

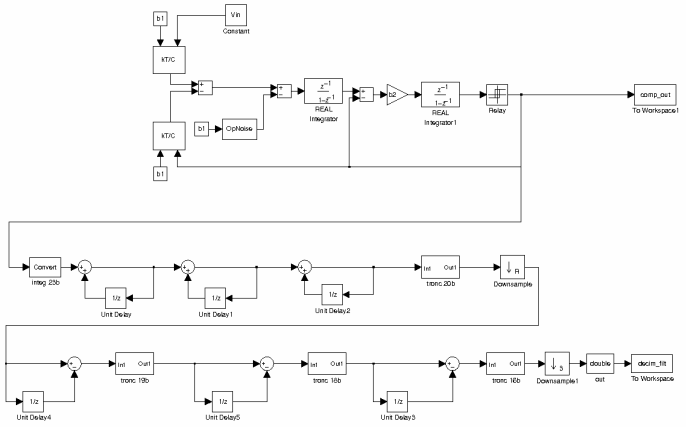


Fig. 1: Simplified SIMULINK model of a switched-capacitor sigma-delta ADC

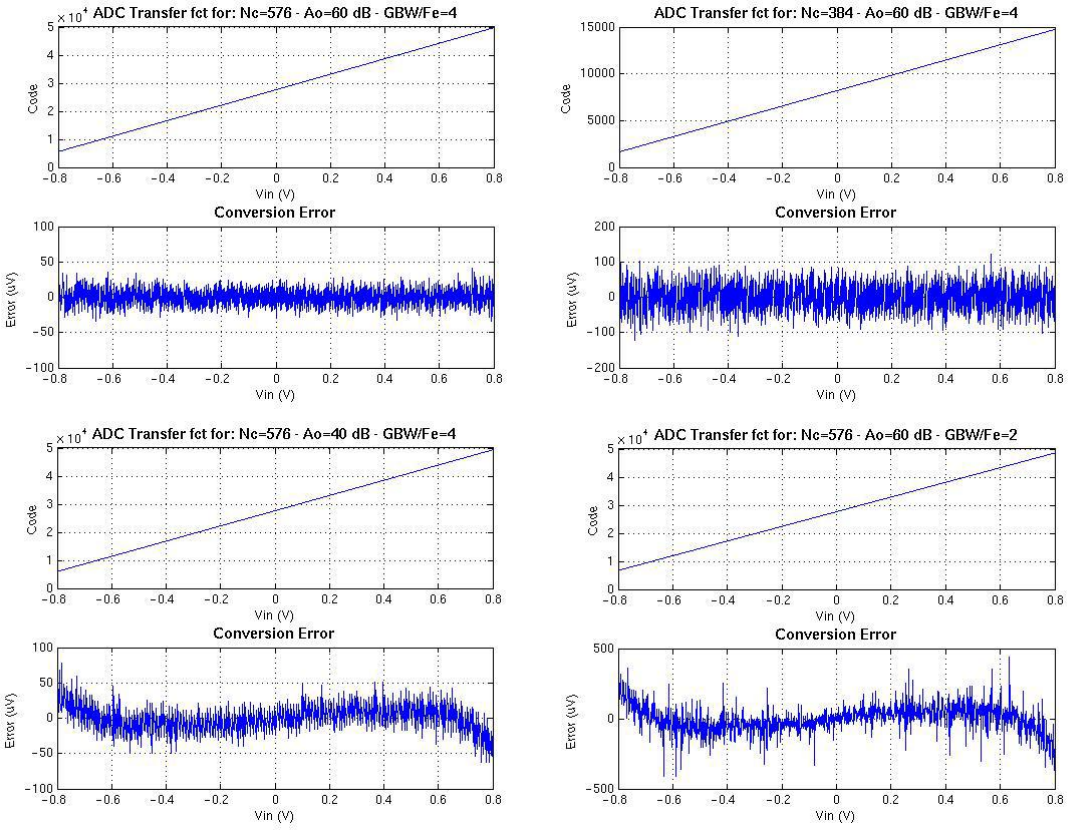


Fig. 2 : Results of system simulations for various parameters

3.2. Modulator design

We designed a fully differential second-order sigma-delta modulator using switched-capacitor integrators with common-mode feedback. Fig. 3 represents the corresponding diagram. In order to comply with the column ADC sample frequency (25kS/s) for the selected number of cycles, we choose an over-sampled clock frequency of 16.66MHz. The unit capacitance is fixed at 200fF giving a low enough kT/C noise (75μV_{RMS} at 77K). We did not use a higher value so that the capacitance area remains suitable and that the OTA can drive its output load without penalizing power consumption.

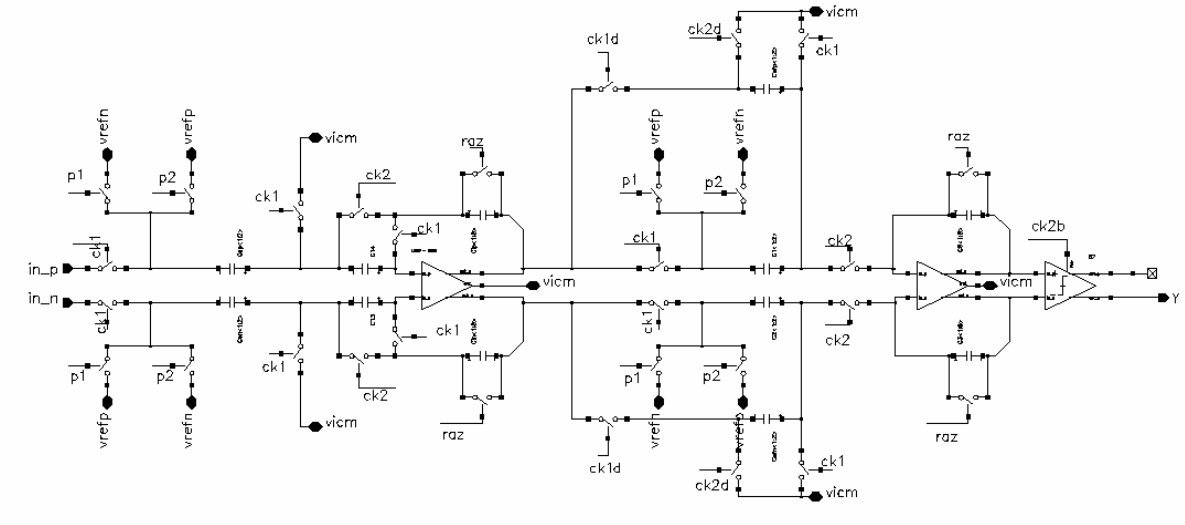
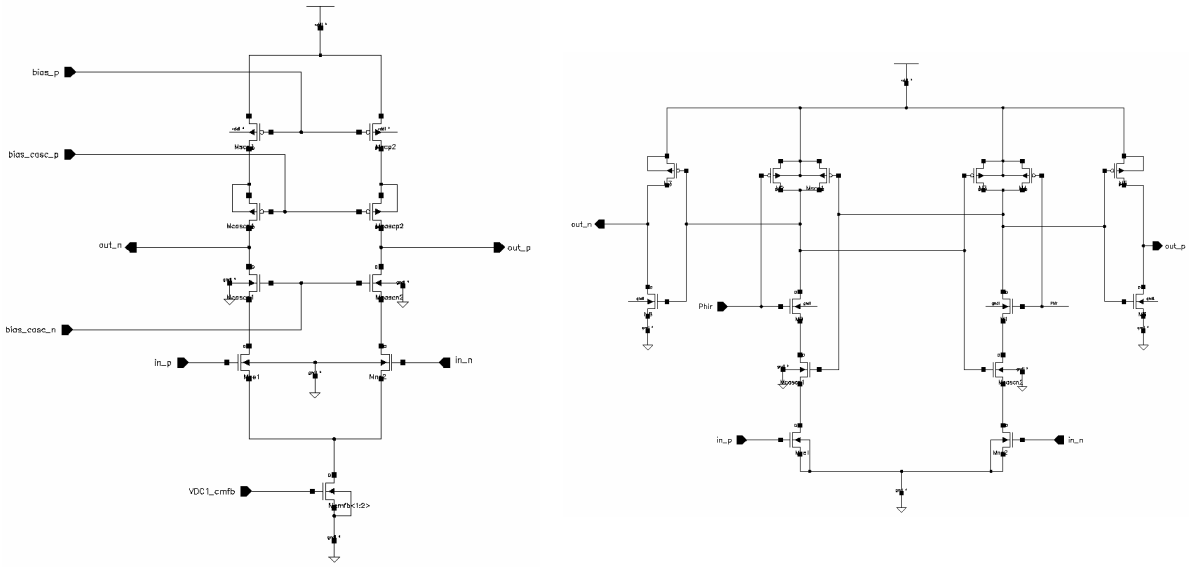


Fig. 3 : Switched-capacitor second-order incremental sigma-delta modulator diagram

The amplifier (Fig. 4a) is based on a single-stage telescopic cascode OTA structure to provide high DC gain while limiting power consumption. A dedicated biasing block shared by the converters is implemented outside the column pitch. This amplifier consumes 18µA on the 3.3V analog supply and achieves 89dB gain and 66MHz gain-bandwidth product. These values match the performance targets set by the system simulations. The design margin on the GBW is quite small due to the power consumption constraint but the biasing is externally adjustable which will allow some flexibility.

A switched-capacitor common-mode feedback circuit not represented here adjusts the current source bias voltage to regulate the OTA's output common-mode.

The differential comparator (Fig. 4b) is made of a bi-stable structure controlled by a clock signal.



(a) (b)

Fig. 4 : OTA (a) and comparator (b) circuits

3.3. Digital decimation filter design

A third-order sinc digital has been fully integrated in the 25µm column pitch. Its transfer function is given below:

$$H(z) = \left(\frac{1 - z^{-R}}{1 - z^{-1}} \right)^3 \text{ with } R = Nc/3 \tag{1}$$

Even if we target about 13 effective bits, the realized ADC has a 16 bits digital output. The implemented filter is based on the Hogenauer's structure [7] which consists of three integrating stages followed by a down-sampling by R, then three differentiating stages and a final down-sampling by 3.

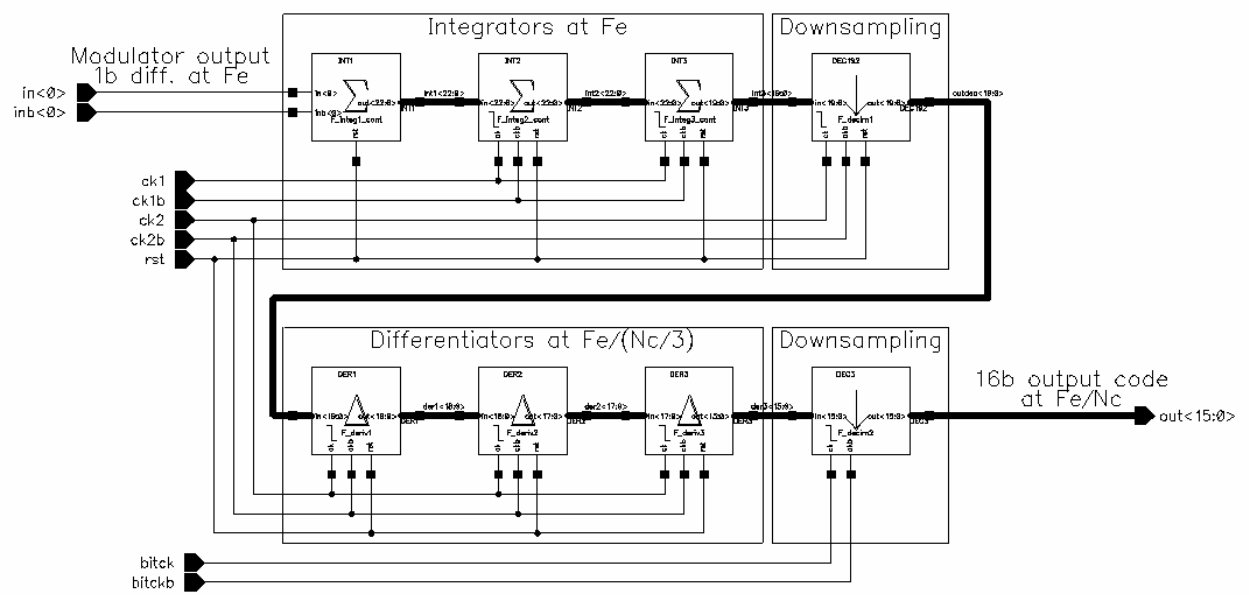


Fig. 5 : Digital decimation filter

As we want the ADC to be able to operate in both incremental and continuous modes (i.e. with and without a reset after Nc cycles) we have to carefully dimension the size of the registers. The equation (1) shows that in the worst case (all filter input bits at high level) the final result reaches R^3. So, a register depth of 23 bits is needed for the intended number of cycles.
The practical realization of the Hogenauer's structure leads to modifying this depth for the different stages in order to minimize the required hardware. Indeed, 23 bits are necessary for the computation but only 16 bits are expected at output. So we get a truncation of 7 bits on the last stage which implies an error at the filter output. Considering this error, we can allow smaller errors on previous stages. This enables to calculate the tolerable truncation among the different stages knowing that the sooner a truncation occurs in the filtering chain the bigger its impact on the output will be. For the realized digital decimation filter, we used the configuration given in Table 1.

Table 1 : Truncation applied to digital filter's stages

Stage	Number of bits	Truncation size
1st integrator	23	0
2nd integrator	23	0
3rd integrator	20	3
1st differentiator	19	4
2nd differentiator	18	5
3rd differentiator	16	7

In order to reduce the power consumption, the digital filter can operate with a reduced supply voltage (2.5V down to 1.2V) and it has been designed in a full-custom approach using dynamic flip-flops. The layout has been optimized to get the maximum density in the 25µm column pitch. We use a standard 0.35µm CMOS process with five metal layers. While lower levels are used for elementary cell layout, the three upper levels are reserved for interconnections and routing the 23 bits bus.
The ADC demonstrator is 3.2mm long and 25µm wide; the digital filter occupies about 70% of this area as can be seen on Fig. 6.

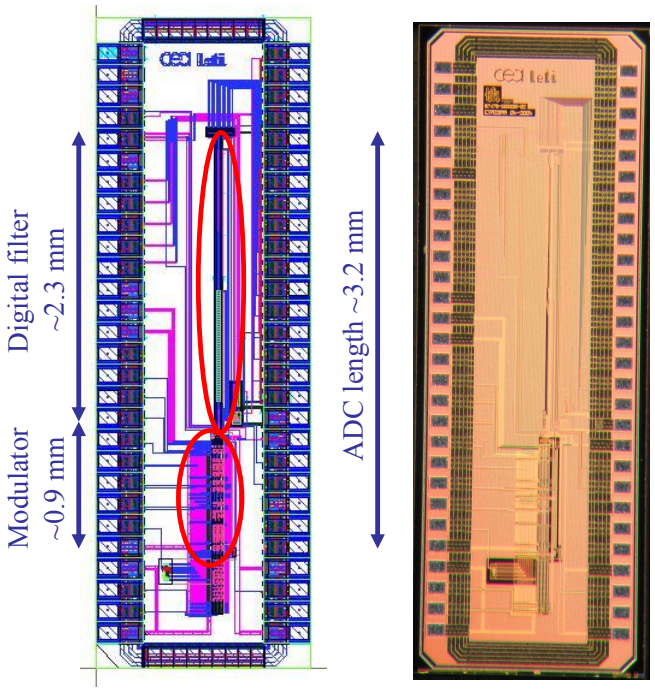


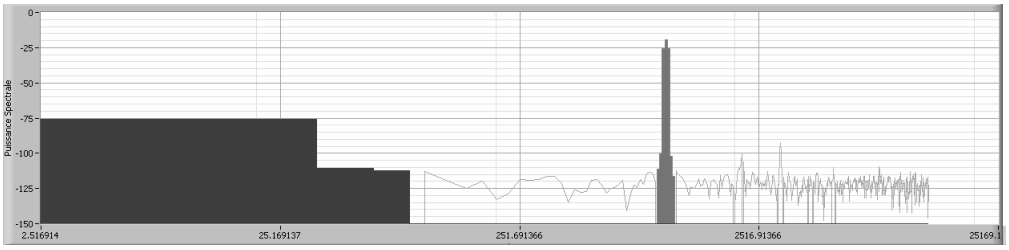
Fig. 6 : ADC demonstrator layout and chip microphotography

4. TEST RESULTS

We received the chips at the beginning of 2007 and the ADC demonstrator has then been assembled in a laboratory dewar to test it at 77K. A dedicated test board including low noise power supplies and adjustable biasing generation has been developed. It also includes digital buffers (with 50Ω line termination on higher speed signals) for the interface between the dewar and the National Instrument PXI based test bench. The analog input is generated with a PXI board embedding a 24bits DAC. The test configuration, the measurements and the data processing tasks are performed thanks to a custom LabView software.
We have the possibility to realize both dynamic (FFT on ADC output when applying input sine wave) and static (ADC transfer response) tests.

The functionality and performance of the whole ADC circuit has been checked. The digital filter is fully operational with a power supply voltage down to 1.1V. Its power consumption is below 50µW at 1.2V.
In nominal conditions, we observed a resolution below our expectations due to an important level of distortion. We could establish that this behavior was related to a bandwidth or slewing limitation of the amplifiers. Indeed, when lowering the over-sampled clock frequency (to 10MHz instead of 16.6MHz) or increasing OTA bias current we noticed a quick improvement. For this reason the following results are obtained at 10MHz.
In this first measurement phase, we discovered that the flexibility of a sigma-delta converter was a real advantage. It is possible to adjust the over-sampled frequency, the number of cycles and the OTA bias current. With the same circuit we can define different configurations depending on specific application requirements. The over-sampled frequency reduction to 10MHz can be done with no impact on the frame rate if we adapt the number of cycles (configuration A). If the circuit is used in lower dimension arrays, we can keep the highest number of cycles and maybe accept a slight power consumption increase in order to get the maximum resolution (configuration B). The results are given in these two configurations. Intermediate configurations are also conceivable, they derive from a tradeoff between circuit performance (resolution, power consumption) and application needs (frame rate, array size).

In configuration A, the number of cycles is reduced to 384 so as to keep a sampling rate compliant with the design goals. It allows the use of converter in large size 640*480 arrays at 50Hz or medium size 320*240 arrays at 100Hz. In this case, the ADC works at 26kS/s and the power consumption of the sigma-delta modulator is 165µW.
The ADC output spectrum is presented on Fig. 7. It shows a non-negligible distortion still due to the limitation of analog amplifiers and gives 11.5 ENOB.
The static measurements illustrated on Fig. 8 give an error about 500µV_{p-p} which mainly appears for high input signal levels.



SNR = 75.5 dB
SINAD = 70.9 dB
THD = -72.5 dB
ENOB = 11.5

Fig. 7 : ADC's output power spectrum in configuration A

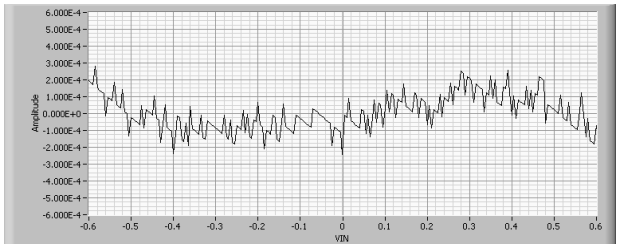
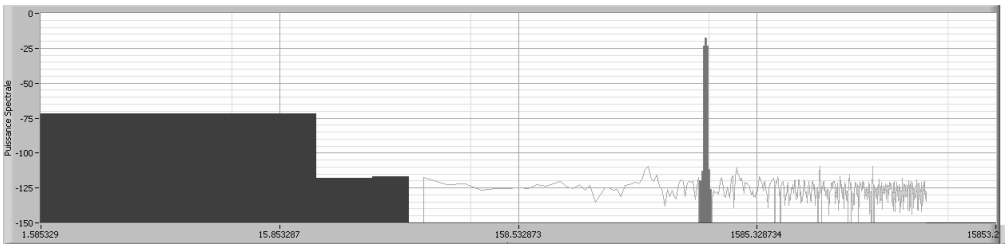


Fig. 8 : ADC's conversion error in configuration A

In configuration B, we keep the number of cycles to its initial value of 576, giving an ADC sampling frequency of 17kS/s. We also increase the OTA's bias current to overcome their frequency limitation. This configuration allows the use of the converter in medium size 320*240 arrays at 70Hz or lower size arrays at higher frame rates. In this case, the power consumption of the sigma-delta modulator is 225µW.
The ADC output spectrum is presented on Fig. 9. It shows that the distortion observed in previous configuration has been removed by increasing the bias current. The resolution now reaches 13 ENOB.
The static measurements illustrated on Fig. 10 give an error about 350µV_{p-p} which remains small at high input signal levels.



SNR = 81.1 dB
SINAD = 80.2 dB
THD = -87.5 dB
ENOB = 13.0

Fig. 9 : ADC's output power spectrum in configuration B

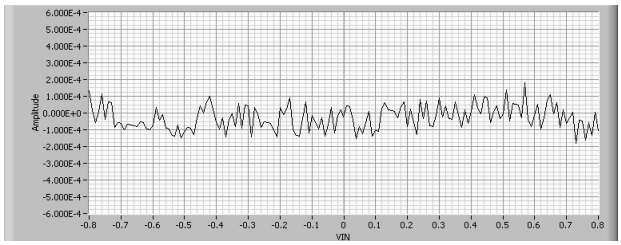


Fig. 10 : ADC's conversion error in configuration B

Table 2 synthesizes the results obtained in the two configurations.

Table 2 : ADC performances

Configuration	**A**	**B**
Fe (MHz)	10	10
Number of cycles	384	576
ADC sampling frequency (kS/s)	26	17
ADC power consumption (µW)	210	270
ENOB	11.5	13.0

5. CONCLUSION

The realized column level ADC demonstrator is fully functional and its performances are consistent with cooled IRFPA requirements. The chosen structure has a potential resolution above 13 effective bits making it well suited for high performance image sensors. Furthermore, the flexibility of incremental sigma-delta ADC enables the use of the realized converter in different configurations by adjusting the trade-off between circuit performances and specific application needs. Concerning the power consumption, the high resolution configuration can be used in low to medium size cooled IRFPA since a 320*240 array will dissipate about 90mW.
The use of a more recent CMOS process (e.g. 0.18µm) for our future ROIC developments will ease the integration of this type of converters by allowing a more compact layout of the digital filter. This step will also further enhance the ADC performances by decreasing the power consumption and overcoming the observed frequency limitations of analog integrators.

The results obtained with this incremental sigma-delta ADC demonstrator open the door to an implementation in future SOFRADIR products. This A/D conversion architecture may also find its way in uncooled applications where power consumption constraints are relaxed.

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