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Review

A column level, low power, 1 M sample/s double ramp A/D converter for monolithic active pixel sensors in high energy physics

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ABSTRACT

Monolithic active pixel sensors (MAPS) using standard low cost CMOS technologies available from industrial manufacturers have demonstrated excellent tracking performances for minimum ionizing particles. The need for highly granular, fast, thin sensors with a full digital output drives an R&D effort, aiming to design and optimize a low power high speed A/D converter integrated at the column level. Following this main issue, a double digital ramp A/D converter has been proposed for CMOS monolithic active pixel sensors in this paper. This A/D converter responds to the constraints of size, power dissipation and precision for CMOS sensors for particle detection. It also represents a first step in order to reach the high speed of conversion needed for this kind of application. The A/D converter has a resolution of 4 bits for conversion speed of 1 M sample/s with only 264 μW of static consumption in a very particular pitch of 25 μm × 900 μm.

Contents

1. Introduction

Silicon detectors have found use in many fields of experimental physics research. Their applications extend to nuclear and particle physics, astrophysics, crystallography and medicine for imaging, tracking, mechanical alignment, etc. Especially in high energy physics experiments highly granular, thin, radiation tolerant, fast and multi-layer silicon detectors have to be installed very close to the interaction region to detect the charged particles [1,2]. In comparison to existing devices (CCDs, hybrid pixels), the CMOS monolithic active pixel sensors (MAPS) are foreseen to fulfill these requirements and may offer an attractive trade-off between granularity, material budget, radiation tolerance and read-out speed for high precision minimum ionizing particle (M.I.P) tracking.

The detection of charged particles in high energy physics or medical imaging applications is a real challenge for today's microelectronics sensors. CMOS monolithic active pixel sensors are charged particle tracking devices, integrating on the same substrate radiation sensitive detector elements with their front-end readout electronics. They are fabricated using standard CMOS processes available through many commercial microelectronics foundries. The detection principle of a MAPS is illustrated in Fig. 1. When a charged particle passes through the sensor, a number of electrons are created in the epitaxial (epi) layer. These electrons will be collected with thermal diffusion by the diode D_1 and then converted by the capacitors C_{qonv} to a voltage, the value of which is directly determined by the number of electrons created in the epi layer.

The most significant advantage of CMOS technology is that the sensitive volume and the front end readout electronics are integrated on the same substrate [3]. Furthermore CMOS technology features a good radiation tolerance [4]. MAPS technology is investigated in the development of a vertex detector

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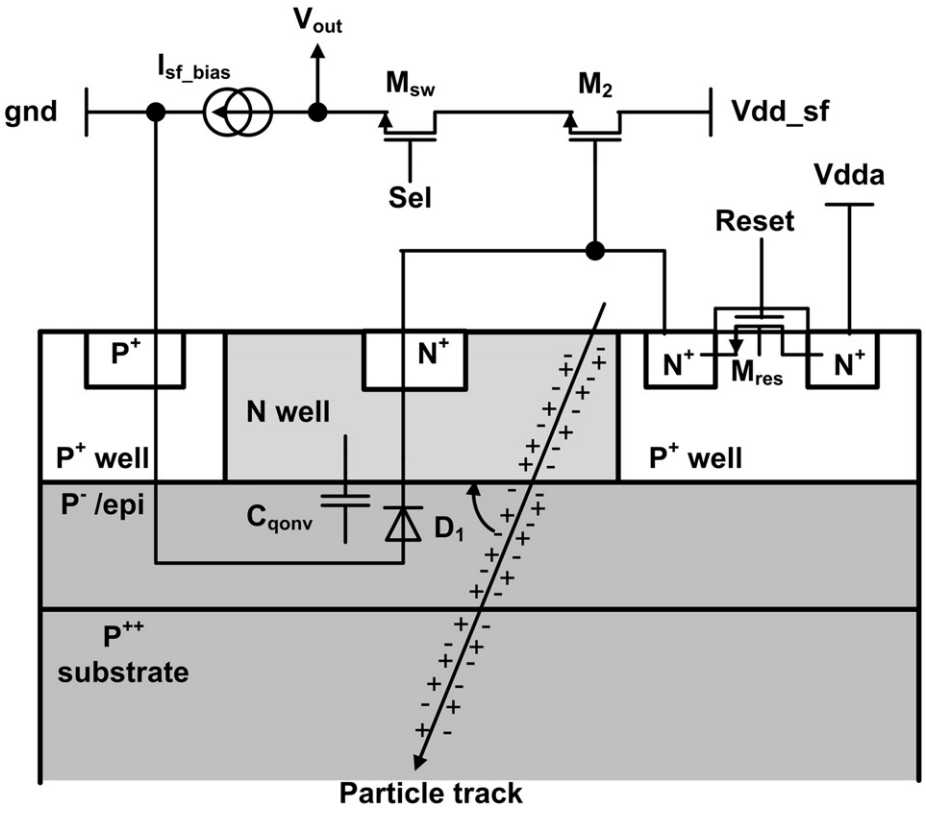

Fig. 1. MAPS architecture.

for high energy physics experiments [5]. The architecture of such device is shown in Fig. 2. A vertex detector for the international linear collider (ILC) [6] will be composed of five layers of detectors, each of which consists of ladders of CMOS sensors. An artist's view of the vertex detectors is presented in Fig. 2(a). The first layer of the detector will be the hardest to design because of several requirements: high radiation tolerance, high spatial resolution and huge data rate. This layer will be directly installed on the vacuum tube. In the past four years the research effort has concentrated on the development of an array of CMOS pixels with a discriminator at the end of each column. Efficient circuits have been developed with very promising results [7,8]. For the ILC experiment a better spatial resolution on the matrix is needed; in order to obtain this resolution ($\sim$2 μm of spatial resolution) an analog to digital converter (ADC) must be integrated instead of a discriminator at the end of each column.

As shown in Fig. 2(b), the pitch of the A/D converter is directly set by the pixel pitch; in this application a pitch of 25 μm has been used. Moreover, the vertex detector is the first layer in the global detector architectures. Therefore the power dissipation has to be very low because the complete architecture of the vertex detectors does not allow heavy cooling devices; consequently the maximum power dissipation for the A/D converter for this kind of application must be under 500 μW.

When a charged particle passes through a CMOS sensor, the charge created in the epitaxial layer is collected by a cluster of pixels due to thermal diffusion. About $\sim$25–30% of the charge is collected by the seed pixel (1 in Fig. 3) and the rest is shared among other pixels in the cluster (2 in the Fig. 3). Table 1 shows the ADC resolution versus position resolution for a pixel pitch of 20 μm. As shown in Table 1, the position resolution does not improve linearly with the precision of the ADC. A 4 bit ADC allows a precision of 2 μm on the cluster, which corresponds to the requirements for the ILC experiment. At the end of the column the noise level is $\sim$2–3 mV rms after amplification. In order to keep a good resolution on the lower code of the ADC the least significant bit (LSB) is set to two times the noise level. For a 4 bit ADC with 125 mV full dynamic range the LSB represents 7.4 mV.

The digitalization of information is the critical point of every actual electronic system. For each application with its specific requirements, a correct A/D converter architecture has to be chosen according to accuracy, speed and power consumption. Each ADC has its advantages and weakness that make it more compatible with different applications. To compare the different architectures some formulae have been developed using the key points generally accepted for a converter design: the speed of conversion, the accuracy in bits, power dissipation, etc [9].

Different column level A/D converter architectures have been developed like [10], or [11], with some good results, but all these A/D converters were designed for low frequency applications like image sensors for the visible spectrum. For vertex detector applications the conversion speed must be higher than 1 M samples/s to allow an efficient tracking of particles. For this reason a new approach is presented in this paper.

Considering the different drawbacks set by our applications, such as integrating the A/D converter in a pitch of 25 μm, a conversion speed of 1 M samples/s and a power consumption of 500 μW, the Wilkinson ADC represents a good choice to fulfill the requirements.

2. Classic Wilkinson A/D converter

The complete architecture is presented in Fig. 4. When the comparator output is low (input voltage larger than integrator output), the integrator charges the capacitor with a constant

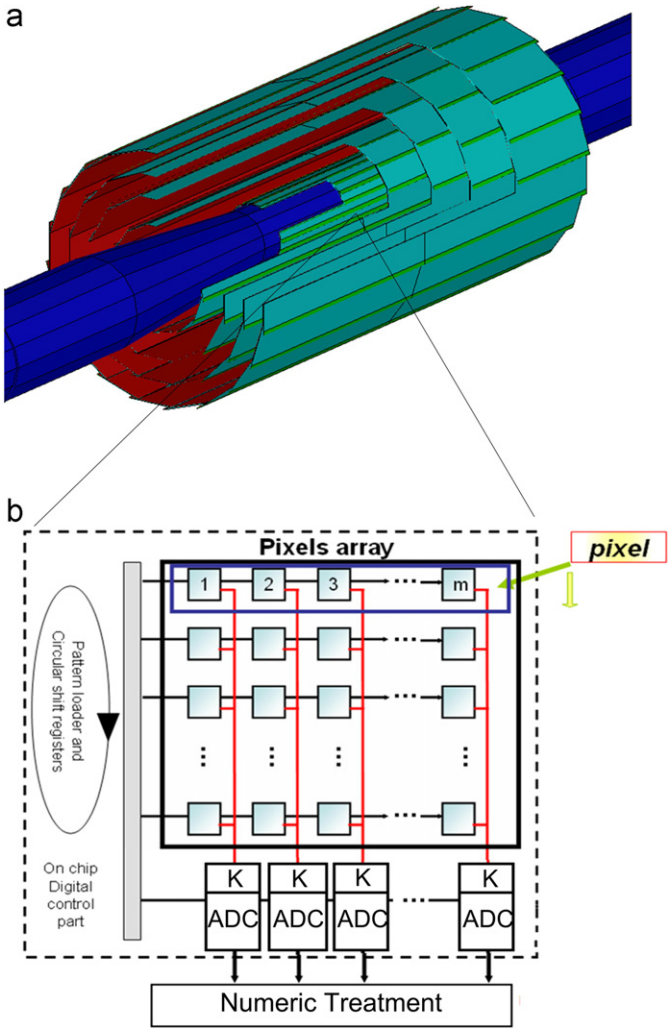

Fig. 2. (a) Vertex detector. (b) CMOS sensor.

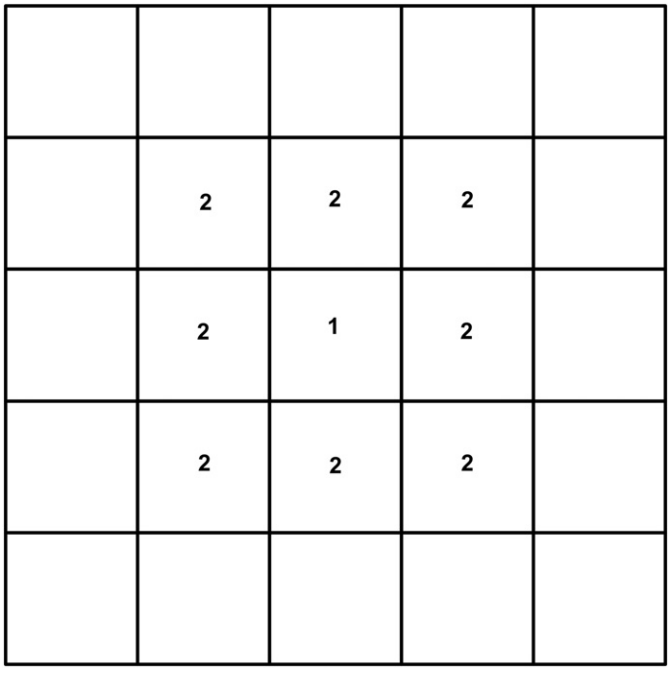

Fig. 3. Concept of the seed pixel.

Table 1
Number of bits of the ADC versus spatial resolution on the matrix.

Number of bits	12	5	4	3
Spatial resolution in μm	1.55	1.7	2	2.2

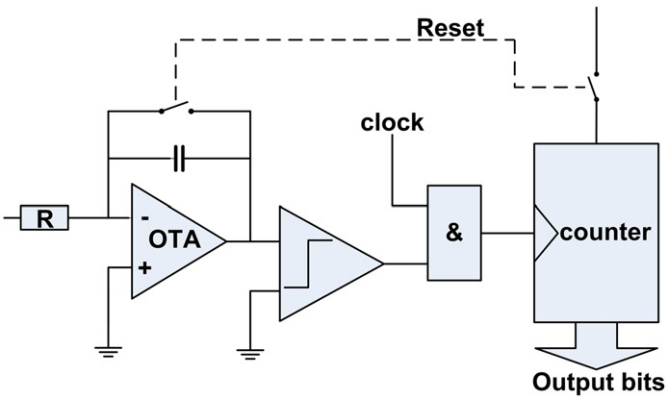

Fig. 4. ADC classic Wilkinson architecture.

current creating a linear ramp. Meanwhile, the counter (CTR) is counting at a rate fixed by the precision clock frequency. The time needed to charge up the capacitor to the input voltage level depends on the input signal level and the combination of the current (I) and the capacitor (C) with the simple equation $dv/dt=i/c$. When the voltage integration in the capacitor reaches the converted voltage level, the comparator output becomes high, loading the counter's output into the shift register, which contains now the digital conversion value. The switch transistor is closed by the comparator's high output, discharging the capacitor back to zero volt. When the integrator output voltage falls to zero, the comparator output switches back to a low state, clearing the counter and enabling the integrator to start a new analog ramp voltage for an another conversion.

The precision of the Wilkinson A/D converter depends on two main blocks: the ramp generator and the counter. The precision of the ramp directly determines the precision of the conversion. The bit number of the counter must be correlated with the precision of the ramp to achieve efficiently the design accuracy. The speed of Wilkinson A/D is directly determined by the counter, i.e. by the clock frequency. A high speed Wilkinson converter will need a high frequency, which involves larger dynamic power consumption. For example, a 4 bit conversion needs 16 clocks. This implies a clock frequency of 20 MHz for a conversion speed of 1 μs.

The Wilkinson architecture has several advantages for the applications of a vertex detector. The principle is simple; consequently the static power dissipation is very low, and moreover this simplicity implies also a small pitch size, because the architecture does not need too many elements. As mentioned above, the Wilkinson A/D converter also exhibits some weakness: the ramp generator is the critical design block. If the application has a small dynamic range for the ramp, the effects of clock feedthrough from the MOS switches will become a real perturbation. Another problem for a classic Wilkinson architecture comes from the dispersion of process parameters on the capacitor designed in polysilicon from the ramp generator. A Monte Carlo analysis shows that for a polysilicon capacitor in Austriamicrosystems 0.35 μm technology, the process dispersion is an important problem. For an analog ramp generator using a 200 fC capacitor, a maximum gain error of 20% for a 100 mV_{ramp} has been

observed. This gain error is greater than twice the LSB and cannot be accepted for vertex detecting applications.

The problem with the offset can be fixed by using an offset compensation device, which implies an augmentation of the surface of the A/D converter. All this observation forced us to develop a new architecture based on the Wilkinson A/D conversion principle.

3. Double digital slope Wilkinson converter

As discussed above, the analog ramp generator is a critical block which cannot deliver satisfying results for our application. A new architecture shown in Fig. 5 has been proposed. The analog ramp is replaced by a digital ramp generator with a 4 bit D/A converter. One interesting benefit of the use of a digital ramp generator instead of an analog one is the decrease of static power dissipation. Moreover the main advantage of the new architecture is to transform a conversion associated with a 4 bit counter into two conversions associated with a two bits counter, which consists of a double ramp conversion and increases effectively the conversion speed.

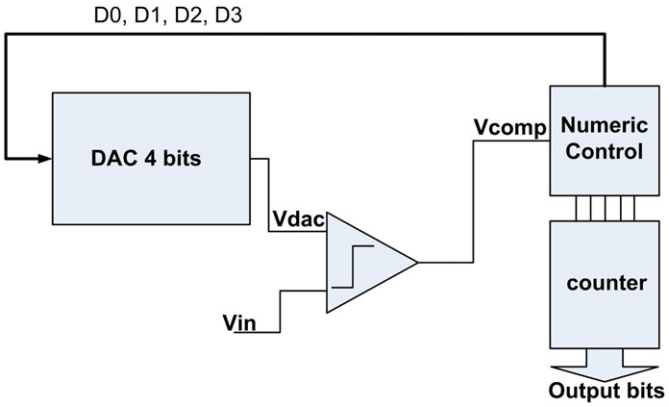

Fig. 5. New proposed architecture.

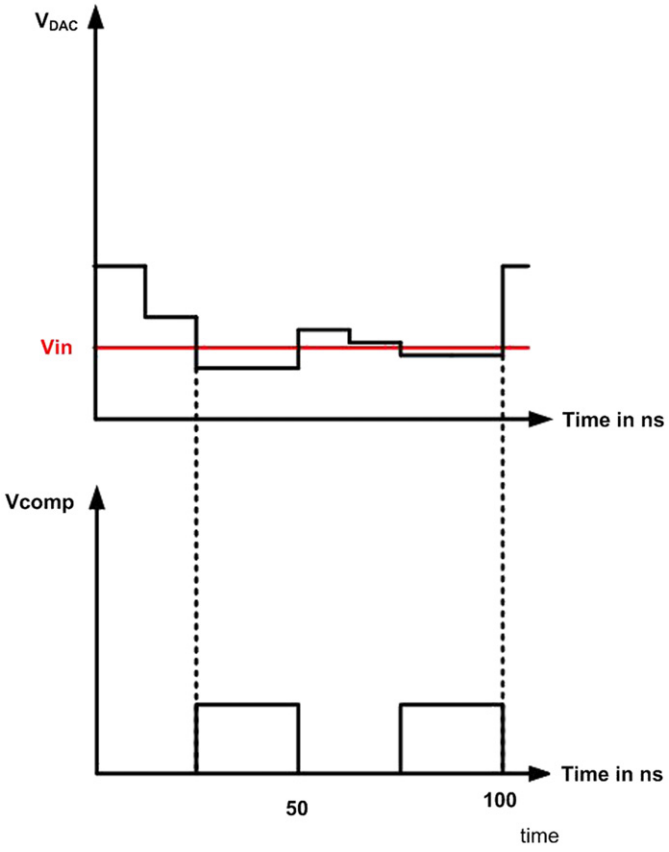

Fig. 6. Example of a complete conversion.

In the first part, a conversion is made with two bits on the full scale of the converter: a digital control selects a decreasing binary code into the D/A converter with the signals D0, D1, D2, D3. Then the D/A converter generates the correct level of voltage associated with the code. This voltage is then compared with the voltage to convert by a latched comparator driven by the signal latch. When V_{dac} decreases below V_{in} the comparator flips and the state of the signals D0, D1, D2, D3 is stored. This signal is memorized and gives the two most significant bits (MSB). In the second part a second two bit conversion is made starting on the last MSB analog value but this time with a full scale of only one MSB. The outputs of the D/A converter and of the comparator for a complete conversion are shown in Fig. 6.

This way to convert in the new architecture offers a main advantage. Only eight clock counts are needed to convert a 4 bit word instead of sixteen for a classic Wilkinson structure. This is a gain of a factor two in clock counts and implies that for a 1 M sample/s a 10 MHz clock could be used instead of 20 MHz for the same conversion speed. This kind of architecture could be even more powerful for higher resolution A/D conversion with a saving of $2(n/2\text{-}1)$ clock counts compared to the classic Wilkinson architecture (with n=number of bits).

This architecture could be compared to a successive approximation register A/D converter (SAR ADC) [13]. The major difference between these two architectures is the principle of conversion. In a SAR ADC each bit is tested and the result of this test is used for the test of the next bit. As a result of the successive approximation register is much more complex to design. This digital part of the SAR converter requires a greater surface and a greater number of logic gates (and so a greater dynamic power consumption) than the double digital slope Wilkinson converter.

The new A/D converter has to cover a dynamic range of 125 mV or a minimum step of 7.8 mV corresponding to the LSB changes. The sampling rate is 1 M sample/s with a clock frequency of 10 MHz and the static power consumption of 264 μW can be calculated. The estimated dynamic power dissipation is 480 μW at a conversion rate of 1 M Sample/s.

4. Building blocks design and ADC simulations

The comparator is an important element for an A/D converter design [12] in order to get high resolution, high conversion speed and lower power dissipation. The solution developed here is classical latch architecture. This architecture is commonly used in ADCs. Fig. 7 shows the detail of the design. The comparator is composed of a first amplifier stage in order to get a good amplification of the signal. Then two buffers allow to avoid any kickback from the clock through the latch stage. And the structure ends with a latch block. Each edge on the clock signal will cause the comparator to perform a comparison. In our simulation the comparator shows a gain of four and a total static power dissipation of 264 μW. The response time of the complete structure is 2 ns. The architecture of the latch presented in Fig. 8 is a conventional sens-amplifier flip flop with an equalization of the voltages on the regenerative nodes.

For a comparator without any offset compensation system, a Monte Carlo analysis allows determining a random offset of 8 mV,

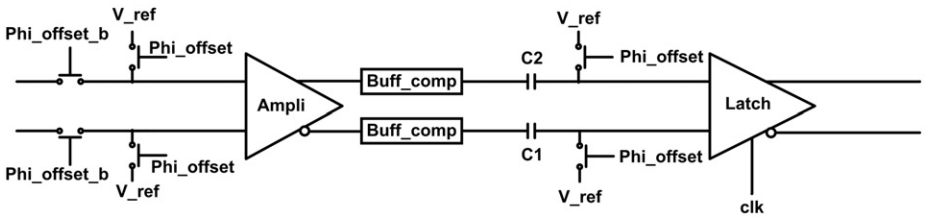

Fig. 7. Architecture of the latched comparator.

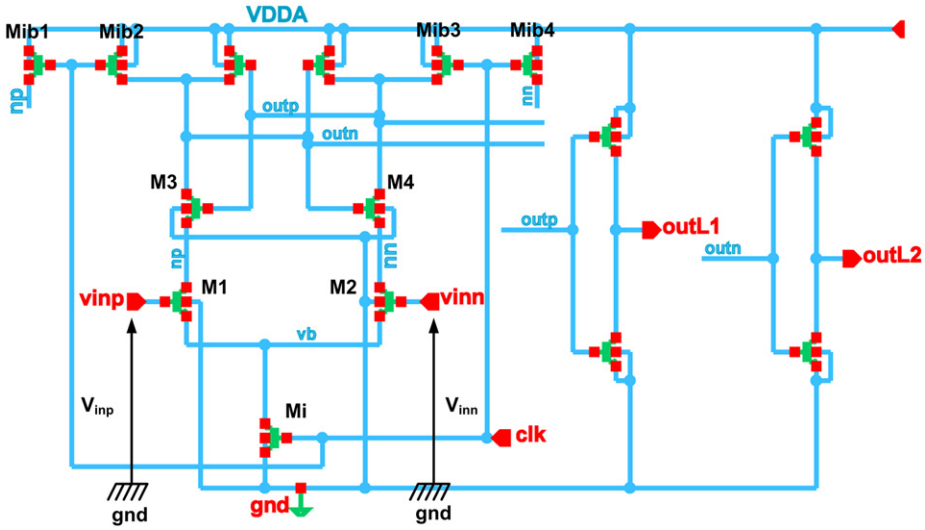

Fig. 8. Detail of the latch structure of the comparator.

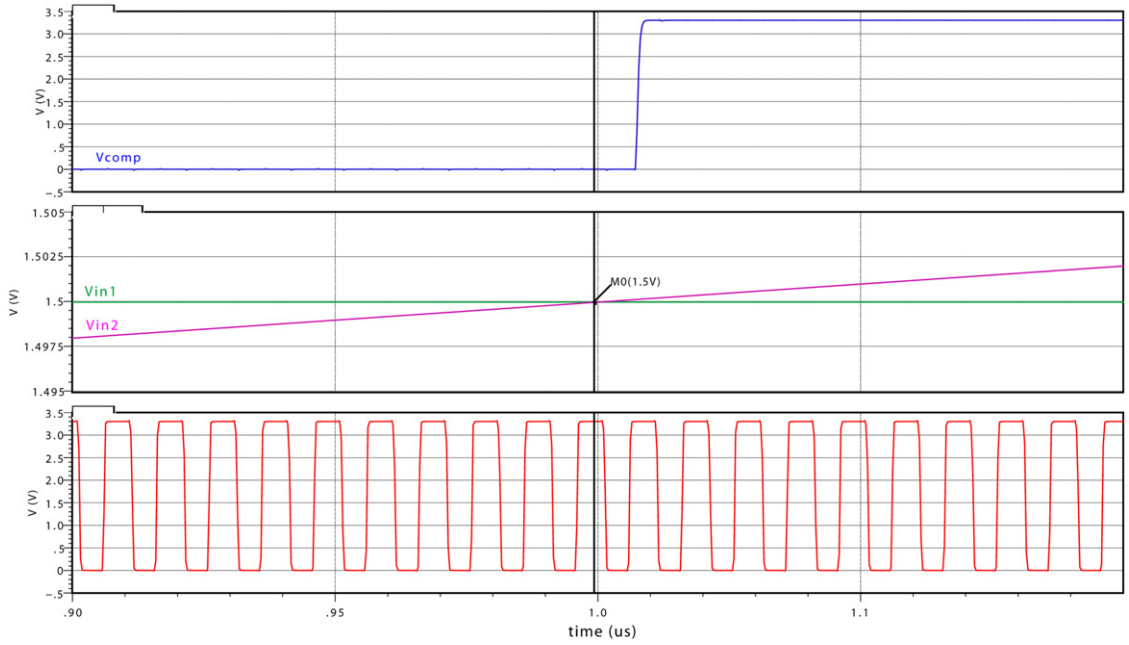

Fig. 9. A simulation for the response time of comparator.

which is larger than an LSB of the A/D converter. Then, an offset compensation has to be realized to minimize this offset.

In a comparator design, the offset is well known as an important problem. To reduce this problem an offset compensation has been performed with two capacitors ($C1$ and $C2$). In the first phase the switches controlled by the signal Phi_offset are closed and the switches operated by Phi_offset_b are opened. The offset voltage is stored in the capacitors $C1$ and $C2$. Subsequently the switches controlled by Phi_offset are opened whereas the switches controlled by Phi_offset_b are closed. The offset voltage is subtracted from the input voltage. The offset compensation allow one to lower the offset of the comparator to 2 mV, which is

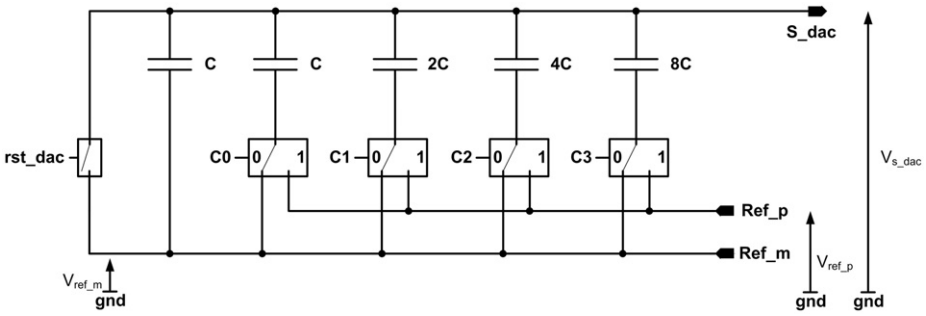

Fig. 10. Architecture of a 4 bit switched capacitors DAC.

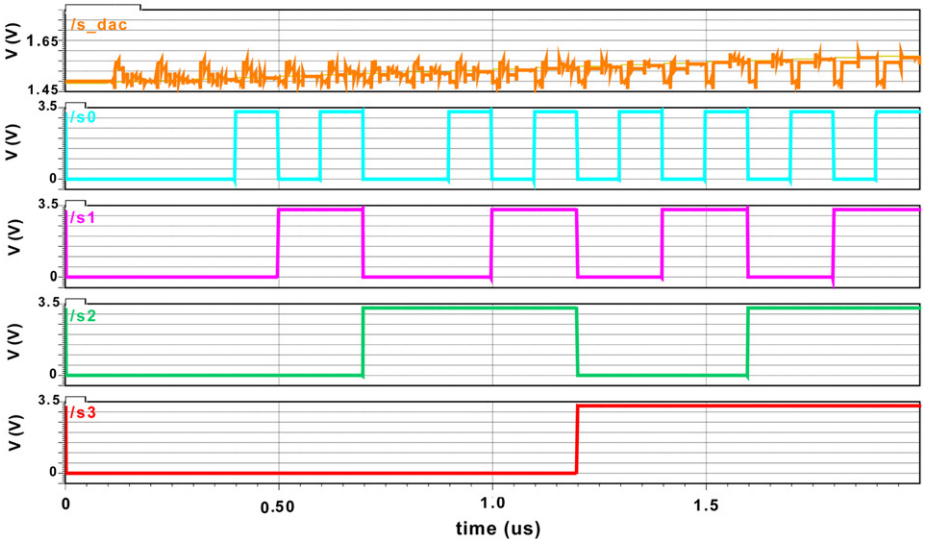

Fig. 11. A complete conversion of the ADC.

less than 1/2 LSB. The preamplifier stage needs a current of 50 μA and the two buffer stages need a current of 15 μA each. Fig. 9 shows the simulated response of the comparator. The first two curves represent the two inputs of the comparator. If $V_{in} > V_{ramp}$, the state of the comparator changes with the next rising edge of the clock with a two nanosecond latency.

A four bit D/A converter with a dynamic range of 125 mV is implemented in the design. The architecture is shown in Fig. 10. It uses an array of binary-scaled capacitors and a set of switches that connect the scaled capacitors to the reference voltages VREFN or VREFP. With the correct set of the switch the output of the D/A converter is set from VREFP to VREFN with a step of 1/16 (VREFP–VREFN). The value chosen for the capacitor C is 200 fF. A complete simulated conversion is presented in Fig. 11. The first signal is the main clock of the ADC. Then, the outputs of the ADC are displayed (signal out0 to out3) and the last plot represents the input to convert (1) and the output of the DAC (2). After a first set phase of 1 μs during which all the systems are reset and the offset is compensated, the first part of the conversion begins. When the input voltage increases above the DAC voltage, the comparator changes state, ending the first part of the conversion. The D/A converter voltage is blocked. Then the second part of the conversion begins. This part is running exactly in the same way as the first except that the input voltage of the D/A converter presents a full dynamic of 1 MSB. When the D/A converter decreases below V_{in} the comparator changes state again and the D/A voltage is blocked. At the end of the conversion the output signals are set to the appropriate value 0110, and a new conversion can be started. It is interesting to note that the initialization part at the beginning of the conversion is only required

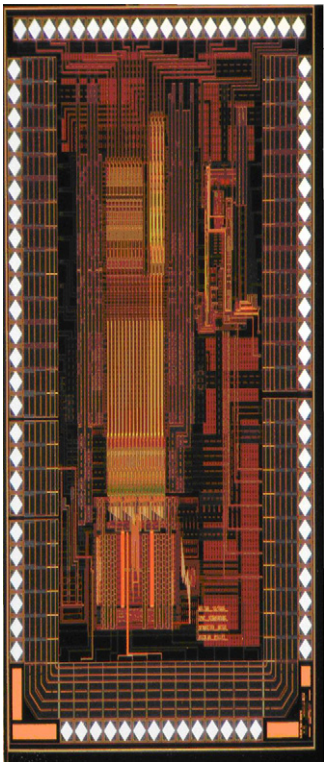

Fig. 12. ADC die picture.

for the first one, later the reset operation needs only 20 ns to be performed.

A kTC noise simulation had been done with mentor graphic ELDO simulation software to establish the noise contribution of the D/A converter. The result of these simulations reveals a noise RMS of 38 μV.

Table 2
ADC measured performances.

Number of bits	4
Power dissipation (static)	350 μW
Conversion speed	1 M samples/s
Dynamic range of conversion (baseline 1.5 V)	128 mV
ENOB	3.89
SINDA (dB)	24.9
LSB	7 mV

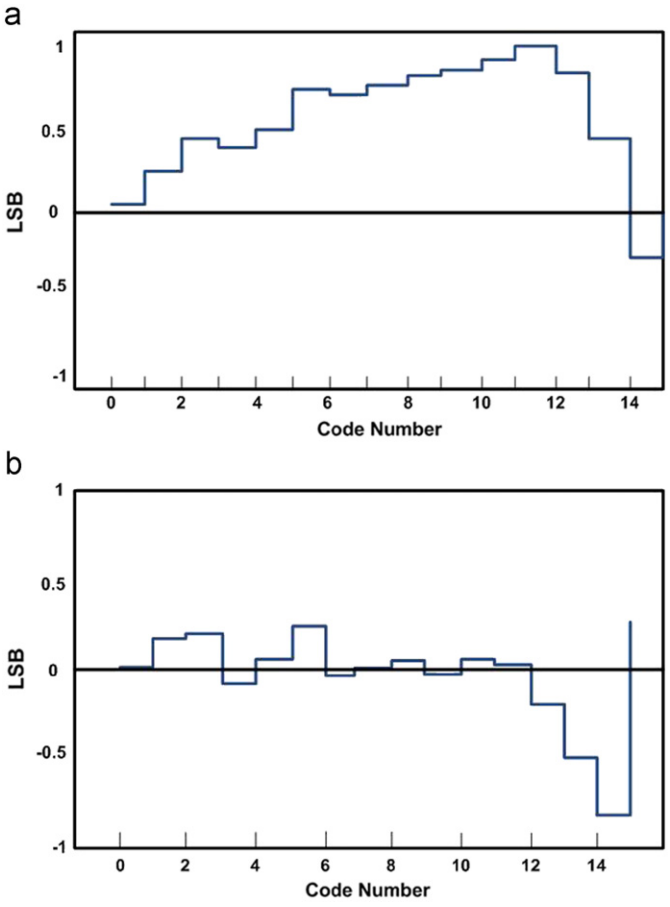

Fig. 13. (a) INL error. (b) DNL error.

5. Measurement results

In order to investigate the feasibility of the A/D converter discussed above, a first prototype of twelve A/D converters with two different architectures of sample and hold on the top of the structure has been designed and fabricated in Austriamicrosystems 0.35 μm CMOS process. The layout of the chip is shown in Fig. 12. With 12 converters the crosstalk between each converter will be studied. In order to be integrated in the column level of the matrix, the ADC has been designed in a pitch of 25 μm × 900 μm. The complete chip size is 3040 μm × 2090 μm. Table 2 summarizes the main results for the ADC.

The ADC test software has been developed in our laboratory using both LabVIEW from national instruments and matlab from the mathworks. The differential non linearity (DNL) error and the integrated non linearity error (INL) are calculated using the code density test [13]. The ADC is fully operative with a dynamic range of 125 mV at a clock frequency of 10 MHz, which corresponds to 1 M samples/s.

Fig. 13 presents the results for DNL and INL plotted for a 1 M samples/s conversion with a 128 mV dynamic. DNL results are between +0.3 and -0.8 LSB (due to a code error) and the INL is between +1 and -0.4 LSB. As explained in the first part, the lower codes of the ADC are the most important. An error of 1 LSB in the INL error for the code 13 is not an important problem for vertex detector application. The results of the DNL and INL for the first six codes are below 0.5 LSB. These results are acceptable for vertex detection in high energy physics.

The response of a slow ramp is shown in Fig. 13. The complete dynamic of conversion was 128 mV with a clock speed of 10 MHz (which represents 1 M samples/s). It is interesting to notice that the error code between code twelve and thirteen is only in the ascendant conversion. This problem is probably due to the fact that three switches are moving together for the transition between code twelve and thirteen. In the layout of the DAC, the command lines of the switch were not properly isolated one from another and generate some perturbation when all the lines switch together. This problem has been fixed by drawing a new layout in which capacitors between command lines have been reduced Fig. 14.

6. Conclusion and outlook

In this paper, a new ADC design based on a Wilkinson architecture integrated at the column level of a CMOS pixel

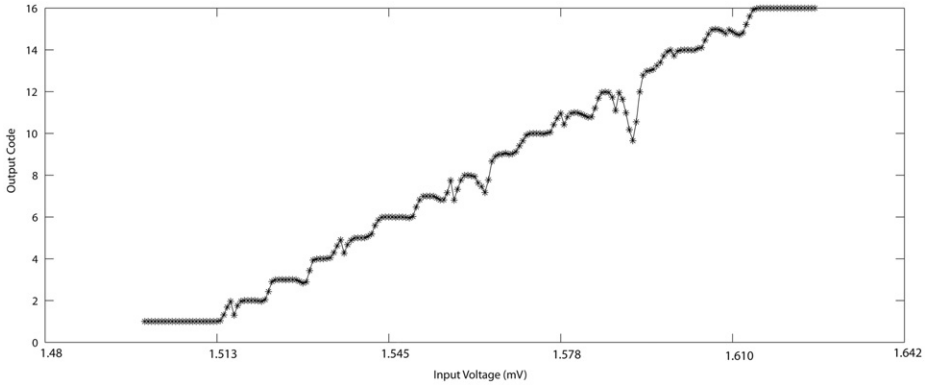

Fig. 14. Response to a 130 mV linear ramp.

matrix has been presented. The simulated results show that the architecture offers many interesting performances such as low power consumption and a high speed sampling rate of 1 MHz/sample. Due to these optimized characteristics, this kind of ADC can be used for CMOS monolithic active pixel sensors in high energy physics. Considering the very encouraging results of this A/D converter a new prototype will be designed with the objective of 10 MS/s to fulfill the requirement for next generation of tracking sensors in future high energy physics experiments.

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