

CMOS APS IMAGER EMPLOYING 3.3V 12 BIT 6.3 MS/S PIPELINED ADC

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ABSTRACT

A novel 256x256 CMOS active pixel sensor (APS) system with 12 bit, 6.3 MSample/s (MS/s) CMOS pipelined analog to digital converter (ADC) integrated on chip is presented. The test chip has been implemented in 0.35 μ m 2P4M process, operated by a 3.3V supply and is expected to dissipate 55mW. The total area of the prototype is 12 mm², and the core area of ADC is 18% from the total area. System architecture and operation are discussed and simulation results are presented.

1. INTRODUCTION

Driven by the demands of multimedia applications, digital cameras rapidly became attractive. The basic requirements of digital cameras, in addition to image capture must include analog-to-digital conversion and digital signal processing. CMOS technology is rapidly scaling down, enabling integration of these functions onto a single chip [1,2,3]. Integration of a CMOS sensor with an ADCs can be done in three fundamental approaches:

- Pixel level approach [4,5]- A separate ADC is allocated for every pixel.
- Column parallel approach [6,7,8]- Each ADC serves one or more columns in the sensor array.
- Chip level approach [9,10]- A single ADC serves the whole image sensor.

Different kinds of ADCs can be integrated with APS imagers, but only a few of them can meet requirements of the chip level approach at video rate. The best options for low power implementation in 5 MS/s sampling rate (and above) and at resolution of 8-12 bit range, are multi-step flash and pipeline configurations. In comparison to multi-step flash, a pipelined ADC has the potential advantages of inherent signal single-path sampling, which gives good high-frequency effective bit performance. In addition, signal amplification down the pipeline followed by digital error correction relaxes the comparator offset constraints, which enables the usage of dynamic comparators. Pipelined ADC has been the subject of investigation during last several years [11,12,13,14]. Recently, a 10 bit, 1.8 V, 65mW, 50MS/s [15], and a 12 bit, 3V, 35mW, 21MS/s CMOS pipelined ADCs [16] have been reported. The advantages of the pipelined ADC, which combines high speed with medium-high resolution and low power consumption seems a promising combination with the standard CMOS APS implementation. This paper presents a novel 256x256 CMOS APS system with 12 bit, 6.3 MS/s CMOS pipelined ADC

integrated on the same chip. The test chip has been implemented in 0.35 μ m 2P4M process, operated by a 3.3V supply and at conversion rate of 6.3 MS/s is expected to dissipate 55mW.

This work is arranged as follows: Section II addresses the system architecture. Section III presents the circuit implementation. Section IV describes the measured results. A summary concludes the paper.

2. SYSTEM ARCHITECTURE

2.1 APS Architecture

The architecture of the sensor is shown in Figure 1. As in a traditional rolling shutter APS the proposed sensor has an imager of 256x256, 3 transistors (3T) pixel array, row decoder, row driver, column decoder Sample & Hold (S/H) circuits, clock and signals generator, timing block, and a 12 bit pipelined ADC.

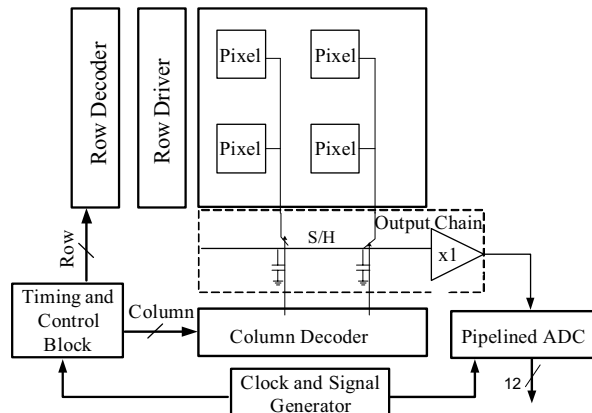


Figure 1: The sensor architecture

The single pixel with an N-well photodiode has a fill factor (FF) of 12% and a pitch of 7 μ m. The operation principle is described in [3] and will be briefly summarized here. The pixel consists of a photodiode reset transistor (RST) and a row select transistor (RS). The charge-to-voltage conversion occurs at the sense node capacitance, which consists of the photodiode capacitance and all other parasitic capacitances connected to that node. The source-follower transistor (SF) acts as a buffer amplifier to isolate the sensing node. When a reset pulse is applied, the photodiode is charged to a known value limited by the threshold voltage of the RST transistor. The integration starts when the RST transistor is switched off. During integration, the photodiode discharges the capacitance of the photodiode node. Finally the value is read out through the SF and the RS. The S/H circuit has to convert the single ended

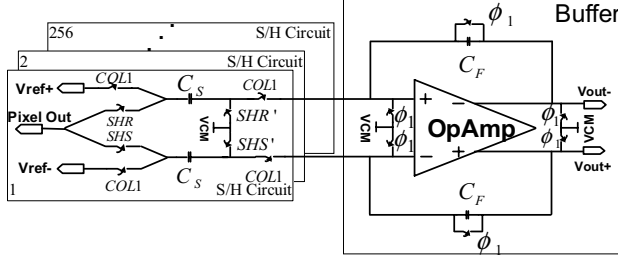


Figure 2: Output chain block diagram

pixel output into a differential mode, since the pipelined ADC was implemented in a fully differential configuration. Figure 2 exhibits the output chain block diagram, which consists of a S/H circuits and a buffer.

The clocks Φ_1 and Φ_2 are non-overlapping and are used for the pipeline timing (Φ_2 is not displayed in Figure 2). The signal COL1 is a result of a logical AND between the column decoder output and Φ_2 . The design (i.e., both the S/H circuit and the pipelined ADC) utilizes a bottom plate sampling technique (i.e., SHS' and SHR'), thus eliminating the first order signal-dependent charge injection distortion. In addition, slow SHS and SHR are applied to minimize charge injection and clock feed-through offsets. 1pF sampling and feedback capacitors, C_s and C_F respectively, are used in order to reduce the kT/C noise. The output chain transfer function is given by:

$$v_{out} = \frac{C_s}{C_F} \left[(v_{rst} - v_{sig}) - v_{ref} \right] \quad [1]$$

A detailed op-amp topology is discussed in section 3.

2.2 Pipelined ADC Architecture

The ADC uses a pipeline 1.5-bit/stage architecture [11] with 11 stages, as shown in Figure 3. Each stage is responsible for resolving two bits from the digital output code. Each stage is composed of a coarse Flash-ADC, a low resolution digital to analog converter (DAC), a S/H circuit, and a residue amplifier. The 2-bit MSB low-resolution ADC determines the two MSBs. The determination of the remaining LSBs is performed in the following steps: (1) The quantization error is found by reconvolving the 2-bit digital to an analog value using the 2-bit DAC. (2) This value is subtracted from the input signal, generating a residue. This residue is then amplified by a gain of two and passed on to the next stage. The second stage performs similar operations on the amplified residue resulting in a determination of the next most significant bits of the input signal. The stages are buffered by switching-capacitors gain blocks that provide a S/H between each stage, allowing concurrent processing. Digital error correction [11,12] is used to generate the 12 bit final output code from the resulting 22 bit. The use of a digital error correction technique in conjunction with a low number of bits per stage relaxes the constraints on the comparator offset voltage.

Figure 4 displays the pipelined ADC stage implementation. Although, a single-ended configuration is shown for simplicity, the actual implementation was fully differential.

The pipelined ADC stage consists of (1) Two comparators

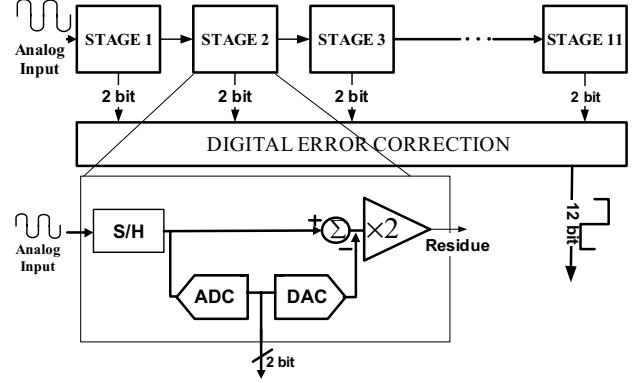


Figure 3: The selected pipelined ADC architecture

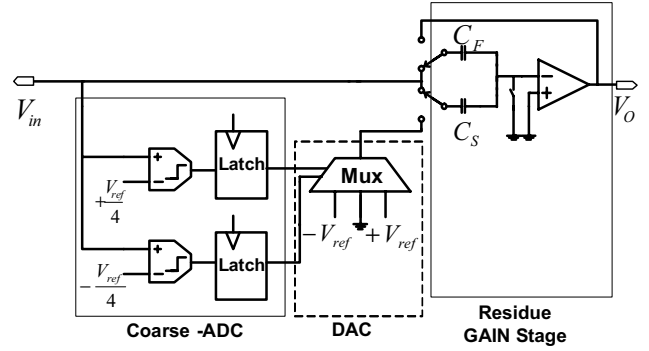


Figure 4: Pipelined ADC stage block diagram

with corresponding threshold voltages $V_{ref}/4$ and $-V_{ref}/4$, which, in fact, assemble the coarse Flash-ADC, (2) An analog mux that actually functions as DAC, with the three corresponding reference voltages $-V_{ref}$, 0, and V_{ref} and (3) Residue gain stage [14]. The residue gain stage, shown in Figure 5, samples the signal input, subtracts it from the relevant reference voltage, and amplifies the residue by the gain of two. When defining $C_F = C_s$, the ideal stage operation is as follows:

$$V_o = \begin{cases} 2 \left(V_i - \frac{V_{ref}}{2} \right) & \text{if } V_i > V_{ref}/4 & d \rightarrow 2(10)_2 \\ 2V_i & \text{if } -V_{ref}/4 < V_i < V_{ref}/4 & d \rightarrow 2(01)_2 \\ 2 \left(V_i + \frac{V_{ref}}{2} \right) & \text{if } V_i < -V_{ref}/4 & d \rightarrow 1(00)_2 \end{cases} \quad [2]$$

where d is the stage digital output code.

Figure 6 shows the ideal transfer characteristics of a pipelined ADC stage. With the use of a digital correction algorithm the overflow of the current stage output from the input range of the following stage can be prevented even with the presence of a large comparator offset, so that this offset error amplified down the pipeline can be detected for correction. With this configuration, the coarse Flash-ADC error, up to $V_{ref}/4$, can be tolerated and digital correction circuit contains adders only. The correction is achieved by adding the output codes of the pipeline stages in overlapping the stage i LSB with stage $i+1$ MSB.

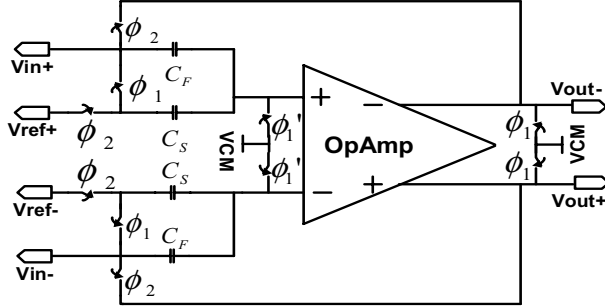


Figure 5: The residue gain stage

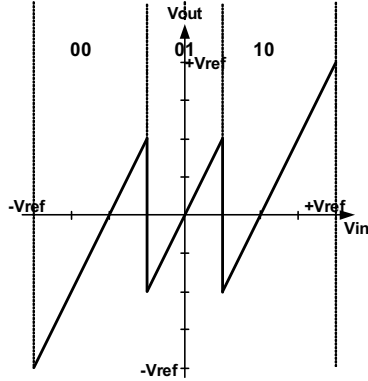


Figure 6: Ideal transfer characteristics of the pipelined ADC stage

The clock timing generator generates non-overlapping multiphase clocks, shown in Figure 7.

3. PIPELINED ADC-CIRCUIT DESCRIPTION

Because of the large dc gain requirement in the high resolution pipeline, and in order to achieve a large voltage swing, a two-stage amplifier is used for this application. The op-amp topology [13] used in the pipeline stages is shown in Figure 8. This two-stage, fully-differential amplifier consists of a folded cascode first stage followed by a common-source second stage with compensation to the cascode node [17]. The fully differential architecture, although improving power supply rejection, requires a common mode feedback as shown. This extra circuitry is needed to establish a common-mode output voltage. The S/H op-amp is the most critical part in the overall design, because it has to settle within at least 13 bit accuracy in one clock phase. Actually, this settling time limits the overall pipeline throughput. Based on BSIM 3v3 simulations, the settling time of the op-amp is less than 70nsec for 13 bit accuracy. The op-amp dc gain is 120dB and its phase margin is 63°. The power dissipation of the op-amp including its bias circuit is less than 2.6 mW. There are a total of ten op-amps in the ADC, since the last stage does not need to generate any analog signal.

The comparator circuit consists of a preamplifier followed by a dynamic latch circuit and buffer [14]. This architecture improves metastability and reduces kick-back noise on the input residue. The pipelined ADC consists of 22 comparators, which dissipate approximately 4.4mW. The interstage capacitor sizes are determined by the kT/C thermal noise constraints. Due to

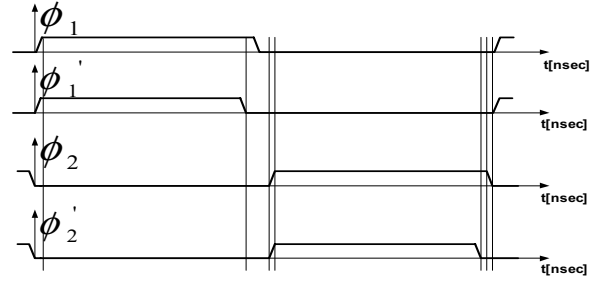


Figure 7: The non-overlapping multiphase clock waveforms implemented

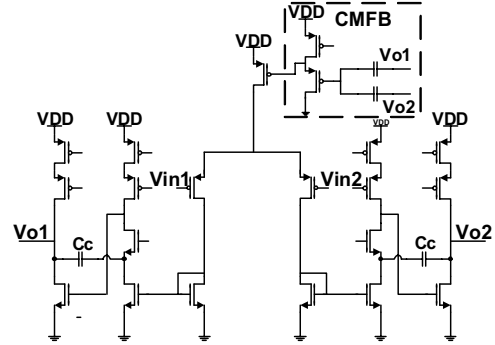


Figure 8: Operational amplifier architecture

relaxed accuracy constraints in later pipeline stages, these capacitors were scaled down to help reduce power consumption [12]. To maximize the matching between the capacitors and minimize bottom plate parasitics, the common-centroid capacitor arrays with dummy capacitors surrounding the arrays are used.

4. SIMULATION RESULTS

Figure 9 shows the layout of the test chip. The total area of the prototype is 12 mm², and the core area of the ADC is 18% from the total area. The test chip has been implemented in 0.35μm 2P4M process, operated by a 3.3V supply. Design simulation has been carried out in SpectreS with BSIM3V3 models of a TSMC 0.35μm 2P4M process. Based on SpectreS simulation, the approximate total power consumption is 55mW. Based on layout extraction, the transient response of the S/H op-amp shows that the maximum settling time to 13 bit accuracy is in 70ns. The chip attributes summary shown in Table I.

4. CONCLUSIONS

The trend toward integration is driven by low cost, and low power implementations. Therefore, for video rate applications, integration of an APS system with a chip-level pipelined ADC appears as a very reasonable option. This work successfully demonstrates a novel 256x256 CMOS APS system with 3.3V, 12 bits, 6.3 MS/s CMOS pipelined ADC integrated on the same chip. This experimental chip has been implemented in a 0.35μm 2P4M process, operated by a 3.3V and at conversion rate of 6.3 MS/s dissipates 55mW.

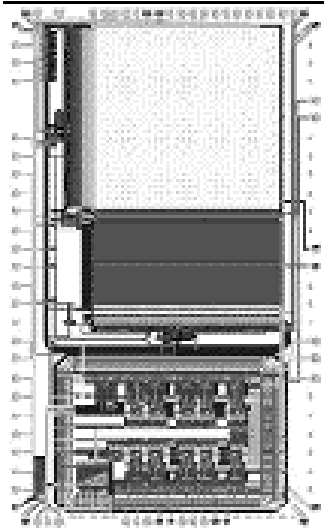


Figure 9: Test chip layout

Power Supply	3.3 V
Technology	0.35 μ m 2P4M CMOS
APS array resolution	256x256
Pixel pitch	7 μ m
Fill factor	12%
ADC resolution	12 bit
ADC conversion rate	6.3 MS/s
ADC input range	± 1 V differential
Die area	12 mm ²
Power dissipation	55 mW

Table 1: chip attributes

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