12.4 SXGA Pinned Photodiode CMOS Image Sensor in 0.35μm Technology

Keith Findlater, Robert Henderson, Donald Baxter, J.E.D. Hurwitz, Lindsay Grant, Yvon Cazaux[1], François Roy[1], Didier Herault[1], Yann Marcellier[1]

STMicroelectronics Imaging Division, Edinburgh, UK
[1]STMicroelectronics Central Research and Development, Crolles, France

CMOS imagers are well known to offer advantages of low-power, low-voltage, and increased integration over the competing charge coupled device (CCD) technology. These benefits enable cost-effective solutions to applications such as mobile imaging [1]. However, for high quality applications, the dark current and the temporal noise floor in CMOS image sensors must be improved. The pinned photodiode pixel [2], commonly used in CCDs, can bring these performance improvements to CMOS imagers while retaining the advantages of increased circuit integration.

To bring the full benefit of the pinned photodiode pixel type elimination of kTC noise, the readout noise floor must be minimized. Column parallel analog-to-digital converters (ADCs) allow low bandwidth readout amplifiers to be used. This is a key advantage of the column-parallel ADC approach over the use of a wide bandwidth single output amplifier such is in CCDs or single ADC CMOS imagers [3].

Figure 12.4.1 shows the architecture of the column-parallel readout ADC imager. The column is composed of a sample and hold stage, comparator, and 11b ADC memory. Single-slope ADC conversion is performed by a voltage ramp to the comparator inputs as a counter drives the random access memory (RAM). The counter value is stored when the individual column comparator switches [1]. A ramp generator provides 2 ramps simultaneously to allow analog white noise balance and which also minimizes quantization noise in the blue channel where the signal is lower. The sensor uses a Bayer pattern color filter array (CFA). To avoid column mismatch in the green channel which causes a fixed pattern noise, the green ramp and pixel data are always converted by odd columns; a multiplexor ensures that the correct pixel color is connected to the appropriate column for each line. While a mismatch is still present between the green channel and the other two colors, this is automatically corrected by automatic white balance during color image reconstruction.

One of the perceived drawbacks of the column parallel ADC approach is the area overhead. To save die size, a 3-transistor dynamic RAM (DRAM) (Fig. 12.4.2) is used for the column ADC memory rather than static RAM. The DRAM requires no additional process steps and occupies only 120μm for two banks of 11b per column. Because of the progressive scan operation of the sensor, the RAM is only required to hold for 1 line time, therefore retention time is much less of a problem than in normal DRAM circuits. The read and write power at 48MHz of the DRAM is <2 mW. This readout rate permits 30frames/s operation at SXGA resolution (1280x1024). The sensor also supports sub-sampled and window-of-interest VGA modes.

The readout noise is composed of the following: thermal and 1/f noise of the pixel source follower, kT/C noise of the sample-and-hold for the ADC, the thermal noise of the ADC comparator, noise on voltage references and supplies and the quantization noise of the ADC. At low light levels, where the analog gain of the ADC is high (i.e. the ramp step size is small), the quantization noise is negligible. Remaining is the design of the ADC bandwidth and the pixel correlated double sampling (CDS) timing to minimize the referred thermal and 1/f noise. Figure 12.4.3 shows the timing of the pinned photodiode pixel. True CDS using the pixel transfer gate eliminates the kTC noise of the sense node reset. Additionally, the CDS serves to attenuate low-frequency, noise such as source follower 1/f noise, at the cost of increasing the thermal white noise power. The time between CDS samples (CDS period) defines the low-frequency cut-off point, reducing this period will attenuate the pixel 1/f noise as is shown in Fig. 12.4.4.

Additionally, limiting the column bandwidth by increasing sample and hold capacitance reduces the pixel white noise contribution and the sampling noise. In this design, the timing between CDS samples is minimized while still allowing for complete settling. An extra bandwidth limitation comes from connecting both sample capacitors to the column for the first CDS sample. Any further reduction in white noise costs area, as larger capacitors are required, and also power, in order to settle in the required time with the larger capacitance. This design employs a CDS period of 1μs with a column capacitor of 1pF. The pixel referred sample and hold kTC noise is therefore 3.5 electrons. The comparator pre-amp bandwidth is limited to 140kHz to minimize its input referred thermal noise to 80μV (3 electrons).

The table of Fig. 12.4.5 gives the performance data from the sensor. A pixel size of 5.6 by 5.6μm is used to give a 1/2 inch optical format. The vertical fixed pattern noise (FPN) of 135μV is very low and is not noticeable over the analog gain range (0-24 dB). The ADC noise floor is 140μV (~7 electrons), however the image noise is limited by low frequency noise from the pixel source follower itself, resulting in a read noise of 14 electrons (340μV). Using on-chip test circuitry with dummy pixels with 16 times the source follower area, but the same W/L ratio and current, 145μV is measured. Measurements confirm that the raised noise floor is due to higher than expected pixel source follower noise (Fig. 12.4.4). The dark current is considerably lower than in previously published 3T-pixel CMOS imagers [1,4]. Further reduction of the dark current and pixel noise continues. As the readout noise is not the limiting factor, a noise floor close to 7 electrons is believed achievable. Figure 12.4.5 shows an example image from the sensor and Fig. 12.4.6 depicts the die micrograph.

References

[1] J. Hurwitz et al, "Miniature Imaging Module for Mobile Applications," *ISSCC Digest of Technical Papers,* pp. 90-91, 2001.
[2] B. Burkey et al, "The Pinned Photodiode for an Interline-Transfer CCD Image Sensor," *IEDM 1984*, pp 28-31
[3] L. J. Koslowski, "Theoretical Basis and Experimental Confirmation Why a CMOS Imager is Superior to a CCD," *Proceedings of SPIE,* Orlando, Apr. 1999, pp.388-396.
[4] J. Hurwitz et al, "A 35mm Film Format CMOS Image Sensor for Camera-Back Applications," *ISSCC Digest of Technical Papers*, p 48-49, 2002.

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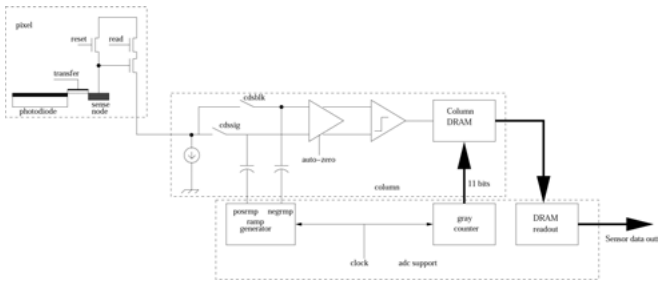

Figure 12.4.1: Column read-out schematic.

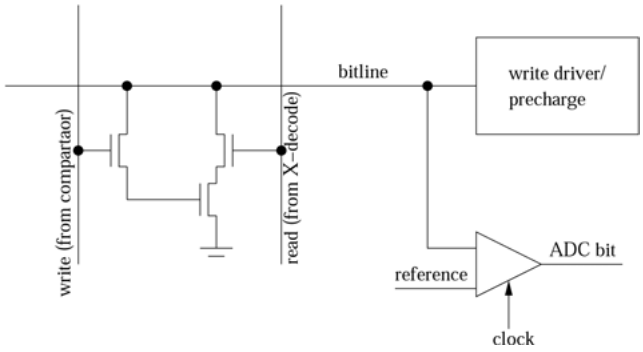

Figure 12.4.2: In-column DRAM circuit.

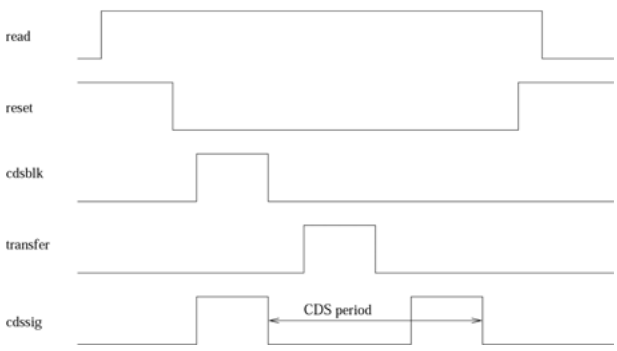

Figure 12.4.3: Pixel timing.

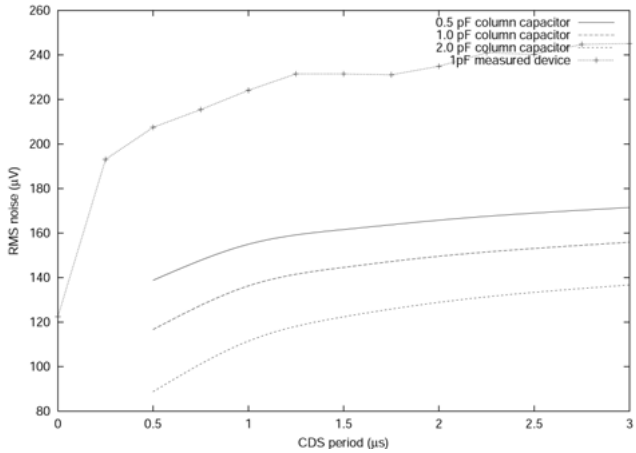

Figure 12.4.4: Simulated and measured read noise.

Technology	0.35µm 1P3M CMOS
Color	Bayer pattern CFA with microlens
Analog supply	2.8V
Digital supply	1.8V
Analog power	75mW at 24MHz
Digital power	4.5mW at 24MHz
Image format	1280 x 1024 (SXGA)
Pixel size	5.6 x 5.6mm
Maximum pixel rate	48MHz (30rames/s SXGA)
ADC resolution	11b
RMS ADC read-out noise	140µV
RMS vertical FPN	135µV
Image read noise	340µV (14 electrons)
Full-well capacity (linear)	20,000 electrons
Sensitivity at ADC input	26µV/electron
Dark current at 25°C	40pAcm^{-2}
Dynamic range (1 line exposure)	63dB
Sensitivity at 550 nm	1.4Vlux^{-1}s^{-1}

Figure 12.4.5: Table of sensor performance data.

Figure 12.4.6: Example SXGA image from sensor.

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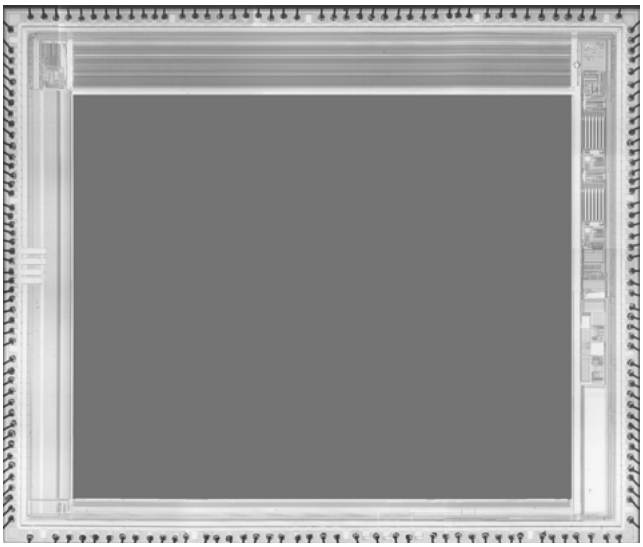

Figure 12.4.7: Die micrograph of the fabricated sensor.

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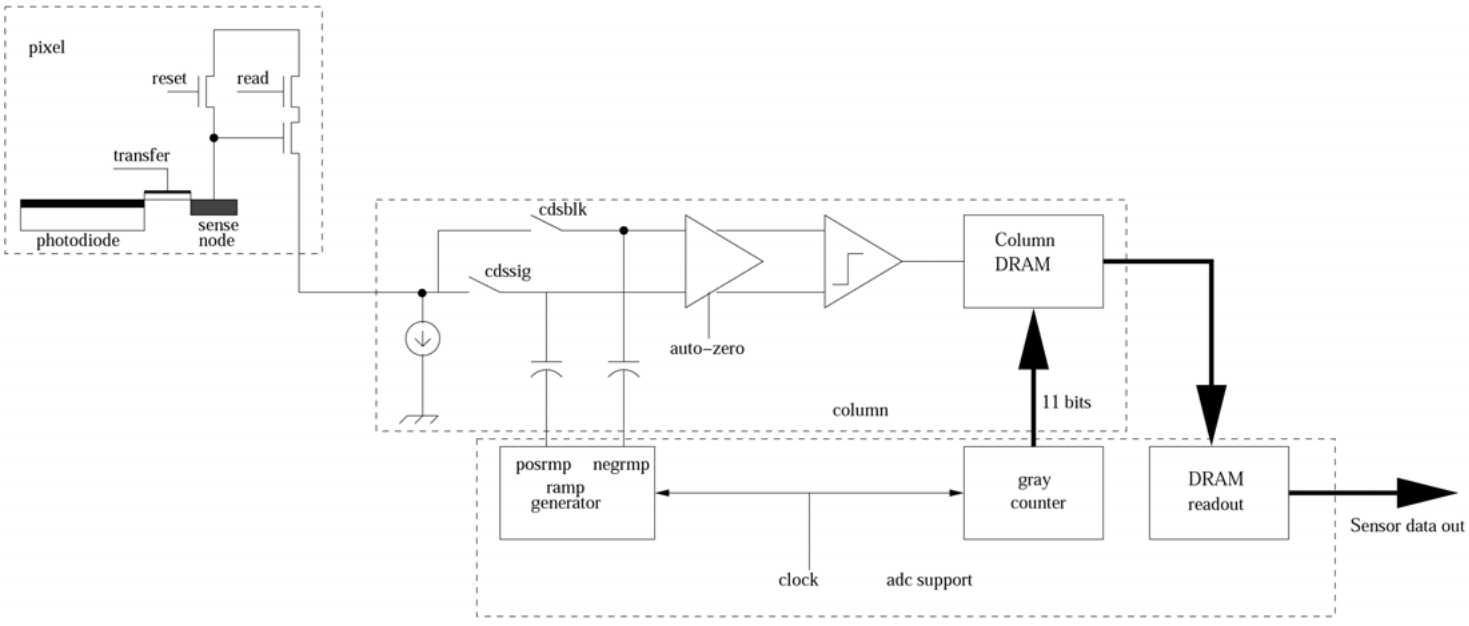

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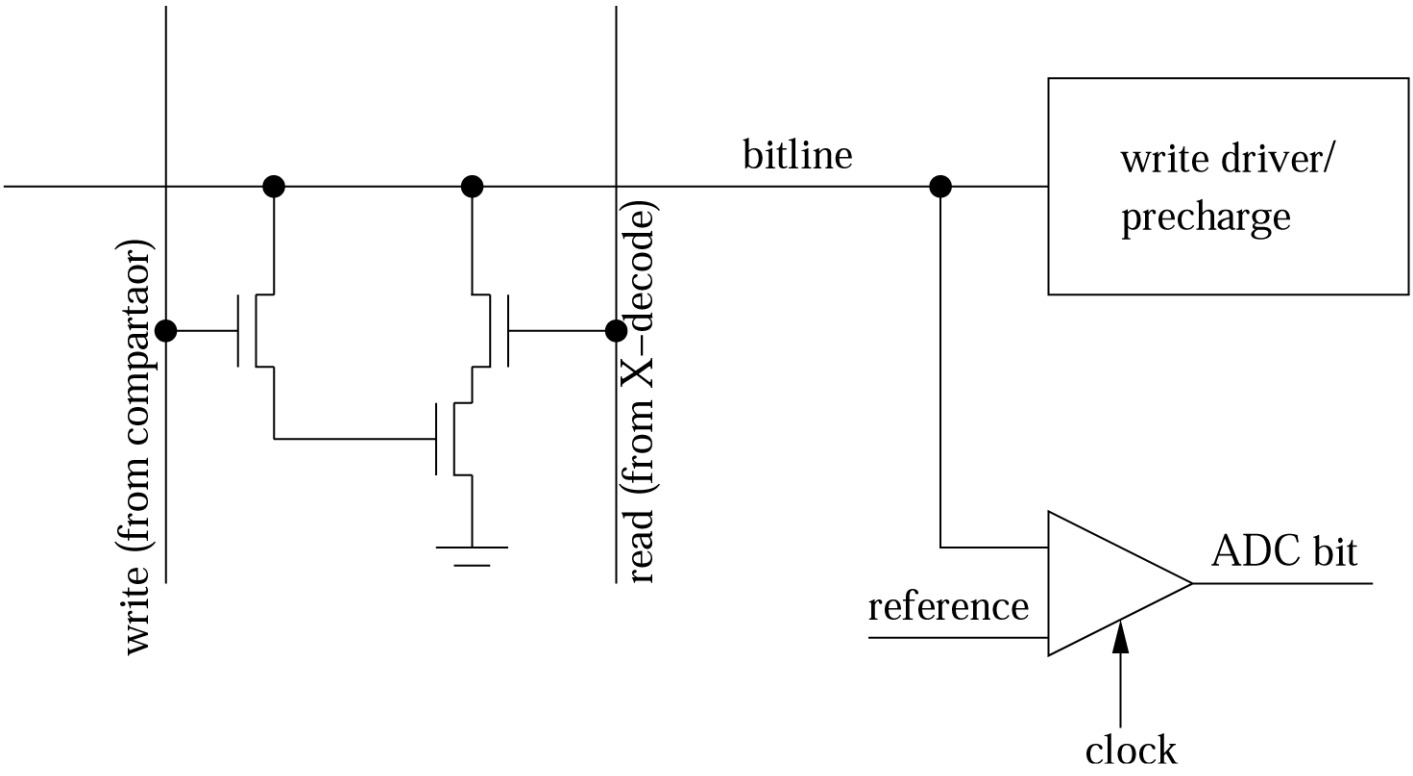


Figure 12.4.2: In-column DRAM circuit.

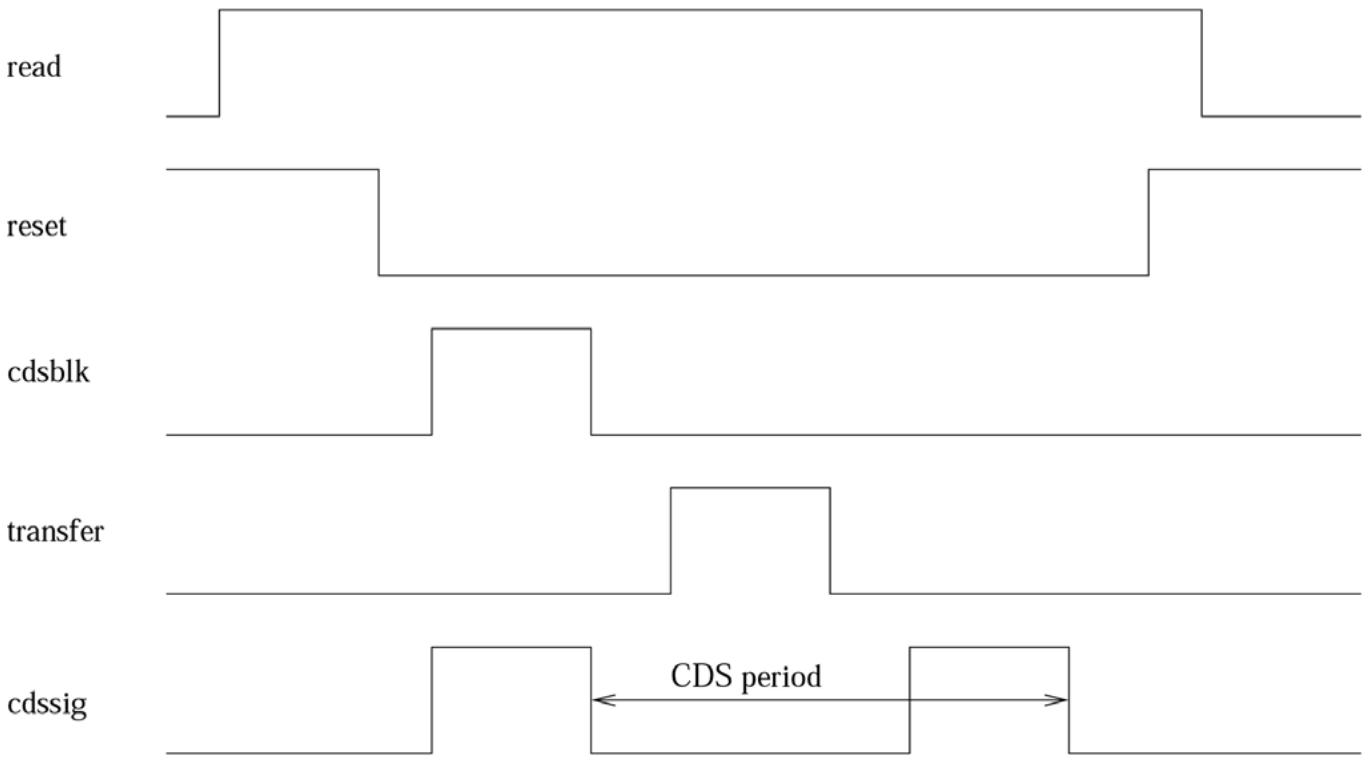
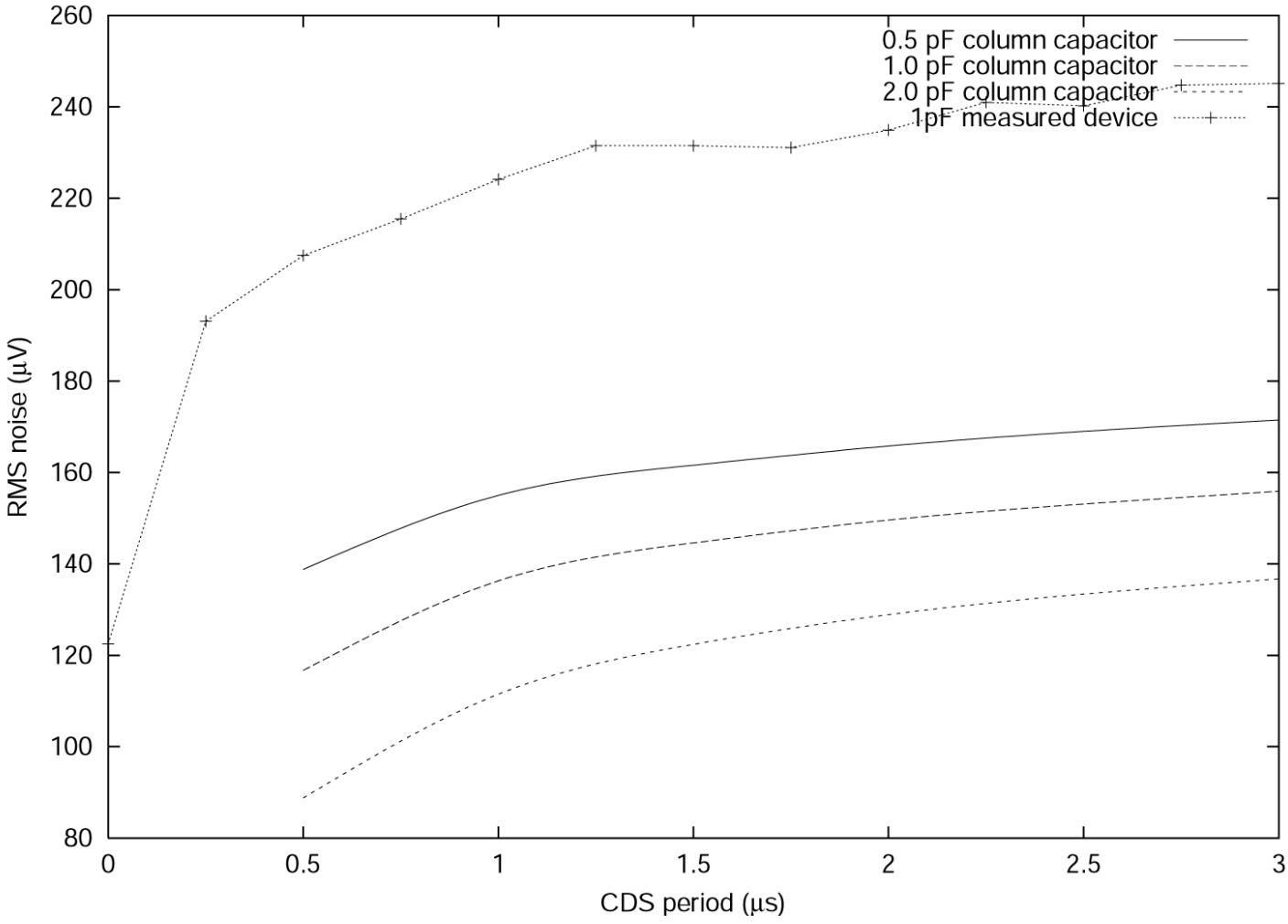


Figure 12.4.3: Pixel timing.



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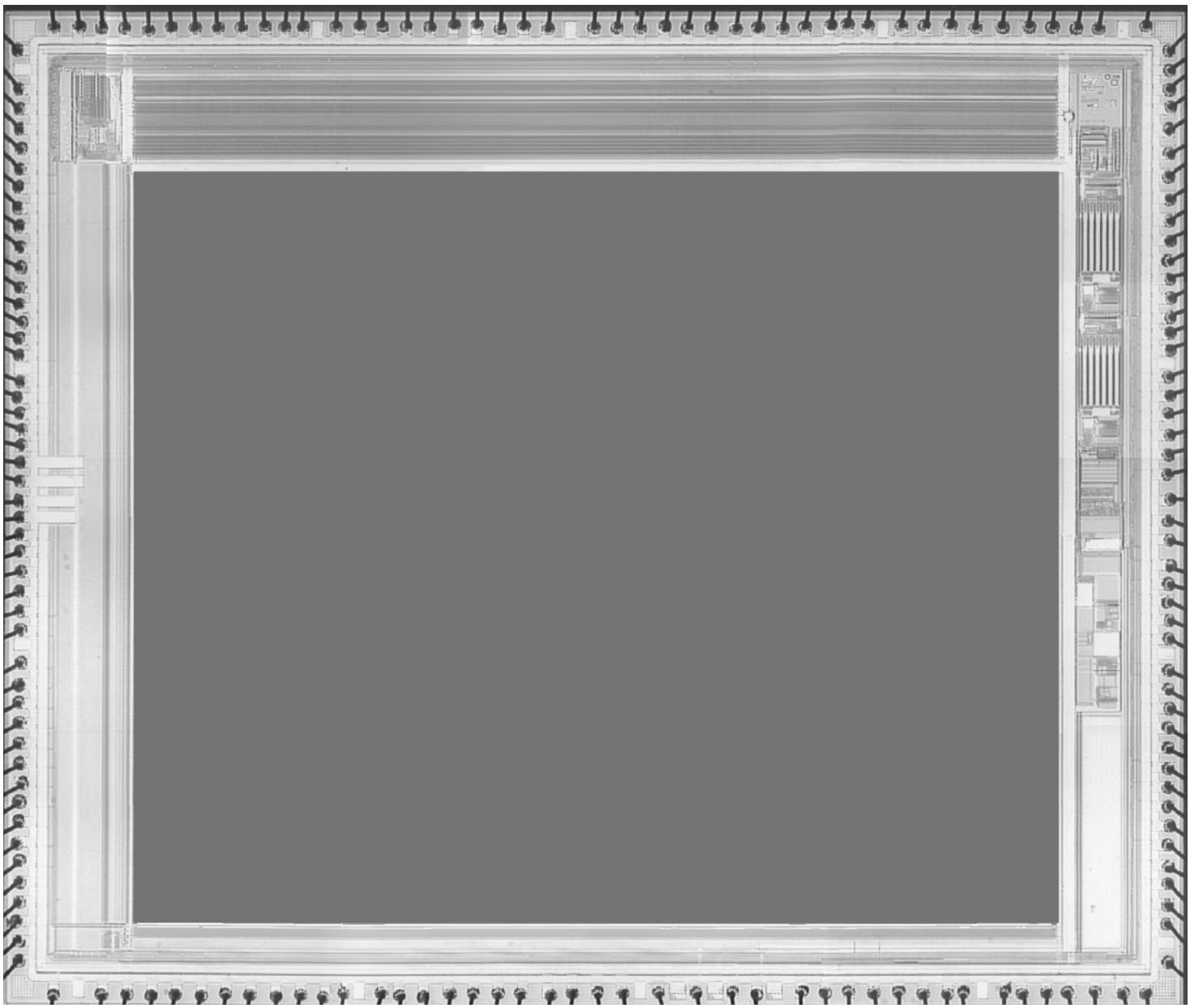

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