Low-Noise In-Pixel Comparing Active Pixel Sensor Using Column-Level Single-Slope ADC

Dongmyung Lee, *Student Member, IEEE*, Kunhee Cho, *Student Member, IEEE*, Dongsoo Kim, *Student Member, IEEE*, and Gunhee Han, *Member, IEEE*

***Abstract*—A conventional active pixel sensor (APS) uses a source follower (SF) in a pixel as a buffer. This SF is one of the major causes of nonlinearity, sensitivity degradation, and pixel readout noise. The proposed in-pixel comparing APS uses pixel transistors as a part of comparator for a single-slope ADC instead of using them as an SF. The prototype sensor was fabricated using a 0.35-μm 2P3M CMOS process. Experimental results show 15-times linearity improvement, 26% sensitivity enhancement, and 33% noise reduction over the conventional APS.**

***Index Terms*—CMOS active pixel sensor (APS), column-level ADC, readout noise, source follower (SF).**

I. Introduction

CMOS ACTIVE pixel sensors (APSs) have been widely used due to their advantages of low-voltage, low-power, and on-chip integration capability [1]. There are three on-chip ADC architectures for CMOS APSs: chip-level, pixel-level, and column-level ADCs. Among these architectures, column-level ADC is the most widely used in CMOS APSs for mobile applications because of its high throughput and low-power consumption [2]. CMOS APSs using the column-level ADC include a source follower (SF) in a pixel as a buffer from the floating diffusion (FD) node to the column line. Although the voltage readout through the SF improves the sensor readout speed and the signal-to-noise ratio (SNR) compared to the charge readout as in passive pixel sensors, the SF introduces nonidealities such as nonlinearity, sensitivity degradation, and noise [3]–[5].

Unity gain amplifier can be employed instead of the SF to improve the linearity and sensitivity [3], but it adds more readout noise compared to the SF while dissipating power comparable to the SF.

Multiple sampling techniques [6]–[8] and gain-adaptive column amplifiers [9]–[11] can be employed to reduce the readout noise. Although multiple sampling techniques are widely used to achieve wide dynamic range, as well as readout noise reduction, they require additional memories, resulting in large silicon area. The use of high-gain column amplifiers enhances the sensitivity of CMOS APSs and reduces the readout noise and quantization noise from the ADC, but it reduces the dynamic range of the sensors due to the saturation of the amplifiers and results in high power consumption.

Digital pixel sensor does not require the SF as a buffer because it performs A/D conversion in the pixel [12], [13]. Although it achieves high SNR and readout speed, it is not applicable to the mobile consumer electronics due to its large pixel size and high power consumption.

In-pixel correlated double sampling (CDS) also eliminates the SF and provides low-power consumption and low readout noise [14]. However, it requires large pixel area as well.

This paper proposes an in-pixel comparing APS (ICAPS) that uses pixel transistors as a part of comparator for a column-level single-slope ADC instead of using them as an SF to improve the nonidealities without any pixel area overhead. Section II describes the architecture and the operation principle of the conventional APS and the proposed ICAPS. Section III presents the performance analysis in terms of linearity, sensitivity, noise, and readout speed. Section IV presents the experimental results, followed by conclusion in Section V.

II. Architecture and Operation Principle

The pixel readout circuit and timing diagram of the conventional APS using a column-level single-slope ADC which employs digital CDS are shown in Fig. 1 [15]. During Φ_1, M_2 is turned off, and light induced electrons are accumulated in the photodiode (PD). When a pixel is selected for readout, *RST* is pulsed to reset the FD node. The FD node potential is read out through the SF, which is composed of M_3, M_4, and $I_{\rm SF}$. The single-slope A/D conversion is then carried out with the ramp signal $V_{\rm RAMP}$. The A/D converted reset level $D_{\rm rst}$ is stored in memory$_1$. After that, *TG* is pulsed to transfer the integrated charge in the PD into the FD node. The readout through the SF and A/D conversion for the sensor signal is then performed again in the same manner, and the result $D_{\rm sen}$ is stored in memory$_2$. The difference between the two memory contents is the light induced signal.

The SF as a voltage buffer introduces several nonidealities such as nonlinearity, sensitivity degradation, and readout noise, as discussed in the next section.

The proposed ICAPS removes the SF by using two pixel transistors M_3 and M_4 as a part of comparator instead of using them as an SF, while the rest of the comparator circuit is located in the column and shared by the pixels in the corresponding column,

Manuscript received May 13, 2008; revised August 22, 2008. Current version published November 26, 2008. This work was supported in part by the Ministry of Knowledge Economy (MKE), Korea, under the Information Technology Research Center (ITRC) support program supervised by the Institute for Information Technology Advancement [(IITA); IITA-2008-(C1090-0801-0012)] and in part by Samsung Electronics Co. Ltd. The review of this paper was arranged by Editor J. Tower.

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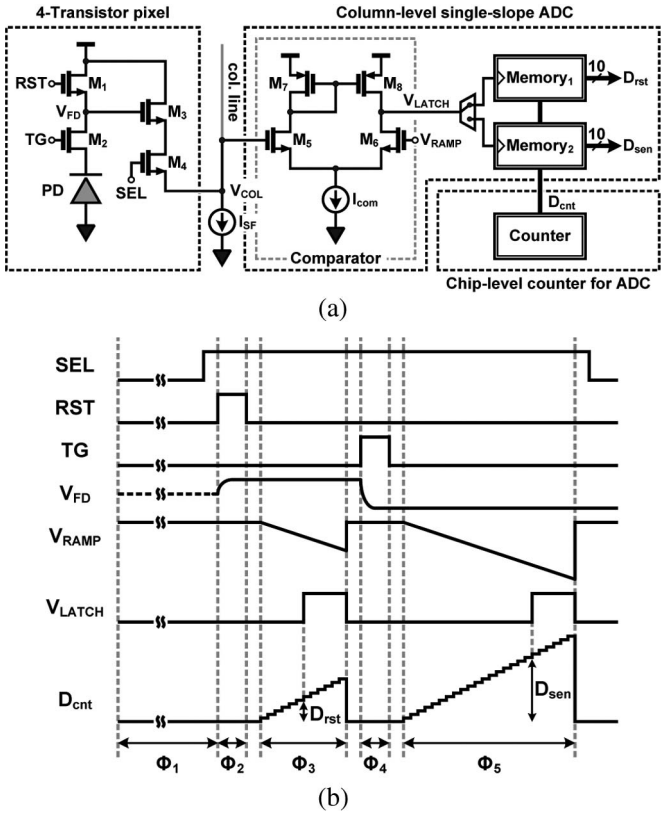
Digital Object Identifier 10.1109/TED.2008.2006735



(a)

(b)

Fig. 1. Conventional APS. (a) Pixel readout circuit. (b) Timing diagram. (Φ_1) Photo current integration. (Φ_2) FD reset. (Φ_3) Reset signal A/D conversion. (Φ_4) Charge transfer. (Φ_5) Sensor signal A/D conversion.

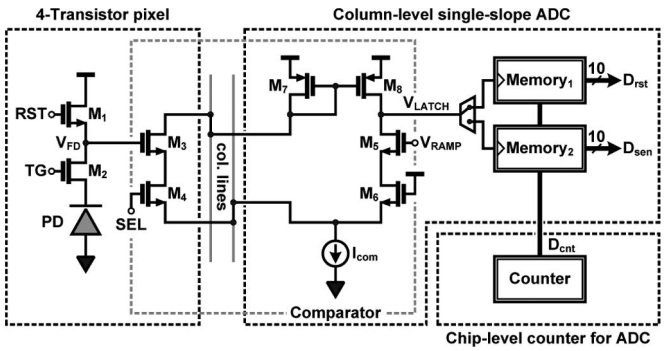


Fig. 2. Pixel readout circuit of the proposed ICAPS.

as shown in Fig. 2. The operation principle and timing diagram of the ICAPS are the same as those of the conventional APS.

III. Performance Analysis

The SF voltage gain A_s from the FD node to the column line (ADC input) can be obtained as follows from a simple small signal analysis:

$$A_s = \frac{\partial \nu_{\rm COL}}{\partial \nu_{\rm FD}} \cong \frac{g_{\rm ms}}{g_{\rm ms}+g_{\rm mb}} = \frac{1}{1+g_{\rm mb}/g_{\rm ms}} \tag{1}$$

where $g_{\rm ms}$ and $g_{\rm mb}$ are the gate-drain and bulk-drain transconductances of the SF input transistor. Therefore, the signal attenuation by the SF reduces the sensitivity by a factor of $(1+g_{\rm mb}/g_{\rm ms})$. Moreover, the nonlinearity of $g_{\rm mb}$ degrades the linearity of the image sensor.

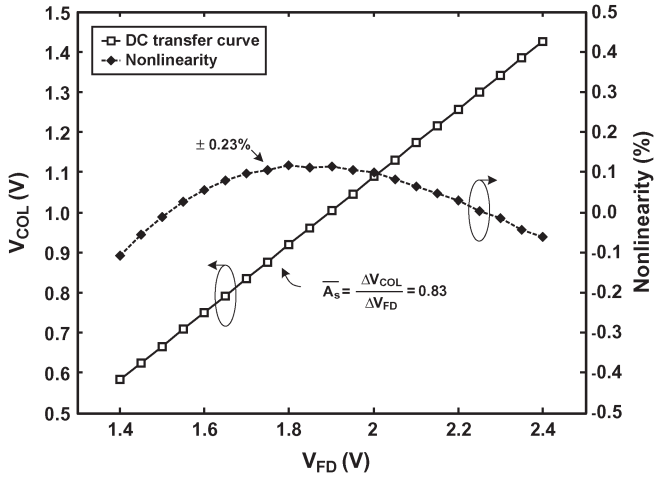
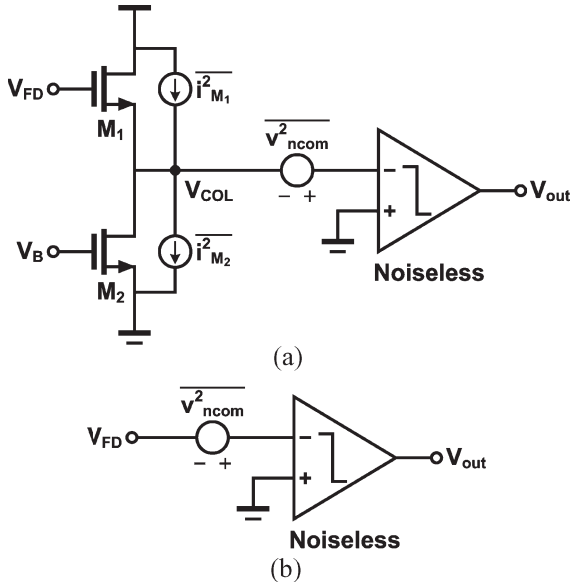


Fig. 3. Simulated dc transfer curve and nonlinearity of an SF.



(a)

(b)

Fig. 4. Readout circuit with equivalent noise sources. (a) Conventional APS. (b) Proposed ICAPS.

Fig. 3 shows the simulated dc transfer curve and the nonlinearity of an SF. Simulation results show a 0.23% linearity error and a 17% sensitivity reduction due to the SF.

The dominant noise source at low illumination is the readout noise, whereas it is the PD shot noise at high illumination [16]–[18]. As the flicker noise of reset transistor, SF, and comparator can be removed substantially by the CDS [19], [20], the thermal noises of the SF and comparator are the most critical readout noise. Fig. 4 shows the readout circuits of the conventional APS and the proposed ICAPS with equivalent noise sources. The total noise of the conventional APS referred to the column line is given by

$$\overline{\nu_{\rm nCOL}^2} = \left(\overline{i_{M_1}^2}+\overline{i_{M_2}^2}\right)|Z_s|^2 + \overline{\nu_{\rm ncom}^2} \tag{2}$$

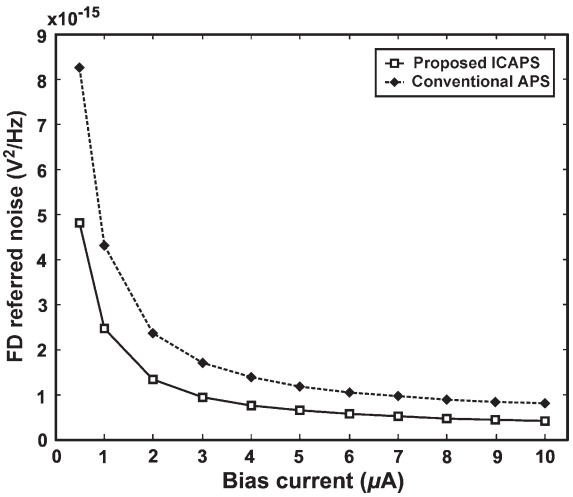


Fig. 5. Simulated FD referred noise as a function of bias current when $I_{\rm SF} = I_{\rm com}$.

where $\overline{i_M^2}$ is the noise current of the MOS transistor given as $(8/3)kTg_m$, Z_s is the output impedance of the SF, and $\overline{\nu_{\rm ncom}^2}$ is the input referred comparator noise [21]. Then, the total noise referred to the FD node can be obtained by dividing the output noise by the SF gain as follows:

$$\overline{\nu_{\rm nFD}^2} = \frac{1}{|A_{\rm s}|^2} \times \overline{\nu_{\rm nCOL}^2} \cong \frac{8}{3}\frac{kT}{g_{\rm ms}} + \left(1 + \frac{g_{\rm mb}}{g_{\rm ms}}\right)^2 \overline{\nu_{\rm ncom}^2}. \quad (3)$$

Consequently, the SF not only adds the noise by itself but also amplifies the comparator noise by a factor of $(1 + g_{\rm mb}/g_{\rm ms})^2$ in the conventional APS. Since the comparator is directly connected to the FD node in the proposed ICAPS, the total readout noise referred to the FD node is equivalent to the input referred noise of the comparator as follows [21]:

$$\overline{\nu_{\rm nFD}^2} = \overline{\nu_{\rm ncom}^2} \cong \frac{16}{3}\frac{kT}{g_{\rm md}} \quad (4)$$

where $g_{\rm md}$ is the transconductance of the transistors in the differential pair of the comparator.

Fig. 5 shows the simulated FD referred readout noise of the conventional APS and the proposed ICAPS as a function of bias current when $(W/L)_{\rm SF} = (W/L)_{\rm comparator}$. To compare the noise performance under the same readout speed, the bias currents of the SF and the comparator are set to be identical. This means that the total power consumption of the proposed circuit is half of that of the conventional one. The total FD referred noise of the ICAPS is reduced to about 2/3 of the conventional APS.

CMOS APS has a relatively large parasitic capacitance in the readout line. This line capacitance is one of the major limiting factors of the high speed readout because the small in-pixel SF of the APS should drive the relatively large line capacitance.

Unlike the conventional APS, the ICAPS has line capacitances within the comparator circuit, as shown in Fig. 6. The influence of the parasitic capacitance associated with the column line for the drain $C_{\rm PD}$ is negligible because the signal swing at this node is small due to the diode-connected configuration of M_7. Meanwhile, the parasitic capacitance associated with the common source node $C_{\rm PS}$ is equivalent to the line capacitance in the conventional APS. Therefore, the settling time of the readout line when the selection switch is turned on is comparable to that of the conventional APS, as shown in Fig. 7.

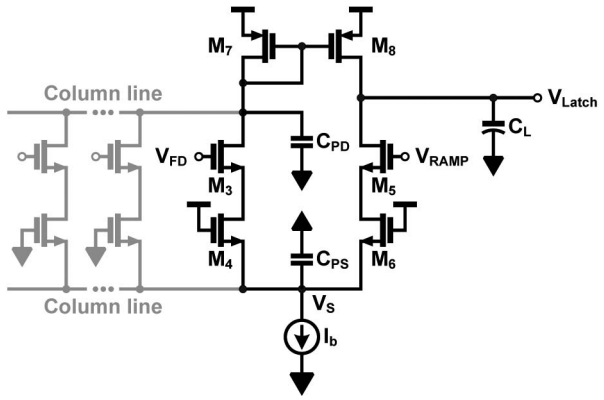


Fig. 6. Comparator including parasitic capacitance.

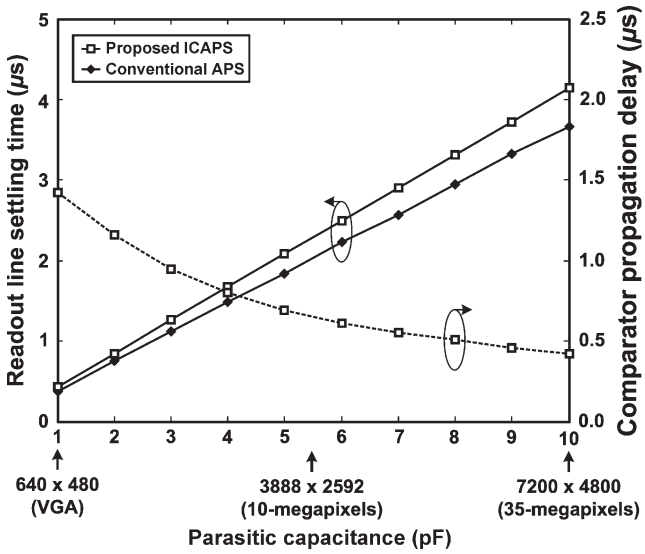


Fig. 7. Simulated settling time and propagation delay when $I_{\rm SF} = I_{\rm com}$.

The $C_{\rm PS}$ also affects the propagation delay of the comparator, defined as the time difference from the moment when the $V_{\rm RAMP}$ reaches to the $V_{\rm FD}$ to the moment when the comparator changes its output. The simulation result of the propagation delay with respect to the parasitic capacitance is also shown in Fig. 7. Layout-extracted column parasitic capacitance for the 160×240 pixel array is about 0.5 pF. Simulation is performed up to an extremely large parasitic capacitance of 10 pF, which corresponds to multimegapixel array. In this simulation, the slope of $V_{\rm RAMP}$ is set to 0.3 V/μs that allows 30 frames/s for the ten-megapixel array. The simulation result shows that the larger parasitic capacitance results in the smaller propagation delay because $C_{\rm PS}$ tends to hold the V_S instead of following $V_{\rm RAMP}$, providing the rapid change of $V_{\rm GS}$.

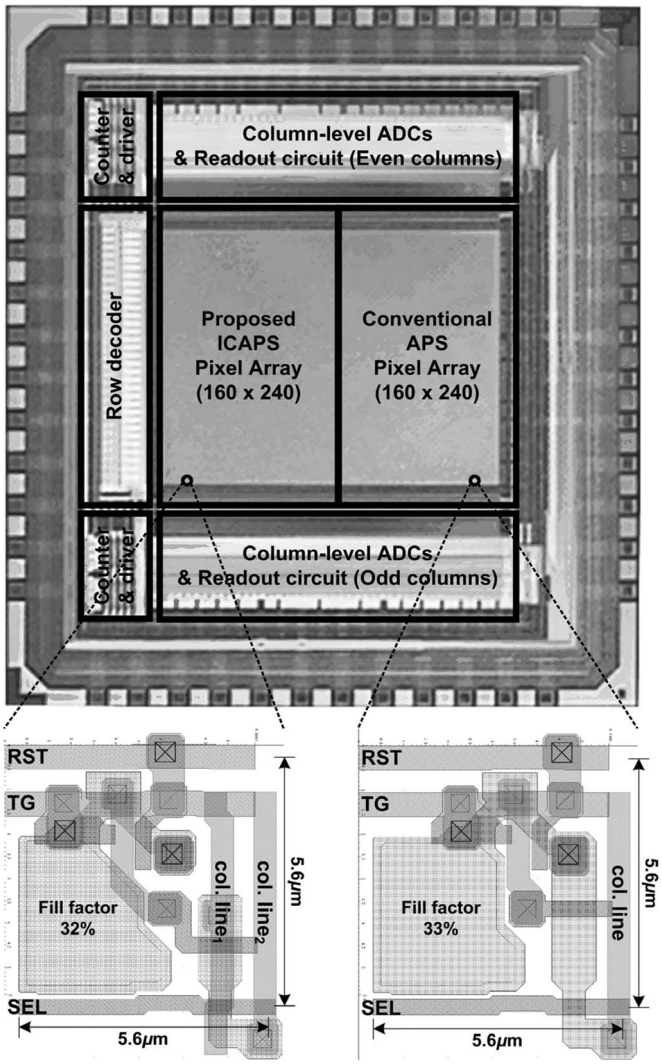


Fig. 8. Microphotograph and pixel layouts of the fabricated prototype sensor.

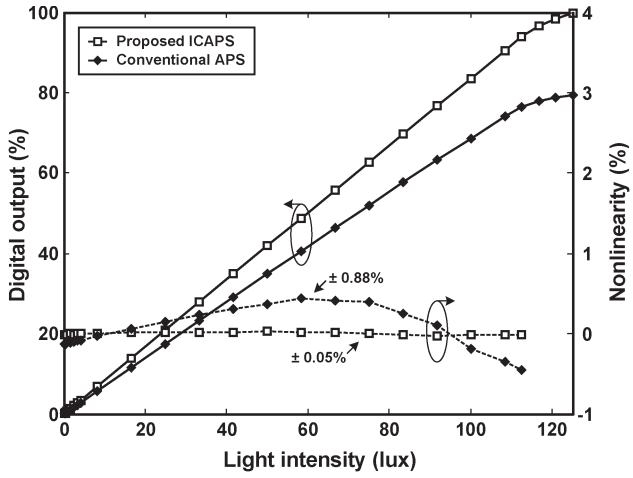


Fig. 9. Measured photoelectric conversion characteristics.

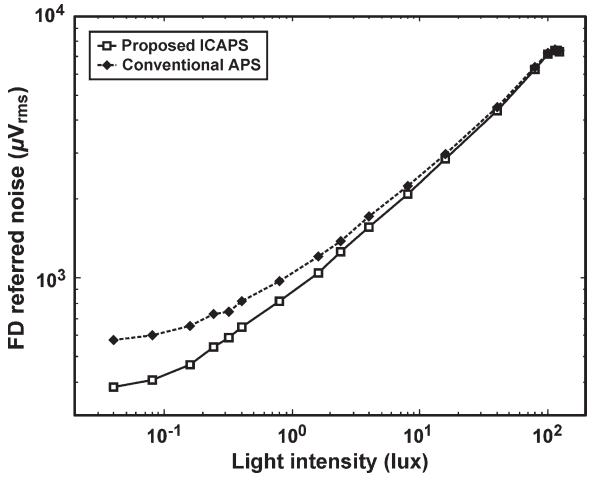


Fig. 10. Measured FD referred noise.

Consequently, the readout speed of the ICAPS is limited by the settling time rather than the comparator propagation delay when the array size exceeds two megapixels (parasitic capacitance of 2.5 pF), as in the conventional APS.

IV. Experimental Results

The proposed ICAPS was designed and fabricated with a 0.35-μm 2P3M CMOS process. A chip microphotograph of the prototype sensor is shown in Fig. 8. Since the performance of the image sensor is strongly dependent on the process, the conventional APS and the proposed ICAPS were integrated on the same chip for the fair performance comparison. The control of both approaches is identical. Each image array has 160 $\times$ 240 pixels of 5.6 μm $\times$ 5.6 μm four-transistor pixel with a pinned PD [22]. The pixel layouts of the conventional APS and the proposed ICAPS are also shown in Fig. 8. The pixel fill factor of the ICAPS is 1% lower than that of the conventional APS due to the additional column line.

Fig. 9 shows the measured photoelectric conversion characteristics from the fabricated chip. The proposed ICAPS shows a 26% increased sensitivity and a 15-times improved linearity.

The measured FD referred noise is shown in Fig. 10. At low illumination, the FD referred noise of the ICAPS is 33% lower than the conventional one. At high illumination, the noise performances of the conventional APS and the ICAPS are almost the same because the photon shot noise in the PD is dominant.

The sample image taken by the prototype sensor is shown in Fig. 11. The image from the (left side) ICAPS is brighter than that from the (right side) conventional APS due to the sensitivity improvement. The performances of the conventional APS and the ICAPS are compared and summarized in Table I.

V. Conclusion

A low-noise APS with an in-pixel comparing scheme was proposed. The proposed ICAPS uses pixel transistors as a part of the comparator for a single-slope ADC instead of using them as an SF. The prototype sensor was fabricated using a 0.35-μm 2P3M CMOS process and achieved 26% sensitivity

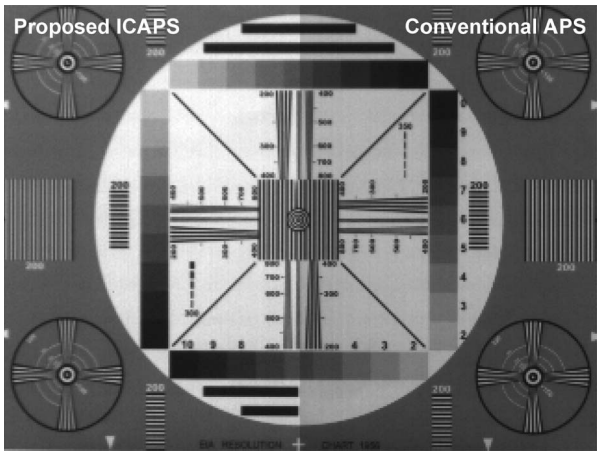


Fig. 11. Sample image from the fabricated sensor.

TABLE I
PERFORMANCE SUMMARY

	Conventional APS	Proposed ICAPS
Process	0.35-μm 2P3M CMOS	
Power supply	3.3 V (Analog) / 1.5 V (Digital)	
ADC	Column-level 10-bit single-slope ADC	
Array format	160 (H) × 240 (V)	
Pixel size	5.6 μm × 5.6 μm	
Full well capacity	20,000e-	
Conversion gain	48 μV/e-	
Fill factor	33%	32%
Sensitivity	0.35 V/lx·s	0.44 V/lx·s
Dynamic range	64.5 dB	68 dB
Nonlinearity	± 0.88%	± 0.05%
FD referred noise at dark	576 μV_{rms}	384 μV_{rms}
Column FPN at 50 lx	0.68%	0.52%
Analog Power consumption	16 μW/column	9 μW/column
Digital Power consumption	4 μW/column	4 μW/column

enhancement, 15-times linearity improvement, and 33% noise reduction compared to the conventional APS. The proposed ICAPS can be applied to mobile consumer electronic image sensor with enhanced image quality at low illumination.

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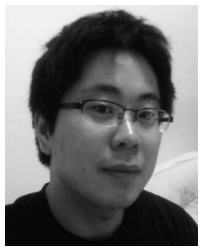

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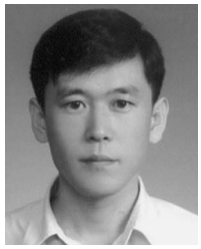

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