Analog Integr Circ Sig Process (2013) 77:29–44
DOI 10.1007/s10470-013-0116-9

A readout IC for an uncooled microbolometer infrared FPA with on-chip self-heating compensation in 0.35 μm CMOS

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Received: 15 February 2013 / Revised: 12 July 2013 / Accepted: 29 July 2013 / Published online: 17 August 2013

Abstract This paper describes a readout integrated circuit architecture for an infrared focal plane array intended for infrared network-attached video cameras in surveillance applications. The focal plane array consists of 352 × 288 uncooled thin-film microbolometer detectors with a pitch of 25 μm, enabling ambient temperature operation. The circuit features a low-noise readout path, detector resistance mismatch correction and a non-linear ramped current pulse scheme for the electrical biasing of the detectors in order to relax the dynamic range requirement of amplifiers and the ADC in the readout channel, imposed by detector process variation and self-heating during readout. The design is implemented in a 0.35-μm standard CMOS process and two versions of a smaller 32 × 32-pixel test chip have been fabricated and measured for evaluation. The latest test chip achieves a dynamic range of 97 dB and an input-referred RMS noise voltage of 6.4 μV yielding an estimated NETD value of 26 mK with *f*/1 optics. At a frame rate of 60 FPS the chip dissipates 170 mW of power from a 3.4 V supply.

Keywords Readout integrated circuit · Uncooled microbolometer · Infrared imaging · High-resolution data conversion · Self-heating compensation · Bias heating compensation

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1 Introduction

Thermal infrared imaging has received much research attention in recent time. It has several applications within different industries, particularly in military, automotive, process and security/surveillance industries. While IR imaging has been available for a long time, it has been in the form of large, bulky photon detector systems in the need for active cooling of the infrared detectors in order to operate properly. This fact has made such imaging systems expensive and of little use in many application areas. With the advent of the thin-film microbolometer detector [1–3], the requirement of cooling the detectors to achieve high performance was removed and this opened up the opportunity to create less expensive and smaller systems operating without cooling while having good enough performance for all but the most extreme applications [4].

In this paper a readout integrated circuit (ROIC) architecture for a 352 × 288-pixel infrared focal plane array (IRFPA) using microbolometers with a pitch of 25 μm is presented. The design is aimed toward a network-attached infrared video camera for use in visual surveillance applications, where infrared imaging can help in conditions where normal imaging would be limited, such as in low light, total darkness, fog or where an object is masked visually but not thermally by another object. This application requires the system to function in ambient temperatures ranging from −10 to 70 °C, which imposes very strict requirements on the electrical biasing of the microbolometer detectors.

The focus of the paper is on the biasing of the detectors to relax the required dynamic range of the ROIC due to process variation and self-heating; and on the low-noise readout channel used to digitize the detector output signals. A well designed scheme for biasing of the microbolometer

detectors is important to remove unwanted signal components due to detector self-heating and process variation. Several such biasing circuits have been reported in literature [5–9], however they focus more on non-uniformity correction than on self-heating compensation.

One common biasing circuit connects the microbolometer in a bridge configuration with a reference bolometer that is fabricated to be blind to the incident infrared radiation and thermally connected to the substrate. The signal is read out by keeping the voltage over the bolometers constant and integrating the signal current with a capacitive transimpedance amplifier (CTIA) [5–7]. In most cases this reference detector is common for one whole column (or row) of pixels and will suffer from mismatch with the other detectors. This static mismatch is normally compensated by changing the voltage levels over the detectors when selecting a new row, however the current from the self-heating is not cancelled and will be directly integrated by the CTIA and will increase the dynamic range requirement on the succeeding readout circuitry. Alternatively, it will limit the useful range of bolometer bias level, which decreases the performance.

Other works use a differential readout structure [8, 9], where the reference and normal detectors are biased separately with constant currents and are integrated and read out differentially with a CTIA to cancel the common signal. Here too the reference detectors are common to a whole column (or row) and will suffer from mismatch. This is usually compensated by changing the bias currents of the detectors. This will cancel the average offset due to the mismatch during the pulse bias period, but the mismatch causes the two self-heating responses to not cancel completely anymore. This will leave a dynamic mismatch component that will put a higher dynamic range requirement on the readout circuitry. Because of the constant current biasing, the self-heating will cause the voltages over the bolometers to decrease and reduce their responsivity. Moreover, the residual self-heating also leads to fixed pattern noise as the temperature drifts.

The ROIC in this paper uses a ramping current source to bias each bolometer such that it experiences a constant voltage. This scheme enables compensation of both static and dynamic mismatch caused by process variations in detector resistances and self-heating to reduce the dynamic range required in the readout circuitry.

The paper is organized as follows: in Sect. 2 the uncooled resistive microbolometer is introduced and design considerations with regard to dynamic range and noise are described. Section 3 introduces the overall architecture of the system with particular attention given to the bolometer biasing scheme and to the readout channel. Measurement results are presented in Sect. 4 and the paper is concluded in Sect. 5.

2 Uncooled resistive microbolometers

The microbolometer is the core of uncooled IRFPA imaging systems. It is fabricated in micro electromechanical system (MEMS) processes that can later be attached to standard CMOS process wafers to complete an integrated solution with both detectors and electronics on a single chip.

The bolometer is made up of a thermistor material, such as amorphous silicon, silicon–germanium or vanadium oxide [10], that changes resistance in relation to the incident infrared radiation. This material is coated on the top side with an absorbing layer and on the bottom with a reflective layer to maximize the absorbed energy. The bolometer is electrically interfaced with the CMOS chip surface by means of two metal legs that are contacted to each side of the bolometer, see Fig. 1. The metal legs support the bolometer detector above the chip surface and provide thermal isolation from the chip as they are made relatively long and thin to reduce thermal conduction. For optimal thermal isolation, the microbolometer must be operated in a vacuum, thus vacuum packaging is used in most infrared imaging detectors.

An important property of the microbolometer is its ability to change resistance according to a change in its temperature, given by the thermal coefficient of resistance (TCR) of the detector material. Given that the incident infrared radiation to a single detector only changes its temperature with a few millikelvin for a change of one kelvin in the observed object [10], a high TCR is necessary to produce a detectable signal response when scene temperature differences are in the range of a few tens of millikelvin. Current research shows TCRs of infrared microbolometers of –2 to –4 %/K [11, 12].

When designing an ROIC for uncooled microbolometers and targeting a performance that is limited by the thermal noise of the bolometers, the dynamic range requirement of

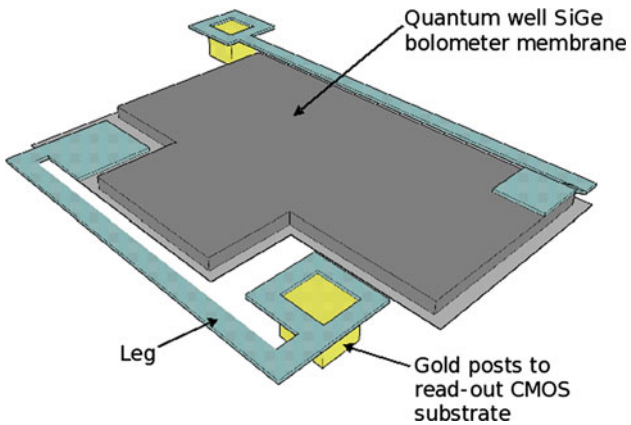


Fig. 1 Example of the structure of an infrared microbolometer

the ROIC becomes a great challenge. The main limiting factors of the dynamic range are the bolometer resistance spread created during manufacturing, the self-heating of the bolometers that occurs during readout, the actual wanted signal and the bolometer noise.

Moreover, flicker noise is an important parameter due to the low signal frequencies as well as the eyes' sensitivity to patterns generated by it. Since the flicker noise is relatively high in a CMOS process, this is something that needs to be addressed in an ROIC.

2.1 Bolometer static mismatch

Just as with resistors in any process, the bolometer resistance will be subject to process variations. During initial development of the bolometers, a resistance spread of up to ± 10 % has been estimated possible. This number is expected to drop as the process matures, but the ROIC must be able to handle 20 % mismatch to be usable during development.

2.2 Self-heating

The resistance of a microbolometer can be measured by biasing it with a current and measuring the voltage drop over it. The bias current in itself will cause it to warm up and, because of the high negative TCR of the bolometer, its resistance will drop. To achieve a sensitive imaging sensor, a low bolometer resistance is desired for a low thermal noise while a high bias voltage is desired for high responsiveness. This causes a high bias power and hence large self-heating during readout.

The change in temperature due to the self-heating depends on the applied biasing energy and the thermal capacity of the bolometer membrane and can be estimated for small variations by the following linearized Eq. [13]:

$$\Delta T \approx \frac{V_{bias}^2 \cdot t_{bias}}{R_{bol} \cdot C_{th,bol}}, \tag{1}$$

where V_{bias} is the applied bias voltage, t_{bias} is the biasing time, R_{bol} is the average bolometer resistance during biasing and $C_{th,bol}$ is the thermal capacity of the bolometer.

A specification of handling self-heating up to 10 K was set to enable good performance. Assuming a reasonable bolometer TCR of -2.6 %/K, the resulting resistance change is then as much as $\Delta R = \Delta T \cdot |TCR| = 26\,\%$.

2.3 Bolometer nominal resistance

The highest bolometer resistance is set by the settling time constant of the bolometer in parallel with the parasitic capacitance from the column bus ($\sim$17 pF) when a new row is selected. If for a desired frame rate of 60 FPS with 352 active rows, the row readout time is 47.3 µs. Allowing 13 % (6.1 µs) of this time for settling and constraining the time constant of the bolometer selection to this, gives an upper limitation on the resistance of $\sim 360\,\text{k}\Omega$. Increasing the resistance further will result in successively reduced performance due to the slow settling that restricts signal build-up and results in lower signal-to-noise ratio. Moreover, high resistance values are undesirable because of the increased thermal noise of the microbolometer.

On the other end of the spectrum, the lowest possible bolometer resistance is mainly determined by the self-heating. The biasing scheme in this paper is based on trying to keep the voltage over the bolometer at a constant level for all effects except incident radiation, meaning that as the bolometer warms up and the resistance drops, more current is sourced into it in a feed-forward loop. The limit is then set by how low this bias voltage can be allowed to be. For this design the bias voltage can be adjusted down to 1.2 V which still gives a reasonable response, but can be adjusted up to 2.14 V on the other end. From (1) this gives a lower bound on the average resistance of $\sim 14\,\text{k}\Omega$, assuming a thermal capacity of $4.3 \times 10^{-10}\,\text{J}/K$ (see Table 1).

For large changes in temperature the relation between the bolometer resistance and its temperature is [13]:

$$R_{bol}(T_{bol}) = R_0 \cdot e^{-TCR \cdot T_0^2 \left(\frac{1}{T_{bol}} - \frac{1}{T_0}\right)} \tag{2}$$

where R_0 is the bolometer resistance at the nominal temperature T_0. The specification says that the readout should work at ambient temperatures up to 70 °C. Including an average 5 K self-heating increase and a mismatch of -10 %, a nominal resistance of 80 kΩ would according to (2) become $\sim 20\,\text{k}\Omega$ at a TCR of -3 %/K. This gives a margin to the minimum resistance and allows operation within the specified ambient temperature range of -10 to 70 °C with a TCR as large as -3 %/K.

2.4 Thermal noise floor

The smallest detectable signal will be determined by the system noise. Here, only the thermal noise of the bolometer itself is considered while its flicker and thermal fluctuation noise is neglected. The total input-referred system electrical noise power can be modeled as the sum of the noise powers of the bolometer resistance, the biasing circuitry as well as the input-referred noise power of the readout channel and the reference generation:

$$\overline{v_{n,tot}^2} = \overline{v_{n,bol}^2} + \overline{v_{n,bias}^2} + \overline{v_{n,roic}^2}. \tag{3}$$

The first term in (3) is set when choosing the size of the bolometer resistance. As will be described in Sect. 3.1 the bolometer bias circuitry will add noise equal to half of the

noise power of the bolometer resistance. The rest of the noise is due to the readout channel and reference generation. Normalized to the bolometer noise, this gives the following relation of the total system electrical noise voltage:

$$\frac{\overline{v_{n,tot}}}{\overline{v_{n,bol}}} = \sqrt{1 + 0.5 + \left(\frac{\overline{v_{n,roic}}}{\overline{v_{n,bol}}}\right)^2}. \quad (4)$$

The relation in (4) shows that the contribution of the ROIC noise to the total noise is non-linear and at some point, further reduction of the total noise does not motivate the cost of reducing the ROIC noise due to the increased power consumption. A total noise voltage of 1.6 times the noise voltage of the bolometer was chosen to have low noise but also reasonable power requirements, but no attempt was made to find the absolute best power-noise trade-off. With a total noise of 1.6 times the bolometer noise, the ROIC noise contribution would according to (4) have to be limited to 1.03 times the bolometer noise.

The thermal noise voltage of the nominal bolometer resistance of 80 kΩ at the nominal temperature of 25 °C and an integration time of $t_{int} = 41.2$ µs can be calculated to be $\overline{v_{n,bol}} = \sqrt{4kTR_{bol}/(2t_{int})} = 4.0\,\mu\text{V}$, where the equivalent noise bandwidth, $1/(2t_{int})$, is derived from a rectangular pulse of length t_{int}. The integration time is taken as 87 % of row time and leaves the initial 13 % for row switching and settling. The total system electrical noise is then $\overline{v_{n,tot}} = 1.6 \cdot \overline{v_{n,bol}} = 6.4\,\mu\text{V}$ and the ROIC is allowed to add $\overline{v_{n,roic}} = 1.03 \cdot \overline{v_{n,bol}} = 4.12\,\mu\text{V}$.

2.5 Noise equivalent temperature difference

An important measure of the performance of an infrared imaging system is its noise equivalent temperature difference (NETD). It quantifies the minimum detectable temperature change in the scene and can be calculated using the following Eqs. [14, 15]:

$$\text{NETD} = \frac{4 \cdot F^2 \cdot \overline{v_{n,sys}}}{\beta \cdot A_b \cdot R_V \cdot \phi_{\Delta\lambda} \cdot \left(\frac{\Delta P}{\Delta T}\right)_{\Delta\lambda}} \quad \text{and} \quad (5)$$

$$R_V = \frac{|TCR| \cdot \varepsilon_{\Delta\lambda} \cdot V_b}{\sqrt{G^2 + \omega^2 \cdot C_{th}^2}}, \quad (6)$$

where F is the f-number of the infrared optics, $\overline{v_{n,sys}}$ is the total system noise voltage, β is the bolometer fill factor, A_b is the nominal bolometer area (usually the square of the pixel pitch), R_V is the detector responsivity, $\phi_{\Delta\lambda}$ is the transmission of the infrared optics in the wavelength interval $\Delta\lambda$, $(\Delta P/\Delta T)_{\Delta\lambda}$ is the change in power per unit area with respect to the temperature change radiated by a blackbody in the wavelength interval $\Delta\lambda$ at a temperature of 300 K, TCR is the temperature coefficient of resistance for the bolometer material, $\varepsilon_{\Delta\lambda}$ is the absorption of the bolometer membrane in the wavelength interval $\Delta\lambda$, V_b is the detector biasing voltage, G is the total thermal conduction between the bolometer and its surroundings, ω is the infrared modulation frequency and C_{th} is the thermal capacity of the bolometer membrane.

Table 1 Parameter values for NETD performance estimation

Parameter	Value	
F	1	
β	62 %	[15]
A_b	6.25×10^{-10} m^2	
$\phi_{8-14\ \mu m}$	98 %	[15]
$\left(\frac{\Delta P}{\Delta T}\right)_{8-14\ \mu m}$	2.624 W/(K m^2)	[14]
TCR	−2.6 %/K	
$\varepsilon_{8-14\ \mu m}$	92 %	[15]
V_b	1.6 V	
G	3.7×10^{-8} W/K	[15]
C_{th}	4.34×10^{-10} J/K	[15]

As (5) and (6) show, the NETD is highly dependent on the bolometer material and its processing as well as the infrared optics. At the moment of writing, the values of these parameters have yet to be finalized for the intended bolometer process. Instead, typical values of these parameters given in [15] have been used and are listed in Table 1 for reference. When estimating the NETD for the 6.4 µV of total system electrical noise derived in Sect. 2.4, it is important to also consider the RMS noise voltage resulting from the thermal fluctuation noise of the bolometer, given by [14]

$$\overline{v_{n,th}} = |TCR| \cdot V_b \cdot \sqrt{\frac{k \cdot T_{bol}^2}{C_{th}}}, \quad (7)$$

where k is the Boltzmann constant and T_{bol} is the bolometer temperature. At 25 °C the noise voltage due to the thermal fluctuation noise is 2.2 µV giving a total system noise of 6.8 µV. At low frequencies the resulting NETD can then be estimated to 26 mK at a bias level of 1.6 V and with f/1 optics. State-of-the-art NETD figures for pixel pitches of <50 µm ranges from 30 to 100 mK [10, 6], showing that this is indeed a competitive value.

2.6 Dynamic range requirement

The dynamic range requirement of the ROIC is found by relating the largest relative change of bolometer resistance that will occur to the smallest relative resistance change that needs to be detected. The relative resistance change of a bolometer detector $\left(\frac{\Delta R_{bol}}{R_{bol}}\right)$ due to a change in scene

temperature (ΔT_{scene}) can be estimated by the following equation derived from (5) and (6):

$$\frac{\Delta R_{bol}}{R_{bol}} = TCR \cdot \frac{\beta \cdot A_b}{G} \cdot \frac{\phi_{\Delta\lambda} \cdot \varepsilon_{\Delta\lambda} \cdot \left(\frac{\Delta P}{\Delta T}\right)_{\Delta\lambda}}{4 \cdot F^2} \cdot \Delta T_{scene}. \quad (8)$$

For a desired relative temperature dynamic range in the scene of 100 K, the maximum relative resistance change due to the signal can be estimated from (8) with parameter values from Table 1 to $\sim$1.6 %. This change in resistance is an order of magnitude lower than that of self-heating and the initially stated bolometer static mismatch. Together these all add up to a relative resistance change of 47.6 %.

Similarly, a system noise level corresponding to an NETD of 26 mK can be estimated to produce a relative resistance change of $\sim$4.2 ppm. Relating this value to the 47.6 % of the signal, self-heating and mismatch yields a dynamic range of $\sim$113,000 or 101 dB. While an ideal, noise-less 17-bit ADC would give the desired dynamic range, in reality additional resolution would be required to suppress the quantization noise enough to allow most of the noise to come from the amplifiers and bias sources. Such high dynamic range—of 18 bits or more—is very difficult to realize in ADCs with high enough throughput while maintaining the capability of time multiplexing the signal sources required for column-parallel readout.

2.7 Flicker noise

Due to the slowly changing infrared signals and the eyes' sensitivity to spatial noise, low-frequency flicker noise must be considered and minimized when designing the ROIC, both in the biasing of the bolometers and in the analog readout channel itself. A too large flicker noise in the ROIC will show up in the image as vertical or horizontal lines, depending on from where it originates, and will degrade the visual quality of the image. Simulations have shown that a flicker noise corner frequency of $\sim$40 Hz is needed to make the visual artifacts from flicker noise insignificant compared to the thermal noise.

3 System architecture

Figure 2 shows the overall architecture of the system. It consists of an FPA of infrared bolometers; circuitry for column-wise biasing of the bolometers; a programmable ramped current pulse bias generation circuit; row selection logic; column readout channels including amplification and digitization; reference voltage and bias current generation circuitry; programmable control logic; and a serial LVDS interface for programming of the chip as well as for output of the read out signals.

For this design, a column-parallel, row-by-row readout of the bolometers was chosen because it offers a good compromise between large parallelism and silicon area. Large parallelism is desirable because it allows longer readout times and thus reduces the noise bandwidth, which in turn allows use of bolometers with higher resistance. Higher resistance bolometers proves advantageous since the effects of noisy parasitic contact resistances in the bolometers are reduced, which relaxes the requirements on transconductance and bandwidth in the readout electronics. However, large parallelism—such as pixel-parallel readout—means that the readout circuit occupies a much greater area and may be difficult to fit in connection with the bolometer array. Exceptions to this exist [16], but performance may be limited by the amount of area available per readout channel—particularly when the pixel pitch is shrinking toward sub-20-μm as state-of-the-art suggests [6]. The column-parallel approach balances these trade-offs in a very regular and practical structure.

The IRFPA consists of 352 × 288 normal bolometers and four columns, two on either side of the array, and two rows, one at the top and one at the bottom, of blind bolometers. These blind bolometers are thermally isolated from the substrate, just as the normal bolometers are, however they are coated with a reflective layer shielding them from the incident infrared radiation. Their resistances can be read out to serve as a reference for the calibration and correction system since they experience the same response as the normal bolometers with respect to ambient temperature changes and self-heating, however they remain largely unaffected by the radiation from the scene.

A conceptual schematic of the bolometer readout is shown in Fig. 3. During readout, the bolometer rows are switched in one after another to a column-wise current bias bus. All columns are then read out by parallel readout channels consisting of preamplifiers and A/D converters. The readout is done through a second bus, separate from the bias bus. The biasing and the readout are separated into two different buses to minimize the flicker noise contribution of the switch transistors. The flicker noise of a MOS transistor is proportional to the amount of current flow through it. The switch transistors for the bias bus carry a large current, however because they are in series with the large impedance of the current source, their flicker noise has a very small effect on the bias current. The switch transistors for the readout bus, on the other hand, carry only the small load current from the readout channel. This current is much smaller than the bias current and hence the flicker noise from these switches is much smaller than it would be if the bias and readout would have been on the same bus.

The time for readout of a row is determined by the frame rate and the number of rows. For an array of 352 rows with

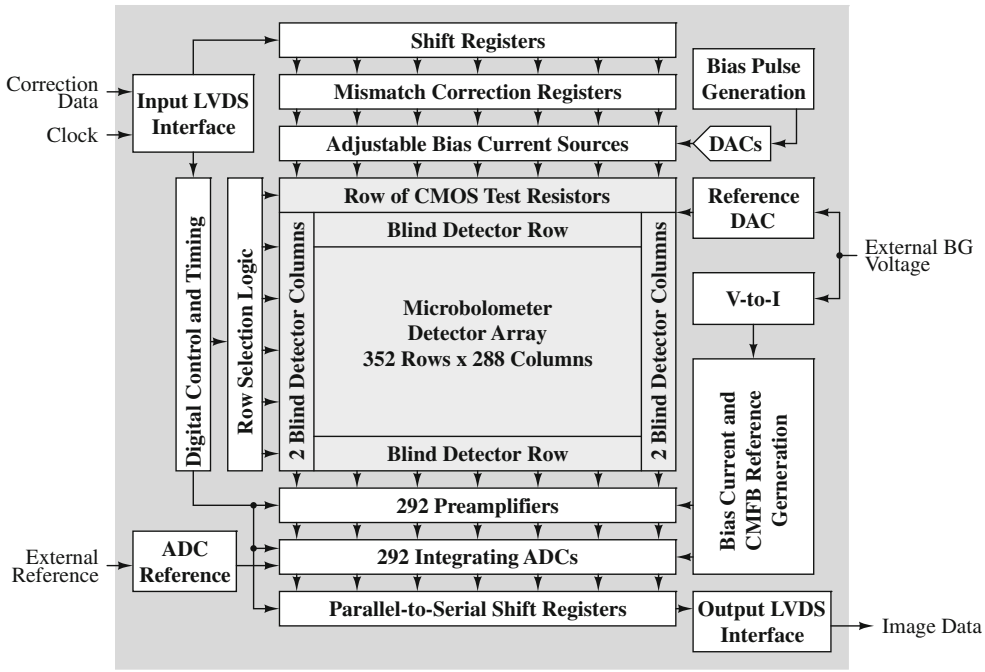


Fig. 2 General system architecture of the ROIC

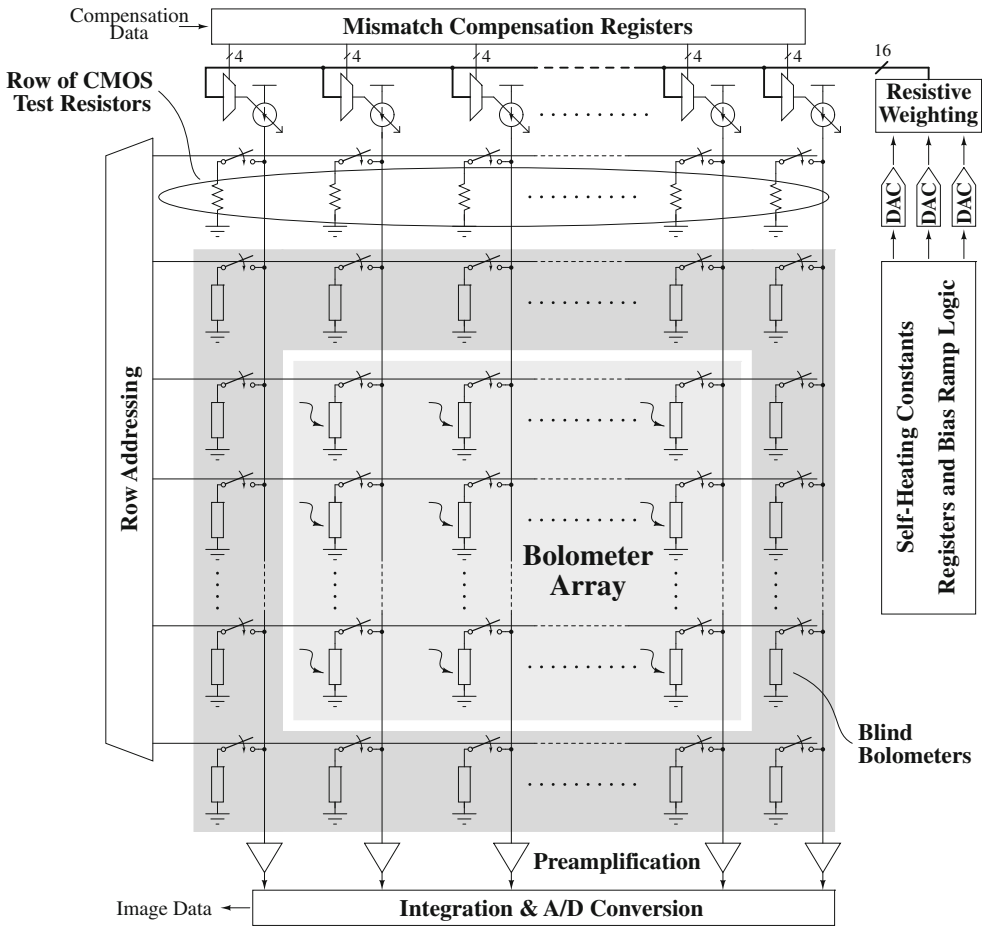


Fig. 3 Simplified bolometer readout and biasing scheme. Each column has a programmable current source whose value is controlled by a digital ramping circuit followed by DACs and interpolation

a frame rate of 60 FPS, this leaves 47.3 μs for readout. Due to the multiplexing of different rows on the same bus, this time also needs to include an initial delay before the start of integration to ensure that any switching transients have died out and a proper signal level is achieved. The length of this initial delay can be programmed.

3.1 Bolometer biasing

As described in Sect. 2.2, the self-heating of the bolometer detector causes its resistance to drop because of its negative TCR. This drop may be an order of magnitude larger than the detector resistance change due to the incident radiation and therefore puts a stricter requirement on the dynamic range of the succeeding analog readout circuitry. In order to relax this requirement, the voltage drop across the detectors caused by the self-heating must be minimized during the readout period. This is accomplished by using ramped current pulse biasing of the bolometers [13]. As shown in Fig. 4, the bias current is successively increased as the bolometer resistance decreases from the self-heating during the readout. When the readout period is finished, the bias current source will be switched to the next detector and the recently read out detector is left to cool off for the remainder of the frame cycle.

The results of a high-level simulation of the biasing current required for a constant voltage over the bolometer during the readout period, for mismatch levels of −10, −5, 0, 5 and 10 %, is shown in Fig. 5. The simulation was performed for a bolometer with a nominal resistance of 80 kΩ and a TCR of −2.6 %/K at an ambient temperature of 70 °C, with the bolometer parameters listed in Table 1. The figure clearly shows that the current required for constant voltage bias is not linear with respect to the mismatch.

The exact shape of the current pulse needs to be tunable in order to fit the response of the bolometer detectors. Because of static mismatch in resistance of the bolometers, this means that the pulse has to be individually tailored for each detector. This is accomplished by digitally synthesizing three different ramp shapes; converting them into

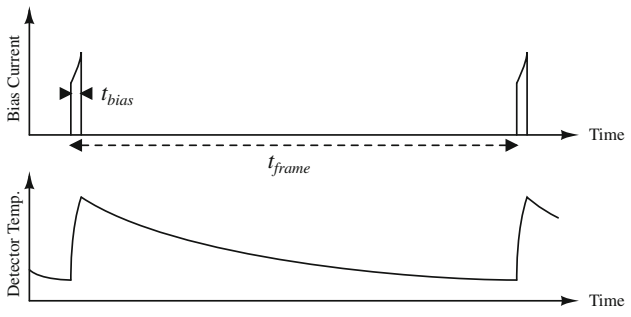


Fig. 4 Detector biasing waveform (*top*) and detector temperature response to the biasing (*bottom*). Figures not to scale

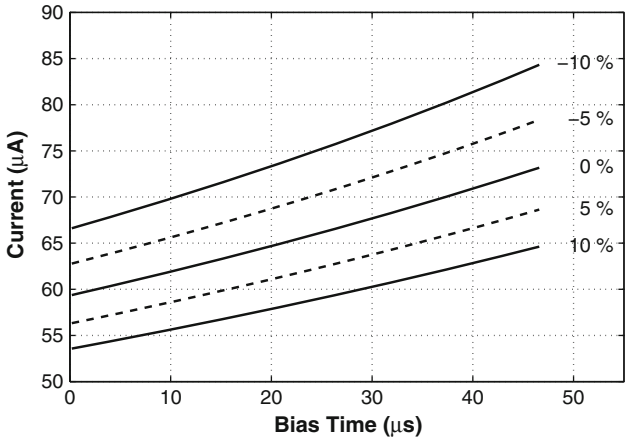


Fig. 5 Simulation of the bias current required to keep the voltage over the bolometer constant during readout, for mismatch levels of −10, −5, 0, 5 and 10 %. This shows a non-linear relationship between self-heating and resistance mismatch

analog voltages; and interpolating between them to generate 16 different bias voltages as shown in Fig. 6. Any of these 16 voltages can then be selected to drive the current source that bias each column by means of a 4-bit correction word that is individually specified for each bolometer in the array.

System-level simulations have shown that by using this bias method, the effects from static mismatch and self-heating are reduced by a factor of 16 and 96, respectively. The dynamic range requirement derived in Sect. 2.6 is thus reduced to ∼7,500 or 77 dB, i.e. 13 bits, for the succeeding amplifiers and ADC. An ADC resolution of 16 bits would then give enough margin to make the quantization noise an insignificant noise contributor; and is also feasible to implement in a column-parallel readout circuit.

Although the relative effect of the static mismatch and self-heating is on the same order (20 and 26 %, respectively) the reduction through this compensation scheme is significantly different (6 times). The reason for this differentiation is that while the mismatch is constant over ROIC temperature changes, the self-heating is not. By having a strong suppression of the self-heating, a more stable response over large changes in ambient temperature is ensured, which reduces the rate at which the shutter must be operated with to suppress fixed pattern noise. Moreover, as the detector process matures, the mismatch is expected to decrease causing less impact on the dynamic range. Also, should the process improve to produce bolometers with higher TCR, then the self-heating would have an even more pronounced effect as seen in Sect. 2.2. Increasing the correction of the mismatch also costs more than the self-heating in terms of circuit complexity and size, particularly in the bias current source and its control voltage generation, that grow exponentially with the added correction resolution.

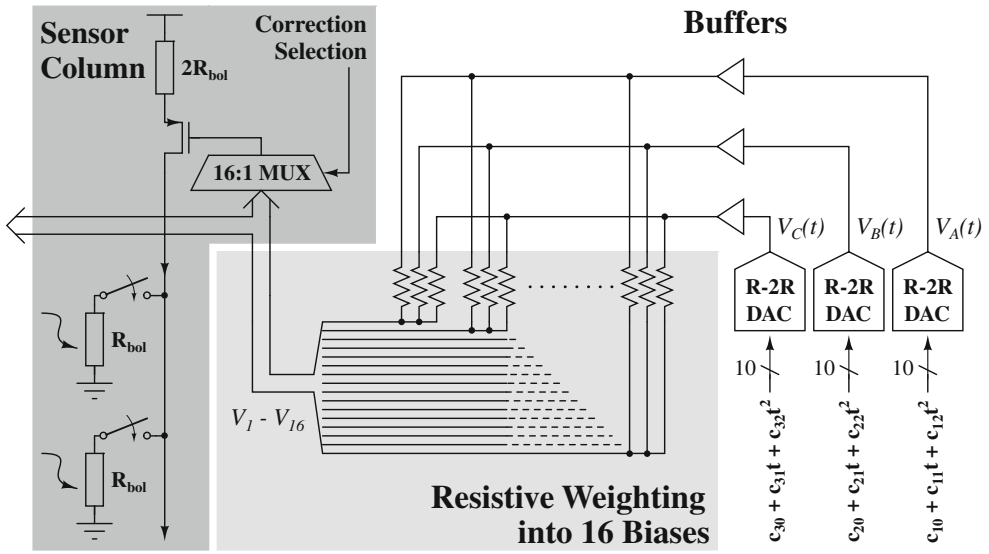


Fig. 6 Bolometer bias current source control. Three ramps are D/A converted and weighted together to form 16 different bias voltages that can be selected individually for each bolometer in the array to drive its bias current source

3.1.1 Circuit implementation

The bias current source is implemented by a source-degenerated PMOS current source as shown in Fig. 7. The noise performance of this current source is very important since any noise from it will show up at the input of the readout circuit. It is readily shown that the power spectral density of the thermal noise voltage over the bolometer in Fig. 7 is

$$\overline{v_{n,bol}^2} = 4kTR_{bol}\left[1 + \frac{R_{bol}}{R_s}\left(1 + \frac{\overline{v_{n,bias}^2}}{4kTR_s}\right)\right], \tag{9}$$

where R_{bol} is the bolometer resistance, R_s is the source degeneration resistance and $\overline{v_{n,bias}^2}$ is the noise voltage at the gate of the transistor; assuming $g_m R_s \gg 1$ and that R_s is lower than the transistor output impedance. From (9) it is clear that the source degeneration resistance should be larger than the detector resistance in order for the current source not to dominate the noise. In this design, the source resistance was set to twice the size of the detector resistance to reduce the noise contribution while keeping the voltage drop over the source resistance manageable. The resistance itself is made up of eight blind bolometers connected serially and in parallel (left side of Fig. 7) to reduce its flicker noise contribution and increase absolute matching by increasing the resistor area.

These blind bolometers are different from the ones attached to the detector array described previously, in that, in addition to the reflective coating, they are also thermally connected to the substrate. This thermal connection greatly reduces their self-heating response to the bias current and thus they only change resistance with the ambient

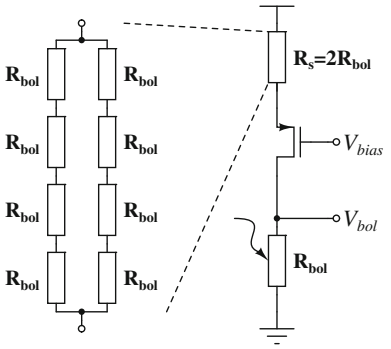


Fig. 7 Source degenerated PMOS current source. The degeneration resistance is made up of eight blind microbolometer detectors for ambient temperature response matching

temperature. A thermally isolated blind bolometer would suffer from severe self-heating in this position due to its constant biasing and thus cannot be used for this purpose. By using the thermally connected type of blind bolometer in the current source, the matching between the current source and detector is maintained over changes in ambient temperature, thus eliminating the need to switch in or out resistances for calibration, as would be the case if using normal resistors.

The high resistance of the source degeneration resistor causes a large voltage drop over it and thus reduces headroom for the transistor. To be able to have an acceptable voltage over the detector (1−2 V) for good responsivity, the current source needs to be connected to a higher supply voltage than the rest of the circuit. This voltage is generated by a DAC and can be changed from 5.8 to 9 V in steps of 100 mV. Currently, the DAC is located off-chip, but it is planned to be included on-chip in a future version of the

chip. Despite the use of this higher supply voltage, a standard 0.35 μm process was used. Only passive devices are connected to this high voltage, and the voltages over the active devices are well within the limits of the standard 3.3 V devices. However, mid-oxide 5 V devices were used in the ESD protection of the high-voltage supply pads.

The generation of the gate voltage of the current source must also be designed for low noise. The straightforward solution to generate this voltage would be through a PMOS current mirror that is driven by an NMOS current DAC, as this would give a simple current-to-current correspondence. However, to meet the low-noise requirement, the DAC would have to occupy a prohibitively large area due to the poor flicker noise performance of the transistors. Instead, the solution with R-2R DACs and resistive weighting in Fig. 6 was used in this design.

Because of the non-linear nature of the self-heating, all three digitally generated pulses have the possibility to include a constant, a linear and a square term on the form

$$V_i(t) = c_{i0} + c_{i1} \cdot t + c_{i2} \cdot t^2, \tag{10}$$

where i is the number of the DAC and coefficients c_{ij} can be programmed independently for each DAC. The logic for generating the digital input codes for each of the DACs are shown in Fig. 8 and it also shows the word lengths of the DC, linear and square coefficients in (10).

While the self-heating equation has higher order non-linear components, a second-order polynomial approximation was chosen as a compromise between implementation complexity and compensation accuracy. The three pulse voltages, $V_A(t) - V_C(t)$ in Fig. 6, are then buffered and weighted into the 16 combinations that are used for the bolometer resistance mismatch correction, $V_1 - V_{16}$. The weighting is such that it allows for correction of non-linear relationship between the mismatch and the self-heating. The weights are given by the following relation:

$$\begin{aligned} V_k(t) = &\left(1 - \frac{k-1}{15}\right) \cdot V_A(t) \\ &+ \left(\frac{k-1}{15} - \frac{(k-1)^2}{225}\right) \cdot V_B(t) \\ &+ \left(\frac{(k-1)^2}{225}\right) \cdot V_C(t) \quad \text{for} \quad k = 1 \ldots 16, \end{aligned} \tag{11}$$

where $V_A(t)$ is the best bias voltage for bolometers with the highest resistance due to mismatch; $V_C(t)$ is the best bias voltage for bolometers with the lowest resistance due to mismatch; and $V_B(t)$ is an additional voltage without the square mismatch term to make it possible to realize a non-linear response for $V_k(t)$ with respect to k.

The coefficients and correction codes are programmed from outside the chip, allowing for digital signal processing to be used to adapt the response of the detectors to the current operating conditions on-the-fly, using the columns of blind bolometers on either side of the array as references.

3.2 Analog readout channel

Digitization of the detector signals in each column can be done either serially or in parallel. In the serial approach, only one ADC is needed to convert all channels. This has the benefit that the conversion exhibits the same response for all channels. Moreover, this also makes it feasible to use digital non-linearity correction techniques for the ADC and it saves area for large arrays. However, the required throughput is proportional to the number of pixels in the design and is significantly increased compared to a parallel scheme, which together with the strict dynamic range requirement make the slower, inherently linear class of converters unsuitable. The higher speed also increases the requirements on the analog multiplexing of the channels and makes it difficult to scale the design to larger arrays. In contrast, the parallel approach—used in this design—reduces the required throughput to be proportional to the number of rows. This makes it possible to use inherently linear converters and have signal integration inside the ADC. Furthermore, the analog multiplexing of channels is removed and this scheme scales better to higher resolution image formats. However, the larger number of converters makes it very difficult to implement individual digital non-linearity correction for them and the converter response will differ between channels.

Due to the time-multiplexed nature of the readout scheme, normal delta-sigma modulators can not be used because of their lack of one-to-one correspondence between input and output samples. Integrating converters can realize high resolution while being inherently linear and compact, however they require 2^N clock cycles for the conversion and at this resolution, array size and frame rate, the sample rate would have to be prohibitively high: over 1 GHz. Similarly, an incremental delta-sigma ADC of the first order also needs 2^N clock cycles. Higher order converters relax this requirement, however they require several OTAs and more complex decimation filters that occupy more area, which makes them difficult to fit in a massively parallel readout architecture with a small pitch. Moreover, higher order modulators are less effective at integrating the noise due to uneven weighting of the input samples over the readout period.

By using an extended counting ADC with a first order modulator, the decimation filter can be a simple counter and the counting conversion phase needs 2^{N-M} clock cycles, where M is the number of bits in the extended conversion phase. In this design, the 16-bit resolution is split equally

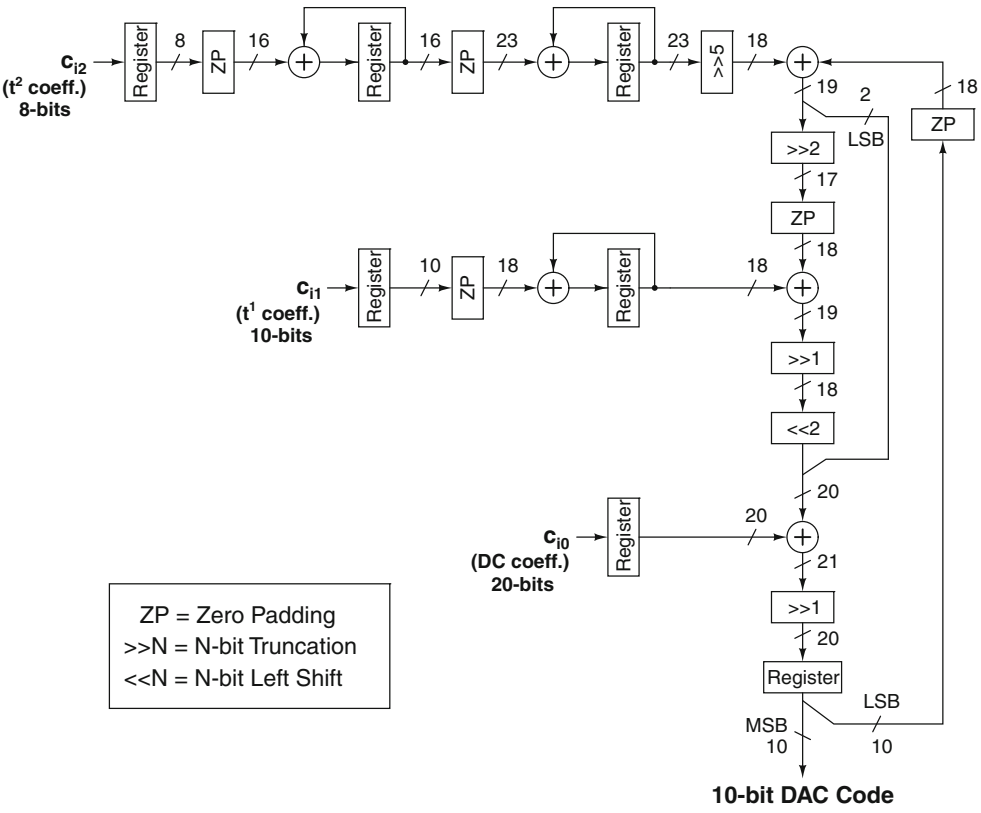
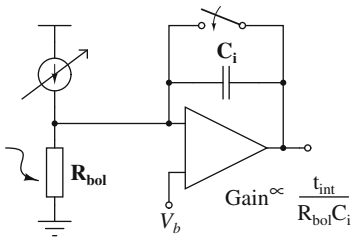


Fig. 8 Digital logic circuitry for generating the input code for each of the DACs that are used to the bias current ramps. The arithmetic is unsigned and the digital word lengths are specified for each part of the generation

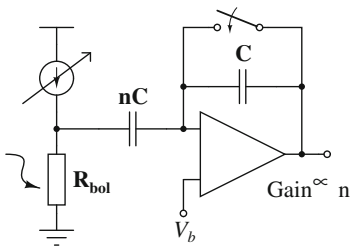
between the two phases; eight bits in the counting phase, and nine bits with one bit redundancy in the extended phase. The total number of required clock cycles, including one for resetting the modulator, is thus 266. The ADC is similar to that in [17], with an in-loop successive approximation converter for the extended phase, but modified for differential operation and with a different switching scheme giving improved performance. The reference voltages to the single-bit DACs in the feedback path are generated by a charge redistribution DAC that is common for all channels, thereby reducing the area required for each channel.

The CTIA shown in Fig. 9(a) is a commonly used circuit for interfacing the bolometer to the ADC in integrated circuits [6, 5, 8]. Since the bolometer is connected directly to the input of the OTA, the voltage over the detector is easily controlled. However, the circuit performs a continuous-time integration of the detector current and, as seen in Fig. 9(a), the gain of the circuit will thus be proportional to $1/R_{bol}C_i$. This gain is difficult to control and will vary with the ambient temperature due to the temperature dependency of the bolometer resistance, R_{bol}—an undesirable effect that would need compensation.

Instead, the capacitive amplifier in Fig. 9(b) is a better choice, since its gain is well defined by a capacitor ratio—as is common in CMOS integrated circuits. A capacitive gain setting network also does not consume any static power, is noiseless in itself and is insensitive to the input common-mode level. Moreover, because the extended counting ADC provides signal integration over the readout time, this should not be done by the interfacing amplifier, as is done in the CTIA. The capacitive amplifier has a high-



(a) The CTIA, a commonly used interface for bolometer readout.



(b) Capacitive amplifier used in this design.

Fig. 9 Comparison of the gain of bolometer readout interface amplifiers; (a) the commonly used CTIA; and (b) the amplifier used in this design

impedance node at its input and is thus susceptible to transistor leakage currents causing a DC voltage drift, as well as the shot noise currents from transistor switches generating low-frequency noise. However, these effects can also be mitigated through the use of offset cancellation techniques such as chopper stabilization or correlated double sampling. The capacitive amplifier together with chopping is the solution used in this design.

A simplified schematic of the complete readout channel is shown in Fig. 10. Two stages of amplification precedes the ADC, the first with a fixed gain of 10 and the second with a programmable gain of 1–16. The whole channel is chopper stabilized to reduce the impact of transistor flicker noise, switch leakage currents and OTA offset. Chopper stabilization also converts the single-ended signal into a differential signal and hence enables the use of differential circuits to improve linearity, SNR and power supply rejection.

As shown in Fig. 10, there are two choppers in the readout channel: one at the input of the first preamplifier and one at the input of the ADC. The frequency of the first chopper can be programmed by means of a programmable clock divider to five different settings: $1, \frac{1}{2}, \frac{1}{4}, \frac{1}{8}$ and $\frac{1}{16}$. This makes it possible to adapt the noise response of the channel to suit the flicker noise corner frequency. However, a changing chopping frequency will complicate the demodulation and signal integration inside the ADC. To make sure that the ADC sees an input signal chopped at a constant frequency, the clock signal to the second chopper is XORed with that of the first, making sure it is only inverting the signal when the first one is not. Hence, the effective chopping frequency at the input of the ADC is constant.

It is important to note that the chopping frequency not only affects the flicker noise performance of the readout channel, but also the input impedance of the channel. A high chopping frequency suppresses flicker noise better, however it also switches more capacitance at the input of the channel and hence loads the bolometer more. This in turn results in a reduced channel gain which leads to increased noise and a higher NETD figure. Inversely, a low chopping frequency results in lower flicker noise suppression, but a higher input impedance and hence higher channel gain. For the lowest possible noise and the best possible NETD, this frequency must be selected such that there is a balance between the amplifier flicker noise contribution and the total channel gain.

4 Chip measurement

During the course of the work, two test chips consisting of a 32 × 32-pixel array that could fit in an multi-project wafer run has been fabricated and measured to evaluate the system before the full 352 × 288-pixel chip is manufactured. Because the process of integrating the microbolometers onto the CMOS chip requires complete wafers for post-processing, these test chips did not contain any bolometers. Instead, to be able to test the readout electronics, additional rows of resistors from the CMOS process with a nominal resistance of 50 kΩ was placed on chip to imitate the microbolometer resistances. CMOS resistors also replaced the blind bolometers used in the source degeneration resistors of the bias current sources.

For the first revision of the test chip, polysilicon resistors were used in place of the microbolometers. As will be seen in the measurement results, these resistors exhibit a very high flicker noise, severely limiting the total noise performance of the circuit. A second revision of the chip

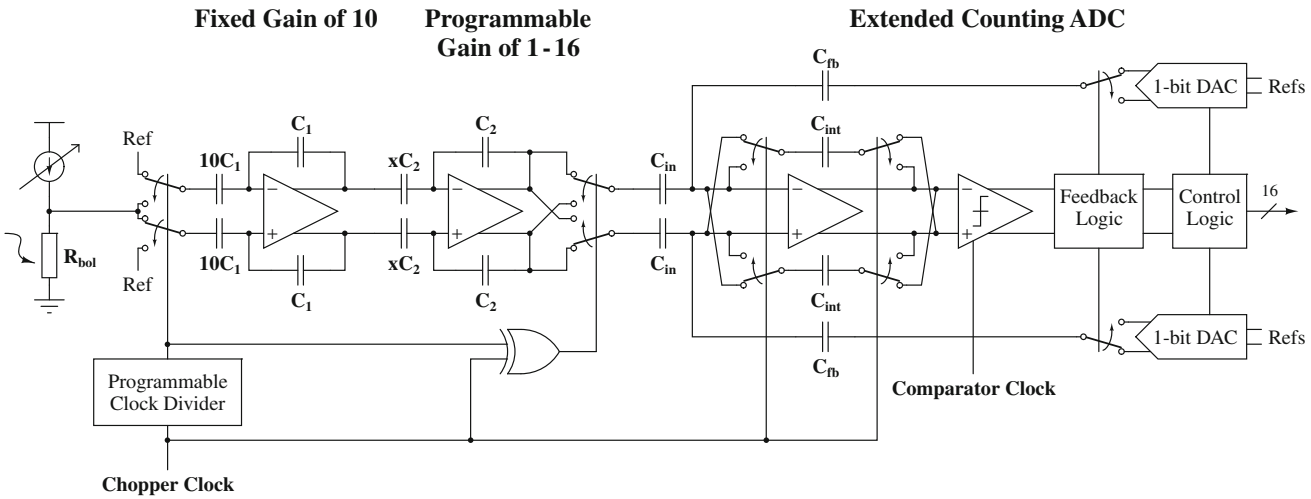


Fig. 10 Analog column readout channel. A 16 bit extended counting ADC is preceded by two preamplification stages. The amplifiers and ADC are chopper stabilized to decrease their flicker noise contributions

was later fabricated to include bug fixes and where the polysilicon resistors were exchanged for p-type diffused resistors that were believed to have lower flicker noise. Subsequent measurements also validated this supposition, showing improved noise performance. However, actual flicker noise performance of the circuit is difficult to evaluate because the flicker noise of the intended microbolometers is highly process dependent and may differ from that of the CMOS resistors.

4.1 Noise performance

Figure 11(a, c) show the input-referred frequency spectrum of the measured signal at the output of the readout channels of the first and the second test chip, respectively, with the inputs of the readout channel shorted together, i.e. without any input signal. This shows the noise performance of the preamplifiers and ADC in the readout path. As seen in the figures, there is no sign of flicker noise at the lower frequencies, meaning that the chopper stabilization works as expected—the flicker noise of the amplifiers and ADC is modulated to higher frequencies and filtered out. The input-referred RMS noise voltage of the readout channel of both revisions of the chip was measured to be 4.0 μV.

The input-referred frequency spectrum measured at the output of the readout channels of the first chip, when the polysilicon resistors are biased with a constant current, is shown in Fig. 11(b). In the figure, the low frequency flicker noise of the polysilicon resistors and bias circuitry is clearly visible. The flicker noise corner frequency was estimated to be 5.9 kHz and the total input-referred RMS noise voltage during bias was measured to be 17.0 μV.

The input-referred noise spectrum of the second chip is shown in Fig. 11(d). The figure shows significantly reduced flicker noise compared to Fig. 11(b), thanks to the lower flicker noise of the diffused resistors used in place of the bolometers. The corner frequency was reduced and estimated to be 290 Hz and the total input-referred RMS noise voltage was measured to be 6.4 μV.

The spectra in Fig. 11 were generated by averaging of the spectra of all 32 channels on the chip. The noise values were all measured with the readout channel gain and chopping frequency setting that gave the lowest noise and at a bias voltage of 1.6 V. The integration time was the same as would be used for the full-size 288 × 352-pixel array at a frame rate of 60 FPS, excluding time for settling as described in Sect. 2.4, i.e. 41 μs. Hence the noise performance of the full size chip is expected to be the same.

While the NETD is highly dependent on microbolometer parameters and performance as well as optics, NETD values resulting from the measured noise values can be estimated in the same way as was done in Sect. 2.5 using the values in Table 1. With an added 2.2 μV of thermal fluctuation noise, this gives the NETD values of 66 and 26 mK for the polysilicon and diffused resistors, respectively. However, it is important to note that these are only estimated values and that they may differ depending on the parameters and flicker noise performance of the microbolometers.

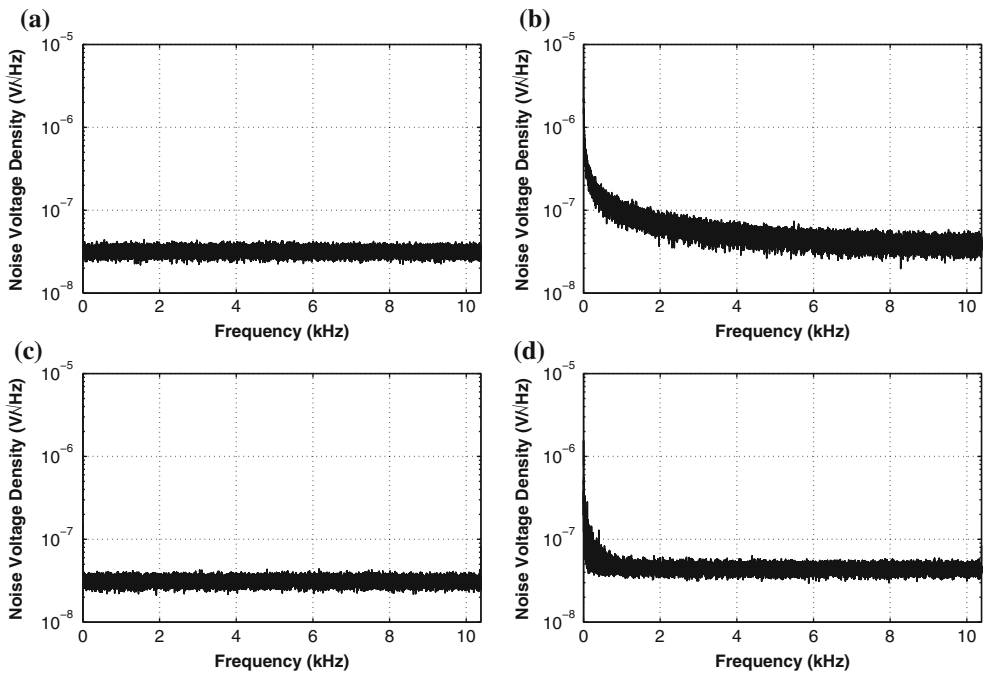


Fig. 11 Input referred noise spectra for the analog readout channel in (**a**) the first chip and (**c**) the second chip; and for the total system noise during biasing with (**b**) polysilicon resistors and (**d**) p-type diffused resistors

4.2 Preamplifier and ADC dynamic range

The dynamic range of the readout channel depends on the total gain of the channel. For the best possible sensitivity and also the lowest input-referred noise value, a high gain is desired. However, at high gain, large signals will saturate the ADC and thereby reduce the dynamic range. For the highest dynamic range the lowest possible gain is desired. The total channel gain is influenced not only by the capacitance ratio in the amplifiers of the readout channel, but also by the voltage division between the detector resistance and the input impedance of the readout channel, which can be altered by changing the chopping frequency. Figure 12 shows the measured dynamic range as a function of the total channel gain and shows that it ranges from 91 to 65 dB for the chip with polysilicon resistors, and from 97 to 75 dB for the chip with diffused resistors.

4.3 Bias current ramps and mismatch correction

The bias current pulse generation and mismatch correction functionality was tested by connecting all columns together and measuring the voltage generated over the test resistors with an oscilloscope. Connecting all columns together was necessary to provide enough drive strength for the oscilloscope. Figure 13(a) shows the 16 different bias currents generated for a linear relationship of the mismatch, and Fig. 13(b) shows the same when realizing a second-order polynomial relationship between the offsets of the currents. Here, time-constant currents were selected to clearly visualize the offset relationships. Any of the 16 currents can be chosen individually for each pixel to correct for resistance mismatch.

The circuits ability to generate time-varying current pulses is shown in Fig. 14. The figure shows four different pulses using different values of the coefficients c_{i0}, c_{i1}, c_{i2} in (10). The constant pulse only has c_{i0} set; the linear pulse has both c_{i0} and c_{i1} set; the square pulse has c_{i0} and c_{i2} set; and the linear and square pulse has all the three coefficients set. This shows that the circuitry can realize ramped current pulses with a second-order shape with respect to time.

A non-linear relationship of pulse magnitudes for the 16 currents can be realized by selecting the first- and/or second-order time coefficients differently between the three DAC voltages and is shown in Fig. 15(a), where the DC coefficients are equal for all three DACs. A combination of all of these possibilities is shown in Fig. 15(b) where the circuit realizes a second-order relationship between the offsets and the pulse magnitudes as well as a second-order shape with respect to time.

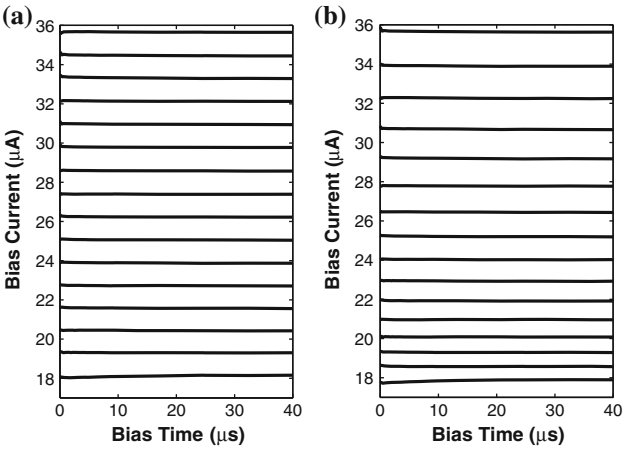


Fig. 13 Measurement of a constant-time bias current from the 16 different precorrection levels when realizing offsets with (**a**) a first-order linear relationship; and (**b**) a second-order polynomial relationship

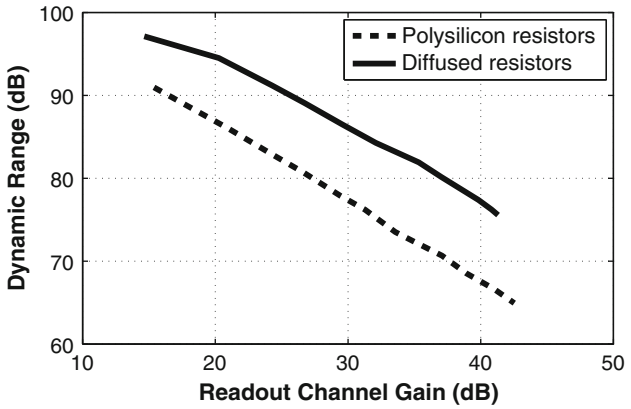


Fig. 12 Dynamic range of the readout channel as a function of channel gain. Peak values reach 91 dB for the polysilicon resistors and 97 dB for the diffused resistors

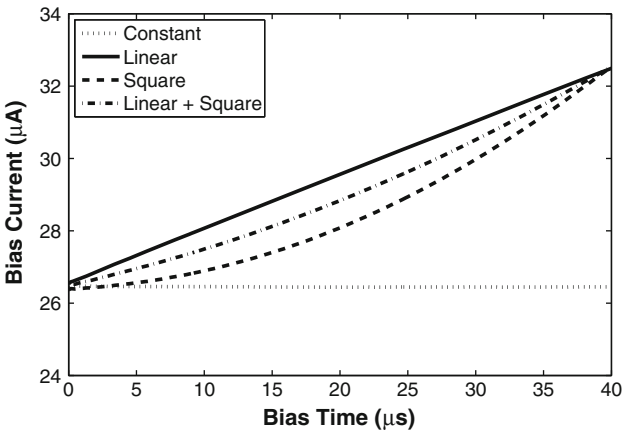


Fig. 14 Measured bias current pulse ramps showing the possibility of shape configuration through coefficient programming. Four different shapes are realized by appropriately selecting the constant, linear and square coefficients for the bias current DACs

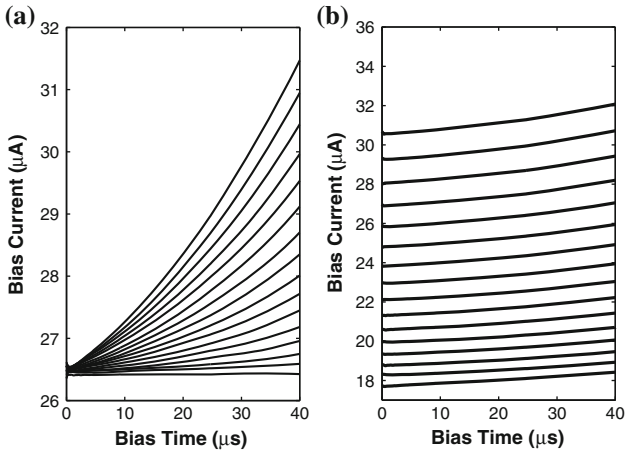


Fig. 15 Measurements of combinations of both second-order mismatch correction and second-order pulse shapes. A non-linear relationship of pulse magnitudes is shown in (**a**) while (**b**) shows a second-order offset as well as a second-order magnitude relationship for the 16 bias currents

Table 2 32 × 32-pixel test chip characteristics

Parameter	Resistors	Value	Unit
Technology		0.35	μm
Array size		32 × 32	pixels
Supply voltage		3.4, 5.8–9	V
Frame rate		60	FPS
Power consumption		170	mW
Noise in readout[1]		4.0	μV_{rms}
Total noise[1]	Poly	17.0	μV_{rms}
	Diffused	6.4	μV_{rms}
Flicker noise corner	Poly	5.9	kHz
	Diffused	290	Hz
Dynamic range	Poly	91	dB
	Diffused	97	dB
NETD[2]	Poly	66	mK
	Diffused	26	mK

[1] RMS noise level referred to the bolometer

[2] Estimated values

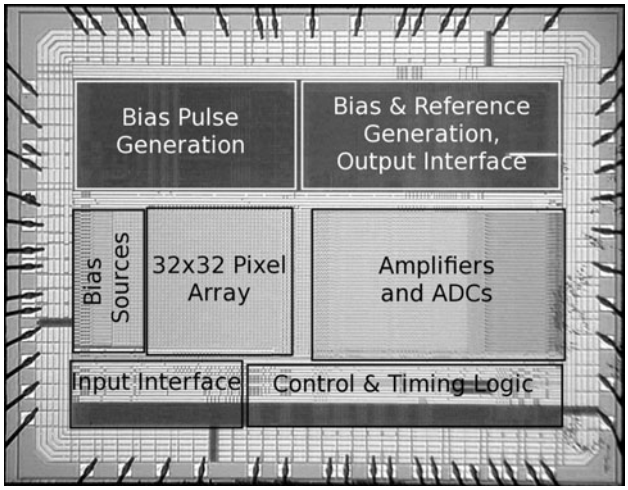


Fig. 16 Die photograph of the 32 × 32-pixel test chip. The die size (including pads) is 12.3 mm^2. The full-size 352 × 288-pixel chip occupies 114.7 mm^2

4.4 System figures and performance comparison

The serial LVDS communication protocol to program, control and read out the data from the ROIC was implemented on an FPGA on a printed circuit board complete with the ROIC, low-noise band-gap references, low-noise power supply regulation and a high-voltage DAC to drive the bolometer bias current sources. The DAC is also controlled through the FPGA, which in turn is accessed from a computer through the USB protocol.

At a frame rate of 60 FPS, the test chips dissipate 170 mW of power from a 3.4 V supply. The circuitry on these test chips are sized the same as for the full-size 352 × 288-pixel array, thus the added power consumption of the full-size array will mainly come from the extra 256 readout channels. Simulations show that one readout channel consumes approximately 890 μW of power making an additional power of 230 mW for an estimated power consumption of 400 mW for the full-size array. Table 2 shows a summary of the performance of the test chips and a chip photograph is shown in Fig. 16.

Table 3 Performance comparison of ROICs for IRFPAs

	[6]	[18]	[8]	[4]	This work
Technology (μm)	–	0.5	0.5	–	**0.35**
Array size	640 × 480	320 × 240	160 × 120	320 × 240	**352 × 288**
Pixel pitch (μm)	17	25	52	50	**25**
Frame rate (FPS)	30	60	50	60	**60**
NETD (mK)	45	63	330	14	**26**[a]
DR (dB)	–	–	60	66	**97**
Power (mK)	350	–	80	–	**400**[a]
Digital output	14 bits	No	No	No	**16 bits**

[a] Estimated values

A performance comparison of state-of-the-art ROICs published in literature is shown in Table 3 and shows that the estimated NETD and dynamic range performance achieved by this work is very competitive. The power consumption of [8] is lower due to lower resolution and digitization of the bolometer signals being done off-chip. The circuits in [4, 18] also use off-chip digitization, but their power consumption was not reported. The ROIC in [6] does support a frame rate of 60 FPS in analog output mode, but performance was only reported for 30 FPS.

5 Conclusions

Uncooled thin-film resistive microbolometers have made thermal infrared imaging at ambient temperature operation of the detector focal plane array, both possible and cost effective. However, the requirements on the readout integrated circuit in terms of dynamic range and noise performance become very high.

The readout integrated circuit for a 352 × 288-pixel IRFPA presented in this paper was designed in a standard 0.35-μm CMOS process and uses a non-linear current pulse biasing scheme to reduce the effects of detector self-heating. It also features programmable correction of detector resistance process variation. A chopper-stabilized readout path removes the flicker noise of the readout circuitry and provides 16-bit digitization of the detector signals.

Two versions of a 32 × 32-pixel test chip were manufactured and evaluated, and have shown that the circuit achieves a very low-noise readout of detector signals. The latest test chip achieves a dynamic range of 97 dB and an input-referred RMS noise voltage of 6.4 μV yielding an estimated NETD of 26 mK with *f*/1 optics. At a frame rate of 60 FPS the chip dissipates 170 mW of power from a 3.4 V supply.

Acknowledgments This work was sponsored by the Swedish Governmental Agency for Innovation Systems (VINNOVA) as part of project INC in co-operation between Linköping University, Faun AB and Axis Communications AB.

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